Preliminary Information [1] *(See Last Page)*

Dual Feed Active-ORing Programmable Hot Swap Controller

FEATURES AND APPLICATIONS

- **Eliminates Passive ORing Diodes for Reduced Power Consumption**
- **High Noise Immunity on All Logic Inputs**
- **Soft Starts Main Power Supply on Card Insertion or System Power Up with Slew Rate Control**
- **Programmable Differential Current Sense**
- **Programmable Inrush Current Limiting**
- **Master Enable to Allow System Control of Power-Up or -Down**
- **Programmable Independent Enabling of up to 4 DC/DC Converters**
- **Programmable Circuit Breaker Level and Mode**
- **Programmable Quick-Trip™ Value, Current Limiting, Duty Cycle Times, Over-Current Filter**
- **Programmable Host Voltage Fault Monitoring**
- **Programmable UV/OV Filter and Hysteresis**
- **Programmable Fault Mode: Latched or Duty Cycle**
- **Internal Shunt Regulator Allows for a Wide Supply Range**

Applications

- **Telecom Hot-Swap Card - AdvancedTCA™**
- **Network Processors**
- **Power-on Ethernet, IEEE 802.3af**

INTRODUCTION

The SMH4814 is an integrated power controller designed to control the hot-swapping of plug-in cards in a distributed power environment. The SMH4814 drives external power MOSFET switches that connect the supply to the load while reducing in-rush current and providing over-current protection. When the source and drain voltages of the external MOSFETs are within specification the SMH4814 asserts the four PUP logic outputs in a programmable cascade sequence to enable the DC/DC converters.

The SMH4814 also monitors two independent –48V feeds. The redundant power supplies allow for high availability and reliability. The traditional method of supplying power from these feeds is via ORing power diodes, which consume a significant amount of power. The SMH4814 allows low-RDS_{ON} FETs to be used in place of ORing diodes to reduce power consumption. The SMH4814 determines when at least one of the –48V feeds is within an acceptable voltage range and switches on the appropriate FET path while providing slew rate control. The SMH4814 continuously monitors the incoming feeds and switches to the most negative feed as necessary. The SMH4814 is programmed and controlled using the I^2C bus as required in ATCA™ applications.

SIMPLIFIED APPLICATIONS DRAWING

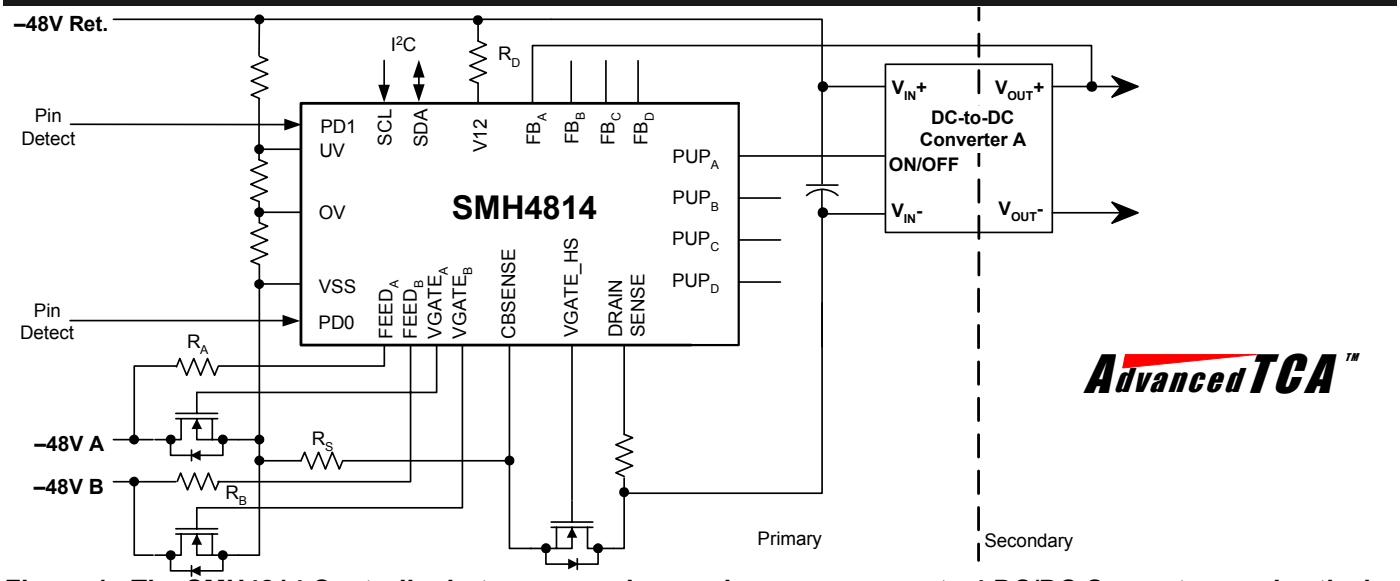


Figure 1. The SMH4814 Controller hot-swaps and cascade sequences up to 4 DC/DC Converters and actively controls the A and B –48V feeds eliminating the need for ORing diodes and the associated voltage drop.

Note: This is an applications example only. Some pins, components and values are not shown.

GENERAL DESCRIPTION

The SMH4814 integrated power controller operates within a wide supply range, typically –32 to –72 volts, and generates the signals necessary to drive isolated-output DC/DC converters.

The device accepts two independent –48V feeds via input pins $FEED_A$ and $FEED_B$. The $VGATE_A$ pin controls the flow of power from $FEED_A$ to the load. The $VGATE_B$ pin controls the flow of power from $FEED_B$ to the load.

The SMH4814 continuously monitors the voltage on $FEED_A$ and $FEED_B$. The supply arbitration block in Figure 2 selects which pin drives power to the device based on the voltage level on each pin and the acceptable voltage range. Once the $FEED_A$ or $FEED_B$ pin is selected the SMH4814 asserts the corresponding VGATE pin. The assertion of this pin turns on the external low-RDS_{ON} FETs to supply power to the load.

Start-up Procedure

The general start-up procedure is as follows:

1. A physical connection must be made with the chassis to discharge any electrostatic voltage potentials when a typical add-in board is inserted into the powered backplane.
2. The board then contacts the long pins on the backplane that provide power and ground.
3. As soon as power is applied the device starts up, but it does not immediately apply power to the output load.
4. Under-voltage and over-voltage circuits inside the controller verify that the input voltage is within a user-specified range.
5. The SMH4814 senses the PD1 and PD0 pin detection signals to indicate the card is seated properly.

These requirements must be met for a Pin Detect Delay period of t_{PDD}. Once this time has elapsed the hot-swap controller enables VGATE_HS to turn on the external power MOSFET switch.

The VGATE_HS output is current limited to I_{VGATE}, allowing the slew rate to be easily modified using external passive components. During the controlled turn-on period the V_{DS} of the MOSFET is monitored by the DRAIN SENSE input. When DRAIN SENSE drops below 2.5V, and VGATE_HS rises above V12 – V_{GT}, the SMH4814 asserts the PUP_A through PUP_D power good outputs to enable the DC/DC controllers.

Steady-state operation is maintained as long as all conditions are normal. Any of the following events may cause the device to disable the DC/DC controllers by shutting down the power MOSFETs:

- An under-voltage or over-voltage condition on the host power supply.
- A failure of the power MOSFET sensed via the DRAIN SENSE pin.
- The PD1/PD0 pin detect signals becoming invalid.
- The master enable (EN/TS) falls below 2.5V.
- Any of the FB inputs driven low by events on the secondary side of the DC/DC controllers.
- The occurrence of an overcurrent.

The SMH4814 may be configured so that after any of these events occurs the VGATE output shuts off, and either latches into an off state or recycles power after a cooling down period, t_{CYC}.

Powering V12

The SMH4814 contains an internal shunt regulator on the V12 pin that prevents the voltage from exceeding 12V. It is necessary to use a dropping resistor (R_D) between the host power supply and the V12 pin in order to limit current into the device and prevent possible damage. The dropping resistor allows the device to operate across a wide range of system supply voltages, typically –32 V to –72V, and also helps protect the device against common-mode power surges. Refer to the Applications Section for help on calculating the R_D resistance value.

INTERNAL FUNCTIONAL BLOCK DIAGRAM

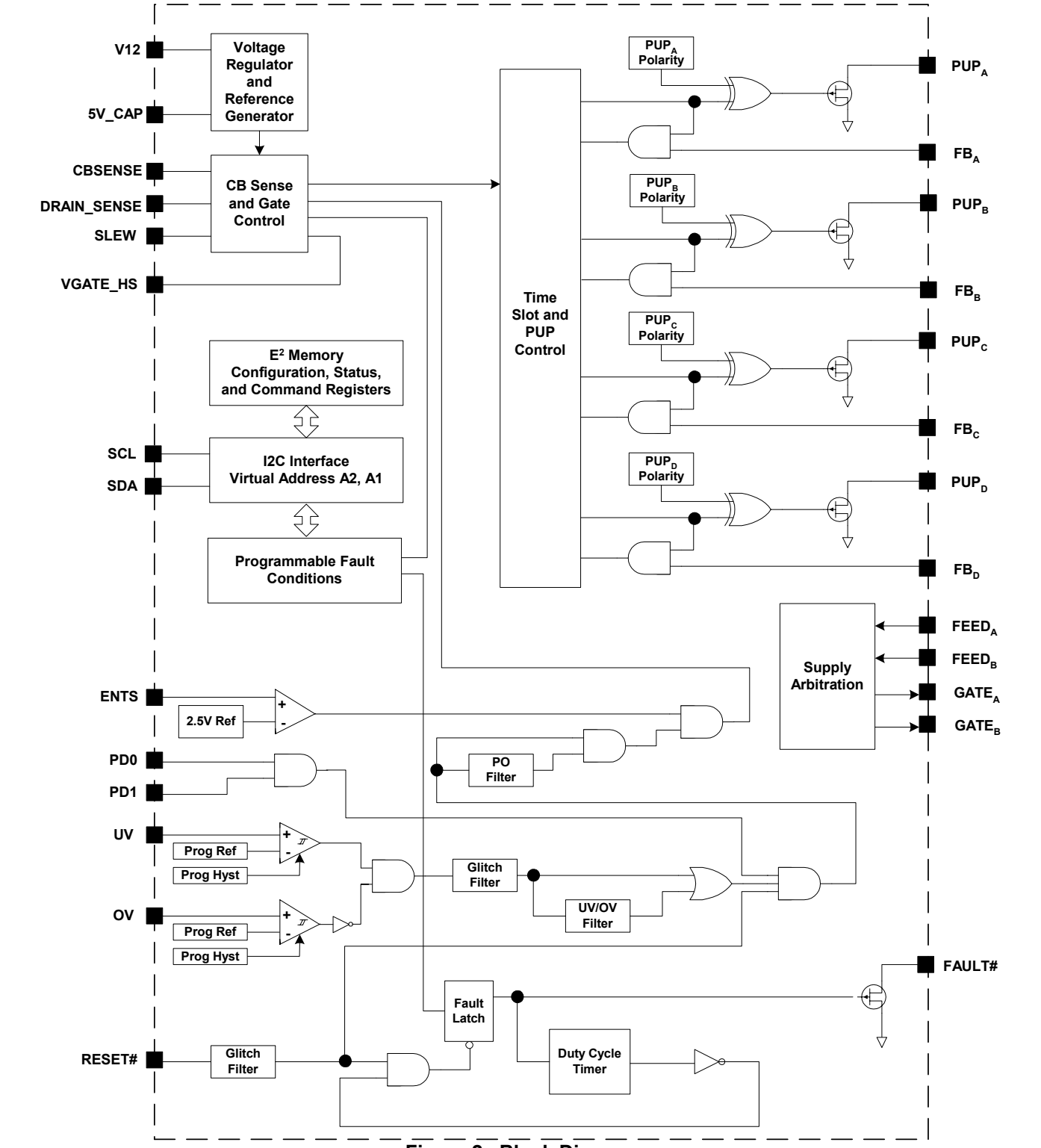


Figure 2. Block Diagram

PIN DESCRIPTION

Pin No. QFN	Pin Type	Name	Description
1,2	I	PD0, PD1	The PD pins are active high, logic level inputs. Protection diodes allow them to be overdriven when used in conjunction with a series limiting resistor. The PD pins have an internal pull-down current sink of 10uA typical.
3	I	RESET#	The RESET# pin is used to clear latched fault conditions. When this pin is asserted, the $VGATE_X$ and PUP_X outputs are immediately disabled. Refer to the section on Circuit Breaker Operation for more information. The RESET# pin has an internal pull-up current source to 5V_CAP of 10uA typical.
4	I	SCL	SCL is the serial clock input.
5	I/O	SDA	SDA is the bidirectional serial data I/O port.
6, 7, 8, 9	O	PUP_A, PUP_B, PUP_C, PUP_D	The PUP_X outputs are programmable active high/low open drain converter enable pins. They can be used in one of 4 programmable sequence positions to switch a load or enable a DC/DC converter after a programmable delay, t_{PGDn}. The voltage on these pins cannot exceed 12V relative to V_{SS}.
10	O	FAULT#	FAULT# is an open-drain, active-low output that indicates the fault status of the device. The device's Status Register may be polled to determine more detailed information about the fault condition.
11	PWR	VSS	This is connected to the negative side of the supply.
12	I	CBSENSE	The circuit breaker sense input is used to detect over-current conditions across an external, low value sense resistor (R_S) tied in series with the Power MOSFET. A voltage drop of greater than V_{CB} (programmable level) across the resistor for longer than t_{CBD} trips the circuit breaker. A programmable Quick-Trip™ sense point is also available.
13	I	UV	The UV pin is used as an under-voltage supply monitor, typically in conjunction with an external resistor ladder. VGATE_HS is enabled when the UV input > Vuv and disabled when UV < Vuv-Vuvhys. An optional programmable filter delay is also available on the UV input.
14	I	OV	The OV pin is used as an over-voltage supply monitor, typically in conjunction with an external resistor ladder. VGATE_HS is disabled when OV > Vov and enabled when OV < Vov-Vovhys. A filter delay is also available on the OV input.
15	I	EN/TS	The Enable/Temperature Sense input is the master enable input. If EN/TS is less than 2.5V, all VGATE outputs are disabled.
16	I	SLEW_CNTL	A capacitor connected to this pin controls the VGATE_HS Slew Rate.
17	I	$FEED_B$	Connect to the -48V 'B' feed using a series 100k resistor. The voltage on this pin is compared with the voltage on the $FEED_A$ pin internally by the supply arbitration logic to determine which voltage will be used.

PIN DESCRIPTION (CONTINUED)

Pin No. QFN	Pin Type	Name	Description
18	I	$FEED_A$	Connect to the -48V 'A' feed using a series 100k resistor. The voltage on this pin is compared with the voltage on the $FEED_B$ pin internally by the supply arbitration logic to determine which voltage will be used.
19	I	DRAIN SENSE	The DRAIN SENSE input monitors the voltage at the drain of the external power MOSFET switch with respect to VSS. An internal 10µA source pulls the DRAIN SENSE signal towards the 5V_CAP level. DRAIN SENSE must be held below 2.5V to enable the PUP_X outputs.
20	O	5V_CAP	External capacitor input used to filter the device's internal operating supply. Also a hold Capacitor to sequence down and to filter any power glitches.
21	O	VGATE_HS	The VGATE_HS output activates an external power MOSFET switch. This signal controls inrush current by modulating the gate of the Hot Swap MOSFET device. It supplies a programmable current output which allows easy adjustment of the MOSFET turn-on slew rate.
22	O	$VGATE_B$	This pin controls the gate of the active FET on $FEED_B$.
23	O	$VGATE_A$	This pin controls the gate of the active FET on $FEED_A$
24	PWR	V12	This is the positive supply input. An internal shunt regulator limits the voltage on this pin to approximately 12V with respect to V_{SS}. A resistor must be placed in series with the V12 pin to limit the regulator current (R_D in the application schematics).
25	I	FB_D	Active-high, logic level input that can be used to indicate when the converter controlled by PUP_D is fully powered. A hold-off timer allows the secondary side (which is not powered up initially) to control shut down via an opto-isolator. See Figures 5 and 6.
26	I	FB_C	Active-high, logic level input that can be used to indicate when the converter controlled by PUP_C is fully powered. A hold-off timer allows the secondary side (which is not powered up initially) to control shut down via an opto-isolator. See Figures 5 and 6.
27	I	FB_B	Active-high, logic level input that can be used to indicate when the converter controlled by PUP_B is fully powered. A hold-off timer allows the secondary side (which is not powered up initially) to control shut down via an opto-isolator. See Figures 5 and 6.
28	I	FB_A	Active-high, logic level input that can be used to indicate when the converter controlled by PUP_A is fully powered. A hold-off timer allows the secondary side (which is not powered up initially) to control shut down via an opto-isolator. See Figures 5 and 6.

PACKAGE AND PIN CONFIGURATION

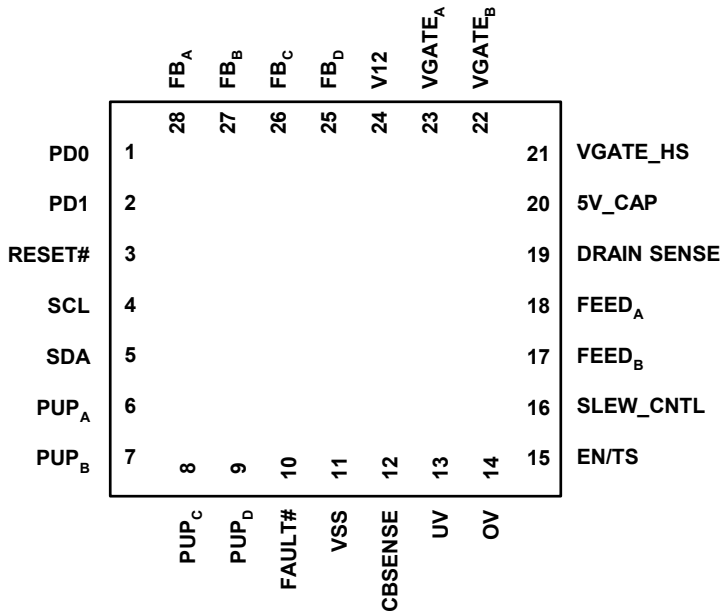


Figure 3A - 28 Pin QFN

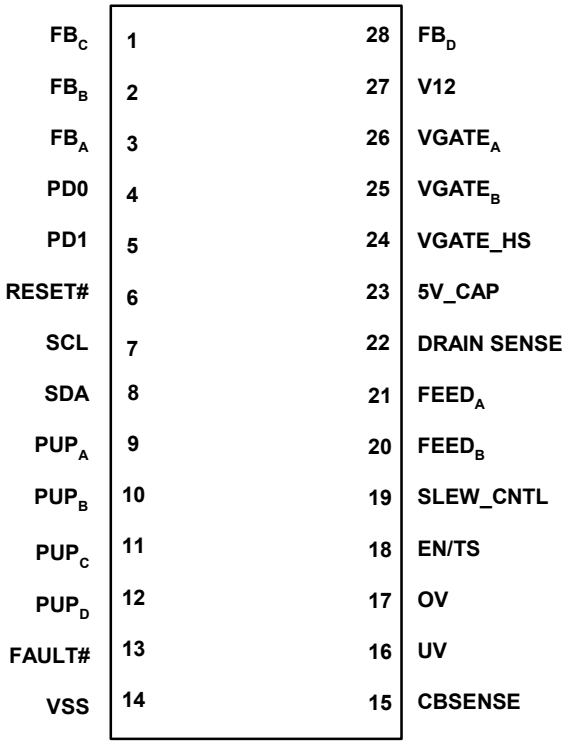


Figure 3B - 28 Pin SOIC

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... –55°C to 125°C
Power Supply Current (I_{DD}) ..... 15 mA
Storage Temperature ..... –65°C to 150°C
Lead Solder Temperature (10 seconds) ..... 300°C
Terminal Voltage with Respect to V_{SS}:

5V_CAP..... -0.3 to +7V
V12, SDA, SCL, UV, OV, CBSENSE, , EN/TS, FAULT#, ... –0.3 to +15V
VGATE_HS, $VGATE_A$, $VGATE_B$ PUP_A, PUP_B, PUP_C, and PUP_D ..... -0.3 to V12+0.7V
PD1, PD0, FB_A, FB_B, FB_C, FB_D, $FEED_A$, $FEED_B$, RESET#, DRAIN SENSE, SLEW_CNTL . -0.3 to 5V_CAP+0.7V

Open Drain Output Short Circuit Current 100mA
Junction Temperature ..... 150°C
ESD Rating per JEDEC 2000V
Latch-Up testing per JEDEC ..... ±100mA

RECOMMENDED OPERATING CONDITIONS

Temperature Range (Industrial) ..... -40°C to 85°C
(Commercial) ..... -5°C to 70°C
Supply Voltage (V_{12}) (I_{DD} = 3 mA) .....11V to 13V
Thermal Resistance (θJA) 28-pin QFN ..... 79°C/W
Thermal Resistance (θJA) 28-pin SOIC ..... 80°C/W

Moisture Classification Level 1 (MSL 1) per J-STD-020
Reliability Characteristics:

Data Retention .....100 Years
Endurance .....100,000 Cycles

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

DC OPERATING CHARACTERISTICS

Over recommended operating conditions, unless otherwise noted. All voltages are relative to V_{SS}.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{12}	Supply Voltage	I_{12} = 4mA	11	12	13	V
I_{12}	Supply Current	(1)	2		13	mA
V_{GATEHI}	$VGATE_A$, $VGATE_B$, VGATE_HS High Voltage		$V_{12} – V_{GT}$		V_{12}	V
V_{GATELO}	$VGATE_A$, $VGATE_B$, VGATE_HS Low Voltage	I_{GATE} = 1mA			0.1	V
V_{SENSE}	Drain Sense Threshold	$V_{SENSE} = V_{SS}$	2.45	2.50	2.55	V
I_{SENSE}	Drain Sense Current		9	10	11	µA
V_{ENTS}	EN/TS Threshold		2.45	2.50	2.55	V
$V_{ENTSHYST}$	EN/TS Hysteresis			10		mV
V_{IH}	RESET#, PD1, PD0, SCL, SDA, FB_A, FB_B, FB_C, FB_D		3		5	V
V_{IL}			–0.1		2	V
V_{OL}	FAULT#, PUP_A, PUP_B, PUP_C, PUP_D	I_{OL} = 3mA	0		0.4	V
I_{IL}	SCL, SDA, CBSENSE, EN/TS, FB_A, FB_B, FB_C, FB_D	$V_{IL} = V_{SS}$			1	µA
$I_{IL\ (PD)}$	PD1, PD0	$V_{IL} = V_{SS}$		10		µA
$I_{IH\ (RESET\#)}$	RESET#	V_{IH} = 5V_CAP		10		µA
V_{GT}	VGATE_HS Threshold		1.5	2.5	4	V

Notes: 1 - This value is set by the R_D resistor (see page 22, Dropper Resistor Selection).

DC OPERATING CHARACTERISTICS (Continued)

Over recommended operating conditions, unless otherwise noted. All voltages are relative to V_{SS}.

DC Programmable Functions (Note 2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{UV}	Under-Voltage Threshold	Default 2.864V	-5	V_{UV}	+5	%
V_{UVHYS}	Under-Voltage Hysteresis	Default 160mV	-5	V_{UVHYS}	+5	%
V_{OV}	Over-Voltage Threshold	Default 3.072V	-5	V_{OV}	+5	%
V_{OVHYS}	Over-Voltage Hysteresis	Default 160mV	-5	V_{OVHYS}	+5	%
V_{CB}	Circuit Breaker Threshold	Default 50mV	-5	V_{CB}	+5	%
V_{CBMAX}	Circuit Breaker Threshold MAX	Default 256mV	-5	V_{CBMAX}	+5	%
V_{CR}	Current Regulation Level	Default V_{CB}+25%	-5	V_{CR}	+5	%
V_{QCB}	Programmable Quick Trip Circuit Breaker Threshold Voltage	Default 100mV	-5	V_{QCB}	+5	%
I_{VGHS_MAX}	VGATE_HS Maximum Current	Default 72µA V_{GATE} = 5V	–5	I_{VGHS_MAX}	+5	%
$I_{VGATEA/B}$	Programmable I_{VGATEA}, I_{VGATEB}	Default 50µA	–25	$I_{VGATEA/B}$	25	%
I_{FEED_SEL}	Programmable FEED current of the selected feed (A or B)	Default 18µA	–5	I_{FEED_SEL}	5	%
I_{FEED_UNSEL}	Programmable FEED current of the unselected feed (A or B)	Default 26µA	–5	I_{FEED_UNSEL}	5	%

Notes: 2 - Default values listed; refer to the Configuration Registers description for the range of values allowed.

AC OPERATING CHARACTERISTICS

Over recommended operating conditions, unless otherwise noted. All voltages are relative to V_{SS}.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{QTSD}	Quick Trip Shutdown	Fig 10, 10% overdrive to start of VGATE_HS turn-off		200		ns

AC Programmable Functions (Note 2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{CBD}	Programmable Over-Current Glitch Filter	Default 40µs (2)	-15	t_{CBD}	+15	%
t_{PGD}	Programmable Power Good Delay	Default 64ms (2)	-15	t_{PGD}	+15	%
t_{CYC}	Circuit Breaker Cycle Mode Cycle Time	Default 5.4s (2)	–15	t_{CYC}	+15	%
t_{PUOVF}	Programmable Under/Over-Voltage Filter	Default 64ms (2)	–15	t_{PUOVF}	+15	%
t_{PDD}	Programmable Pin Detect Delay	Default 64ms (2)	–15	t_{PDD}	+15	%
t_{STT}	Programmable Sequence Termination Timer	Default 64ms (2)	-15	t_{STT}	+15	%
t_{GLITCH}	Glitch Filter	Default 40µs (2)	-15	t_{GLITCH}	+15	%
t_{PCR}	Programmable Current Regulation	Default 64ms (2)	–15	t_{PCR}	+15	%

Notes: 2 - - Default values listed; refer to the Configuration Registers description for the range of values allowed.

I²C 2-WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS – 100/400kHz

Over recommended operating conditions, unless otherwise noted. All voltages are relative to V_{SS}. See Figure 4 Timing Diagram.

Symbol	Description	Conditions	100kHz			400kHz			
			Min	Typ	Max	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency		0		100	0		400	KHz
t_{LOW}	Clock Low Period		4.7			1.3			µs
t_{HIGH}	Clock High Period		4.0			0.6			µs
t_{BUF}	Bus Free Time	Before New Transmission - Note 1/	4.7			1.3			µs
$t_{SU:STA}$	Start Condition Setup Time		4.7			0.6			µs
$t_{HD:STA}$	Start Condition Hold Time		4.0			0.6			µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7			0.6			µs
t_{AA}	Clock Edge to Data Valid	SCL low to valid SDA (cycle n)	0.2		3.5	0.2		0.9	µs
t_{DH}	Data Output Hold Time	SCL low (cycle n+1) to SDA change	0.2			0.2			µs
t_R	SCL and SDA Rise Time	Note 1/			1000			1000	ns
t_F	SCL and SDA Fall Time	Note 1/			300			300	ns
$t_{SU:DAT}$	Data In Setup Time		250			150			ns
$t_{HD:DAT}$	Data In Hold Time		0			0			ns
TI	Noise Filter SCL and SDA	Noise suppression		100			100		ns
t_{WR}	Write Cycle Time	Memory Array			5			5	ms

Note: 1/ - Guaranteed by Design.

TIMING DIAGRAMS

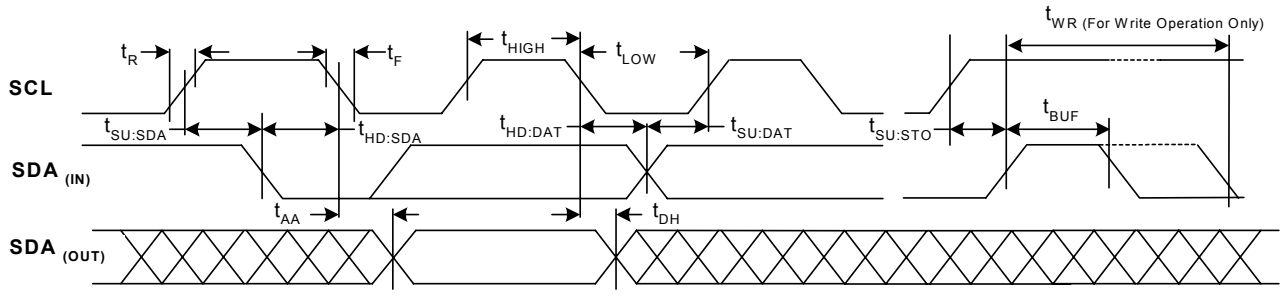


Figure 4 . Basic I²C serial interface timing diagram for the Bus Interface and Memory timing. The table above lists the AC timing parameters. One bit of data is transferred during each clock pulse. Note that data must remain stable when the clock is high.

TIMING DIAGRAMS (CONTINUED)

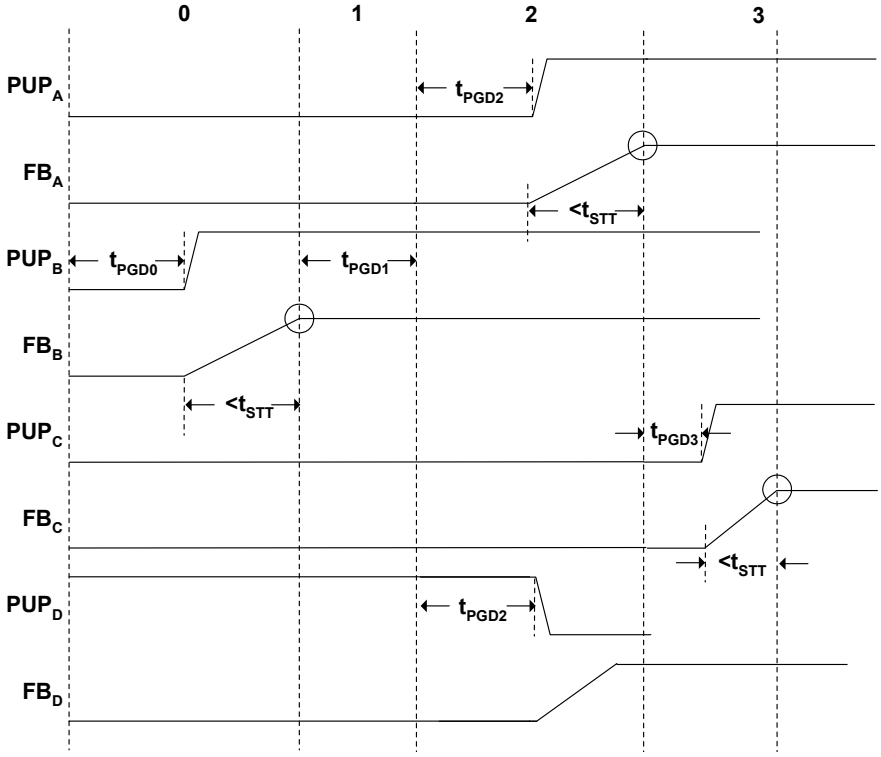


Figure 5 - The SMH4814 cascade sequencing the supplies on and then monitoring for fault conditions.

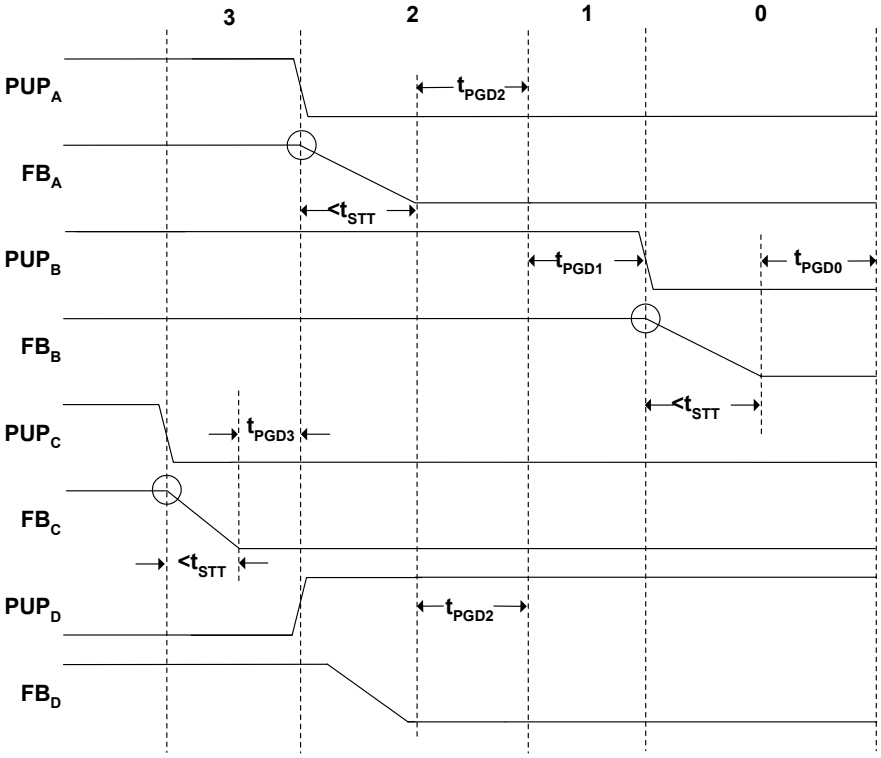


Figure 6 - The SMH4814 cascade sequencing the supplies off.

TIMING DIAGRAMS (CONTINUED)

Power-on Timing

Figure 7 illustrates some power on sequences, including the UV and OV differentials to their reference, and Power Good cascading. Refer to the table on page 17 for more information on the t_{PDD} and t_{CBD} timings.

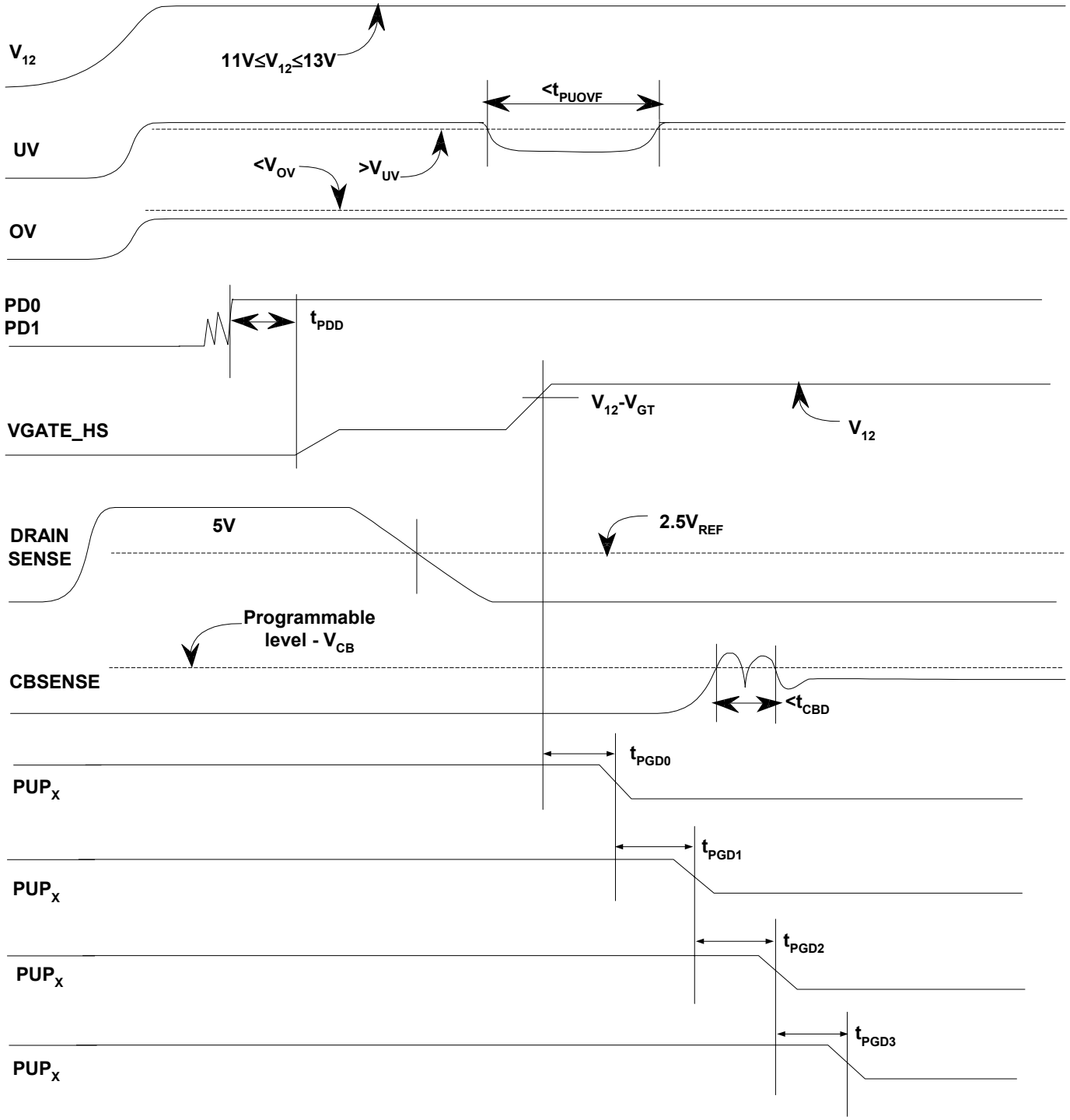


Figure 7 - SMH4814 Power-On Sequences

APPLICATIONS INFORMATION

General Purpose EEPROM

The SMH4814 has 256 bytes of general-purpose EEPROM memory available to the user. These 2k-bits of EEPROM are accessible via the I^2C interface at slave address 1010 or 1011, beginning at word address 0 (0x000) and ending at word address 255 (0x0FF). Refer to the I^2C 2-Wire Serial Interface section for more information.

Configuration Registers

There are also 20 user-programmable, non-volatile configuration registers on the SMH4814. The configuration registers are accessible via the IIC interface at the same slave address as the general purpose EEPROM, beginning at word address 256 (0x100) and ending at address 271 (0x113). These locations will be referred to throughout this document as registers R00 through R13. Individual bits or ranges of bits will be further denoted with square brackets. For example, R00[3:0] refers to Register 0x100, bits 3 through 0. R0D[6,2] refers to Register 0x10D, bits 6 and 2. The configuration registers are responsible for setting all of the programmable parameters described within this document. Refer to the Configuration Register Tables for more detailed information about all the register settings.

Pin Detection

There are several enabling inputs that allow the host to control the SMH4814. The Pin Detect signals (PD1 and PD0) are two active high enables that are generally used to indicate that the add-in circuit card is properly seated. These inputs must be held high for a pin-detect delay period of t_{PDD} before a power-up sequence may be initiated. This is typically done by clamping the inputs to 5v through the implementation of an ejector switch, or alternatively through the use of staggered pins at the card-cage interface.

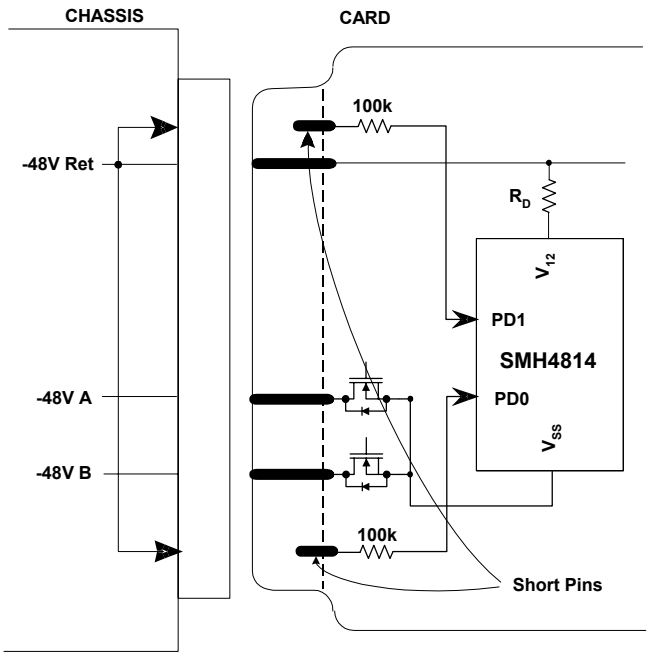


Figure 8 - PD1 and PD0 Inputs, Physical Offset

Two shorter pins, arranged at opposite ends of the connector, force the card to be fully seated before both pin detects are enabled. It is important to use limiting resistors (typically 100k to 1M) in series with the PD inputs to avoid damaging them. An internal shunt prevents the voltage on those pins from reaching unsafe levels.

The PD inputs may be disabled using R0F[2]; however, even if the Pin Detect inputs are disabled or tied directly to 5V, the device must still wait a pin detect delay period before starting up. The pin detect delay (t_{PDD}) timing parameter is controlled by bits R00[3:0]. Refer to Register R00 and R0F for detailed programming information.

EN/TS Input

The EN/TS input provides an active high comparator input that may be used as a master enable or temperature sense input. This input signal must exceed 2.5V to enable the FET turn-on sequence. If EN/TS drops below the 2.5V sense level, the device may be configured to set the FAULT# output or not, and initiates either a Forced Shutdown or Power Down sequence. These options are set using R0D[6,2].

APPLICATIONS INFORMATION (CONTINUED)

Under-/Over-Voltage Sensing

The Under-Voltage (UV) and Over-Voltage (OV) inputs provide a set of comparators that act in conjunction with an external resistive divider ladder to sense whether or not the host supply voltage is within the user-defined limits. The power-up sequence is initiated when the input to the UV pin rises above Vuv and the input to the OV pin remains below Vov for a period of at least t_{PDD} (Pin Detect Delay time). The t_{PDD} filter helps prevent spurious start-up sequences while the card is being inserted.

The default values for Vuv and Vov are 2.86V and 3.07V, respectively. This ratio allows the UV and OV input to be tied together and accommodates standard telecom over and under voltage input ranges. Alternatively, Vuv and Vov may be programmed independently to one of four values, determined by R09[3:0].

Under-/Over-Voltage Filtering

If UV falls below Vuv-Vuvhys or OV rises above Vov for a period of time determined by the UV/OV glitch filter (R06[7:6]), the PUP_X and $VGATE_X$ outputs may be disabled immediately. Alternatively, the SMH4814 can be configured so that an out-of- tolerance condition on UV or OV does not shut off the output immediately. Instead, a filter delay may be inserted so that only sustained under-voltage or over-voltage conditions of longer than the filter delay time (t_{PUOVF} in Figure 9) can shut off the output. The UV and OV filters are enabled with bits 0 and 1, respectively, of register R0F. Refer to R04[3:0] for more information on the filter delay options. Figure 9 shows a sample waveform for when the under-voltage filter is enabled.

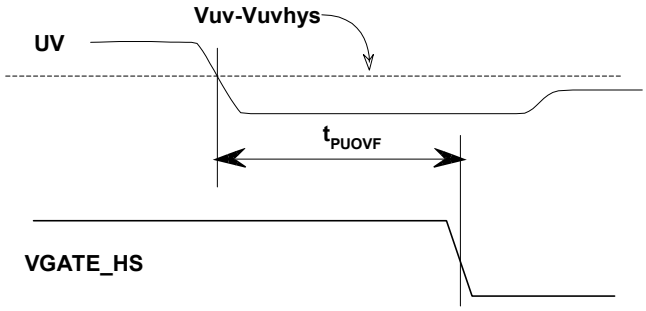


Figure 9 – Example Under-Voltage Filter Timing

Under-/Over-Voltage Latching

By default, an out-of-tolerance condition on UV/ OV will shut off the outputs until the offending condition goes away. At that point, the entire turn on sequence may start over. However, an over or under voltage condition may also be programmed to cause a FAULT condition, using R0D[1:0]. In this case the FAULT# output is asserted, and the user is required to reset the Fault condition before the device will go through another power-up sequence.

Under-/Over-Voltage Hysteresis

The Under and Over Voltage comparator inputs may be configured with a programmable level of hysteresis using Register R08. The falling voltage compare level may be set from 32mV to 512mV below the nominal value, in steps of 32mV. The rising voltage compare level is fixed at either Vuv or Vov, depending on the input. The default under and over voltage hysteresis level is set to 160mV.

Soft Start Slew Rate Control

Once all of the preconditions for powering up the DC/DC controllers have been met as explained in the previous sections, the SMH4814 provides a means to soft start the external power MOSFET. It is important to limit in-rush current to prevent damage to the add-in card or disruptions to the host power supply.

APPLICATIONS INFORMATION (CONTINUED)

The SMH4814 provides three methods for controlling inrush current. The first method entails limiting the current being sourced from the VGATE_HS pin. The maximum current out of this pin (I_{VGHS_MAX}) is a programmable value from 8ua to 128μa (nominal), based on register R0E[3:0]. The importance of having a current-limited gate drive is that the slew rate of the load voltage is roughly equivalent to the slew rate of the FET gate to drain capacitance, once the gate to source potential has reached the FET's threshold voltage. This slew rate (computed by dividing the gate current by the gate-drain capacitance) may be easily modified by adjusting the gate-drain capacitance, which may be a discrete component or capacitance built into the FET structure, or by adjusting the gate current.

A second tool for limiting inrush current is based on further controlling the current being sourced from VGATE_HS. The SLEW_CNTL pin may be used to cause the gate current to linearly ramp from 0μA to the maximum amount (described above) in the following manner. On power-up, SLEW_CNTL is clamped at VSS; when VGATE_HS is enabled, SLEW_CNTL outputs 5μA drawn from the internal 5V supply. If bit 4 of register R0E is set high, then the current out of VGATE_HS is reduced by the ratio of the voltage on SLEW_CNTL divided by 2.5V. Once SLEW_CNTL exceeds 2.5V, then the current is limited to I_{VGHS_MAX}. The advantage of ramping the gate current from zero up to its maximum amount is that the corresponding inrush current will follow a similar pattern, which may lead to less disruption to the overall system. The rate at which the gate current increases is determined by the size of the external capacitor connected to the SLEW_CNTL pin.

The third method for controlling inrush current is based on the SMH4814's Current Regulation feature. Described in more detail in a later section, this feature regulates the current through the FET, and therefore the voltage across an external sense resistor as measured by the CBSENSE input, by controlling VGATE_HS. Normally, this operation attempts to keep CBSENSE from exceeding a programmable threshold voltage, V_{CR}; however, when the load is being initially powered, the regulation point at which CBSENSE is held may be gradually ramped from zero up to V_{CR}. This feature is enabled by setting bit 5 of register R0E high, and by selecting a ratio using R0E[7:6].

In this case, CBENSE is regulated to the voltage on SLEW_CNTL times the ratio determined by R0E, up to the value of V_{CR}.

The methods described here for controlling inrush current may be used separately or together. Once the voltage on SLEW_CNTL is within a p-ch threshold voltage of 5V_CAP, it must remain above this voltage.

Load Control — Sequencing the Secondary Supplies

The PUP_A through PUP_D output pins are used to enable the external DC/DC controllers. Once the load has been fully powered, PUP sequencing may begin. The SMH4814 checks that two conditions have been met to indicate that the load is fully powered:

1) DRAIN SENSE input voltage must be < 2.5V

And

2) VGATE_HS voltage must be > $V_{12} – V_{GT}$.

The DRAIN SENSE input helps ensure that the power MOSFET is not absorbing excessive steady state power from operating at a high V_{DS}. This sensor remains active at all times (except when current regulation is enabled). The VGATE sensor makes sure that the power MOSFET is operating well into its saturation region before allowing the loads to be switched on. Once VGATE reaches $V_{12} – V_{GT}$ this sensor is latched.

PUP Outputs

The SMH4814 has four programmable-polarity, open-drain PUP (Power-Up Permitted) outputs that may be used to control the sequencing order of DC-DC converters. After the soft start process has been completed and the load capacitance has been fully charged, there are four sequential time slots into which each of the PUP outputs may be assigned (Figure 5).

A given time slot may have more than one PUP output assigned to it; likewise, a time slot may have no PUP outputs assigned to it. Time Slot 0 begins after the gate of the main soft-start FET is fully enhanced and the load is fully charged.

APPLICATIONS INFORMATION (CONTINUED)

The duration of each time slot is programmable to one of 16 values ranging from 250µs to 768ms. When Time Slot 0 times out, then the PUP outputs assigned to that time slot are enabled. Time Slot 1 begins when the affiliated feedback pins are pulled high. For example, if PUP_A and PUP_C are assigned to Time Slot 0, then Time Slot 1 begins only after PUP_A and PUP_C are enabled, and FB_A and FB_C are pulled high. If there are no PUP outputs assigned to a given time slot, then the next time slot commences as soon as the current time slot times out. This process continues until all four time slots have timed out and all feedback pins have been pulled high. At this point, the brick sequencing is complete. The device also sequences down in the same manner (Figure 6).

The PUPx outputs have a 12V withstand capability, so high voltages must not be connected to these pins. Bipolar transistors or opto-isolators can be used to boost the withstand voltage to that of the host supply

FB Inputs

The FBx pins are designed to receive feedback from the secondary side of the bricks and are used to indicate that an enabled brick has powered up properly. The previous section described the PUP_X output enabling sequence when the SMH4814 receives the expected feedback from the secondary side. This section describes what happens when a FB_X pin stays low or goes low unexpectedly.

As described above, when a given time slot times out, the appropriate PUP output is enabled. The next time slot will not commence until the associated FB pin is pulled high. The sequence termination timer (STT) is used to protect against a stalled Power-on sequence. This timer commences when the PUPx outputs within a given time slot are enabled, and it continues running until either all associated FBx inputs go high or the sequence termination timer times out (t_{STT}). If the STT times out before the appropriate FB inputs go high the device will power down the PUP and VGATE outputs. This control mechanism allows supplies that have dependencies based on the other voltages in the system to be cascaded properly.

The status registers contain bits that indicate the sequence has been terminated and in which sequence position the timer timed out.

Active FET Gate Control

Throughout the power-up process, the Active-ORing FET's are kept off. Current flows by means of the body diodes of those MOSFET devices. Once all of the PUP outputs of the SMH4814 have been enabled, one of the Active-ORing FET's may now be enabled. Initially, the feed with the lowest negative potential is the one selected to power the load. To determine the lowest supply, an on-board comparator determines which input ($FEED_A$ or $FEED_B$) is lower. Since the actual feeds may both be below VSS due to the drop across the body diodes, the $FEED_A$ and $FEED_B$ inputs are level shifted up by delivering a current across a dropper resistor (typically 100k). The FEED output current is programmable from 10µA-25µA, using R07[7:4]. The VGATE output corresponding to the lowest FEED input is driven to V12.

The $FEED_A$ and $FEED_B$ inputs are continually monitored for the lowest input level so that the corresponding power feed will be the one used to energize the load. However, once one of the Active FET gates has been driven high, the level shifting currents being delivered out of $FEED_A$ and $FEED_B$ may be skewed to offer some degree of hysteresis. The current driven out of the non-selected feed is increased by anywhere from 0 to 15µA, as determined by R07[3:0]. The effect of the increased current is to make the non-selected feed appear to have an even higher potential, and thereby offering a level of hysteresis. The hysteresis will help to reduce the amount of unnecessary switching between feeds in cases where the two potentials are very close together or where there is excessive noise on the feeds.

When it is determined that the selected feed is no longer the most appropriate one to power the load, the corresponding VGATE output is immediately switched off via a powerful pull-down device. The complementary output is then enabled using a current limited pull-up. The amount of current is selectable from 10µA –200µA using R05[5:4].

APPLICATIONS INFORMATION (CONTINUED)

Circuit Breaker Operation

The SMH4814 provides a highly configurable method for detecting and controlling over-current events. A sustained over-current condition can cause physical damage to the card edge connector, the load circuitry, and may even disrupt operation of other cards in the system. To detect such over-current conditions, a series sense resistor (R_S) is connected between the MOSFET source (which is tied to CBSENSE) and V_{SS}. The board's load current passes through the sense resistor, and the CBSENSE input is monitored for excessive voltage drop across R_S.

The SMH4814 compares the CBSENSE input against three important voltage levels (V_{CB}, V_{QCB}, and V_{CR}) and takes appropriate action as each successive level is reached. The first voltage, V_{CB}, is the circuit breaker trip point, which is determined by R0A[7:0]. V_{CB} may be set to any one of 256 levels up to a maximum voltage of V_{CBMAX}, which is a configurable voltage of 128mV, 256mV, 512mV or 1024mV, as determined by R09[5:4]. For example, if V_{CBMAX} is set to 256mV, then V_{CB} may be programmed to any value between 0 and 255mV, in 1mV increments. (Refer to the Register Description for more information.) If CBSENSE exceeds V_{CB} for a period of time longer than the glitch filter delay associated with that input, t_{CBD} (set using R06[1:0]), then the device is considered to be in an over-current state. Once in an over-current state, the SMH4814 will either shut down immediately, or if the Current Regulation option is selected (R05[3]), the device will begin another timer. Refer to the description of Current Regulation for more information on these actions.

Quick-Trip™ Circuit Breaker

The second voltage level that the CBSENSE input is compared against is the Quick-Trip™ Circuit Breaker level, V_{QCB}. V_{QCB} is determined by the contents of R0B[7:0], in a manner similar to V_{CB}. (Note that the value stored in R0B is a 2's complement number; refer to the Register Description for more information.) Unlike the V_{CB} comparator, the output of the V_{QCB} comparator is a high-speed, non-filtered signal designed to shutdown the MOSFET gate very quickly. If the Current Regulation option is not selected, then exceeding the Quick-Trip level causes an immediate shutdown of the PUP outputs and MOSFET gate; however, if Current Regulation is selected, the PUP outputs will not be immediately shut off. Refer to the description of Current Regulation for more information.

Figure 10 shows the circuit breaker 'Quick Trip' response. In this figure, the voltage rises above V_{QCB}, causing VGATE to be deasserted.

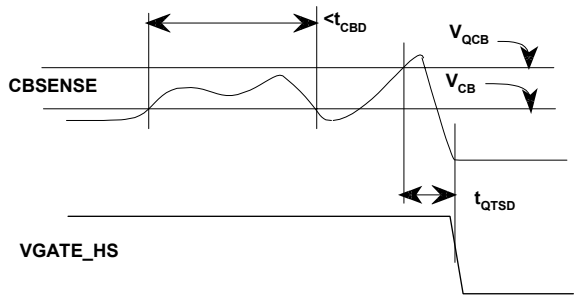


Figure 10 - Circuit Breaker Quick Trip Response without current regulation.

Current Regulation

The Current Regulation mode is an optional feature that provides a means to regulate current through the MOSFET for a programmable period of time. This mode allows the system to "ride out" temporary disruptions that might otherwise cause traditional circuit breakers to trip. The Current Regulation trip point, V_{CR}, is the third voltage level against which the CBSENSE input is compared. V_{CR} is determined by register R09[7:6] and is expressed as a percentage above the V_{CB} level. There are four choices: 12.5%, 25%, 50% and 100%. Note that the Quick-Trip level V_{QCB} should be chosen to fall above V_{CR} in order for Current Regulation to be effective.

Current Regulation works by modulating VGATE_HS so that CBSENSE is always less than or equal to V_{CR}. In order to avoid overheating the MOSFET by operating in its linear region for too long, a timer is started whenever CBSENSE goes above V_{CB} or VGATE_HS falls at least V_{GT} below V12. If either of these conditions exist for the duration of the current regulation timer, t_{CR}, then the PUP and VGATE outputs are shut down. There are actually two different Current Regulation timers; R00[7:4] controls the timing for the initial VGATE_HS turn on, and R04[7:4] controls the timing for all subsequent current regulation events.

APPLICATIONS INFORMATION (CONTINUED)

In the case when Current Regulation is enabled and CBSENSE exceeds V_{QCB} before the circuitry has time to modulate VGATE_HS, the Quick-Trip circuit assists the modulation by pulling down on the gate immediately. Rather than pull all the way to VSS, the Quick-Trip circuitry may also be configured to only pull down to within one, two or three diode of VSS (R05[7:6]). Once CBSENSE falls back below V_{QCB}, the pull-down circuitry will shut off. By this point, the Current Regulation circuit will have had time to activate, and VGATE_HS will be modulated to keep the CBSENSE level at V_{CR}. Figure 11 and Figure 12 illustrate the current regulation function.

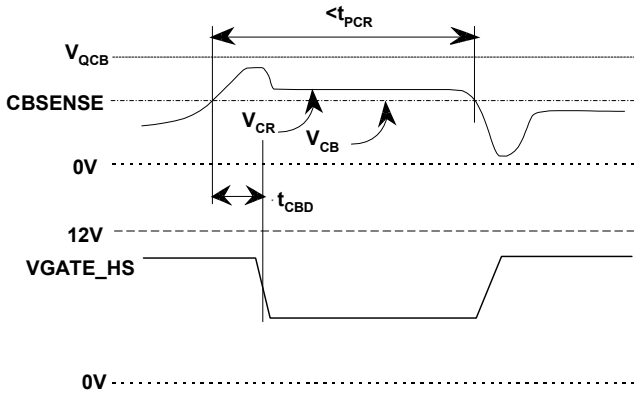


Figure 11 - Current Regulation With Recovery

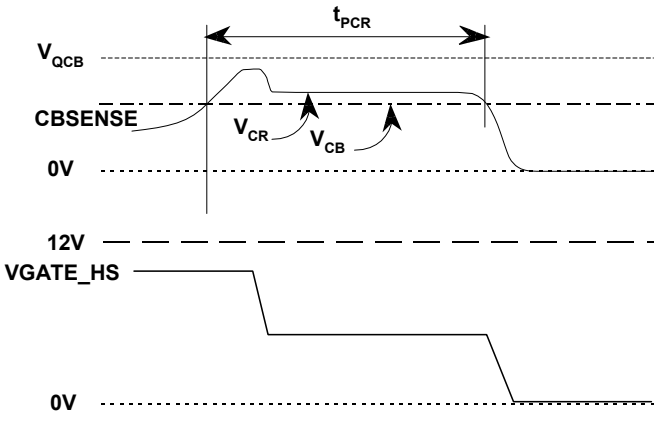


Figure 12 - Current Regulation Without Recovery

Resetting FAULT#

When the circuit breaker trips and, in the case in which current regulation is enabled, t_{PCR} times out, the VGATE_HS and PUP outputs are turned off and FAULT# is driven low. Other events may also be configured to cause a Fault, as determined by R0D[3:0] and R10[7:4]. Once a Fault has occurred, the SMH4814 may be configured (using R05[2]) to either restart on its own after a programmable cooling off period of t_{CYC} (Figure 13), or it may be configured to stay latched off until the Fault is manually reset (Figure 14). The duty cycle timeout period t_{CYC} is set using R03[7:4] and can range from 7ms to 21.5s. The Fault condition may be manually reset by driving RESET# low, or through the use of the Command Register.

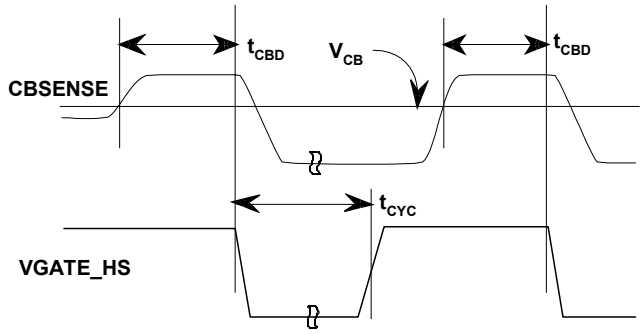


Figure 13 - Circuit Breaker Duty Cycle Operation with RESET# High

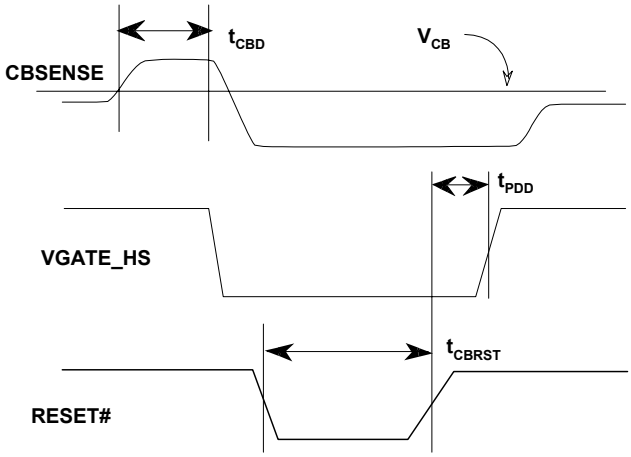


Figure 14 - Circuit Breaker Reset with RESET#

APPLICATIONS INFORMATION (CONTINUED)

Command Register:

The command register (Table 1) provides useful software functionality for the SMH4814. It is accessed using the 1001 slave address, and a word address of 0x000. To invoke any of the functions of the command register, simply write a "1" to the appropriate bit position. The other bits should receive a "0". Note that invoking contradictory commands, such as Power Down and Power Up, simultaneously will cause indeterminate results. The following table describes the command byte:

Bit	Description
7	Clear Fault
6	Check Fuse
5	Clear WP
4	Set WP
3	Check Short FET
2	Forced Shut Down
1	Power Down
0	Power Up

Table 1 – Command Register

Status/Fault Registers:

There are three Status/Fault Registers, accessed at slave address 1001 with address bit A8 set low, at word address 0x02-0x04. These registers generally act as status registers, giving the user the current state of the device. However, when a fault occurs, the state of the device becomes latched, allowing the user to access the state of the part at the time of fault.

Once latched into the Fault state, the only way to set these registers back to Status registers is to use the command register to clear the fault.

Refer to the Status/Fault Register Tables (page 40) for more detailed information about the meaning of each bit.

Serial Interface

The SMH4814 uses the industry standard I^2C, 2-wire serial data interface. This interface provides access to the general purpose EEPROM, the command and status registers, and the configuration registers. The interface has two address inputs A1 and A2 (determined by R0F[7:6]), allowing up to four devices on the same bus. This allows multiple devices on the same board or multiple boards in a system to be controlled with two signals; SDA and SCL.

Device configuration utilizing the Windows based SMH4814 graphical user interface (GUI) is highly recommended. The software is available from the Summit website (www.summitmicro.com/). Using the GUI in conjunction with this datasheet, simplifies the process of device prototyping and the interaction of the various functional blocks. A programming Dongle (SMX3200) is available from Summit to communicate with the SMH4814. The Dongle connects directly to the parallel port of a PC and programs the device through a cable using the I^2C bus protocol.

APPLICATIONS INFORMATION (CONTINUED)

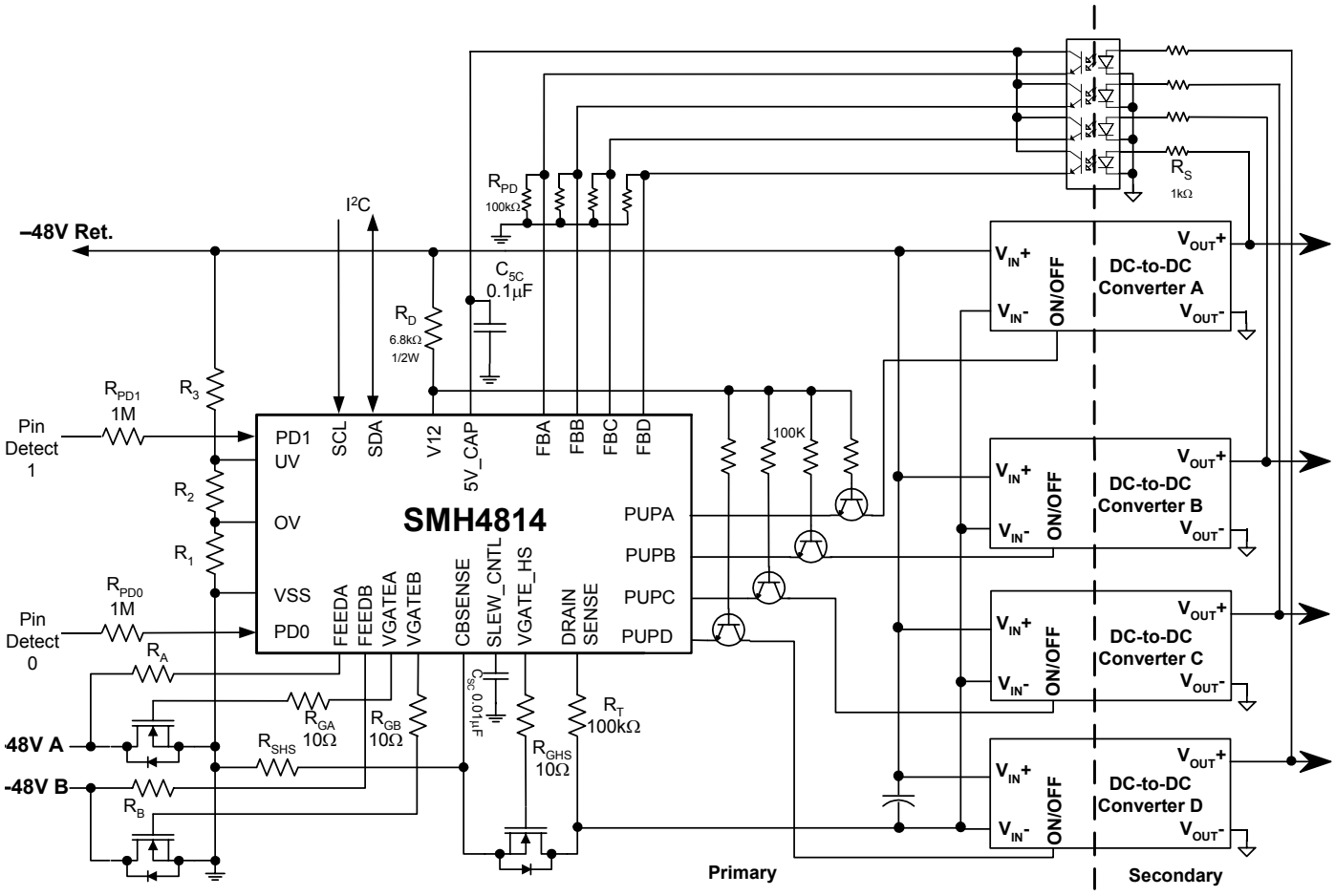


Figure 15A - Full Application Schematic with all isolation components shown. The value of RD can be chosen to be a single 1/2W resistor as shown or a parallel combination of smaller 1/10W resistors as shown in Figure 15B.

APPLICATIONS INFORMATION (CONTINUED)

Operating at High Voltages

The breakdown voltage of the external active and passive components limits the maximum operating voltage of the SMH4814 hot-swap controller. Components that must be able to withstand the full supply voltage are: the input and output decoupling capacitors, the protection diode in series with the DRAIN SENSE pin, the power MOSFET switch and the capacitor connected between its drain and gate, the high-voltage transistors connected to the power good outputs, and the dropper resistor connected to the controller's V_{DD} pin.

Over-Voltage and Under-Voltage Resistors

In Figure 15A, the three resistors (R1, R2, and R3) connected to the OV and UV inputs must be capable of withstanding the maximum supply voltage of several hundred volts. The resistor values should be chosen so that the UV or OV input reaches its corresponding trip point (Vuv or Vov) when the incoming power feed reaches its low or high operational limit. As the input impedance of UV and OV is very high, large value resistors can be used in the resistive divider. The divider resistors should be high stability, 1% metal-film resistors to keep the under-voltage and over-voltage trip points accurate.

Telecom Design Example

A hot-swap telecom application may use a 48V power supply with a –25% to +50% tolerance (i.e., the 48V supply can vary from 36V to 72V). The formula for calculating R1, R2, and R3 are as follows.

First, a peak current, ID_{MAX}, must be specified for the resistive network. The value of the current is arbitrary, but it cannot be too high (self-heating in R3 becomes a problem), or too low (the value of R3 becomes very large, and leakage currents can reduce the accuracy of the OV and UV trip points). The value of IDMAX should be ≥200µA for the best accuracy at the OV and UV trip points. A value of 250µA for IDMAX is used to illustrate the following calculations.

With V_{OV} (2.864V) being the over-voltage trip point, R1 is calculated by the formula:

$$R1 = \frac{V_{OV}}{ID_{MAX}}$$

Substituting:

$$R1 = \frac{2.864V}{250\mu A} = 11.46\ k\Omega$$

The closest standard 1% resistor value is 11.8kΩ

Next the minimum current that flows through the resistive divider, ID_{MIN}, is calculated from the ratio of minimum and maximum supply voltage levels:

$$ID_{MIN} = \frac{ID_{MAX} \times VS_{MIN}}{VS_{MAX}}$$

Substituting:

$$ID_{MIN} = \frac{250\mu A \times 36V}{72\ V} = 125\ \mu A$$

Now the value of R3 is calculated from ID_{MIN}:

$$R3 = \frac{VS_{MIN} \times V_{UV}}{ID_{MIN}}$$

V_{UV} is the under-voltage trip point, also 2.864V. Substituting:

$$R3 = \frac{36V \times 2.864V}{125\ \mu A} = 825\ k\Omega$$

The closest standard 1% resistor value is 825kΩ

Then R2 is calculated:

$$(R1 + R2) = \frac{V_{UV}}{ID_{MIN}}$$

Or

$$R2 = \frac{V_{UV}}{ID_{MIN}} - R1$$

Substituting:

$$R2 = \frac{2.864V}{125\mu A} - 11.8\ k\Omega = 20\ k\Omega - 10\ k\Omega = 11\ k\Omega$$

An Excel spread sheet is available at: (*http://www.summitmicro.com/*) or contact Summit to simplify the resistor value calculations and tolerance analysis for R1, R2, and R3.

APPLICATIONS INFORMATION (CONTINUED)

Dropper Resistor Selection

The SMH4814 is powered from the high-voltage supply via a dropper resistor, R_D. The dropper resistor must provide the SMH4814 (and its loads) with sufficient operating current under minimum supply voltage conditions, but must not allow the maximum supply current to be exceeded under maximum supply voltage conditions.

The dropper resistor value is calculated from:

$$R_D = \frac{VS_{MIN} - VDD_{MAX}}{I_{DD} - I_{LOAD}}$$

where VS_{MIN} is the lowest operating supply voltage, V_{DDMAX} is the upper limit of the SMH4814 supply voltage, I_{DD} is minimum current required for the SMH4814 to operate, and I_{LOAD} is any additional load current from the 2.5V and 5V outputs and between V_{DD} and V_{SS}.

Calculate the minimum wattage required for RD from:

$$P_{R0} \geq \frac{(VS_{MAX} - VDD_{MIN})^2}{R_D}$$

where V_{DDMIN} is the lower limit of the SMH4814 supply voltage, and VS_{MAX} is the highest operating supply voltage.

The dropper resistor value should be chosen such that the minimum and maximum I_{DD} and V_{DD} specifications of the SMH4814 are maintained across the host supply's valid operating voltage range. First, subtract the minimum V_{DD} of the SMH4814 from the low end of the voltage, and divide by the minimum I_{DD} value. Using this value of resistance as R_D find the operating current that would result from running at the high end of the supply voltage to verify that the resulting current is less than the maximum I_{DD} current allowed. If some range of supply voltage is chosen that would cause the maximum I_{DD} specification to be violated, then an external zener diode with a breakdown voltage of ~12V should be used across V_{DD}.

As an example of choosing the proper R_D value, assume the host supply voltage ranges from 36 to 72V. The largest dropper resistor that can be used is: (36V-11V)/3mA = 8.3kΩ. Next, confirm that this value of R_D also works at the high end: (72V-13V)/8.3kΩ = 7.08mA, which is less than 8mA.

In circumstances where the input voltage may swing over a wide range (*e.g., from 20V to 100V)* the maximum current may be exceeded. In these circumstances it may be necessary to add an 11V Zener diode between V_{DD} and V_{SS} to handle the wide current range. The Zener voltage should be below the nominal regulation voltage of the SMH4814 so that it becomes the primary regulator.

MOSFET V_{DS}(ON) Threshold

The drain sense input on the SMH4814 monitors the voltage at the drain of the external power MOSFET switch with respect to V_{SS}. When the MOSFET's V_{DS} is below the user-defined threshold the MOSFET switch is considered to be ON. The $V_{DS}(ON)_{THRESHOLD}$ is adjusted using the resistor, R_T.

The $V_{DS}(ON)_{THRESHOLD}$ is calculated from:

$$V_{DS}(ON)_{THRESHOLD} = V_{SENSE} - (I_{SENSE} \times R_T)$$

The $V_{DS}(ON)_{THRESHOLD}$ varies over temperature due to the temperature dependence of I_{SENSE}. The calculation below gives the $V_{DS}(ON)_{THRESHOLD}$ under the worst case condition of 85°C ambient. Using a 100kΩ resistor for R_T gives:

$$V_{DS}(ON)_{THRESHOLD} = 2.5V - (15\mu A \times 100k\Omega) = 1V$$

The voltage drop across the MOSFET switch and sense resistor, V_{DSS}, is calculated from:

$$V_{DSS} = I_D (R_S + R_{DSON})$$

where I_D is the MOSFET drain current, R_S is the circuit breaker sense resistor and R_{DSON} is the MOSFET on resistance.

APPLICATIONS INFORMATION (CONTINUED)

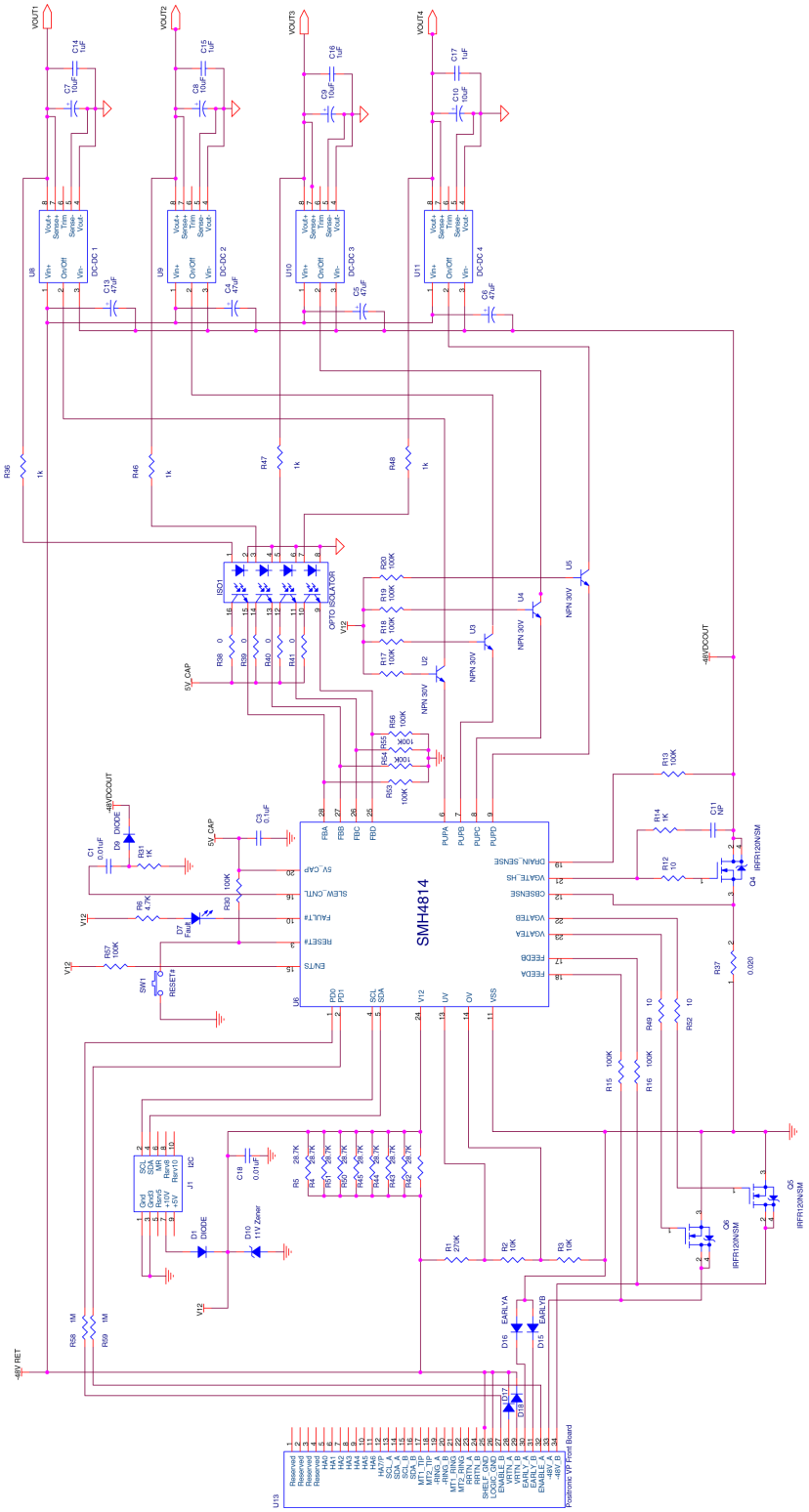


Figure 15B – ATCA™ application Schematic

I²C 2-WIRE SERIAL INTERFACE

Programming Information

I²C Bus Interface

The I²C bus interface is a standard two-wire serial protocol that allows communication between integrated circuits. The data line (SDA) is a bi-directional I/O; the clock line (SCL) runs at speeds of up to 400kHz. The SDA line must be connected to a positive logic supply through a pull-up resistor located on the bus.

Start and Stop Conditions

Both the SDA and SCL pins remain high when the bus is not busy. Data transfers between devices may be initiated with a Start condition. A high-to-low transition of the SDA input while the SCL pin is high is defined as a Start condition. A low-to-high transition SDA while SCL is high is defined as a Stop condition. Figure 16 shows a timing diagram of the start and stop conditions.

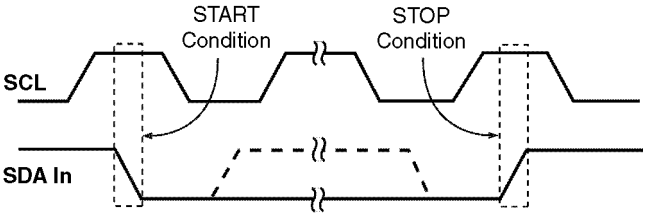


Figure 16 - Start and Stop Conditions

Master/Slave Protocol

The master/slave protocol defines any device that sends data onto the bus as a transmitter, and any device that receives data as a receiver. The device controlling data transmission is called the Master, and the controlled device is called the Slave. In all cases the SMH4814 is referred to as a Slave device since it never initiates any data transfers. One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock high time, because a change on the data line while SCL is high is interpreted as either a Start or a Stop condition.

Acknowledge

Data is always transferred in bytes. Acknowledge (ACK) is used to indicate a successful data transfer. The transmitting device releases the bus after transmitting eight bits. During the ninth clock cycle the Receiver pulls the SDA line low to acknowledge that it received the eight bits of data. This is shown by the ACK callout in Figure 17.

When the last byte has been transferred to the Master during a read of the SMH4814, the Master leaves SDA high for a Not Acknowledge (NACK) cycle. This causes the SMH4814 part to stop sending data, and the Master issues a Stop on the clock pulse following the NACK.

Figure 17 shows the Acknowledge timing.

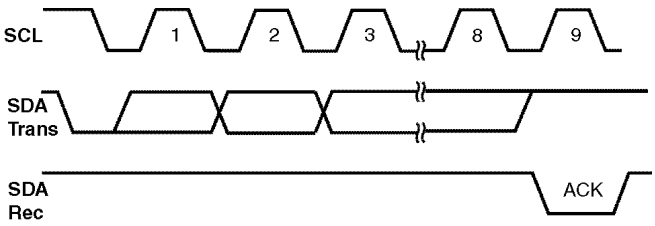


Figure 17 - Acknowledge Timing

Read and Write

The first byte from a Master is always made up of a 7-bit Slave address and the Read/Write (R/W) bit. The R/W bit tells the Slave whether the Master is reading data from the bus or writing data to the bus (1 = Read, 0 = Write). The first four of the seven address bits are called the Device Type Identifier (DTI). In the case of the SMH4814, the next two bits are Bus Address values , used to distinguish multiple devices on a common bus. The seventh bit of the slave address represents the ninth bit of the word address. The SMH4814 issues an Acknowledge after recognizing a Start condition and its DTI. Figure 18 shows an example of a typical master address byte transmission.

I²C 2-WIRE SERIAL INTERFACE (CONTINUED)

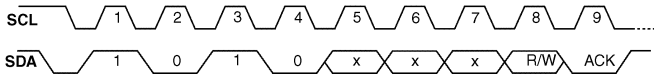


Figure 18 - Typical Master Address Byte Transmission

During a read by the Master device, the SMH4814 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected, and no Stop condition is generated by the Master, the SMH4814 continues to transmit data. If an Acknowledge is not detected (NACK), the SMH4814 terminates any subsequent data transmission. The read transfer protocol on SDA is shown in Figure 19.

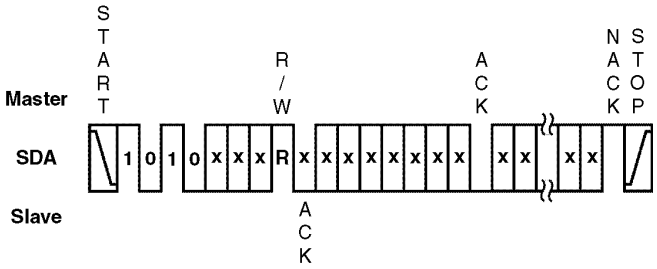


Figure 19 - Read Protocol

During a Master write, the SMH4814 receives eight bits of data, then generates an Acknowledge signal. It device continues to generate the ACK condition on SDA until a Stop condition is generated by the Master. The write transfer protocol on SDA is shown in Figure 20.

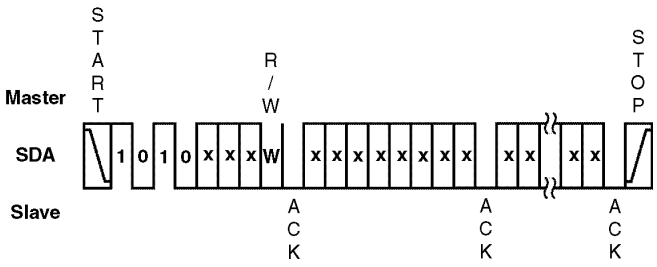


Figure 20 - Write Protocol

Random Access Read

Random address read operations allow the Master to access any memory location in a random fashion. This operation involves a two-step process. First, the Master issues a Write command which includes the Start condition and the Slave address field (with the R/W bit set to Write) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMH4814 to the desired address.

After the word address Acknowledge is received by the Master, it immediately reissues a Start condition followed by another Slave address field with the R/W bit set to Read. The SMH4814 responds with an Acknowledge and then transmits the 8 data bits stored at the addressed location. At this point, the Master sets the SDA line to NACK and generates a Stop condition. The SMH4814 discontinues data transmission and reverts to its standby power mode.

Sequential Reads

Sequential reads can be initiated as either a current address read or a random access read. The first word is transmitted as with the other byte Read modes (current address byte Read or random address byte Read). However, the Master now responds with an Acknowledge, indicating that it requires additional data from the SMH4814.

The SMH4814 continues to output data for each Acknowledge received. The Master sets the SDA line to NACK and generates a Stop condition. During a sequential Read operation the internal address counter is automatically incremented with each Acknowledge signal.

For Read operations all address bits are incremented, allowing the entire array to be read using a single Read command. After a count of the last memory address the address counter rolls over and the memory continues to output data.

I²C 2-WIRE SERIAL INTERFACE (CONTINUED)

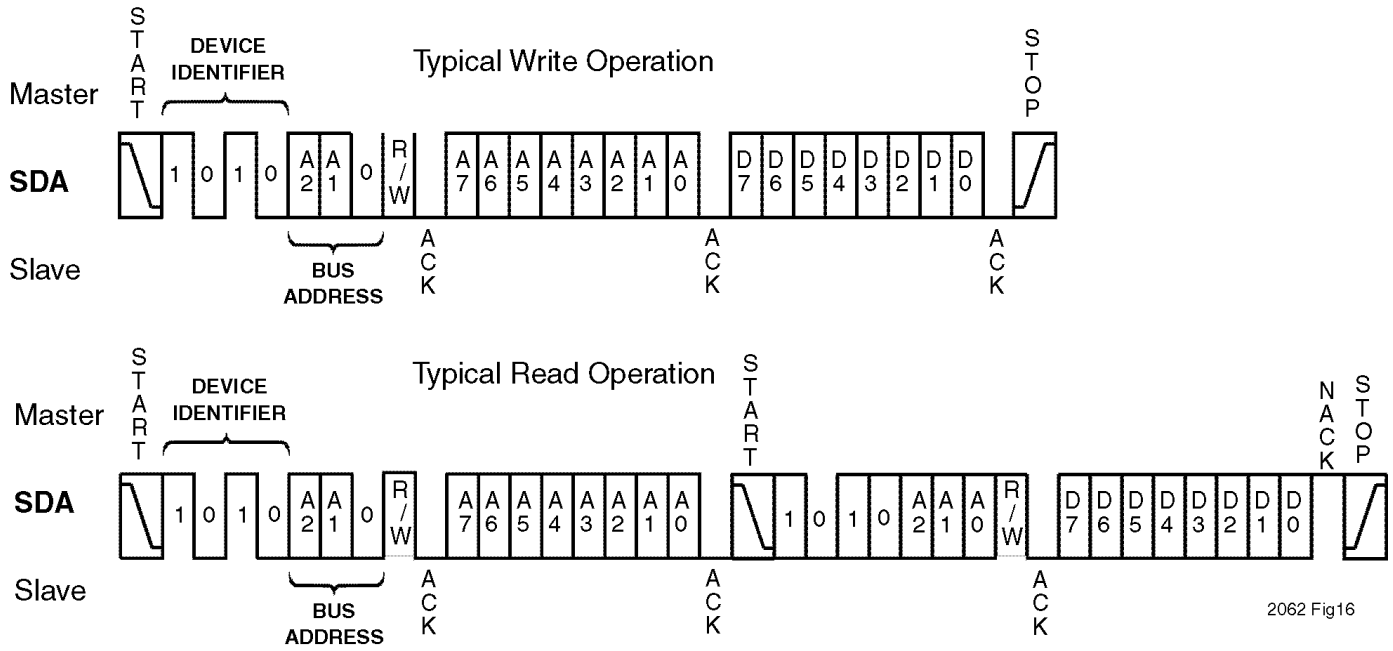


Figure 21 - Typical EE Memory Write and Random Read Operations

Register Access

The SMH4814 contains a 2-wire bus interface for register access as explained in the previous section. This bus is highly configurable, while maintaining the industry standard protocol. The SMH4814 responds to one of two selectable Device Type Addresses: 1010_{BIN}, generally assigned to NV-memories and the default address for the SMH4814, or 1011_{BIN}. The Device Type Address is assigned by programming bit 3 of Register 0x0F.

The configuration registers may be locked out by setting bit 5 of register 0x0F high. This is a one-time, non-reversible operation.

The SMH4814 has two virtual address pins, A[2:1] (set with R0F[7:6]), associated with the 2-wire bus. The SMH4814 can be configured to respond to:

1. only to the proper serial data string of the Device Type Address and specific bus addresses (Register 0x0F, bit 4 cleared).
2. the Device Type Address and any bus address (Register 0x0F, bit 4 set).

Slave Address	Bus Address	Register Type
1001_{BIN}	A2 A1 0	Command and Status Registers,
1010_{BIN} or 1011_{BIN}	A2 A1 0	2-k Bits of General-Purpose Memory
	A2 A1 1	Configuration Registers

Table 2 - Address bytes used by the SMH4814.

I²C PROGRAMMING INFORMATION (CONTINUED)

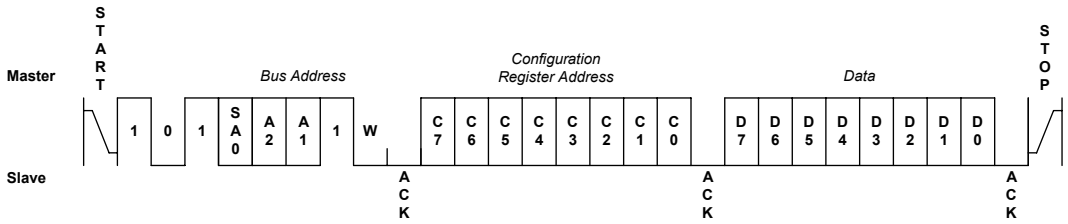


Figure 23 – Configuration Register Byte Write

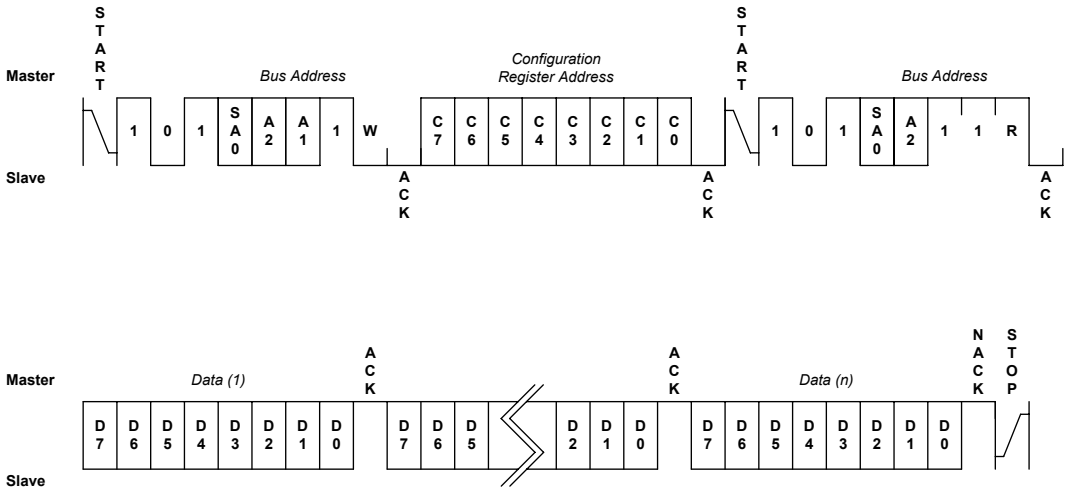


Figure 25 - Configuration Register Read

I²C PROGRAMMING INFORMATION (CONTINUED)

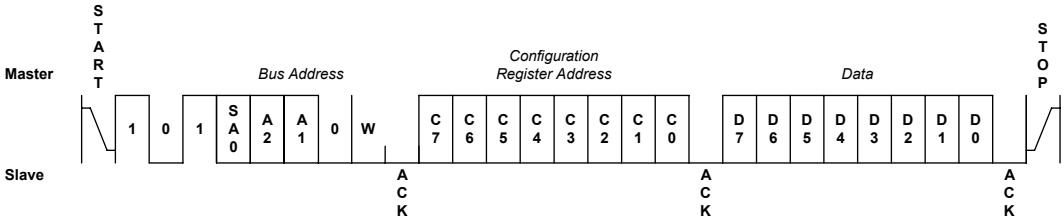
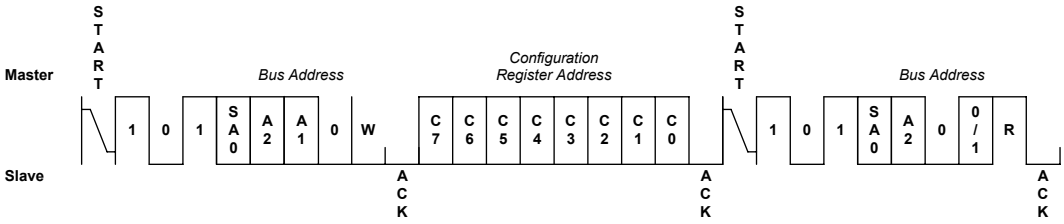


Figure 28 – General Purpose Memory Byte Write



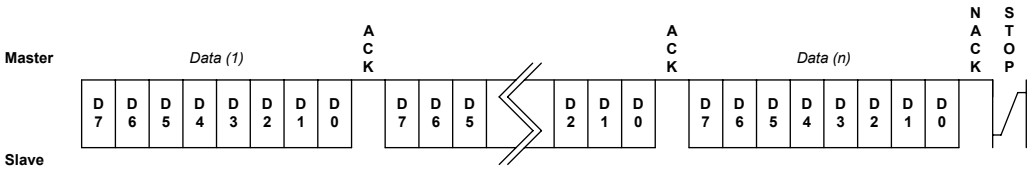


Figure 30 - General Purpose Memory Read

I²C PROGRAMMING INFORMATION (CONTINUED)

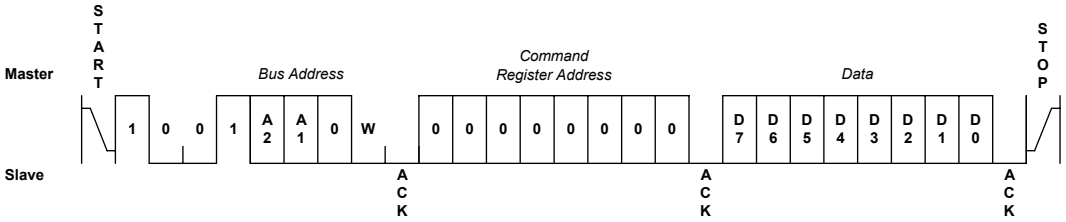
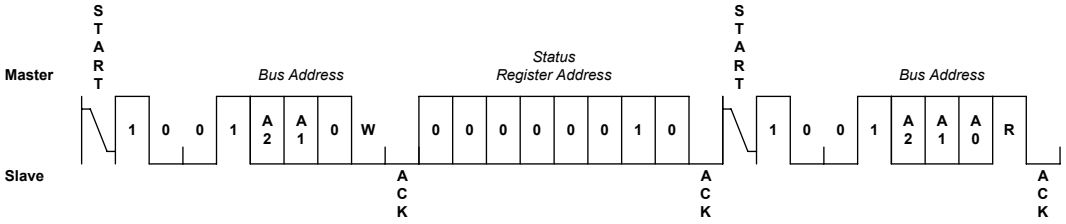


Figure 31 – Command Register Write



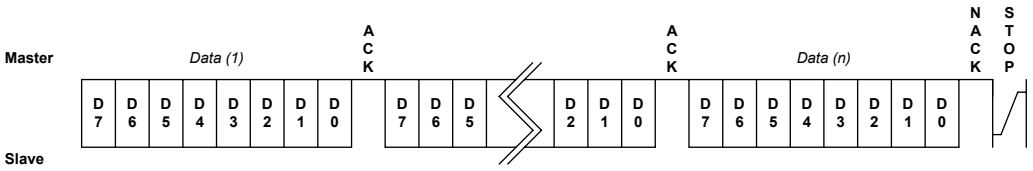


Figure 32 - Status Register Read

DEVELOPMENT HARDWARE & SOFTWARE

The end user can obtain the Summit SMX3200 programming system for device prototype development. The SMX3200 system consists of a programming Dongle, cable and Windows™ GUI software. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3200 is available from the website (www.summitmicro.com).

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus.

The Windows GUI software will generate the data and send it in I^2C serial bus format so that it can be directly downloaded to the SMH4814 via the programming Dongle and cable. An example of the connection interface is shown in Figure 34.

When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

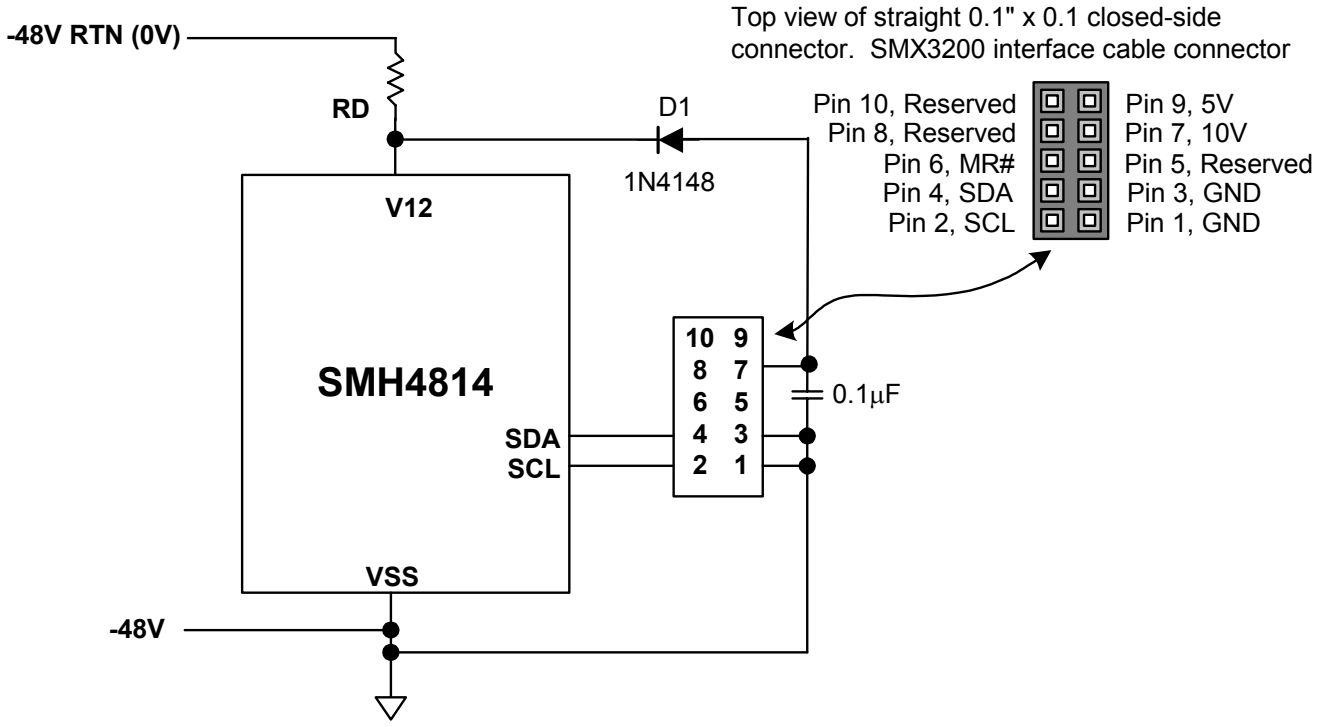


Figure 34– SMX3200 Programmer I^2C serial bus connections to program the SMH4814.
Caution: Damage may occur when connecting the dongle to a system utilizing an earth-connected positive terminal.

CONFIGURATION REGISTERS

Configuration Registers:

There are 20 user programmable configuration registers in the SMH4814. The following tables describe the configuration register bits in detail.

In cases where a timer is used, refer to the Timers Table 3 for a description of the codes required for each timeout selection.

Table 3 - Timers

All timers may be configured to one of the following sixteen choices:

Bit Code	Timer (ms)	Bit Code	Timer (ms)	Bit Code	Timer (ms)	Bit Code	Timer (ms)
0000	0.25	0100	16	1000	64	1100	256
0001	2	0101	24	1001	96	1101	384
0010	8	0110	32	1010	128	1110	512
0011	12	0111	48	1011	192	1111	768

Register R00 – Initial Current Regulation and PD power-on delay.

Bits D[7:4] control the Initial Current Regulation Timer (defines the amount of time current regulation is allowed during initial power-on). Bits D[3:0] control the Pin Detect delay (defines the time from when the PD's are enabled and UV & OV are valid until VGATE_HS is allowed to turn on)

Register R00								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	**0**	**0**	**0**	**X**	**X**	**X**	**X**	Initial Current Regulation Timer – 64ms, See Table 3
X	**X**	**X**	**X**	**1**	**0**	**0**	**0**	Pin Detect Delay – 64ms, See Table 3

Register R01 –Sequence position.

Bits D[7:4] control the Time Slot 1 (time from FB high to second PUP allowed to go active). Bits D[3:0] control the Time Slot 0, which is the time from when the FET is fully on to when the first PUP goes active.

Register R01								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	**0**	**0**	**0**	**X**	**X**	**X**	**X**	Time Slot 1 - Time from FB_X high to second PUP_X allowed to go active– 64ms, See Table 3
X	**X**	**X**	**X**	**1**	**0**	**0**	**0**	Time Slot 0 - Time from FB_X high to first PUP_X allowed to go active – 64ms, See Table 3

CONFIGURATION REGISTERS (CONTINUED)

Register R02 –Time Slots.

Bits D[7:4] control the Time Slot 1 (time from FB high to second PUP allowed to go active). Bits D[3:0] control the Time Slot 0 (time from FET fully on to first PUP allowed to go active). See timer table for bit codes.

Register R02								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	**0**	**0**	**0**	**X**	**X**	**X**	**X**	Time Slot 3 - Time from FB_X high to fourth PUP_X allowed to go active – 64ms, See Table 3
X	**X**	**X**	**X**	**1**	**0**	**0**	**0**	Time Slot 2 - Time from FB_X high to third PUP_X allowed to go active – 64ms, See Table 3

Register R03 –Duty Cycle and Sequence Termination Timers.

Bits D[7:4] control the Duty Cycle Timer (restart time after fault; short circuit detect cycle time; multiply standard times by 28X). Bits D[3:0] control the Sequence Termination Timer (defines time from PUP active until FB must go high).

Register R03								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	**0**	**1**	**1**	**X**	**X**	**X**	**X**	Duty Cycle Timer – defines the time between when a Fault occurs and the device attempts to restart the power up sequence. Note that these times are actually 28X of that listed in the table.
X	**X**	**X**	**X**	**1**	**0**	**0**	**0**	Sequence Termination Timer – time from when a PUP is enabled until its corresponding FB input must go high – 64ms, See Table 3

Register R04 –Current Regulation and UV/OV Filter Timers.

Bits D[7:4] control the Subsequent Current Regulation Timer (except for initial power on). Bits D[3:0] control the UV/OV Filter Timer (when enabled).

Register R04								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	**0**	**0**	**0**	**X**	**X**	**X**	**X**	Current Regulation Timer – defines the amount of time that the FET can be held in the linear region to regulate current to the load – 64ms, See Table 3
X	**X**	**X**	**X**	**1**	**0**	**0**	**0**	UV/OV Filter Time – defines the length of time that an under or over voltage condition must be sustained to trip the sensor – 64ms, See Table 3

CONFIGURATION REGISTERS (CONTINUED)

Register R05 – Pull-downs, Pull-ups, current regulation and fault latch.

Bits D[7:6] control the fast pull down level by the number of diodes connected in series with the gate pull-down transistor of the Quick Trip sensor. Bits D[5:4] control the GATEA/GATEB Pull-up Current. Bit D[3] controls the Current Regulation. Bit D[2] controls the Fault Latches Off versus Duty Cycle. Bits D[1:0] control the Drain Sense Glitch Filter.

Register R05								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	-	-	-	-	-	-	Fast pull down level - no diodes connected in series with the gate pull-down transistor of the Quick Trip sensor.
0	**1**	-	-	-	-	-	-	Fast pull down level –1 diode connected in series with the gate pull-down transistor of the Quick Trip sensor.
1	**0**	-	-	-	-	-	-	Fast pull down level - 2 diodes connected in series with the gate pull-down transistor of the Quick Trip sensor.
1	**1**	-	-	-	-	-	-	Fast pull down level – 3 diodes connected in series with the gate pull-down transistor of the Quick Trip sensor.
-	-	**0**	**0**	-	-	-	-	VGATEA/VGATEB Pull-up Current 10μa
-	-	**0**	**1**	-	-	-	-	VGATEA/VGATEB Pull-up Current 50μa
-	-	**1**	**0**	-	-	-	-	VGATEA/VGATEB Pull-up Current 100μa
-	-	**1**	**1**	-	-	-	-	VGATEA/VGATEB Pull-up Current 200μa)
-	-	-	-	**0**	-	-	-	Enable Current regulation.
-	-	-	-	**1**	-	-	-	Disable Current regulation.
-	-	-	-	-	**0**	-	-	Fault condition must be manually cleared
-	-	-	-	-	**1**	-	-	Fault cleared after Duty cycle timeout
-	-	-	-	-	-	**0**	**0**	Drain Sense Glitch Filter is 1μs.
-	-	-	-	-	-	**0**	**1**	Drain Sense Glitch Filter is 14μs.
-	-	-	-	-	-	**1**	**0**	Drain Sense Glitch Filter is 40μs.
-	-	-	-	-	-	**1**	**1**	Drain Sense Glitch Filter is 119μs.

CONFIGURATION REGISTERS (CONTINUED)

Register R06 – Glitch Filters.

Bits D[7:6] control the UV/OV Glitch Filter. Bits D[5:4] control the RESET# Glitch Filter. Bits D[3:2] control the FBX Glitch Filter. Bits D[1:0] control the CBSENSE Glitch Filter.

Register R06								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**-**	**-**	**-**	**-**	**-**	**-**	UV/OV Glitch Filter is 1µs.
0	**1**	**-**	**-**	**-**	**-**	**-**	**-**	UV/OV Glitch Filter is 14µs.
1	**0**	**-**	**-**	**-**	**-**	**-**	**-**	UV/OV Glitch Filter is 40µs.
1	**1**	**-**	**-**	**-**	**-**	**-**	**-**	UV/OV Glitch Filter is 119µs.
-	**-**	**0**	**0**	**-**	**-**	**-**	**-**	RESET# Glitch Filter is 1µs.
-	**-**	**0**	**1**	**-**	**-**	**-**	**-**	RESET# Glitch Filter is 14µs.
-	**-**	**1**	**0**	**-**	**-**	**-**	**-**	RESET# Glitch Filter is 40µs.
-	**-**	**1**	**1**	**-**	**-**	**-**	**-**	RESET# Glitch Filter is 119µs.
-	**-**	**-**	**-**	**0**	**0**	**-**	**-**	FBX Glitch Filter is 1µs.
-	**-**	**-**	**-**	**0**	**1**	**-**	**-**	FBX Glitch Filter is 14µs.
-	**-**	**-**	**-**	**1**	**0**	**-**	**-**	FBX Glitch Filter is 40µs.
-	**-**	**-**	**-**	**1**	**1**	**-**	**-**	FBX Glitch Filter is 119µs.
-	**-**	**-**	**-**	**-**	**-**	**0**	**0**	CBSENSE Glitch Filter is 1µs.
-	**-**	**-**	**-**	**-**	**-**	**0**	**1**	CBSENSE Glitch Filter is 14µs.
-	**-**	**-**	**-**	**-**	**-**	**1**	**0**	CBSENSE Glitch Filter is 40µs.
-	**-**	**-**	**-**	**-**	**-**	**1**	**1**	CBSENSE Glitch Filter is 119µs.

Register R07 – FEEDA/B Current.

Bits D[7:4] control the FEED Offset Current. Bits D[3:0] control the FEED Hysteresis Current

Register R07								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	**0**	**0**	**0**	**X**	**X**	**X**	**X**	FEED Offset Current is defined by the value in this register, plus 10 uA. The range of offset current is 10-25uA. The default value shown here represents 18uA (8b+10).
X	**X**	**X**	**X**	**1**	**0**	**0**	**0**	FEED Hysteresis current ranges from 0-15ua. The default shown here is 8uA

CONFIGURATION REGISTERS (CONTINUED)

Register R08 – OV/UV Hysteresis.

Bits D[7:4] control the OV Hysteresis Voltage level. Bits D[4:0] control the UV Hysteresis Voltage level.

Register R08								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**1**	**0**	**0**	**X**	**X**	**X**	**X**	OV Hysteresis = ((n+1)*32), where n is the value stored in bits 7:4. OV Hystersis ranges from 32mV to 512mV, with a default value (shown here) of 160mV
X	**X**	**X**	**X**	**0**	**1**	**0**	**0**	UV Hysteresis = ((n+1)*32), where n is the value stored in bits 7:4. UV Hystersis ranges from 32mV to 512mV, with a default value (shown here) of 160mV

Register R09 – Current regulation Offsets, Current DAC max and OV/UV reference voltage

Bits D[7:6] control the Current Regulation Offset. Bits D[5:4] control the Current DAC Max Voltage. Bits D[3:2] control the OV reference voltage range. Bits D[1:0] control the UV reference voltage range.

Register R09								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**-**	**-**	**-**	**-**	**-**	**-**	Current Regulation Offset is 12.5% (This is the percentage above the Over Current trip point at which current is regulated)
0	**1**	**-**	**-**	**-**	**-**	**-**	**-**	Current Regulation Offset is 25%
1	**0**	**-**	**-**	**-**	**-**	**-**	**-**	Current Regulation Offset is 50%
1	**1**	**-**	**-**	**-**	**-**	**-**	**-**	Current Regulation Offset is 100%
-	**-**	**0**	**0**	**-**	**-**	**-**	**-**	Current DAC Max Voltage is 128mV
-	**-**	**0**	**1**	**-**	**-**	**-**	**-**	Current DAC Max Voltage is 256mV (default)
-	**-**	**1**	**0**	**-**	**-**	**-**	**-**	Current DAC Max Voltage is 512mV
-	**-**	**1**	**1**	**-**	**-**	**-**	**-**	Current DAC Max Voltage is 1.024V
-	**-**	**-**	**-**	**0**	**0**	**-**	**-**	OV Reference is 2.048V
-	**-**	**-**	**-**	**0**	**1**	**-**	**-**	OV Reference is 2.864V
-	**-**	**-**	**-**	**1**	**0**	**-**	**-**	OV Reference is 3.072V
-	**-**	**-**	**-**	**1**	**1**	**-**	**-**	OV Reference is 4.096V
-	**-**	**-**	**-**	**-**	**-**	**0**	**0**	UV Reference is 2.048V
-	**-**	**-**	**-**	**-**	**-**	**0**	**1**	UV Reference is 2.864V
-	**-**	**-**	**-**	**-**	**-**	**1**	**0**	UV Reference is 3.072V
-	**-**	**-**	**-**	**-**	**-**	**1**	**1**	UV Reference is 4.096V

CONFIGURATION REGISTERS (CONTINUED)

Register R0A – Over Current Level

Bits D[7:0] control the Over Current Level.

Register R0A								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**1**	**1**	**0**	**0**	**1**	**0**	Over Current Level = Current DAC Max Voltage (R09[5:4]) * n/256, where n is the value in this register. The default value (shown here) is 50mV

Register R0B – Quick-Trip™ Over Current Level.

Bits D[7:0] control the Fast Response Over Current Level

Register R0B								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	**0**	**0**	**1**	**1**	**1**	**0**	**0**	Fast Response Over Current Level (2's complement) = Current DAC Max Voltage * (256-n)/256. The default value (shown here) is 100mV.

Register R0C – PUP_X Sequence Time Slot

Bits D[7:6] control the PUP_D Time Slot. Bits D[5:4] control the PUP_C Time Slot. Bits D[3:2] control the PUP_B Time Slot. Bits D[1:0] control the PUP_A Time Slot.

Register R0C								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**-**	**-**	**-**	**-**	**-**	**-**	PUP_D Time Slot = 0
0	**1**	**-**	**-**	**-**	**-**	**-**	**-**	PUP_D Time Slot = 1
1	**0**	**-**	**-**	**-**	**-**	**-**	**-**	PUP_D Time Slot = 2
1	**1**	**-**	**-**	**-**	**-**	**-**	**-**	PUP_D Time Slot = 3
-	**-**	**0**	**0**	**-**	**-**	**-**	**-**	PUP_C Time Slot = 0
-	**-**	**0**	**1**	**-**	**-**	**-**	**-**	PUP_C Time Slot = 1
-	**-**	**1**	**0**	**-**	**-**	**-**	**-**	PUP_C Time Slot = 2
-	**-**	**1**	**1**	**-**	**-**	**-**	**-**	PUP_C Time Slot = 3
-	**-**	**-**	**-**	**0**	**0**	**-**	**-**	PUP_B Time Slot = 0
-	**-**	**-**	**-**	**0**	**1**	**-**	**-**	PUP_B Time Slot = 1
-	**-**	**-**	**-**	**1**	**0**	**-**	**-**	PUP_B Time Slot = 2
-	**-**	**-**	**-**	**1**	**1**	**-**	**-**	PUP_B Time Slot = 3
-	**-**	**-**	**-**	**-**	**-**	**0**	**0**	PUP_A Time Slot = 0
-	**-**	**-**	**-**	**-**	**-**	**0**	**1**	PUP_A Time Slot = 1
-	**-**	**-**	**-**	**-**	**-**	**1**	**0**	PUP_A Time Slot = 2
-	**-**	**-**	**-**	**-**	**-**	**1**	**1**	PUP_A Time Slot = 3

CONFIGURATION REGISTERS (CONTINUED)

Register R0D – Power Down or Forced Shutdown, Fault or no Fault

These bits control how the given inputs affect the power off.

Register R0D								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	FB low w/ FET on: Power Down
1	-	-	-	-	-	-	-	FB low w/ FET on: Forced Shutdown
-	**0**	-	-	-	-	-	-	ENTS low w/ FET on: Power Down
-	**1**	-	-	-	-	-	-	ENTS low w/ FET on: Forced Shutdown
-	-	**0**	-	-	-	-	-	OV condition: Power Down
-	-	**1**	-	-	-	-	-	OV condition: Forced Shutdown
-	-	-	**0**	-	-	-	-	UV condition: Power Down
-	-	-	**1**	-	-	-	-	UV condition: Forced Shutdown
-	-	-	-	**0**	-	-	-	FB low w/ FET on: don't set FAULT
-	-	-	-	**1**	-	-	-	FB low w/ FET on: set FAULT
-	-	-	-	-	**0**	-	-	ENTS low w/ FET on: don't set FAULT
-	-	-	-	-	**1**	-	-	ENTS low w/ FET on: set FAULT
-	-	-	-	-	-	**0**	-	OV condition: don't set FAULT
-	-	-	-	-	-	**1**	-	OV condition: set FAULT
-	-	-	-	-	-	-	**0**	UV condition: don't set FAULT
-	-	-	-	-	-	-	**1**	UV condition: set FAULT

Register R0E – Slew Rate Control

Bits D[7:6] control the PUP_D Time Slot. Bits D[5:4] control the PUP_C Time Slot. Bits D[3:2] control the PUP_B Time Slot. Bits D[1:0] control the PUP_A Time Slot.

Register R0E								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	-	-	-	-	-	-	Scale Factor SLEW_CNTL to Curr. Reg. = 1/100
0	**1**	-	-	-	-	-	-	Scale Factor SLEW_CNTL to Curr. Reg. = 1/50
1	**0**	-	-	-	-	-	-	Scale Factor SLEW_CNTL to Curr. Reg. = 1/20
1	**1**	-	-	-	-	-	-	Scale Factor SLEW_CNTL to Curr. Reg. = 1/10
-	-	**0**	-	-	-	-	-	Use SLEW_CNTL for Current Regulation Voltage = Curr. Reg. Voltage is fixed by registers R09 and R0A
-	-	**1**	-	-	-	-	-	Use SLEW_CNTL for Current Regulation Voltage = Curr. Reg. Voltage = SLEW CNTL*scale factor D[7:6]
-	-	-	**0**	-	-	-	-	Use SLEW_CNTL for FET GATE Current Ramp = FET GATE current is fixed at Max Current
-	-	-	**1**	-	-	-	-	Use SLEW_CNTL for FET GATE Current Ramp = FET GATE current = (Max Current)*(SLEW CNTL)/2.5
-	-	-	-	**1**	**1**	**1**	**1**	Max FET GATE Current = (8+(n X 8))μA Largest FET GATE Current = (8+(15 X 8)) = 136μA
-	-	-	-	**0**	**0**	**0**	**0**	Lowest FET GATE Current = (8+(0 X 8)) = 8μA
-	-	-	-	**1**	**0**	**1**	**1**	FET GATE Current = (8+(11 X 8)) = 96μA

CONFIGURATION REGISTERS (CONTINUED)

Register R0F – Interface Control

Register R0F								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	Virtual Bus Address A2 = 0
1	-	-	-	-	-	-	-	Virtual Bus Address A2 = 1
-	**0**	-	-	-	-	-	-	Virtual Bus Address A1 = 0
-	**1**	-	-	-	-	-	-	Virtual Bus Address A1 = 1
-	-	**0**	-	-	-	-	-	Configuration lockout = unlocked
-	-	**1**	-	-	-	-	-	Configuration lockout = locked
-	-	-	**0**	-	-	-	-	Respond to only respond to virtual bus address match
-	-	-	**1**	-	-	-	-	Respond to all bus addresses
-	-	-	-	**0**	-	-	-	Slave Address = 1010
-	-	-	-	**1**	-	-	-	Slave Address = 1011
-	-	-	-	-	**0**	-	-	Enable PD's = Disabled
-	-	-	-	-	**1**	-	-	Enable PD's = Enabled
-	-	-	-	-	-	**0**	-	Enable OV filter delay = Disabled
-	-	-	-	-	-	**1**	-	Enable OV filter delay = Enabled
-	-	-	-	-	-	-	**0**	Enable UV filter delay = Disabled
-	-	-	-	-	-	-	**1**	Enable UV filter delay =-Enabled

CONFIGURATION REGISTERS (CONTINUED)

Register R10 – Power Down or Forced Shutdown, Fault or no Fault

.

Register R10								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**-**	**-**	**-**	**-**	**-**	**-**	Shorted FET Detection disabled
0	**1**	**-**	**-**	**-**	**-**	**-**	**-**	Shorted FET sets fault
1	**0**	**-**	**-**	**-**	**-**	**-**	**-**	Shorted FET causes power down
1	**1**	**-**	**-**	**-**	**-**	**-**	**-**	Shorted FET causes forced shutdown
-	**-**	**0**	**0**	**-**	**-**	**-**	**-**	Blown Fuse Detection disabled
-	**-**	**0**	**1**	**-**	**-**	**-**	**-**	Blown sets fault
-	**-**	**1**	**0**	**-**	**-**	**-**	**-**	Blown causes power down
-	**-**	**1**	**1**	**-**	**-**	**-**	**-**	Blown causes forced shutdown
-	**-**	**-**	**-**	**0**	**-**	**-**	**-**	Enable Fuse Check High (works in conjunction with R10 D[5:4])
-	**-**	**-**	**-**	**1**	**-**	**-**	**-**	Disable Fuse Check High (works in conjunction with R10 D[5:4])
-	**-**	**-**	**-**	**-**	**0**	**-**	**-**	Disable Periodic Fuse Checking
-	**-**	**-**	**-**	**-**	**1**	**-**	**-**	Enable Periodic Fuse Checking
-	**-**	**-**	**-**	**-**	**-**	**0**	**0**	Short Circuit Level = 256V (defines the amount Drain Sense has to move during Short Detect)
-	**-**	**-**	**-**	**-**	**-**	**0**	**1**	Short Circuit Level = 512V (defines the amount Drain Sense has to move during Short Detect)
-	**-**	**-**	**-**	**-**	**-**	**1**	**0**	Short Circuit Level = 1.024V (defines the amount Drain Sense has to move during Short Detect)
-	**-**	**-**	**-**	**-**	**-**	**1**	**1**	Short Circuit Level = 2.048V (defines the amount Drain Sense has to move during Short Detect)

Register R11 – PUP polarity, Power-up command.

.

Register R11								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**-**	**-**	**-**	**-**	**-**	**-**	**-**	Command Not Required for Power-Up
1	**-**	**-**	**-**	**-**	**-**	**-**	**-**	Command is Required for Power-Up
-	**0**	**0**	**0**	**-**	**-**	**-**	**-**	Power Up/Down Configuration
-	**-**	**-**	**-**	**0**	**-**	**-**	**-**	PUP_D polarity = active low
-	**-**	**-**	**-**	**1**	**-**	**-**	**-**	PUP_D polarity = active high
-	**-**	**-**	**-**	**-**	**0**	**-**	**-**	PUP_C polarity = active low
-	**-**	**-**	**-**	**-**	**1**	**-**	**-**	PUP_C polarity = active high
-	**-**	**-**	**-**	**-**	**-**	**0**	**-**	PUP_B polarity = active low
-	**-**	**-**	**-**	**-**	**-**	**1**	**-**	PUP_B polarity = active high
-	**-**	**-**	**-**	**-**	**-**	**-**	**0**	PUP_A polarity = active low
-	**-**	**-**	**-**	**-**	**-**	**-**	**1**	PUP_A polarity = active high

CONFIGURATION REGISTERS (CONTINUED)

Register R12 – Write protect and Write lockout, feedback pin control settings.

Register R12								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	-	-	-	-	-	-	Not Used
-	-	**0**	-	-	-	-	-	Set WP on Power-up (0-don't set WP; 1-set WP)
-	-	**1**	-	-	-	-	-	Set WP on Power-up (0-don't set WP; 1-set WP)
-	-	-	**0**	-	-	-	-	Write Lockout = allows writes to the config or memory)
-	-	-	**1**	-	-	-	-	Write Lockout = prevents writes to the config or memory
-	-	-	-	**0**	-	-	-	FBD enable = disable pin input
-	-	-	-	**1**	-	-	-	FBD enable = enable pin input
-	-	-	-	-	**0**	-	-	FBC enable = disable pin input
-	-	-	-	-	**1**	-	-	FBC enable = enable pin input
-	-	-	-	-	-	**0**	-	FBB enable = disable pin input
-	-	-	-	-	-	**1**	-	FBB enable = enable pin input
-	-	-	-	-	-	-	**0**	FBA enable = disable pin input
-	-	-	-	-	-	-	**1**	FBA enable = enable pin input

Fault/Status Registers

The following tables describe the 24 bits within the Fault/Status Registers. When Bit 7 of Register 0x04 (Slave address 1001) is low, then the data within these registers represents the real-time state of the part. When Bit 7 is high, then these registers represent data that was latched at the time that the Fault occurred. There are three Status/Fault Registers, accessed at slave address 1001 with address bit A8 set low, at word address 0x02-0x04.

Register 0x02 Bit #	**Description**
7	PUP_D
6	PUP_C
5	PUP_B
4	PUP_A
3	FB_D
2	FB_C
1	FB_B
0	FB_A

Regsiter 0x03 Bit #	**Description**
7	GATEB OFF
6	GATEA OFF
5	Over-Current Fault
4	FET is ON
3	ENTS Fault
2	PD Fault
1	OV Fault
0	UV Fault

Regsiter 0x04 Bit #	**Description**
7	Fault Register is Latched
6	Write Protect Status
5	reserved
4	reserved
3	FB Fault
2	reserved
1	reserved
0	reserved

DEFAULT CONFIGURATION REGISTER SETTINGS – SMH4814NC-184

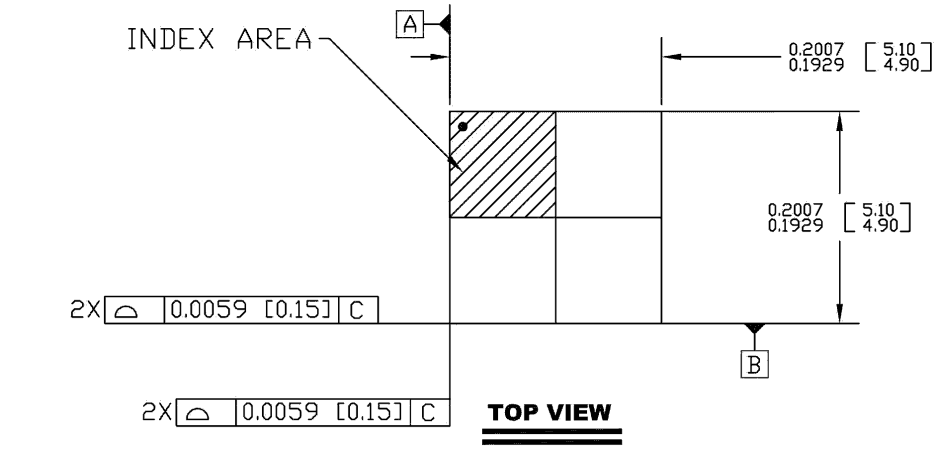
Register	Contents	Register	Contents
R00	88	R0A	32
R01	88	R0B	64
R02	88	R0C	E4
R03	B8	R0D	F8
R04	88	R0E	78
R05	56	R0F	12
R06	AA	R10	02
R07	88	R11	00
R08	44	R12	0F
R09	59		

The default device ordering number is SMH4814NC-184, is programmed as described above and tested over the commercial temperature range.

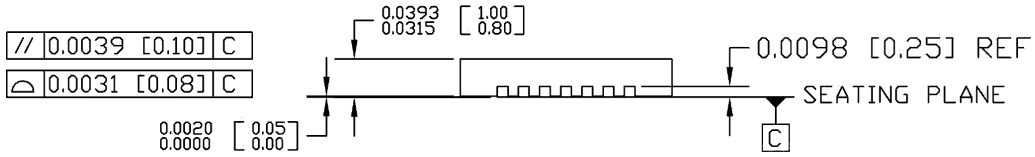
PACKAGING

28 Pad QFN

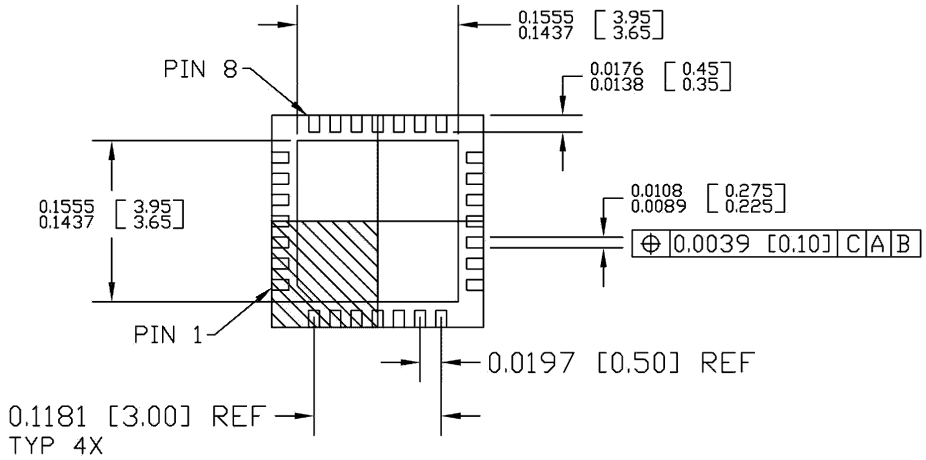
REFERENCE JEDEC MO-220



TOP VIEW



SIDE VIEW

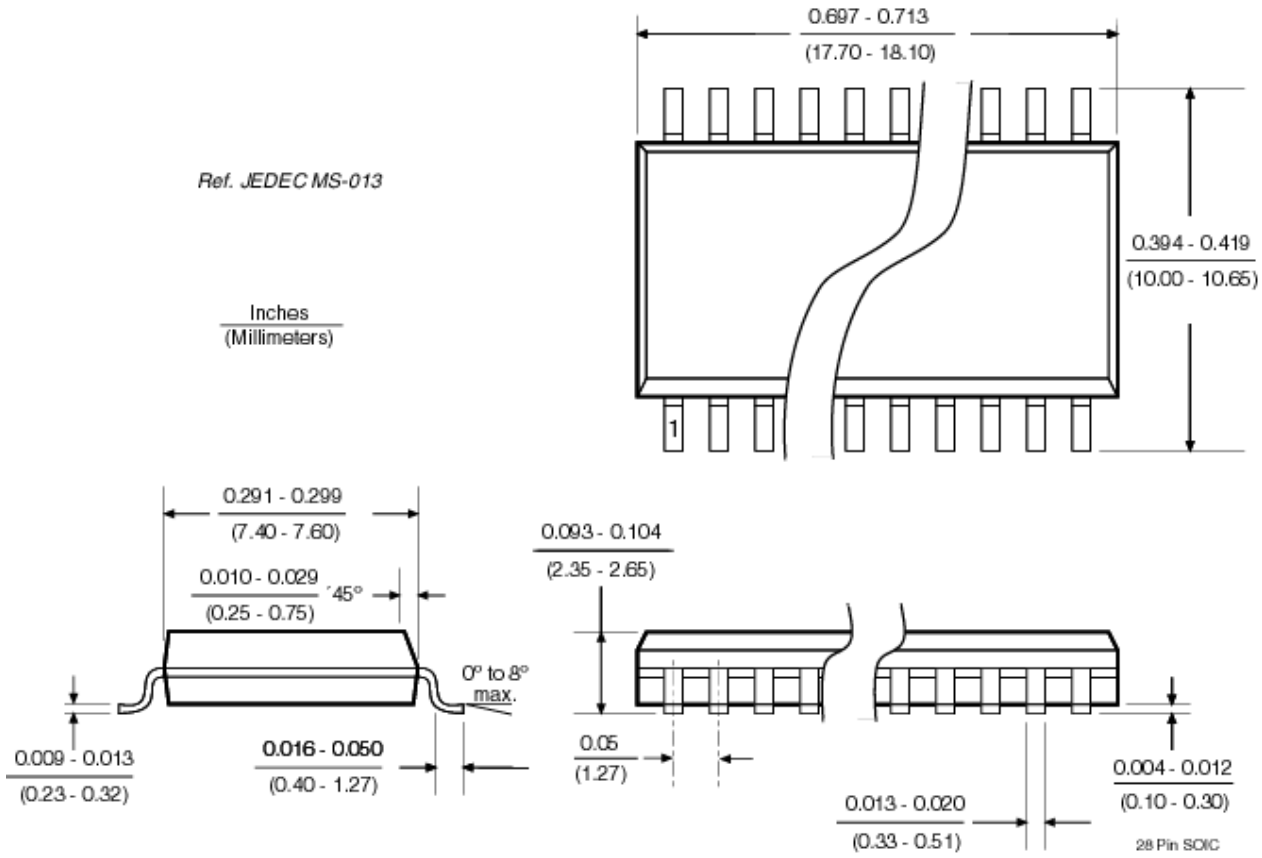


BOTTOM VIEW

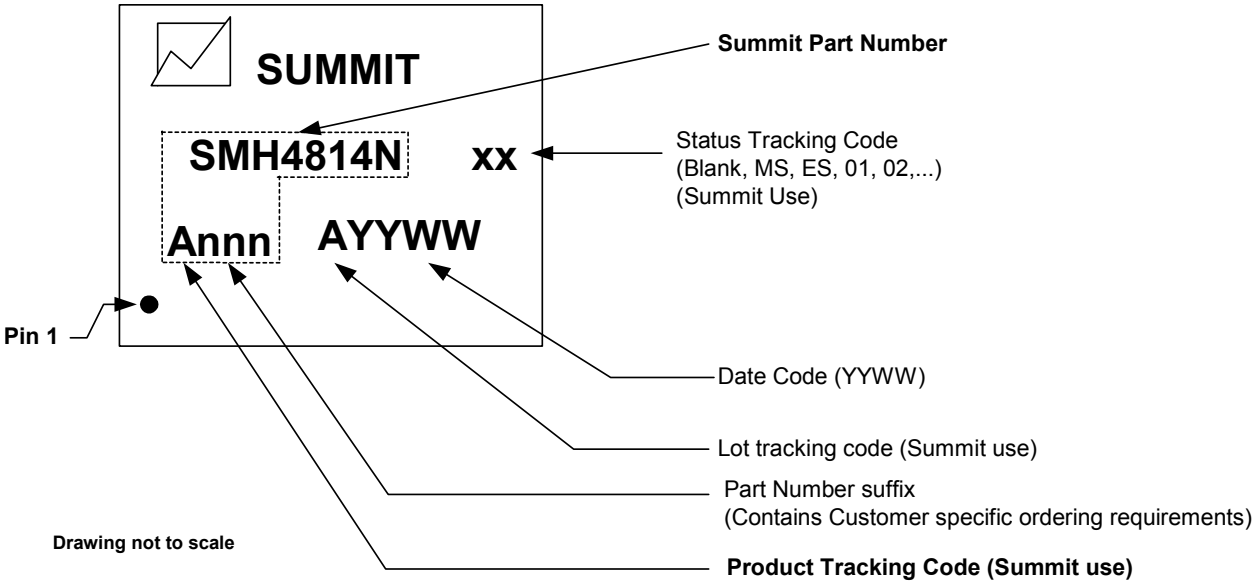
Inches Max [mm Max
Inches Min mm Min]

PACKAGING

28 Pin SOIC



PART MARKING



ORDERING INFORMATION

SMH4814 N C nnn

Summit Part Number

Package
N = 28 Pad QFN
S = 28 Lead SOIC

Temp Range
C=Commercial
Blank=Industrial

Part Number Suffix (see page 41)
Customer specific requirements are contained in the suffix such as Hex code, Hex code revision, etc.

NOTICE

NOTE 1 - NOTE 1 - This is a ***Preliminary Information*** data sheet that describes a Summit product currently in pre-production with limited characterization.

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