



### GENERAL DESCRIPTION

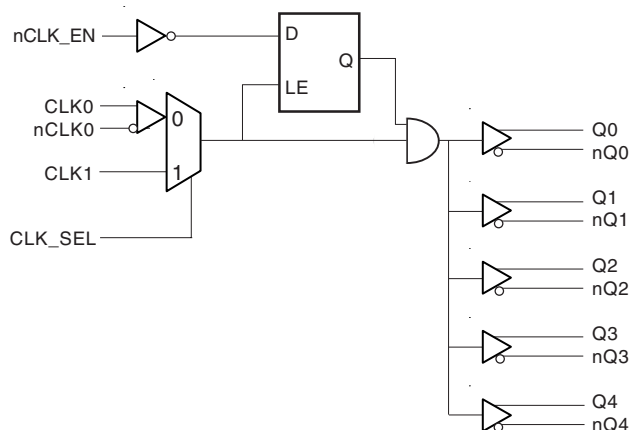


The ICS85214I is a low skew, high performance 1-to-5 Differential-to-HSTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The CLK0, nCLK0 pair can accept most standard differential input levels. The single ended CLK1 input accepts LVCMOS or LVTTTL input levels. Guaranteed output and part-to-part skew characteristics make the ICS85214I ideal for those clock distribution applications demanding well defined performance and repeatability.

### FEATURES

- 5 differential HSTL compatible outputs
- Selectable differential CLK0, nCLK0 or LVCMOS/LVTTTL clock inputs
- CLK0, nCLK0 pair can accept the following differential input levels: LVDS, LVPECL, HSTL, SSTL, HCSL
- CLK1 can accept the following input levels: LVCMOS or LVTTTL
- Output frequency up to 700MHz
- Translates any single ended input signal to HSTL levels with resistor bias on nCLK0 input
- Output skew: 40ps (maximum)
- Part-to-part skew: 300ps (maximum)
- Propagation delay: 1.8ns (maximum)
- 3.3V core, 1.8V output operating supply
- Lead-Free package fully RoHS compliant
- -40°C to 85°C ambient operating temperature

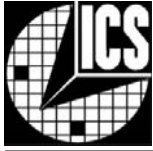
### BLOCK DIAGRAM



### PIN ASSIGNMENT

Q0	1	20	VDD0
nQ0	2	19	nCLK_EN
Q1	3	18	VDD
nQ1	4	17	nc
Q2	5	16	CLK1
nQ2	6	15	CLK0
Q3	7	14	nCLK0
nQ3	8	13	nc
Q4	9	12	CLK_SEL
nQ4	10	11	GND

**ICS85214I**  
**20-Lead TSSOP**  
6.5mm x 4.4mm x 0.92mm package body  
**G Package**  
Top View



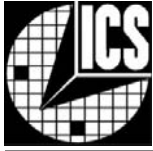
**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. HSTL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. HSTL interface levels.
5, 6	Q2, nQ2	Output		Differential output pair. HSTL interface levels.
7, 8	Q3, nQ3	Output		Differential output pair. HSTL interface levels.
9, 10	Q4, nQ4	Output		Differential output pair. HSTL interface levels.
11	GND	Power		Power supply ground.
12	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0, nCLK0 input. LVTTTL / LVCMOS interface levels.
13, 17	nc	Unused		No connect.
14	nCLK0	Input	Pullup	Inverting differential clock input.
15	CLK0	Input	Pulldown	Non-inverting differential clock input.
16	CLK1	Input	Pulldown	Clock input. LVTTTL / LVCMOS interface levels.
18	V <sub>DD</sub>	Power		Core supply pin.
19	nCLK_EN	Input	Pulldown	Synchronizing clock enable. When LOW, clock outputs follow clock input. When HIGH, Q outputs are forced low, nQ outputs are forced high. LVTTTL / LVCMOS interface levels.
20	V <sub>DDO</sub>	Power		Output supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

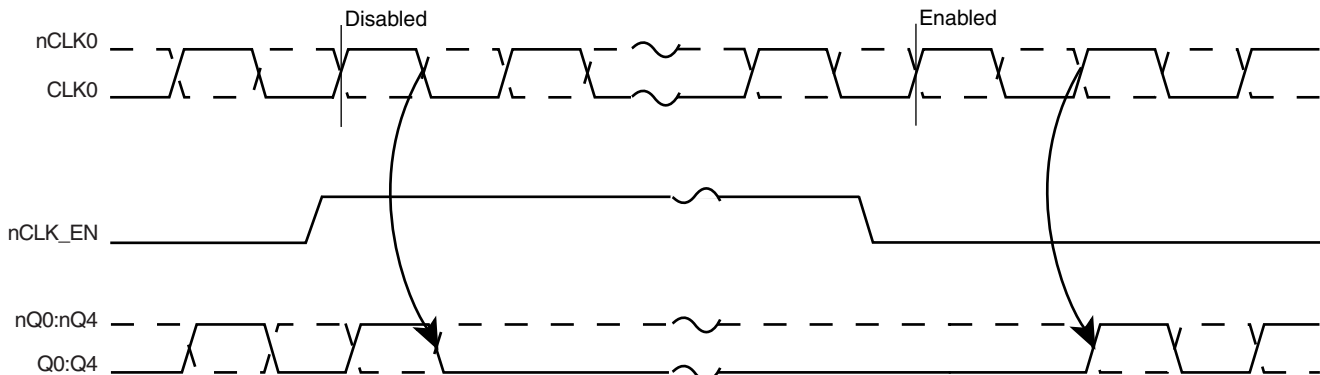


**TABLE 3A. CONTROL INPUT FUNCTION TABLE**

Inputs	Outputs	
nCLK_EN	Q0:Q4	nQ0:nQ4
0	Enabled	Enabled
1	Disabled; LOW	Disabled; HIGH

After nCLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

In the active mode, the state of the outputs are a function of the CLK0, nCLK0 inputs as described in Table 3B.



**FIGURE 1. nCLK\_EN TIMING DIAGRAM**

**TABLE 3B. CLOCK INPUT FUNCTION TABLE**

Inputs				Outputs		Input to Output Mode	Polarity
CLK_SEL	CLK0	nCLK0	CLK1	Q0:Q4	nQ0:nQ4		
0	0	1	X	LOW	HIGH	Differential to Differential	Non Inverting
0	1	0	X	HIGH	LOW	Differential to Differential	Non Inverting
0	0	Biased; NOTE 1	X	LOW	HIGH	Single Ended to Differential	Non Inverting
0	1	Biased; NOTE 1	X	HIGH	LOW	Single Ended to Differential	Non Inverting
0	Biased; NOTE 1	0	X	HIGH	LOW	Single Ended to Differential	Inverting
0	Biased; NOTE 1	1	X	LOW	HIGH	Single Ended to Differential	Inverting
1	X	X	0	LOW	HIGH	Single Ended to Differential	Non Inverting
1	X	X	1	HIGH	LOW	Single Ended to Differential	Non Inverting

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	73.2°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Input Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Power Supply Voltage		1.6	1.8	2.0	V
$I_{DD}$	Power Supply Current				80	mA

**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

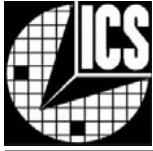
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	nCLK_EN, CLK_SEL	2		$V_{DD} + 0.3$	V
		CLK1	2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	nCLK_EN, CLK_SEL	-0.3		0.8	V
		CLK1	-0.3		1.3	V
$I_{IH}$	Input High Current	CLK1, CLK_SEL, nCLK_EN $V_{DD} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IL}$	Input Low Current	CLK1, CLK_SEL, nCLK_EN $V_{DD} = 3.465V, V_{IN} = 0V$	-5			$\mu A$

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	nCLK0	$V_{DD} = V_{IN} = 3.465V$		5	$\mu A$
		CLK0	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
$I_{IL}$	Input Low Current	nCLK0	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
		CLK0	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		0.5		$V_{DD} - 0.85$	V

NOTE 1: For single ended applications the maximum input voltage for CLK0, nCLK0 is  $V_{DD} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .



**TABLE 4D. HSTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		1		1.4	V
$V_{OL}$	Output Low Voltage; NOTE 1		0		0.4	V
$V_{OX}$	Output Crossover Voltage		$38\% \times (V_{OH} - V_{OL}) + V_{OL}$		$60\% \times (V_{OH} - V_{OL}) + V_{OL}$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

NOTE 1: Outputs terminated with  $50\Omega$  to ground.

**TABLE 5. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency	CLK0, nCLK0			700	MHz
		CLK1			300	MHz
$t_{PD}$	Propagation Delay; NOTE 1	$f \leq 700MHz$	1.0		1.8	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4				40	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				300	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		800	ps
odc	Output Duty Cycle	CLK0, nCLK0	46		54	%
		CLK1	$f \leq 266MHz$	44		56

All parameters measured at  $f_{MAX}$  unless noted otherwise.

The cycle to cycle jitter on the input will equal the jitter on the output. The part does not add jitter.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

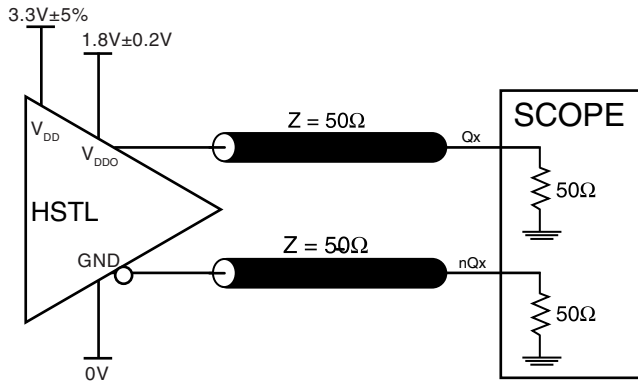
Measured at output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

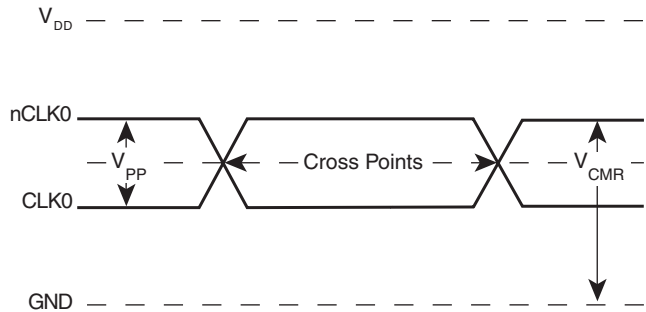
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



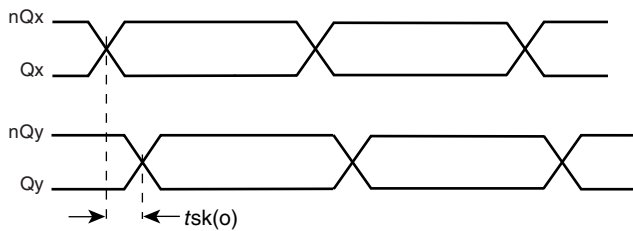
## PARAMETER MEASUREMENT INFORMATION



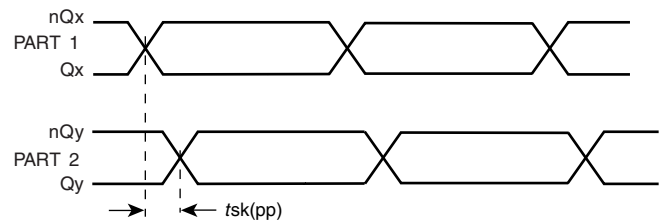
**3.3V/1.8V OUTPUT LOAD AC TEST CIRCUIT**



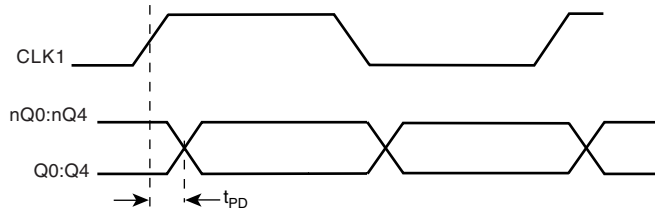
**DIFFERENTIAL INPUT LEVEL**



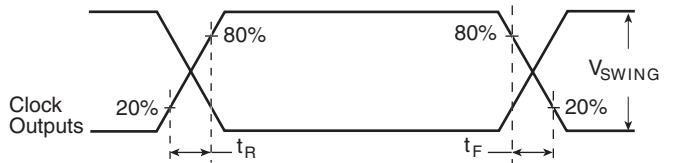
**OUTPUT SKEW**



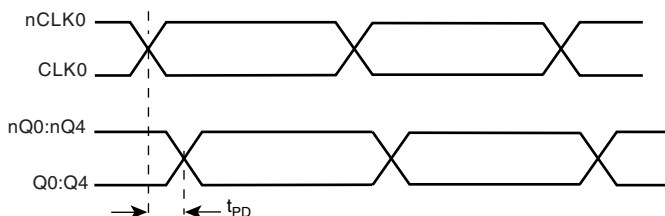
**PART-TO-PART SKEW**



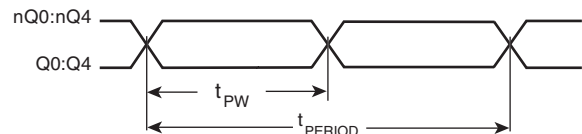
**PROPAGATION DELAY**



**OUTPUT RISE/FALL TIME**

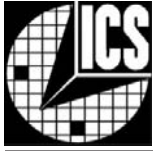


**PROPAGATION DELAY**



**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$



## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

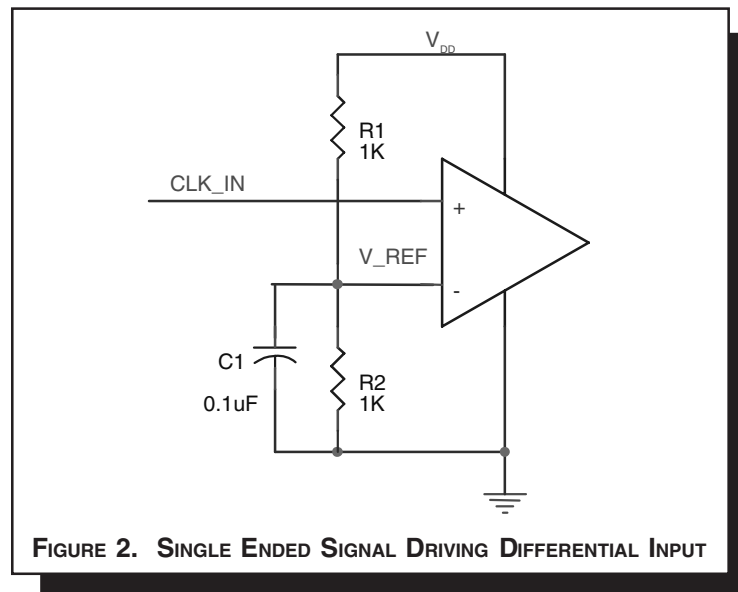
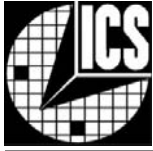


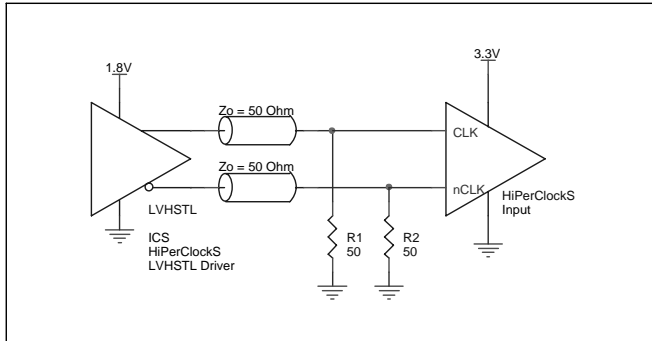
FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT



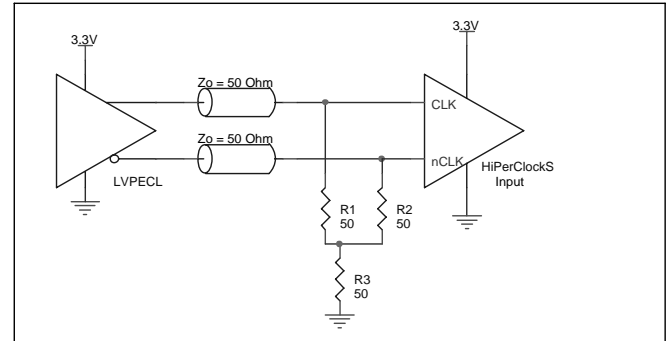
### DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

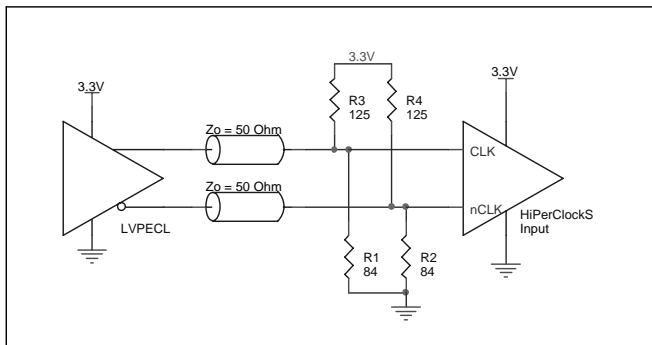
here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A*, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



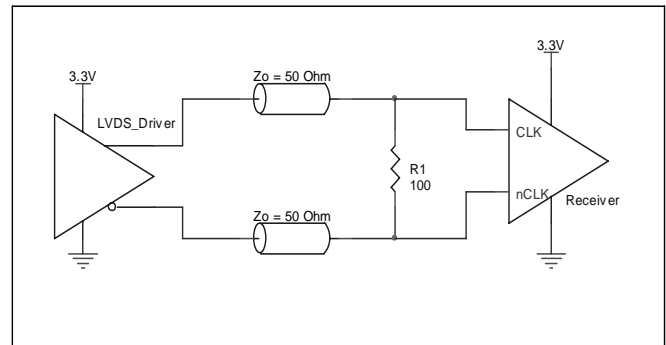
**FIGURE 3A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER**



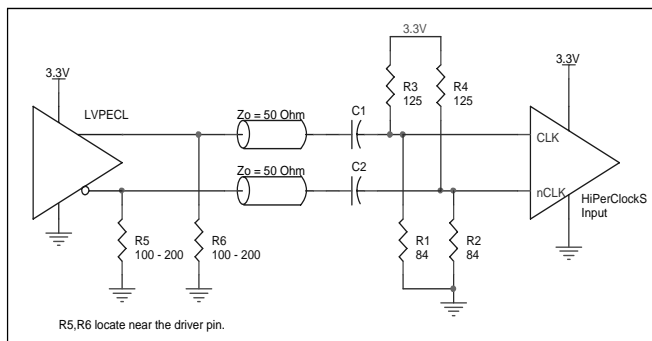
**FIGURE 3B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



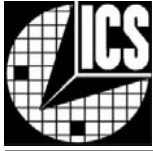
**FIGURE 3C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**



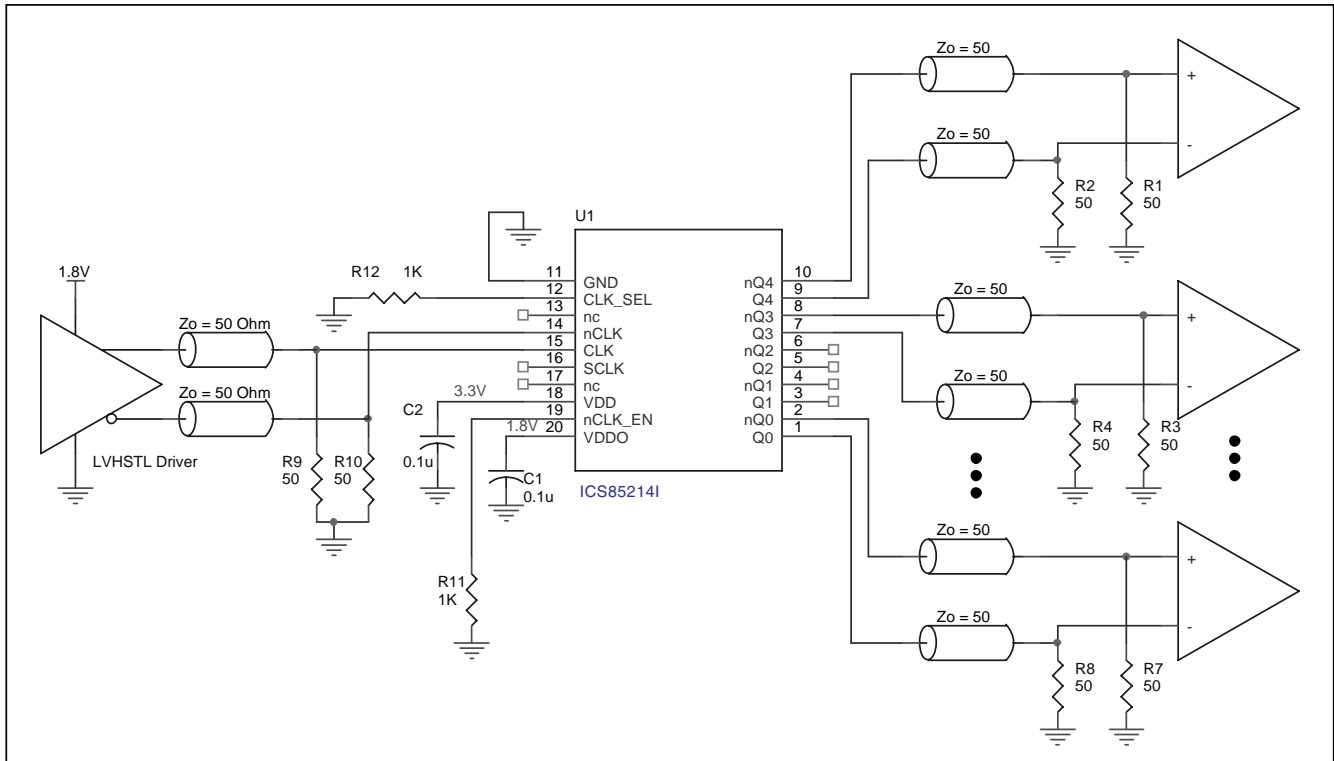
**FIGURE 3E. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE**



**SCHEMATIC EXAMPLE**

Figure 4 shows a schematic example of the ICS85214I. In this example, the input is driven by an ICS HiPerClockS HSTL driver. The decoupling capacitors should be physically located

near the power pin. For ICS85214I, the unused outputs can be left floating.



**FIGURE 4. ICS85214I HSTL BUFFER SCHEMATIC EXAMPLE**



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85214I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS85214I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{DD\_MAX} = 3.465V * 80mA = 227.2mW$
- Power (outputs)<sub>MAX</sub> = **32.8mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $5 * 32.8mW = 164mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 227.2mW + 164mW = 391.2mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below. Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.391W * 66.6^\circ C/W = 111^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 20-PIN TSSOP, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

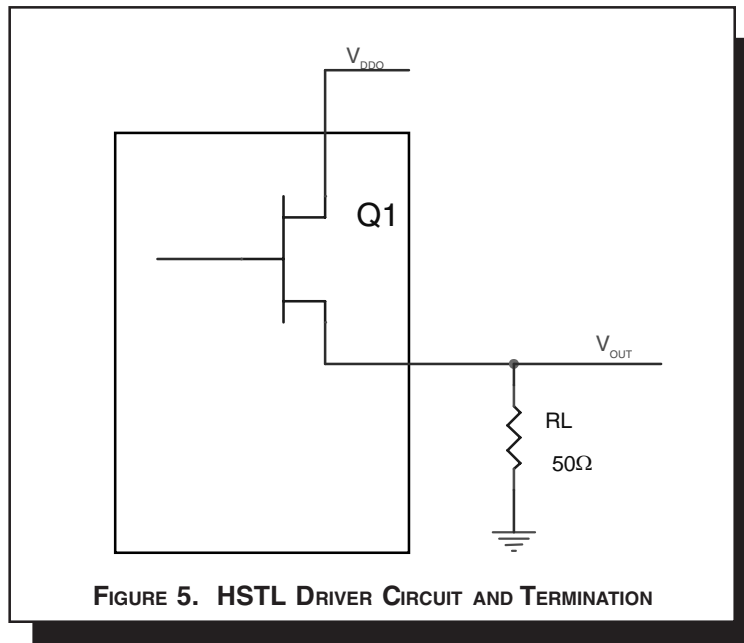
**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 5*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd<sub>H</sub> is power dissipation when the output drives high.  
Pd<sub>L</sub> is the power dissipation when the output drives low.

$$Pd_H = (V_{OH\_MIN} / R_L) * (V_{DDO\_MAX} - V_{OH\_MIN})$$

$$Pd_L = (V_{OL\_MAX} / R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$$

$$Pd_H = (1.0V/50\Omega) * (2V - 1.0V) = \mathbf{20mW}$$

$$Pd_L = (0.4V/50\Omega) * (2V - 0.4V) = \mathbf{12.8mW}$$

Total Power Dissipation per output pair = Pd<sub>H</sub> + Pd<sub>L</sub> = **32.8mW**



## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 20 LEAD TSSOP

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS85214I is: 674



PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

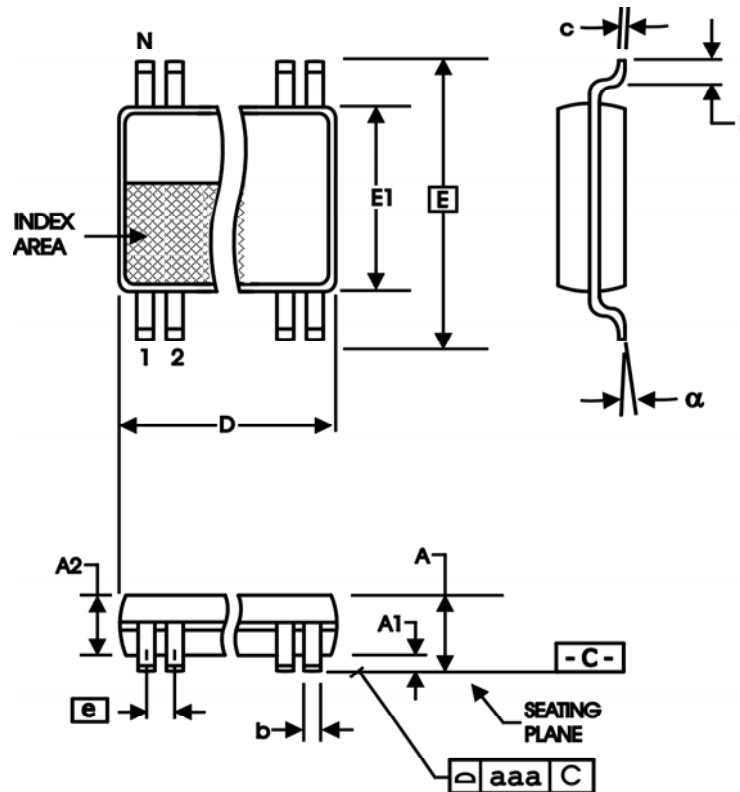
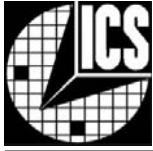


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153



Integrated  
Circuit  
Systems, Inc.

# ICS85214I

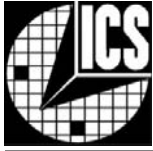
## LOW SKEW, 1-TO-5 DIFFERENTIAL-TO-HSTL FANOUT BUFFER

**TABLE 9. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Count	Temperature
ICS85214AGI	ICS85214AGI	20 lead TSSOP	tube	-40°C to 85°C
ICS85214AGI	ICS85214AGI	20 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS85214AGILF	ICS85214AGIL	20 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS85214AGILF	ICS85214AGIL	20 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Integrated  
Circuit  
Systems, Inc.

**ICS85214I**  
LOW SKEW, 1-TO-5  
DIFFERENTIAL-TO-HSTL FANOUT BUFFER

**REVISION HISTORY SHEET**

<b>Rev</b>	<b>Table</b>	<b>Page</b>	<b>Description of Change</b>	<b>Date</b>
A	T9	14	Added Lead-Free marking in Ordering Information table.	6/1/05