

Genesys Logic, Inc.

GL843

High Speed USB 2.0 With ADF
2-in-1 Scanner Controller

For 3x Series

Datasheet
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Revision History

Revision	Date	Description
1.00	04/14/2005	First formal release
1.01	11/10/2005	Add 208 QFP PinOut, Pin List, Package Dimension
1.02	03/13/2006	Delete"V_{ESD}", Table 7.1, P.81

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CHAPTER 1 GERERAL DESCRIPTION

Genesys Logic's single-chip GL843 (GeneScan™ series) is a high speed, high performance, low cost and rich scalability controller for scanner. It successfully integrates scanner function ASIC and USB 2.0 interface controller into one single-chip. With its high performance design architecture, GL843 is not only ready for supporting CIS or CCD image sensors (600, 1200, 2400, 3200, 3600, 4800dpi resolution) that are used in sheetfed, flatbed or transparency scanners, but is able to co-work with unipolar or bipolar stepping motors. Advanced features of GL843 include five motor acceleration/ deceleration curve tables for high speed motor moving.

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CHAPTER 2 FEATURES

- Highly integrated scanner controller chip (2-in-1; Scanner Controller and USB 2.0 Interface)
- USB 2.0 High Speed (480Mbit) compliant
- Designed for sheetfed, flatbed and transparency scanners
- Supports key-matrix with latch function
- Embedded RISC CPU for scanning, run-in and diagnostic tests
- Supports external 24Kbytes flash ROM or internal 24Kbyte mask ROM
- Firmware download to external flash ROM
- 12MHz low frequency clock input for better EMI
- Flexible 3.3V/5V operating voltage for I/O pads
- Adjustable working clock of scanner controller for different usage (12M, 24M, 30M, 40M, 48M, 60MHz)
- Supports linear or stagger CCD, such as NEC, Toshiba or Sony CCD
- Available sensor types: 600, 1200, 2400, 3200, 3600 and 4800dpi color CIS or CCD
- Multi-TG control for CCD (separately controls the R/G/B exposure time)
- Shutter-control for CCD (separately controls the R/G/B exposure time)
- Supports two scanning types: pixel-by-pixel (pixel rate), line-by-line (line rate)
- Support 48-bits color, 16-bits gray and 1-bit line-art
- “True gray” with R, G and B weightings
- 16 bits white/dark shading and 16-to-8 bits Gamma correction
- 0.3us per pixel for color scanning under 40MHz working clock
- 0.2us per pixel for color scanning under 60MHz working clock
- Supports LCM/LCD interface to display messages
- Supports RS232 interface for special applications
- Supports EEPROM (93C46) interface for special applications
- Supports ADF (Auto-Document-Feeder) function with document, ADF and cover sensors
- Lossless data compression
- Lines packing for stagger CCD or R/G/B line differences
- Fine CDS sampling adjustment to avoid the digital noise influence (8.33ns adjustment)
- Digital average and hardware deletion for various resolutions
- Hardware deletion for various resolutions (from 4800~1dpi with 1dpi decrement)
- Supports 1M*16, 4M*16, 8M*16, 16M*16 and 32M*16 SDRAM
- Supports 5 acceleration/deceleration motor tables for high speed motor moving and wall hitting protection
- Supports controllable bipolar motor in full, half, quarter and eighth steps moving
- Supports controllable unipolar motor in full and half steps moving
- Supports V-reference automatic control for motor driver Ics
- Build-in PWM control phase for unipolar motors

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- Programmable dummy lines to resolve start/stop (discontinuous) problem
- Watchdog protection for lamp, motor and ASIC
- Lamp time-out (sleeping) control
- Supports 21 GPIO pins and 6 GPO pins for 128-pin package
- Supports 27 GPIO pins and 6 GPO pins for 208-pin package
- Supports 2 PWM outputs for flatbed/transparency lamp control with programmable duties and frequencies
- Supports LED blinking
- Supports back-scanning
- Supports multi-film scanning

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CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts

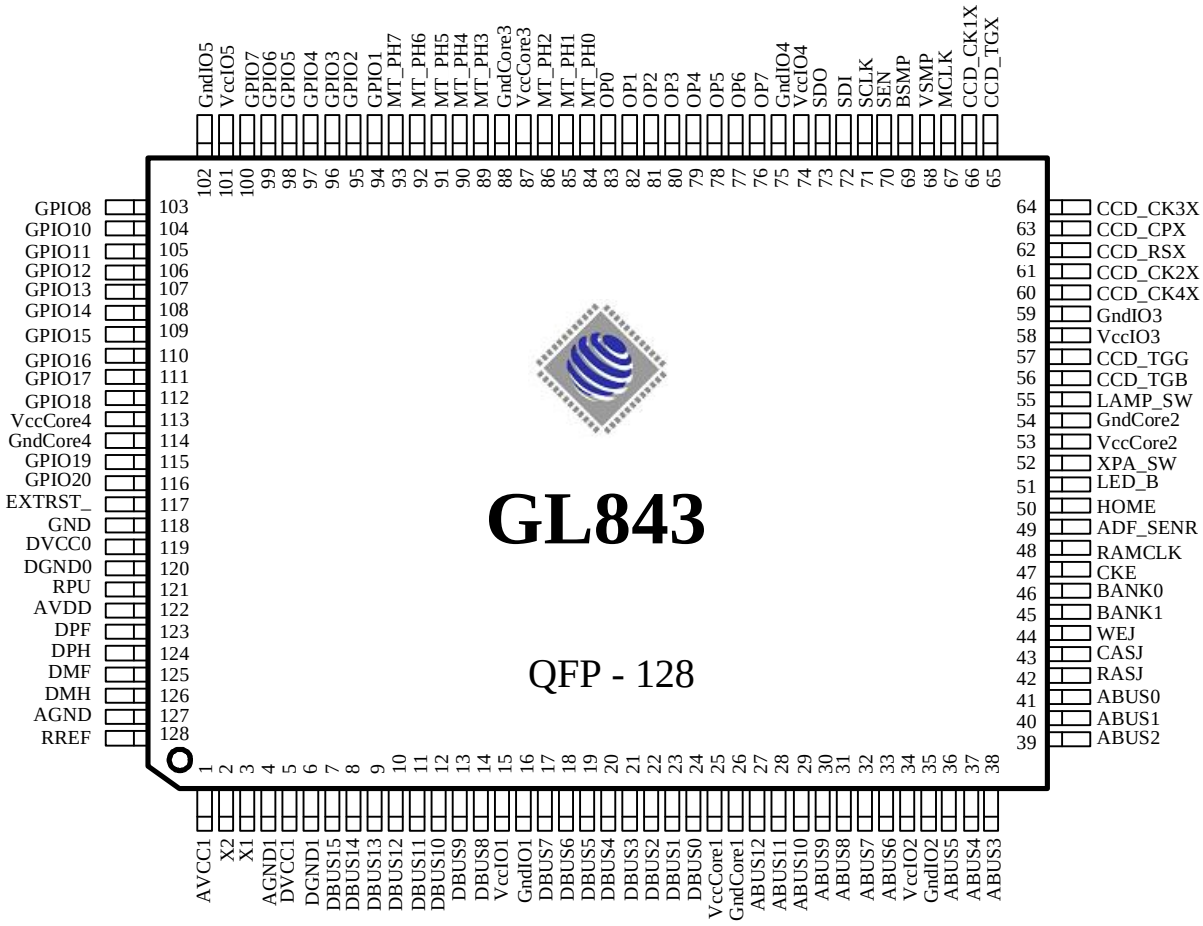


Figure 3.1 – 128 Pin QFP Pinout Diagram

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Figure 3.1 – 208 Pin QFP Pinout Diagram

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3.2 Pin List

Table 3.1 – 128 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	AVCC1	P	33	ABUS6	O	65	CCD_TGX	O	97	GPIO4	I/O
2	X2	O	34	VccIO2	P	66	CCD_CK1X	O	98	GPIO5	I/O
3	X1	I	35	GndIO2	P	67	MCLK	O	99	GPIO6	I/O
4	AGND1	P	36	ABUS5	O	68	VSMP	O	100	GPIO7	I/O
5	DVCC1	P	37	ABUS4	O	69	BSMP	O	101	VccIO5	P
6	DGND1	P	38	ABUS3	O	70	SEN	O	102	GndIO5	P
7	DBUS15	I/O	39	ABUS2	O	71	SCLK	O	103	GPIO8	I/O
8	DBUS14	I/O	40	ABUS1	O	72	SDI	O	104	GPIO10	I/O
9	DBUS13	I/O	41	ABUS0	O	73	SDO	I	105	GPIO11	I/O
10	DBUS12	I/O	42	RASJ	O	74	VccIO4	P	106	GPIO12	I/O
11	DBUS11	I/O	43	CASJ	O	75	GndIO4	P	107	GPIO13	I/O
12	DBUS10	I/O	44	WEJ	O	76	OP7	I	108	GPIO14	I/O
13	DBUS9	I/O	45	BANK1	O	77	OP6	I	109	GPIO15	I/O
14	DBUS8	I/O	46	BANK0	O	78	OP5	I	110	GPIO16	I/O
15	VccIO1	P	47	CKE	O	79	OP4	I	111	GPIO17	I/O
16	GndIO1	P	48	RAMCLK	O	80	OP3	I	112	GPIO18	I/O
17	DBUS7	I/O	49	ADF_SENR	I/O	81	OP2	I	113	VccCore4	P
18	DBUS6	I/O	50	HOME	I	82	OP1	I	114	GndCore4	P
19	DBUS5	I/O	51	LED_B	O	83	OP0	I	115	GPIO19	I/O
20	DBUS4	I/O	52	XPA_SW	O	84	MT_PH0	O	116	GPIO20	I/O
21	DBUS3	I/O	53	VccCore2	P	85	MT_PH1	O	117	EXTRST_	O
22	DBUS2	I/O	54	GndCore2	P	86	MT_PH2	O	118	GND	P
23	DBUS1	I/O	55	LAMP_SW	O	87	VccCore3	P	119	DVCC0	P
24	DBUS0	I/O	56	CCD_TGB	O	88	GndCore3	P	120	DGND0	P
25	VccCore1	P	57	CCD_TGG	O	89	MT_PH3	O	121	RPU	-
26	GndCore1	P	58	VccIO3	P	90	MT_PH4	O	122	AVDD	P
27	ABUS12	O	59	GndIO3	P	91	MT_PH5	O	123	DPF	I/O
28	ABUS11	O	60	CCD_CK4X	O	92	MT_PH6	O	124	DPH	I/O
29	ABUS10	O	61	CCD_CK2X	O	93	MT_PH7	O	125	DMF	I/O
30	ABUS9	O	62	CCD_RSX	O	94	GPIO1	I/O	126	DMH	I/O
31	ABUS8	O	63	CCD_CPX	O	95	GPIO2	I/O	127	AGND	P
32	ABUS7	O	64	CCD_CK3X	O	96	GPIO3	I/O	128	RREF	I/O

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Table 3.2 – 208 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1			33	GndCore1	P	65	FSHA0	O	97	GPIO25	I/O
2			34	ABUS12	O	66	FSHA1	O	98	CCD_CPX	O
3	NC		35	ABUS11	O	67	ADF_SENR	I/O	99	GPIO24	I/O
4	NC		36	ABUS10	O	68	FSHA2	O	100	CCD_CK3X	O
5	NC		37	ABUS9	O	69	FSHA3	O	101	GPIO23	I/O
6	NC		38	ABUS8	O	70	HOME	I	102	NC	
7	NC		39	ABUS7	O	71	FSHA4	O	103	NC	
8	AVCC1	P	40	ABUS6	O	72	FSHA5	O	104	NC	
9	X2	O	41	VccIO2	P	73	LED_B	O	105	NC	
10	X1	I	42	GndIO2	P	74	FSHA6	O	106	NC	
11	AGND1	P	43	ABUS5	O	75	FSHA7	O	107	NC	
12	DVCC1	P	44	ABUS4	O	76	XPA_SW	O	108	NC	
13	DGND1	P	45	ABUS3	O	77	FSHA8	O	109	NC	
14	DBUS15	I/O	46	NC		78	VccCore2	P	110	CCD_TGX	O
15	DBUS14	I/O	47	NC		79	GndCore2	P	111	CCD_CK1X	O
16	DBUS13	I/O	48	NC		80	FSHA9	O	112	MCLK	O
17	DBUS12	I/O	49	NC		81	LAMP_SW	O	113	VSMP	O
18	DBUS11	I/O	50	NC		82	FSHA10	O	114	BSMP	O
19	DBUS10	I/O	51	NC		83	FSHA11	O	115	SEN	O
20	DBUS9	I/O	52	NC		84	CCD_TGB	O	116	SCLK	O
21	DBUS8	I/O	53	NC		85	FSHA12	O	117	SDI	O
22	VccIO1	P	54	NC		86	FSHA13	O	118	SDO	I
23	GndIO1	P	55	ABUS2	O	87	CCD_TGG	O	119	VccIO4	P
24	DBUS7	I/O	56	ABUS1	O	88	VccIO3	P	120	GndIO4	P
25	DBU6	I/O	57	ABUS0	O	89	GndIO3	P	121	OP7	I
26	DBUS5	I/O	58	RASJ	O	90	FSHA14	O	122	OP6	I
27	DBUS4	I/O	59	CASJ	O	91	CCD_CK4X	O	123	OP5	I
28	DBUS3	I/O	60	WEJ	O	92	FSH_OEB	O	124	OP4	I
29	DBUS2	I/O	61	BANK1	O	93	FSH_WEB	O	125	OP3	I
30	DBUS1	I/O	62	BANK0	O	94	CCD_CK2X	O	126	OP2	I
31	DBUS0	I/O	63	CKE	O	95	GPIO26	I/O	127	OP1	I
32	VccCore1	P	64	RAMCLK	O	96	CCD_RSX	O	128	OP0	I

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129	FSHD0	I/O	161	NC		193	AGND	P			
130	MT_PH0	O	162	FSHD4	I/O	194	RREF	I/O			
131	MT_PH1	O	163	GPIO8	I/O	195	NC				
132	MT_PH2	O	164	GPIO9	I/O	196	NC				
133	VccCore3	P	165	FSHD5	I/O	197	NC				
134	GndCore3	P	166	GPIO10	I/O	198	NC				
135	MT_PH3	O	167	GPIO11	I/O	199	NC				
136	FSHD1	I/O	168	GPIO12	I/O	200	NC				
137	MT_PH4	O	169	FSHD6	I/O	201	NC				
138	MT_PH5	I/O	170	GPIO13	I/O	202	NC				
139	MT_PH6	O	171	GPIO14	I/O	203	NC				
140	MT_PH7	O	172	GPIO15	I/O	204	NC				
141	FSHD2	I/O	173	FSHD7	I/O	205	NC				
142	GPIO1	I/O	174	GPIO16	I/O	206	NC				
143	GPIO2	I/O	175	GPIO17	I/O	207	NC				
144	GPIO3	I/O	176	GPIO18	I/O	208	NC				
145	GPIO4	I/O	177	GPIO21	I/O						
146	FSHD3	I/O	178	VccCore4	P						
147	GPIO5	I/O	179	GndCore4	P						
148	GPIO6	I/O	180	GPIO19	I/O						
149	GPIO7	I/O	181	GPIO20	I/O						
150	VccIO5	P	182	GPIO22	I/O						
151	GndIO5	P	183	EXTRST_	O						
152	NC		184	GND	P						
153	NC		185	DVCC0	P						
154	NC		186	DGND0	P						
155	NC		187	RPU	?						
156	NC		188	AVDD	P						
157	NC		189	DPF	I/O						
158	NC		190	DPH	I/O						
159	NC		191	DMF	I/O						
160	NC		192	DMH	I/O						

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3.3 Pin Descriptions

Table 3.3 - Pin Descriptions

Pin Name	Type	Description
GPIO1~8,10~20	I/O	General Purpose Input/Output, EEPROM serial data clock or LCM data bit0
MT_PH0~5	O	Bi-polar (3967): MT_PH5=RESETJ MT_PH4=ENABLEJ MT_PH3=DIR MT_PH2=STEP MT_PH1=MS2 MT_PH0=MS1 Bi-polar (3955): MT_PH7=PHASE_A MT_PH6=PHASE_B MT_PH5=D2A MT_PH4=D1A MT_PH3=D0A MT_PH2=D2B MT_PH1=D1B MT_PH0=D0B Bi-polar (1939): MT_PH3=IN1 MT_PH2=IN2 MT_PH1=ENA1 MT_PH0=ENA2 Bi-polar (2916 or 6219): MT_PH5=PHASE1 MT_PH4=PHASE2 MT_PH3=I11 MT_PH2=I01 MT_PH1=I12 MT_PH0=I02 Uni-polar(2003): MT_PH3=PHASE A MT_PH2=PHASE B MT_PH1=PHASE /A MT_PH0=PHASE /B
MT_PH6~7	O	Motor phase 6~7
ADF_SENR	I/O	ADF sensor for ADF
HOME	I	Document sensor for ADF

Pin Name	Type	Description
CCD_CK1X	O	CCD Shift register clock1 or CIS clock output
CCD_CPX	O	CCD Clamp gate clock or CIS clock output
CCD_TGX	O	CCD Transfer gate clock for R channel or CIS Line start pulse
CCD_CK2X	O	CCD Shift register clock2 or CIS clock output
CCD_RSX	O	CCD Reset gate clock or CIS clock output
CCD_CK3X	O	CCD Shift register clock3
CCD_CK4X	O	CCD Shift register clock4

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CCD_TGG	O	CCD Transfer gate clock for G channel
CCD_TGB	O	CCD Transfer gate clock for B channel
LAMP_SW	O	Flatbed lamp power control or CIS Red LED array control
XPA_SW	O	Transparency lamp power control or CIS Green LED array control
LED_B	O	CIS Blue LED array control

Pin Name	Type	Description
OP7~0	I	AFE digital data input
SEN	O	Serial interface load pulse
SCLK	O	Serial interface clock output
SDI	O	Serial data output
SDO	I	Serial data input
BSMP	O	Video sample synchronization pulse
VSMP/CDSCLK2	O	Video sample synchronization pulse
MCLK/ADCCLK	O	Master clock.

Pin Name	Type	Description
DBUS15~0	I/O	DRAM data bus
ABUS12~0	O	DRAM address bus
RASJ		SDRAM row address strobe
CASJ	O	SDRAM column address strobe
WEJ	O	SDRAM write enable
BANK0~1	O	SDRAM bank select
CKE	O	SDRAM clock enable
RAMCLK	O	SDRAM clock

Pin Name	Type	Description
X1	I	Clock input for crystal (12MHz)
X2	I/O	Clock output for crystal
EXTRST_	I	Hardware reset input

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Pin Name	Type	Description
RPU	-	3.3V Pull up control for DPF
DPF	I/O	Positive USB differential data (Full Speed)
DPH	I/O	Positive USB differential data (High Speed)
DMF	I/O	Negative USB Differential Data (Full Speed)
DMH	I/O	Negative USB Differential Data (High Speed)
RREF	-	510 Ω reference resistor input

Pin Name	Type	Description
AVDD, AVCC1	P	Analog power input for USB2.0 transceiver 3.3V
AGND, AGND1	P	Analog ground input for USB2.0 transceiver
DVCC0, DVCC1	P	Digital power input for USB2.0 controller 3.3V
DGND0, DGND1	P	Digital ground input for USB2.0 controller.
VccCore1~4	P	Digital power input for scanner controller logic core 3.3V
GndCore1~4, GndIO1~5	P	Digital ground input for scanner controller.
VccIO1~2	P	For Pin7~Pin48 3.3V
VccIO3	P	For Pin49~Pin66 3.3V
VccIO4	P	For Pin67~Pin83 3.3V
VccIO5	P	For Pin84~Pin117 3.3V
GND	P	Ground

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	SO	Automatic output low when suspend
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up
	odpu	Open drain with internal pull up

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CHAPTER 4 REGISTERS

4.1 Registers Base Address

Table 4.1 - Base Address for Registers

Offset (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
01h	CISSET	DOGENB	DVDSET	STAGGER	COMPENB	TRUEGRAY	SHDAREA	SCAN	-
02h	NOTHOME	ACDCDIS	AGOHOME	MTRPWR	FASTFED	MTRREV	HOMENEG	LONGCURV	-
03h	LAMPDOG	AVEENB	XPASEL	LAMPPWR	LAMPTIM[3:0]				8'h94
04h	LINEART	BITSET	AFEMOD[1:0]		FILTER[1:0]		FESET[1:0]		8'h00
05h	DPIHW[1:0]		MTLLAMP[1:0]		GMMENB	ENB20M	MTLBASE[1:0]		8'h00
06h	SCANMOD[2:0]			PWRBIT	GAIN4	OPTEST[2:0]			8'h00
07h	LAMPSIM	CCDCTL	DRAMCTL	MOVCTL	RAMSEL	FASTDMA	DMASEL	DMARDWR	8'h00
08h	X	DECFLAG	GMMFFR	GMMFFG	GMMFFB	GMMZR	GMMZG	GMMZB	8'h00
09h	MCNTSET[1:0]		EVEN1ST	BLINE1ST	BACKSCAN	ENHANCE	SHORTTG	NWAIT	8'h00
0Ah	LCDSEL	LCMSEL	ADFSEL	LPWMEN	EPROMSEL	RS232SEL	BAUDRAT[1:0]		8'h00
0Bh	CLKSET[2:0]			RFHDIS	ENBDRAM	DRAMSEL[2:0]			8'h00
0Ch	SWSH[4:0]					CCDLMT[2:0]			8'h00
0Dh	JAMPCMD	DOCCMD	CCDCMD	FULLSTP	SEND	CLRMCNT	CLRDOCJM	CLRLNCNT	-
0Eh	SCANRESET								-
0Fh	MOVE								-
10h	EXPR[15:8]								8'h00
11h	EXPR[7:0]								8'h00
12h	EXPG[15:0]								8'h00
13h	EXPG[7:0]								8'h00
14h	EXPB[15:8]								8'h00
15h	EXPB[7:0]								8'h00
16h	CTRLHI	TOSHIBA	TGINV	CK1INV	CK2INV	CTRLINV	CKDIS	CTRLDIS	8'h32
17h	TGMODE[1:0]		TGW[5:0]						8'h14
18h	CNSET	DCKSEL[1:0]		CKTOGGLE	CKDELAY[1:0]		CKSEL[1:0]		8'h00
19h	EXPDMY[7:0]								8'h00
1Ah	TGLSW2	TGLSW1	MANUAL3	MANUAL1	CK4INV	CK3INV	LINECLP	X	8'h00
1Bh	GRAYSET	CHANSEL	BGRENB	ICGENB	ICGDLY[3:0]				8'h00
1Ch	CK4MTGL	CK3MTGL	CK1MTGL	CKAREA	MTLWD	TGTIME[2:0]			8'h00
1Dh	CK4LOW	CK3LOW	CK1LOW	TGSHLD[4:0]					8'h04
1Eh	WDTIME[3:0]				LINESEL[3:0]				8'h20
1Fh	SCANFED[7:0]								8'h00
20h	BUFSEL[7:0]								8'h00
21h	STEPNO[7:0]								8'h00
22h	FWDSTEP[7:0]								8'h00
23h	BWDSTEP[7:0]								8'h00
24h	FASTNO[7:0]								8'h00
25h	X	X	X	X	LINCNT[19:16]				8'h00
26h	LINCNT[15:8]								8'h00

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27h	LINCNT[7:0]								8'h00
28h	"GMMWRDATA"								-
29h	X	X	X	RAMADDR[20:16]					8'h00
2Ah	RAMADDR[15:8]								8'h00
2Bh	RAMADDR[7: 0]								8'h00
2Ch	X	X	DPISET[13:8]						8'h00
2Dh	DPISET[7:0]								8'h00
2Eh	BWHI[7:0]								8'h00
2Fh	BWLOW[7:0]								8'h00
30h	STRPIXEL[15:8]								8'h00
31h	STRPIXEL[7:0]								8'h00
32h	ENDPIXEL[15:8]								8'h00
33h	ENDPIXEL[7:0]								8'h00
34h	DUMMY[7:0]								8'h00
35h	MAXWD[24:17]								8'h00
36h	MAXWD[16:9]								8'h00
37h	MAXWD[8:1]								8'h00
38h	LPERIOD[15:8]								8'h2A
39h	LPERIOD[7:0]								8'h30
3Ah	X	X	X	X	X	X	X	FEWRDATA[8]	-
3Bh	FEWRDATA[7:0]								-
3Ch	"RAMWRDATA"								-
3Dh	X	X	X	X	FEEDL[19:16]				8'h00
3Eh	FEEDL[15:8]								8'h00
3Fh	FEEDL[7:0]								8'h00
40h	DOCSNR	ADFSNR	COVERSNR	CHKVER	DOCJAM	HISPDFLG	MOTMFLG	DATAENB	-
41h	PWRBIT	BUFEMPTY	FEEDFSH	SCANFSH	HOMESNR	LAMPSTS	FEBUSY	MOTORENB	-
42h	VALIDWORD[24:17]								8'h00
43h	VALIDWORD[16:9]								8'h00
44h	VALIDWORD[8:1]								8'h00
45h	"RAMRDDATA"								-
46h	X	X	X	X	X	X	X	FERDDATA[8]	-
47h	FERDDATA[7:0]								-
48h	X	X	X	X	FEDCNT[19:16]				8'h00
49h	FEDCNT[15:8]								8'h00
4Ah	FEDCNT[7:0]								8'h00
4Bh	X	X	X	X	SCANCNT[19:16]				8'h00
4Ch	SCANCNT[15:8]								8'h00
4Dh	SCANCNT[7:0]								8'h00
4Eh	"GMMRDDATA"								-
4Fh	X	X	DOGON	ROMBSY	LCMBSY	TX232BSY	RX232BSY	RXREADY	-
50h	X	X	FERDA[5:0]						8'h00
51h	X	X	FEWRA[5:0]						8'h00
52h	X	X	X	RHI[4:0]					8'h00
53h	X	X	X	RLOW[4:0]					8'h00
54h	X	X	X	GHI[4:0]					8'h00
55h	X	X	X	GLOW[4:0]					8'h00

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56h	X	X	X	BHI[4:0]					8'h00
57h	X	X	X	BLOW[4:0]					8'h00
58h	VSMP[4:0]					VSMPW[2:0]			8'h00
59h	BSMP[4:0]					BSMPW[2:0]			8'h00
5Ah	ADCLKINV	RLCSEL	CDSREF[1:0]		RLC[3:0]				8'h00
5Bh	X	MTRTBL	GMMADDR[13:8]						8'h00
5Ch	GMMADDR[7:0]								8'h00
5Dh	HISPD[7:0]								8'h00
5Eh	DECSEL[2:0]			STOPTIM[4:0]					8'h00
5Fh	FMOVDEC[7:0]								8'h00
60h	X	X	X	Z1MOD[20:16]					8'h00
61h	Z1MOD[15:8]								8'h00
62h	Z1MOD[7:0]								8'h00
63h	X	X	X	Z2MOD[20:16]					8'h00
64h	Z2MOD[15:8]								8'h00
65h	Z2MOD[7:0]								8'h00
66h	PHFREQ[7:0]								8'h00
67h	STEPSEL[1:0]		MTRPWM[5:0]						8'h7F
68h	FSTPSEL[1:0]		FASTPWM[5:0]						8'h7F
69h	FSHDEC[7:0]								8'h00
6Ah	FMOVNO[7:0]								8'h00
6Bh	MULTFILM	GPOM13	GPOM12	GPOM11	GPOCK4	GOPCP	GPOLEDB	GPOADF	8'h00
6Ch	GPIO16	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	8'h00
6Dh	GPIO8	GPIO7	GPOI6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	8'h00
6Eh	GPOE16	GPOE15	GPOE14	GPOE13	GPOE12	GPOE11	GPOE10	GPOE9	8'h00
6Fh	GPOE8	GPOE7	GPOE6	GPOE5	GPOE4	GPOE3	GPOE2	GPOE1	8'h00
70h	X	X	X	RSH[4:0]					8'h06
71h	X	X	X	RSL[4:0]					8'h08
72h	X	X	X	CPH[4:0]					8'h08
73h	X	X	X	CPL[4:0]					8'h0A
74h	X	X	X	X	X	X	CK1MAP[17:16]		8'h00
75h	CK1MAP[15:8]								8'h00
76h	CK1MAP[7:0]								8'h00
77h	X	X	X	X	X	X	CK3MAP[17:16]		8'h00
78h	CK3MAP[15:8]								8'h00
79h	CK3MAP[7:0]								8'h00
7Ah	X	X	X	X	X	X	CK4MAP[17:16]		8'h00
7Bh	CK4MAP[15:8]								8'h00
7Ch	CK4MAP[7:0]								8'h00
7Dh	CK1NEG	CK3NEG	CK4NEG	RSNEG	CPNEG	BSMPNEG	VSMPNEG	DLYSET	8'h00
7Eh	GPOLED25	GPOLED24	GPOLED23	GPOLED22	GPOLED21	GPOLED10	GPOLED9	GPOLED8	8'h00
7Fh	BSMPDLY[1:0]		VSMPDLY[1:0]		LEDCNT[3:0]				8'h00
80h	VRHOME[1:0]		VRMOVE[1:0]		VRBACK[1:0]		VRSCAN[1:0]		8'h00
81h	X	X	X	LOADSET[4:0]					8'h00
82h	CONTB[3:0]				CONTA[3:0]				8'h00
83h	IMGSET[7:0]								8'h00

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84h	PACK[1:0]		PACKCNT[5:0]						8'h00
87h	X	YENB	YBIT	ACYCNRLC	ENOFFSET	LEDADD	CK4ADC	AUTOCONF	8'h00
88h	X	X	X	RDNUM[4:0]					8'h00
89h	RS232WD[7:0]								-
8Ah	RS232RD[7:0]								-
8Bh	ROMADDR[7:0]								8'h00
8Ch	ROMWD[15:8]								-
8Dh	ROMWD[7:0]								-
8Eh	ROMRD[15:8]								-
8Fh	ROMRD[7:0]								-
90h	PREFED[15:8]								8'h00
91h	PREFED[7:0]								8'h00
92h	PSTFED[15:8]								8'h00
93h	PSTFED[7:0]								8'h00
94h	MTRPLS[7:0]								8'h00
95h	X	X	X	X	SCANLEN[19:16]				8'h00
96h	SCANLEN[15:8]								8'h00
97h	SCANLEN[7:0]								8'h00
98h	ONDUR[15:8]								8'h00
99h	ONDUR[7:0]								8'h00
9Ah	OFFDUR[15:8]								8'h00
9Bh	OFFDUR[7:0]								8'h00
9Ch	LCMWD[7:0]								-
9Dh	RAMDLY[1:0]		MOTLAG	CMODE	STEPTIM[1:0]		MULDMYLN	IFRS	8'h00
9Eh	X	SEL3INV	TGSTIME[2:0]			TGWTIME[2:0]			8'h00
9Fh	LCDCTL	LCMCTL	EPROMCTL	TGCTL	MPUCTL	MOTMPU	NEC8884	DPI9600	X
A0h	X	X	LNOFSET[5:0]						X
A1h	X	X	X	STGSET[4:0]					X
A2h	X	X	X	RFHSET[4:0]					8'h00
A3h	TRUER[7:0]								-
A4h	TRUEG[7:0]								-
A5h	TRUEB[7:0]								8'h00
A6h	GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	8'h00
A7h	GPOE24	GPOE23	GPOE22	GPOE21	GPOE20	GPOE19	GPOE18	GPOE17	8'h00
A8h	X	X	GPOE27	GPOE26	GPOE25	GPO27	GPO26	GPO25	8'h00
A9h	X	X	GPO33	GPO32	GPO31	GPO30	GPO29	GPO28	8'h00
ABh	GPOM9	MULSTOP[2:0]			NODECEL	TB3TB1	TB5TB2	FIX16CLK	8'h00
ACh	VRHOME3	VRHOME2	VRMOME3	VRMOME2	VRBACK3	VRBACK2	VRSCAN3	VRSCAN2	8'h00
ADh	X	X	ADFTYP[1:0]		CCDTYP[3:0]				
AEh	X	X	MOTSET[2:0]			PROCESS[2:0]			
AFh	SCANTYP[2:0]			FEDTYP[1:0]		ADFMOVE[2:0]			

Notation:

R/W Read / Write

R/O Read Only

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W/O	Write Only
R/W1C	Readable and Write-1-Clear
R/W/C	Read / Write and hardware automatic Clear

4.2 Register Descriptions

Offset 01h

CISSET	DOGENB	DVDSET	STAGGER	COMPENB	TRUEGRAY	SHDAREA	SCAN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	**CISSET**	0	CCD scan type.
		1	CIS scan type.
6	**DOGENB**	0	Disable watchdog function.
		1	Enable watchdog function (set time out duration in Reg1E[7:4]).
5	**DVDSET**	0	Disable shading function.
		1	Enable shading function (include whole line shading and area shading).
4	**STAGGER**	1	Enable double shading.
		0	Disable double shading.
3	**COMPENB**	0	Disable data compression.
		1	Enable lossless data compression.
2	**TRUEGRAY**	0	Disable true gray function.
		1	Enable true gray function. The weightings are stored in Reg A3,A4 and A5.
1	**SHDAREA**	0	Select whole-line shading.
		1	Select area-shading (depend on scan area and scan dpi).
0	**SCAN**	0	Disable scanning process.
		1	Enable scanning process.

Offset 02h

NOTHOME	ACDCDIS	AGOHOME	MTRPWR	FASTFED	MTRREV	HOMENEG	LONGCURV
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	**NOTHOME**	0	In auto-go-home function, carriage will not stop until touching the home sensor.
		1	In auto-go-home function, moving steps of carriage depends on steps setting from software (Reg 3D, 3E and 3F).
6	**ACDCDIS**	0	Enable carriage backtracking when image buffer is full.
		1	Disable carriage backtracking when image buffer is full.
5	**AGOHOME**	0	Disable auto-go-home function.
		1	Enable auto-go-home function. It's for carriage to go home automatically after scanning finished.
4	**MTRPWR**	0	Turn off MOTOR power and phase to idle state.
		1	Turn on MOTOR power and phase.
3	**FASTFED**	0	Move to scanning window by only one acceleration/deceleration tables.
		1	Move to scanning window by two acceleration/deceleration tables.
2	**MTRREV**	0	Set motor to move in forward direction.
		1	Set motor to move in reverse direction.
1	**HOMENEG**	0	Motor will be decelerated when home sensor input (HOME) changes from low to high (rising edge).
		1	Motor will be decelerated when home sensor input (HOME) changes from high to low (falling edge).
0	**LONGCURV**	0	The deceleration curve of the fast moving is defined in table 4 or use default

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curve.
1 The deceleration curve of the fast moving is defined in table 5 to protect wall-hitting.

Offset 03h …….……..…… Default value = 8'h94

LAMPDOG	AVEENB	XPASEL	LAMPPWR	LAMPTIM3	LAMPTIM2	LAMPTIM1	LAMPTIM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 LAMPDOG
0 To disable sleep mode of lamp.
1 To start sleep mode of lamp (default on).

6 AVEENB
0 Select dpi deletion function
1 Select dpi average function.

5 XPASEL
0 Select flatbed lamp on.
1 Select transparency lamp on.

4 LAMPPWR
0 Turn off LAMP power.
1 Turn on LAMP power.

3-0 LAMPTIM[3:0] Counter of the sleep mode of lamp (default: 4).
The unit is minute.

Offset 04h ……..……..……..…… Default value = 8'h00

LINEART	BITSET	AFEMOD1	AFEMOD0	FILTER1	FILTER0	FESET1	FESET0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 LINEART
0 Color/Gray scanning.
1 Black/White scanning.

6 BITSET
0 8 bits image data type (= byte).
1 16 bits image data type (= word).

5-4 AFEMOD[1:0] AFE operation mode.

Wolfson Type					
AFEMOD	SCANMOD	Description	CDS Available	Max Sample Rate	Timing Requirements
2	0,1,7	Slow color Pixel-by-pixel	Yes	5MSPS *3 channel	MCLK:VSMP Rate is 8:1
1	0,1,6,7	Color pixel-by-pixel	Yes	6.67MSPS *3 channel	MCLK:VSMP Rate is 6:1
0	0,1,4,5,6	Fast Mono	Yes	13.3MSPS *1 channel	MCLK:VSMP Rate is 3:1
Analog Device Type					
AFEMOD	SCANMOD	Description	CDS Available	Max Sample Rate	Timing Requirements
2	0,1,6,7	Slow color Pixel-by-pixel	Yes		MCLK:VSMP Rate is 3:1
1	0,1,6,7	Mono	Yes		MCLK:VSMP Rate is 2:1
0	0,1,6,7	Fast Mono	Yes		MCLK:VSMP Rate is 1:1

3-2 FILTER[1:0] Scan color type:
00 Color

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01 R
10 G
11 B

1-0 FESET[1:0] Front end operation type:
00 ESIC type 1
01 ESIC type2
10 ADI type
11 Reserved

Offset 05h …….. Default value = 8'h00

DPIHW1	DPIHW0	MTLLAMP1	MTLLAMP0	GMMENB	ENB20M	MTLBASE1	MTLBASE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 DPIHW[1:0] To set CCD/CIS resolution.
00 600 dpi
01 1200 dpi
10 2400 dpi
11 4800 dpi

5-4 MTLLAMP[1:0] Multiply coefficient for time-out counter of lamp.
00 1* LAMPTIM
01 2* LAMPTIM
10 4* LAMPTIM
11 Reserved

3 GMMENB 0 Disable gamma correction.
1 Enable gamma correction.

2 ENB20M 0 CCD_CK1X output clocks according to designer's settings .
1 CCD_CK1X generate 20MHz clock to CCD or CIS sensors.

1-0 MTLBASE[1:0] To set output CCD pixel number under each system pixel time.
00 1 CCD pixel/sstem pixel time.
01 2 CCD pixel/sstem pixel time.
10 3 CCD pixel/sstem pixel time.
11 4 CCD pixel/sstem pixel time.

Offset 06h …….. Default value = 8'h00

SCANMOD2	SCANMOD1	SCANMOD0	PWRBIT	GAIN4	OPTEST2	OPTEST1	OPTEST0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-5 SCANMOD[2:0] To set operation mode.
000 12 clocks/pixel ; normal mode operation for scanning.
Color scanning : 24 bits image with gamma correction
Gray scanning : 8 bits image with gamma correction
16 bits image without gamma correction
Line art scanning : 1 bit image with gamma correction
001 12 clocks/pixel ; bypass mode operation for calibration.
Include color(pixel rate) , gray line-art.
010 Reserved
011 Reserved
100 Reserved
101 Reserved
110 18 clocks/pixel.
Color scanning : 24 bits image with gamma correction
48 bits image without gamma correction
Gray scanning : 8 bits image with gamma correction
16 bits image without gamma correction

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Line art scanning : 1 bit image with gamma correction
111 16 clocks/pixel.
Color scanning : 24 bits image with gamma correction
48 bits image without gamma correction
Gray scanning : 8 bits image with gamma correction
16 bits image without gamma correction
Line art scanning : 1 bit image with gamma correction

4 PWRBIT The hardware will reset this bit during power-on initial process. It can be set and checked by S/W to know if the power had been turned off or not.
Default is reset.

3 GAIN4
0 Digital shading gain=8 times system.
1 Digital shading gain=4 times system.
Note: If you want to get more precise image quality,you can set GAIN4 bit.

2-0 OPTEST[2:0] Select ASIC operation type.
000 Set normal mode to capture AFE image.
001 Set SDRAM bank testing and power-on moving testing for ASIC simulation
010 Pixel count pattern for ASIC image test.
011 Line count pattern for ASIC image test.
100 Counter and adder test for ASIC simulation test.
101 Reserved.
110 Reserved.
111 Reserved.

Offset 07h …….……..……..……. Default value = 8'h00

LAMPSIM	CCDCTL	DRAMCTL	MOVCTL	RAMSEL	FASTDMA	DMASEL	DMARDWR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 LAMPSIM for timer simulation
6 CCDCTL for CCD timing control
5 DRAMCTL for SRAM & DRAM access control
4 MOVCTL for motor driver IC style control
3 SRAMSEL
0 DMA access for DRAM.
1 DMA access for SRA
2 FASTDMA
0 4clocks/access,that is to say 4clocks/16bits or 4clocks/8bits for DMA access.
1 2clocks/access,that is to say 2clocks/16bits or 2clocks/8bits for DMA access.
1 DMASEL
0 MPU access DRAM under command mode.
1 DMA access DRAM under command mode.
0 DMARDWR
0 DMA read DRAM under command mode.

Note: Please do not write other values than 00H into this register under normal condition.

Offset 08h …….……..……..……. Default value = 8'h00

X	DECFLAG	GMMFFR	GMMFFG	GMMFFB	GMMZR	GMMZG	GMMZB
X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 RESERVED -
6 DECFLAG
0 Select gamma table in increment type
1 Select gamma table in decrement type.
5 GMMFFR
0 This function is not enabled
1 Gamma table address FFH of red channel is a special value.

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4	**GMMFFG**	0	This function is not enabled.
		1	Gamma table address FFH of green channel is a special value.
3	**GMMFFB**	0	This function is not enabled.
		1	Gamma table address FFH of blue channel is a special value.
2	**GMMZR**	0	This function is not enabled.
		1	Gamma table address 00H of red channel is a special value.
1	**GMMZG**	0	This function is not enabled.
		1	Gamma table address 00H of green channel is a special value.
0	**GMMZB**	0	This function is not enabled.
		1	Gamma table address 00H of blue channel is a special value.

Offset 09h ……..……..……..……. Default value = 8'h00

MCNTSET1	MCNTSET0	EVEN1ST	BLINE1ST	BACKSCAN	ENHANCE	SHORTTG	NWAIT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6	**MCNTSET[1:0]**	To select the unit of motor table counter.	
		00	Pixel count.
		01	System clock*2.
		10	System clock*3.
		11	System clock*4.
5	**EVEN1ST**	0	The first pixel of stagger CCD is located at odd sensor line.
		1	The first pixel of stagger CCD is located at even sensor line.
4	**BLINE1ST**	0	The first sensor of CCD is red line.
		1	The first sensor of CCD is blue line.
3	**BACKSCAN**	0	Select forward scanning function.
		1	Select backward scanning function.
2	**ENHANCE**	0	Select normal mode for embedded EPP interface.
		1	Select enhance mode for embedded EPP interface.
1	**SHORTTG**	0	Disable this function.
		1	Enable short CCD SH(TG) period for film scanning.
0	**NWAIT**	0	No delay for nWait.
		1	To delay nWait (H_BUSY) for one clock.

Offset 0Ah ……..……..……..……. Default value = 8'h00

LCDSEL	LCMSEL	ADFSEL	LPWMEN	EPROMSEL	RS232SEL	BAUDRAT1	BAUDRAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	**LCDSEL**	0	Disable LCD display function.
		1	Enable LCD display function and the specific GPIOs are defined to drive LCD.
6	**LCMSEL**	0	Disable LCM display function.
		1	Enable LCM display function and the specific GPIOs are defined to drive LCM.
5	**ADFSEL**	0	Disable ADF function.
		1	Enable ADF function and the specific GPIOs are defined to drive ADF module.
4	**LPWMEN**	0	Disable ADF function.
		1	Enable PWM function of lamp.
3	**EPROMSEL**	0	Disable external EEPROM (93C46) interface.
		1	Enable external EEPROM (93C46) interface and the specific GPIOs are defined to connect EEPROM.
2	**RS232SEL**	0	Disable RS232 interface.

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1 Enable RS232 interface for special application and the specific GPIOs are defined to implement RS232 protocol.

1-0 BAUDRAT[1:0] Set boud rate of RS232.
00 2400bps.
01 4800bps.
10 9600bps.
11 19200bps.

Offset 0Bh ……..……..……..……. Default value = 8'h00

CLKSET2	CLKSET1	CLKSET0	RFHDIS	ENBDRAM	DRAMSEL2	DRAMSEL1	DRAMSEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-5 CLKSET[2:0] To select the system clock frequency.
000 24MHz.
001 30MHz.
010 40MHz.
011 48MHz.
100 60MHz.
101 Reserved.
110 Reserved.
111 Reserved.

4 RFHDIS 0 Enable auto-refresh mode for SDRAM.
1 Enable self-refresh mode for SDRAM.

3 ENBDRAM A rising edge from low to high: to start power on sequence of SDRAM.

2-0 DRAMSEL[2:0] Select the SDRAM size.
000 Reserved.
001 16M bit.
010 64M bit.
011 128M bit.
100 256M bit.
101 512M bit.
110 Reserved.
111 Reserved.

Offset 0Ch ……..……..……..……. Default value = 8'h00

SWSH4	SWSH3	SWSH2	SWSH1	SWSH0	CCDLMT2	CCDLMT1	CCDLMT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-3 SWSH [4:0] To set the distance from SEL3 to TG for NEC8884. the width s SWSH[4:2]*2 ^{TGSTIME}

2-0 CCDLMT[2:0] To set the lines count which is synchronized for CCD timing(like NEC8884).

Offset 0Dh

JAMPCMD	DOCCMD	CCDCMD	FULLSTP	SEND	CLRMCNT	CLRDOCJM	CLRLNCNT
W	W	W	W	W	W	W	W

Command: Scanner command.

7 JAMPCMD To control jamp when scanner is working on ADF.

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6	**DOCCMD**	To control document when scanner is working on ADF.
5	**CCDCMD**	To control CCD when abnormal status happens.
4	**FULLSTP**	To reset steps type to full step.
3	**SEND**	To send the RS232 data.
2	**CLRMCNT**	To clear FEDCNT(Reg48,Reg49,Reg4A) counter information.
1	**CLRDOCJM**	0 Don't clear document jam message for ADF module. 1 To clear document jam message for ADF module.
0	**CLRLNCNT**	0 Don't clear SCANCNT. 1 To clear SCANCNT (Reg4B,Reg4C,Reg4D).

Note: 1.For each scanning, designers must clear SCANCNT before starting process.
2.Other bits in this register are not defined.

Offset 0Eh

SCANRESET
W

Command: Scanner software reset.

It can initiate AISC system including lamp and motor, control registers, internal circuit; but not including tables in DRAM, like gamma table, shading table and acceleration/deceleration table.

Note: In normal condition, it is unnecessary to reset scanner unless the scanner is out of control.

Offset 0Fh

MOVE
W

Command: Motor moving.

Start motor forward/backward moving.

Offset 10h …….……..……..……. Default value = 8'h00

EXPR15	EXPR14	EXPR13	EXPR12	EXPR11	EXPR10	EXPR9	EXPR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 EXPR[15:8] Exposure time setting (in pixel time) for Red-LED of CIS or Red channel of CCD.

Note: It cannot be programmed to logic zero.

Offset 11h …….……..……..……. Default value = 8'h00

EXPR7	EXPR6	EXPR5	EXPR4	EXPR3	EXPR2	EXPR1	EXPR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 EXPR[7:0] Exposure time setting (in pixel time) for Red-LED of CIS or Red channel of CCD.

Note: It cannot be programmed to logic zero.

Offset 12h …….……..……..……. Default value = 8'h00

EXPG15	EXPG14	EXPG13	EXPG12	EXPG11	EXPG10	EXPG9	EXPG8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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7-0 EXPG[15:8] Exposure time setting (in pixel time) for Green-LED of CIS or Red channel of CCD.
Note: It cannot be programmed to logic zero.

Offset 13h …….……..……..……. Default value = 8'h00

EXPG7	EXPG6	EXPG5	EXPG4	EXPG3	EXPG2	EXPG1	EXPG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 EXPG[7:0] Exposure time setting (in pixel time) for Green-LED of CIS or Red channel of CCD.
Note: It cannot be programmed to logic zero.

Offset 14h …….……..……..……. Default value = 8'h00

EXPB15	EXPB14	EXPB13	EXPB12	EXPB11	EXPB10	EXPB9	EXPB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 EXPB[15:8] Exposure time setting (in pixel time) for Blue-LED of CIS or Red channel of CCD.
Note: It cannot be programmed to logic zero.

Offset 15h …….……..……..……. Default value = 8'h00

EXPB7	EXPB6	EXPB5	EXPB4	EXPB3	EXPB2	EXPB1	EXPB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 EXPB[7:0] Exposure time setting (in pixel time) for Blue-LED of CIS or Red channel of CCD.
Note: It cannot be programmed to logic zero.

Offset 16h …….……..……..……. Default value = 8'h32

CTRLHI	TOSHIBA	TGINV	CK1INV	CK2INV	CTRLINV	CKDIS	CTRLDIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 CTRLHI
0 CCD CP & RS will be low when TG goes high.
1 CCD CP & RS will be high when TG goes high.

6 TOSHIBA
0 Not TOSHIBA CIS.
1 To indicate the image sensor is TOSHIBA CIS.

5 TGINV
0 Don't reverse.
1 To reverse CCD TG.

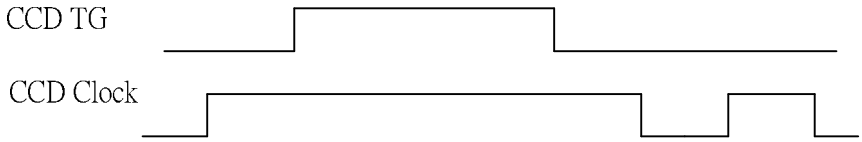
4 CK1INV
0 Don't reverse.
1 To reverse CCD Clock 1.

3 CK2INV
0 Don't reverse.
1 To reverse CCD Clock 2.

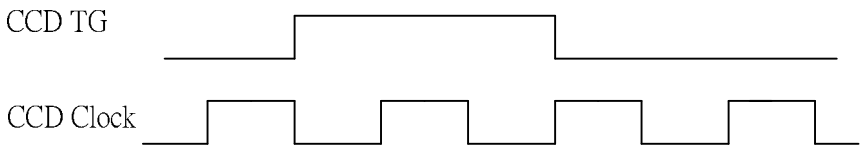
2 CTRLINV
0 Don't reverse.
1 To reverse CCD CP & RS.

1 CKDIS
0 Disable clock1 and 2 under CCD TG position as illustrated.

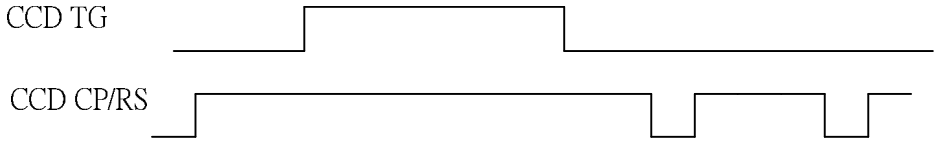
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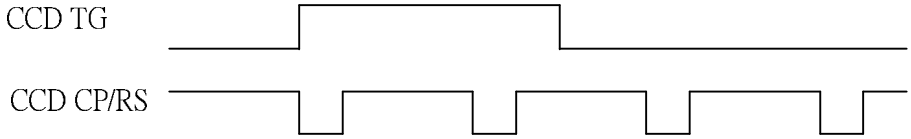
0 Enable clock 1 and 2 under CCD TG position as illustrated.



0 CTRLDIS 1 Disable CCD CP & RS signals under CCD TG position as illustrated.



0 Enable CCD CP & RS signals under CCD TG position as illustrated.



Offset 17h …….. Default value = 8'h14

TGMODE1	TGMODE0	TGW5	TGW4	TGW3	TGW2	TGW1	TGW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 TGMODE[1:0] To set CCD TG mode.
- 00 normal CCD TG type.
- 01 CCD TG control with dummy line.
- 10 CCD TG control with dummy lines for transparency scanning type.
- 11 reserved for ASIC simulation.

5-0 TGW[5:0] To set CCD TG plus width (in pixel time).

Note: It cannot be programmed to logic zero.

Offset 18h …….. Default value = 8'h00

CNSET	DCKSEL1	DCKSEL0	CKTOGGLE	CKDELAY1	CKDELAY0	CKSEL1	CKSEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 CNSET
- 0 Select TG and clock to be non-Canon CIS style.
- 1 Select TG and clock to be Canon CIS style.

6-5 DCKSEL1[1:0]
- 00 Speed 1: one CCD clock per system pixel time in shifting dummy lines.
- 01 Speed 2: two CCD clock per system pixel time in shifting dummy lines.
- 10 Speed 3: three CCD clock per system pixel time in shifting dummy lines.

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11 Speed 4: four CCD clock per system pixel time in shifting dummy lines.

4 CKTOGGLE 0 One cycle per pixel.
1 Half cycle per pixel for CCD clock 1 & 2.

3-2 CKDELAY[1:0] 00 No delay
01 Delay one system clock for CCD Clock 1/2.
10 Delay two systems clock for CCD Clock 1/2.
11 Delay three systems clock for CCD Clock 1/2.

1-0 CKSEL[1:0] 00 Speed 1: one CCD clock per system pixel time in capturing image.
01 Speed 2: two CCD clock per system pixel time in capturing image.
10 Speed 3: three CCD clock per system pixel time in capturing image.
11 Speed 4: four CCD clock per system pixel time in capturing image.

Note: Speed limitation of CCD clock in different scanning modes:

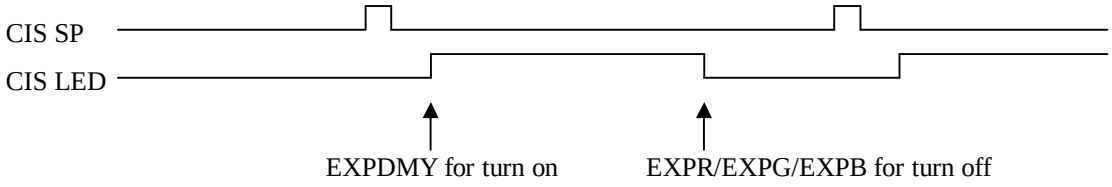
1. SCANMOD=0,1 : 12 clocks/pixel a. toggle CCD : supports speed 1,2,3,4.
   b. non-toggle CCD : supports speed 1,2,3.
2. SCANMOD=2 : Reserved.
3. SCANMOD=3 : Reserved.
4. SCANMOD=4 : Reserved.
5. SCANMOD=5 : Reserved.
6. SCANMOD=6 : 18 clocks/pixel a. toggle CCD : supports speed 1,2,3.
   b. non-toggle CCD : supports speed 1,2,3,4.
7. SCANMOD=7 : 16 clocks/pixel a. toggle CCD : supports speed up 1,2,4.
   b. non-toggle CCD : supports speed 1,2,4.

Note: Toggle CCD **à** CCD which can output one pixel in one half cycle of CCD clock.
Non-toggle CCD **à** CCD which always output one pixel in one CCD clock cycle.

Offset 19h …….……..……. Default value = 8'h00

EXPDMY7	EXPDMY6	EXPDMY5	EXPDMY4	EXPDMY3	EXPDMY2	EXPDMY1	EXPDMY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 EXPDMY[7:0] To set exposure time of dummy lines (unit = 256 pixels time) or CIS LED turn-on tme.



Note: It cannot be programmed to logic zero.

Offset 1Ah ……..……..……. Default value = 8'h00

TGLSW2	TGLSW1	MANUAL3	MANUAL1	CK4INV	CK3INV	LINECLP	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	X

7 TGLSW2 Set CCD SW2 output.

6 TGLSW1 Set CCD SW1 output.

5 MANUAL3 0 CCD Clock 3,Clock4 automatic output.
1 CCD Clock 3,Clock4 manual output.

4 MANUAL1 0 CCD Clock 1,Clock2 automatic output.
1 CCD Clock 1,Clock2 manual output.

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3	**CK4INV**	0	Don't reverse.
		1	To reverse CCD Clock4.
2	**CK3INV**	0	Don't reverse.
		1	To reverse CCD Clock 3.
1	**LINECLP**	0	To select CCD pixel clamping.
		1	To select CCD line clamping.
0	**RESERVED**	-	

Offset 1Bh ……..……..……..……..…. Default value = 8'h00

GRAYSET	CHANSEL	BGRENB	ICGENB	ICGDLY3	ICGDLY2	ICGDLY1	ICGDLY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	**GRAYSET**	0	Select single channel output.
		1	Select two channel output.
6	**CHANSEL**	0	Fast true gray latch is 2 and 3 position.
		1	Fast true gray latch is 1 and 2 position.
5	**BGRENB**	0	The order is R-G-B.
		1	The order of latching A/D data is B-G-R.
4	**ICGENB**	0	To disable ICG control.
		1	To enable CCD shutter control signal ICG.
3-0	**ICGDLY[3:0]**		CCD ICG delay for rising/falling edge.

Offset 1Ch ……..……..……..…… Default value = 8'h00

CK4MTGL	CK3MTGL	CK1MTGL	CKAREA	MTLWD	TGTIME2	TGTIME1	TGTIME0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	**CK4MTGL**	0	Disable toggle function in CCD clock 4.
		1	Enable toggle function in CCD clock 4.
6	**CK3MTGL**	0	Disable toggle function in CCD clock 3.
		1	Enable toggle function in CCD clock 3.
5	**CK1MTGL**	0	Disable toggle function in CCD clock 1 & 2.
		1	Enable toggle function in CCD clock 1 &2.
4	**CKAREA**	0	This function is disabled.
		1	CCD clock speed depends on CKSEL in scan area and DCKSEL in non-scan area.
3	**MTLWD**	0	Set the watchdog time-out as WDTIME[3:0].
		1	Set the watchdog time-out as WDTIME[3:0] * 2.
2-0	**TGTIME[2:0]**		CCD line period selection.
		000	1*LPERIOD(Reg38,Reg39)
		001	2*LPERIOD
		010	4*LPERIOD
		011	8*LPERIOD
		100	16*LPERIOD
		101	32*LPERIOD
		110	Reserved.
		111	Reserved.

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Offset 1Dh ……..…….. Default value = 8'h04

CK4LOW	CK3LOW	CK1LOW	TGSHLD4	TGSHLD3	TGSHLD2	TGSHLD1	TGSHLD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 CK4LOW 0 Clock 4 will be high when TG goes high.
1 Clock 4 will be low when TG goes high.

6 CK3LOW 0 Clock 3 will be high when TG goes high.
1 Clock 3 will be low when TG goes high.

5 CK1LOW 0 Clock 1 & 2 will be high when TG goes high.
1 Clock 1 & 2 will be low when TG goes high.

4-0 TGSHLD[4:0] CCD TG shoulder width (in pixel time). Please refer to Reg34.

Note: Designers have to program the TGSHLD >= 2 (more than two).

Offset 1Eh ……..…….. Default value = 8'h20

WDTIME3	WDTIME2	WDTIME1	WDTIME0	LINESEL3	LINESEL2	LINESEL1	LINESEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-4 WDTIME[3:0] To set watch-dog time.
The unit is 30 seconds.

3-0 LINESEL[3:0] To set vertical resolution for CIS or dummy lines for CCD.
CIS : LINESEL = 0 full resolution.
= 1 1/2 resolution.
= 2 1/3 resolution .
…..
= 15 1/16 resolution.
CCD : LINESEL = 0 no dummy line.
= 1 1 dummy line.
= 2 2 dummy lines.
…..
= 15 15 dummy lines.
Note: In contrary to dummy line feature in CCD, for low resolution in CIS, the scanning speed is improved by implementing fast motor moving.

Offset 1Fh ……..…….. Default value = 8'h00

SCANFED7	SCANFED6	SCANFED5	SCANFED4	SCANFED3	SCANFED2	SCANFED1	SCANFED0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 SCANFED[7:0] Steps number setting for moving to scanning position.
Please refer to description of Reg6A
Note: 1.it cannot be programmed to logic zero.
2.it can be multiplied by $2^{*STEPTIM}$

Offset 20h ……..…….. Default value = 8'h00

BUFSEL7	BUFSEL6	BUFSEL5	BUFSEL4	BUFSEL3	BUFSEL2	BUFSEL1	BUFSEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 BUFSEL[7:0] To set buffer condition.
When buffer is full, scanner will stop and wait for host to read out image data from SDRAM.
The valid data count (has not been read) is represented by VALIDWORD (in word).

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If VALIDWORD < buffer condition, then the scanner will re-start to scan.

Following are the units of this register under various SDRAM size.
16M bits SDRAM : 4k words
64M bits SDRAM : 16k words
128M bits SDRAM : 32K words
256M bits SDRAM : 64K words
512M bits SDRAM : 128K words

Offset 21h ……..……..……..……..……. Default value = 8'h00

STEPNO7	STEPNO6	STEPNO5	STEPNO4	STEPNO3	STEPNO2	STEPNO1	STEPNO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 STEPNO[7:0] Steps number of "table one" for the acceleration/deceleration of scanning moving.
Please refer to section 6.19 and the descriptions of Reg24 & Reg6A.
Note: 1.It cannot be programmed to logic zero.
2.it can be multiplied by2*STEPTIM

Offset 22h ……..……..……..……..……. Default value = 8'h00

FWDSTEP7	FWDSTEP6	FWDSTEP5	FWDSTEP4	FWDSTEP3	FWDSTEP2	FWDSTEP1	FWDSTEP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FWDSTEP[7:0] Steps number for forward moving when buffer condition is met.
Please refer to section 6.19 and the descriptions of Reg20 & Reg24.
Note: 1.It cannot be programmed to logic zero.
2.it can be multiplied by2*STEPTIM

Offset 23h ……..……..……..……..……. Default value = 8'h00

BWDSTEP7	BWDSTEP6	BWDSTEP5	BWDSTEP4	BWDSTEP3	BWDSTEP2	BWDSTEP1	BWDSTEP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

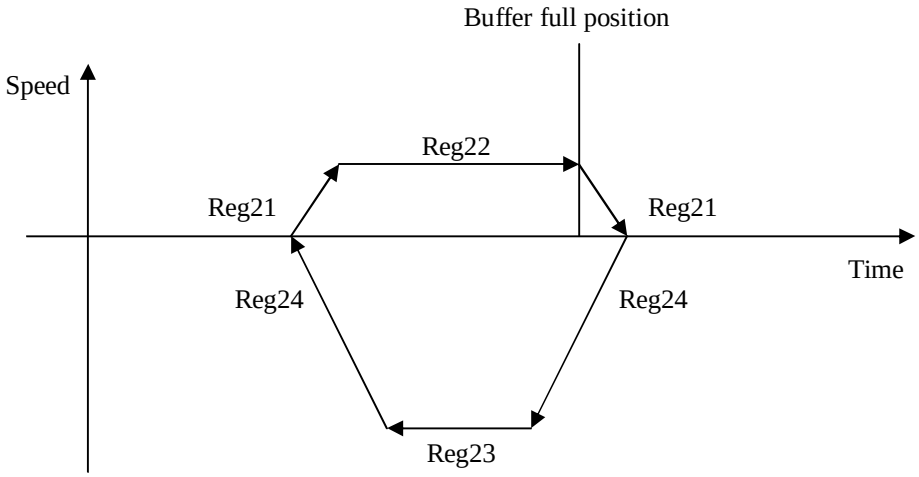
7-0 BWDSTEP[7:0] Steps number for backward moving when image buffer is full.
Please refer to section 6.19 and the descriptions of Reg24.
Note: 1.It cannot be programmed to logic zero.
2.it can be multiplied by2*STEPTIM

Offset 24h ……..……..……..……..……. Default value = 8'h00

FASTNO7	FASTNO6	FASTNO5	FASTNO4	FASTNO3	FASTNO2	FASTNO1	FASTNO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FASTNO[7:0] Steps number of "table two" for the acceleration/deceleration when image buffer is full.
Please refer to section 6.19 and the descriptions of Reg20.
Note: It cannot be programmed to logic zero.

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Offset 25h ……..…….……..……..…..……. Default value = 8'h00

X	X	X	X	LINCNT19	LINCNT18	LINCNT17	LINCNT16
X	X	X	X	R/W	R/W	R/W	R/W

7-4 RESERVED -

3-0 LINCNT[19:16] Scanning lines count specified by designers.
Note: It cannot be programmed to logic zero.

Offset 26h ……..…….……..……..…..……. Default value = 8'h00

LINCNT15	LINCNT14	LINCNT13	LINCNT12	LINCNT11	LINCNT10	LINCNT9	LINCNT8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 LINCNT[15:8] Scanning lines count specified by designers.
Note: It cannot be programmed to logic zero.

Offset 27h ……..…….……..……..…..……. Default value = 8'h00

LINCNT7	LINCNT6	LINCNT5	LINCNT4	LINCNT3	LINCNT2	LINCNT1	LINCNT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 LINCNT[7:0] Scanning lines count specified by designers.
Note: It cannot be programmed to logic zero.

Offset 28h ……..…….……..……..…..……. Default value = 8'h00

GMMWRDATA
W

GMMWRDATA This port is for designers to write gamma table.

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Offset 29h ……..……..……..…….. Default value = 8'h00

X	X	X	RAMADDR20	RAMADDR19	RAMADDR18	RAMADDR17	RAMADDR16
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

4-0 RAMADDR[20:16] SDRAM start address (in word) to access data. The unit is 16 words.
Note: The real SDRAM address IRAM_A[24:0]={RAMADDR[20:0] appended by 0000}.

Offset 2Ah ……..……..……..…….. Default value = 8'h00

RAMADDR15	RAMADDR14	RAMADDR13	RAMADDR12	RAMADDR11	RAMADDR10	RAMADDR9	RAMADDR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 RAMADDR[15:8] SDRAM start address (in word) to access data. The unit is 16 words.
Note: The real SDRAM address IRAM_A[24:0]={RAMADDR[20:0] appended by 0000}.

Offset 2Bh ……..……..……..…….. Default value = 8'h00

RAMADDR7	RAMADDR6	RAMADDR5	RAMADDR4	RAMADDR3	RAMADDR2	RAMADDR1	RAMADDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 RAMADDR[7:0] SDRAM start address (in word) to access data. The unit is 16 words.
Note: The real SDRAM address IRAM_A[24:0]={RAMADDR[20:0] appended by 0000}.

Offset 2Ch ……..……..……..…….. Default value = 8'h00

X	X	DPISET13	DPISET12	DPISET11	DPISET10	DPISET9	DPISET8
X	X	R/W	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

4-0 DPISET[13:8] Set resolution in dpi for average or deletion type.
A. average type : digital average function support 1/2,1/3,1/4,1/5,1/6,1/8,1/10,1/12,1/15.
a. 9600 dpi mode CCD:support 4800,3200,2400,1920,1600,1200,960,800,640 dpi.
b. 4800 dpi mode CCD:support 2400,1600,1200,960,800,480,400,320 dpi.
c. 2400 dpi mode CCD:support 1200,800,600,480,400,300,240,200,160 dpi.
d. 1200 dpi mode CCD:support 600,400,300,240,200,150,120,100,80 dpi.
e. 600 dpi mode CCD:support 300,200,150,120,100,75,60,50,40 dpi.
B. deletion type : 9600,4800,2400,1200 or 600dpi to 1 dpi setting decrement by one dpi.
Note: It cannot be programmed to logic zero.

Offset 2Dh ……..……..……..…….. Default value = 8'h00

DPISET7	DPISET6	DPISET5	DPISET4	DPISET3	DPISET2	DPISET1	DPISET0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 DPISET[7:0] Set resolution in dpi for average or deletion type.
A. average type : digital average function support 1/2,1/3,1/4,1/5,1/6,1/8,1/10,1/12,1/15.
a. 9600 dpi mode CCD:support 4800,3200,2400,1920,1600,1200,960,800,640 dpi.
b. 4800 dpi mode CCD:support 2400,1600,1200,960,800,480,400,320 dpi.
c. 2400 dpi mode CCD:support 1200,800,600,480,400,300,240,200,160 dpi.

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d. 1200 dpi mode CCD:support 600,400,300,240,200,150,120,100,80 dpi.
e. 600 dpi mode CCD:support 300,200,150,120,100,75,60,50,40 dpi.

B. deletion type : 9600,4800,2400,1200 or 600dpi to 1 dpi setting decrement by one dpi.

Note: It cannot be programmed to logic zero.

Offset 2Eh …….……..……..……..……..……..……..…… Default value = 8'h00

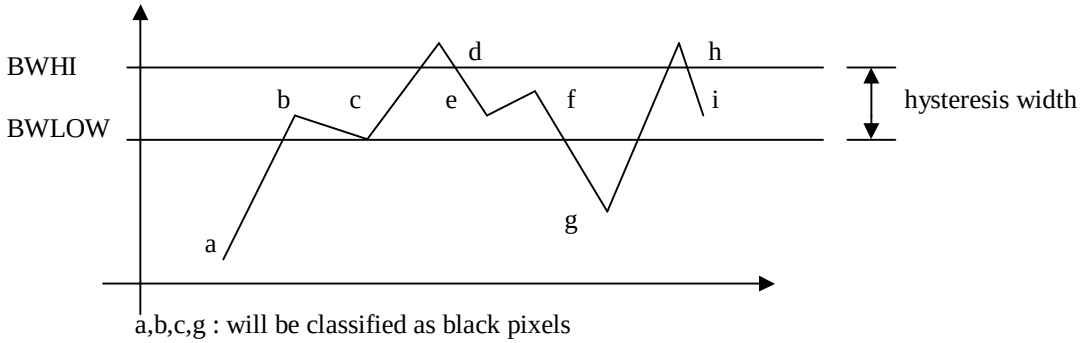
BWHI7	BWHI6	BWHI5	BWHI4	BWHI3	BWHI2	BWHI1	BWHI0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 BWHI[7:0] High level of Black & White threshold.

Offset 2Fh …….……..……..……..……..……..……..…… Default value = 8'h00

BWLOW7	BWLOW6	BWLOW5	BWLOW4	BWLOW3	BWLOW2	BWLOW1	BWLOW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 BWLOW[7:0] Low level of Black & White threshold.



a,b,c,g : will be classified as black pixels
d,e,f,h,i : will be classified as white pixels

Offset 30h …….……..……..……..……..……..……..…… Default value = 8'h00

STRPIXEL15	STRPIXEL14	STRPIXEL13	STRPIXEL12	STRPIXEL11	STRPIXEL10	STRPIXEL9	STRPIXEL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 STRPIXEL[15:8] The start pixel position of horizontal line (unit : pixel count).
STRPIXEL=(TGW+2*TGSHLD)+start pixels number (count from CCD pixel 0)
Note: 1.It cannot be programmed to logic zero.
2.If the DPI9600 control bit is set to "1",the STRPIXEL is doubled.

Offset 31h …….……..……..……..……..……..……..…… Default value = 8'h00

STRPIXEL7	STRPIXEL6	STRPIXEL5	STRPIXEL4	STRPIXEL3	STRPIXEL2	STRPIXEL1	STRPIXEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 STRPIXEL[7:0] The start pixel position of horizontal line (unit : pixel count).
STRPIXEL=(TGW+2*TGSHLD)+start pixels number (count from CCD pixel 0)
Note: 1.It cannot be programmed to logic zero.
2.If the DPI9600 control bit is set to "1",the STRPIXEL is doubled.

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Offset 32h ……..……..……..…….. Default value = 8'h00

ENDPIXEL15	ENDPIXEL14	ENDPIXEL13	ENDPIXEL12	ENDPIXEL11	ENDPIXEL10	ENDPIXEL9	ENDPIXEL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 ENDPIXEL[15:8] The end pixel position of horizontal line (unit : pixel count).
ENDPIXEL=(TGW+2*TGSHLD)+end pixels number (count from CCD pixel 0)
Note: 1.It cannot be programmed to logic zero.
2.If the DPI9600 control bit is set to "1",the STRPIXEL is doubled.

Offset 33h ……..……..……..…….. Default value = 8'h00

ENDPIXEL7	ENDPIXEL6	ENDPIXEL5	ENDPIXEL4	ENDPIXEL3	ENDPIXEL2	ENDPIXEL1	ENDPIXEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

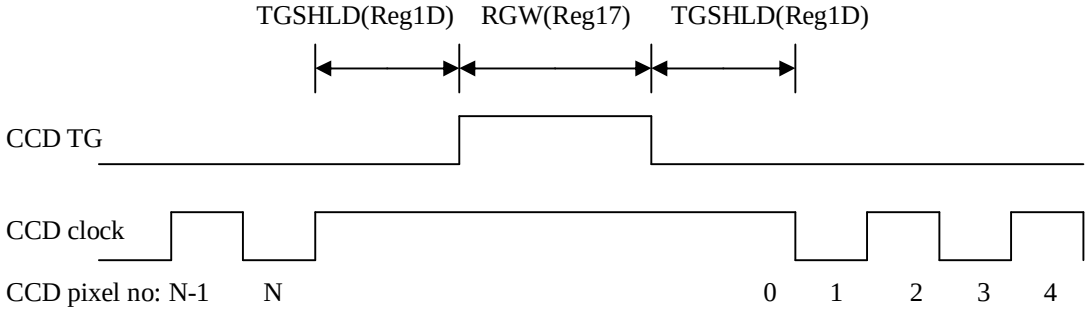
7-0 ENDPIXEL[7:0] The end pixel position of horizontal line (unit : pixel count).
ENDPIXEL=(TGW+2*TGSHLD)+end pixels number (count from CCD pixel 0)
Note: 1.It cannot be programmed to logic zero.
2.If the DPI9600 control bit is set to "1",the STRPIXEL is doubled.

Offset 34h ……..……..……..…….. Default value = 8'h00

DUMMY7	DUMMY6	DUMMY5	DUMMY4	DUMMY3	DUMMY2	DUMMY1	DUMMY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 DUMMY[7:0] The CCD dummy & optical black pixels number (unit : pixel count).
Note: It cannot be programmed to logic zero.

Reg30,31,32,33 and 34 setting rule.



For example, start pixel is 65 ,end pixel is 100 and CCD dummy pixel is 64,
Then STRPIXEL=(TGW+2*TGSHLD)+65.
ENDPIXEL=(TGW+2*TGSHLD)+100.
DUMMY =(TGW+2*TGSHLD)+64.

Offset 35h ……..……..……..…….. Default value = 8'h00

MAXWD24	MAXWD23	MAXWD22	MAXWD21	MAXWD20	MAXWD19	MAXWD18	MAXWD17
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 MAXWD[24:17] Maximum word size per line for ASIC estimation. The unit is 2 words.
If available buffer size < MAXWD, then "buffer full" state will be set. The scanner execute backtracking.

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Offset 36h …….. Default value = 8'h00

MAXWD16	MAXWD15	MAXWD14	MAXWD13	MAXWD12	MAXWD11	MAXWD10	MAXWD9
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 MAXWD[16:9] Maximum word size per line for ASIC estimation. The unit is 2 words.
If available buffer size < MAXWD, then "buffer full" state will be set. The scanner execute backtracking.

Offset 37h …….. Default value = 8'h00

MAXWD8	MAXWD7	MAXWD6	MAXWD5	MAXWD4	MAXWD3	MAXWD2	MAXWD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 MAXWD[8:1] Maximum word size per line for ASIC estimation. The unit is 2 words.
If available buffer size < MAXWD, then "buffer full" state will be set. The scanner execute backtracking.

Offset 38h …….. Default value = 8'h2A

LPERIOD15	LPERIOD14	LPERIOD13	LPERIOD12	LPERIOD11	LPERIOD10	LPERIOD9	LPERIOD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 LPERIOD[15:8] Line period (or exposure time) for CCD or CIS.
Unit : pixel count
Note: It cannot be programmed to logic zero.

Offset 39h …….. Default value = 8'h30

LPERIOD7	LPERIOD6	LPERIOD5	LPERIOD4	LPERIOD3	LPERIOD2	LPERIOD1	LPERIOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 LPERIOD[7:0] Line period (or exposure time) for CCD or CIS.
Unit : pixel count
Note: It cannot be programmed to logic zero.

Offset 3Ah

X	X	X	X	X	X	X	FEWRDATA8
X	X	X	X	X	X	X	W

7-1 RESERVED -

0 FEWRDATA8 This port is for designers to write control register of front-end.

Offset 3Bh

FEWRDATA7	FEWRDATA6	FEWRDATA5	FEWRDATA4	FEWRDATA3	FEWRDATA2	FEWRDATA1	FEWRDATA0
W	W	W	W	W	W	W	W

7-0 FEWRDATA[7:0] This port is for designers to write control register of front-end.

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Offset 3Ch

RAMWRDATA
W

RAMWRDATA This port is for designers to write data into SDRAM.

Offset 3Dh …….……..……..……..……..……..……..……..…. Default value = 8'h00

X	X	X	X	FEEDL19	FEEDL18	FEEDL17	FEEDL16
X	X	X	X	R/W	R/W	R/W	R/W

7-4 RESERVED -

3-0 FEEDL[19:16] Steps number of motor moving.
Note: It cannot be programmed to logic zero.

Offset 3Eh …….……..……..……..……..……..……..……..…. Default value = 8'h00

FEEDL15	FEEDL14	FEEDL13	FEEDL12	FEEDL11	FEEDL10	FEEDL9	FEEDL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FEEDL[15:8] Steps number of motor moving.
Note: It cannot be programmed to logic zero.

Offset 3Fh …….……..……..……..……..……..……..……..…. Default value = 8'h00

FEEDL7	FEEDL6	FEEDL5	FEEDL4	FEEDL3	FEEDL2	FEEDL1	FEEDL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FEEDL[7:0] Steps number of motor moving.
Note: It cannot be programmed to logic zero.

Offset 40h

DOCSNR	ADFSNR	COVERSNR	CHKVER	DOCJAM	HISPDFLG	MOTMFLG	DATAENB
R	R	R	R	R	R	R	R

7 DOCSNR Respond to document sensor status for ADF function.

6 ADFSNR Respond to ADF sensor status for ADF function.

5 COVERSNR Respond to cover sensor status for ADF function.

4 CHKVER It is fixed to '1' to indicate that the value in Reg00 is valid.

3 DOCJAM Respond to document feeding status for ADF function.
0 No jam happened.
1 Document jammed.

2 HISPDFLG
0 Motor is not in high-speed moving.
1 Motor is in high-speed moving.

1 MOTMFLG
0 Motor is stop.
1 Motor is moving.

0 DATAENB
0 Scanner is in command mode. Designers can access other data in SDRAM rather than image data.
1 Scanner is in scanning mode. Designers can only read the image data.

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Offset 41h

PWRBIT	BUFEMPTY	FEEDFSH	SCANFSH	HOMESNR	LAMPSTS	FEBUSY	MOTORENB
R	R	R	R	R	R	R	R

7	**PWRBIT**		To indicate power status. If it is reset, the power had been turned off. Power on initial process will set PWRBIT to 0. This bit will have the same value as bit 4 of Reg06 except for it's read only.
6	**BUFEMPTY**	0	The image buffer is not empty.
		1	The image buffer is empty.
5	**FEEDFSH**	0	Motor feeding is not finished.
		1	Motor feeding is finished.
4	**SCANFSH**	0	Scanning is not finished.
		1	Scanning is finished.
3	**HOMESNR**	0	Home sensor is on (is not located in home position).
		1	Home sensor is off (located in home position).
2	**LAMPSTS**	0	Lamp is off.
		1	Llamp is on.
1	**FEBUSY**	0	Front end is ready for read/write operations.
		1	Front end is busy and can not perform read/write operations.
0	**MOTORENB**	0	Motor is not operation.
		1	Motor is operation.

Offset 42h …….……..……..……..……..……..……..……..……. Default value = 8'h00

VALIDWORD 24	VALIDWORD 23	VALIDWORD 22	VALIDWORD 21	VALIDWORD 20	VALIDWORD 19	VALIDWORD 18	VALIDWORD 17
R	R	R	R	R	R	R	R

7-0	**VALIDWORD [24:17]**	The available image data stored in SDRAM for host to read. The unit is in two words.

Offset 43h …….……..……..……..……..……..……..……..……. Default value = 8'h00

VALIDWORD 16	VALIDWORD 15	VALIDWORD 14	VALIDWORD 13	VALIDWORD 12	VALIDWORD 11	VALIDWORD 10	VALIDWORD 9
R	R	R	R	R	R	R	R

7-0	**VALIDWORD [16:9]**	The available image data stored in SDRAM for host to read. The unit is in two words.

Offset 44h …….……..……..……..……..……..……..……..……. Default value = 8'h00

VALIDWORD 8	VALIDWORD 7	VALIDWORD 6	VALIDWORD 5	VALIDWORD 4	VALIDWORD 3	VALIDWORD 2	VALIDWORD 1
R	R	R	R	R	R	R	R

7-0	**VALIDWORD [8:1]**	The available image data stored in SDRAM for host to read. The unit is in two words.

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Offset 45h

RAMRDDATA
R

RAMRDDATA This port for designers to read data from SDRAM.

Offset 46h

X	X	X	X	X	X	X	FERDDATA8
X	X	X	X	X	X	X	R

7-1 RESERVED -

0 FERDDATA8 This port is for designers to read control register from front-end.

Offset 47h

FERDDATA7	FERDDATA6	FERDDATA5	FERDDATA4	FERDDATA3	FERDDATA2	FERDDATA1	FERDDATA0
R	R	R	R	R	R	R	R

7-0 FERDDATA[7:0] This port is for designers to read control register from front-end.

Offset 48h …….……..……..……..……..……..……..……..……. Default value = 8'h00

X	X	X	X	FEDCNT19	FEDCNT18	FEDCNT17	FEDCNT16
X	X	X	X	R	R	R	R

7-4 RESERVED -

3-0 FEDCNT[19:16] Steps number which motor has moved.
For example, after setting the moving steps number (Reg 3D, 3E 3F) and execute the moving command (Reg 0F), designers can get steps number which has been moved via these registers. It can be reset to by FULLSTP command.

Offset 49h …….……..……..……..……..……..……..……..……. Default value = 8'h00

FEDCNT15	FEDCNT14	FEDCNT13	FEDCNT12	FEDCNT11	FEDCNT10	FEDCNT9	FEDCNT8
R	R	R	R	R	R	R	R

7-0 FEDCNT[15:8] Steps number which motor has moved.
For example, after setting the moving steps number (Reg 3D, 3E 3F) and execute the moving command (Reg 0F), designers can get steps number which has been moved via these registers .It can be reset to by FULLSTP command.

Offset 4Ah …….……..……..……..……..……..……..……..……. Default value = 8'h00

FEDCNT7	FEDCNT6	FEDCNT5	FEDCNT4	FEDCNT3	FEDCNT2	FEDCNT1	FEDCNT0
R	R	R	R	R	R	R	R

7-0 FEDCNT[7:0] Steps number which motor has moved.
For example, after setting the moving steps number (Reg 3D, 3E 3F) and execute the moving command (Reg 0F), designers can get steps number which has been moved via these registers.It can be reset to by FULLSTP command.

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Offset 4Bh …….……..……..……..……..……..……..……..……. Default value = 8'h00

X	X	X	X	SCANCNT19	SCANCNT18	SCANCNT17	SCANCNT16
X	X	X	X	R	R	R	R

7-4 RESERVED -

3-0 SCANCNT[19:16] Line number which scanner has finished.
For example, after setting the line number (Reg 25, 26 27) and execute the scanning enable (bit 0 of Reg 01), designers can get line number which has been finished via these registers.

Offset 4Ch …….……..……..……..……..……..……..……..……. Default value = 8'h00

SCANCNT15	SCANCNT14	SCANCNT13	SCANCNT12	SCANCNT11	SCANCNT10	SCANCNT9	SCANCNT8
R	R	R	R	R	R	R	R

7-0 SCANCNT[15:8] Line number which scanner has finished.
For example, after setting the line number (Reg 25, 26 27) and execute the scanning enable (bit 0 of Reg 01), designers can get line number which has been finished via these registers.

Offset 4Dh …….……..……..……..……..……..……..……..……. Default value = 8'h00

SCANCNT7	SCANCNT6	SCANCNT5	SCANCNT4	SCANCNT3	SCANCNT2	SCANCNT1	SCANCNT0
R	R	R	R	R	R	R	R

7-0 SCANCNT[7:0] Line number which scanner has finished.
For example, after setting the line number (Reg 25, 26 27) and execute the scanning enable (bit 0 of Reg 01), designers can get line number which has been finished via these registers.

Offset 4Eh

GMMRDDATA
R

GMMRDDATA This port is for designers to read gamma table back.

Offset 4Fh

X	X	X	ROMBSY	LCMBSY	TX232BSY	RX232BSY	RXREADY
X	X	X	R	R	R	R	R

7-5 RESERVED -

4 ROMBSY
0 EEPROM is ready for access.
1 EEPROM (93C46) is busy and can not be accessed.

3 LCMBSY
0 LCM interface is ready for access.
1 LCM interface is busy and can not be accessed.

2 TX232BSY
0 RS232 transmitter is ready for access.
1 RS232 transmitter is busy and can not be accessed.

1 RX232BSY
0 RS232 receiver is ready for access.
1 RS232 receiver is busy and can not be accessed.

0 RXREADY
0 The receiving has not been completed.

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1 Has received data number specified in Reg 88 from RS232.

Offset 50h …….. Default value = 8'h00

X	X	FERDA5	FERDA4	FERDA3	FERDA2	FERDA1	FERDA0
X	X	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RESERVED -

5-0 FERDA[5:0] Address of control register of front-end in read operation.
Before reading control register of front-end (Reg 46, 47), designers have to specify address of the control register by writing address to this port.

Offset 51h …….. Default value = 8'h00

X	X	FEWRA5	FEWRA4	FEWRA3	FEWRA2	FEWRA1	FEWRA0
X	X	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RESERVED -

5-0 FEWRA[5:0] Address of control register of front-end in write operation.
Before writing control register of front-end (Reg 3A, 3B), designers have to specify address of the control register by writing address to this port.

Offset 52h …….. Default value = 8'h00

X	X	X	RHI4	RHI3	RHI2	RHI1	RHI0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

4-0 RHI[4:0] The latch point for high-byte of R channel of AFE in every pixel.
For example, if a system is designed to have 12 clocks/pixel, and designer wants to latch the high-byte of R channel at 1'st clock in every pixel, designer has to fill '00001' to RHI [4:0].

Offset 53h …….. Default value = 8'h00

X	X	X	RLOW4	RLOW3	RLOW2	RLOW1	RLOW0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

4-0 RLOW[4:0] The latch point for low-byte of R channel of AFE in every pixel
For example, if a system is designed to have 12 clocks/pixel, and designer wants to latch the high-byte of R channel at 1'st clock in every pixel, designer has to fill '00001' to RHI [4:0].

Offset 54h …….. Default value = 8'h00

X	X	X	GHI4	GHI3	GHI2	GHI1	GHI0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

4-0 GHI[4:0] The latch point for high-byte of G channel of AFE in every pixel.

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Offset 55h …….. Default value = 8'h00

X	X	X	GLOW4	GLOW3	GLOW2	GLOW1	GLOW0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

4-0 GLOW[4:0] The latch point for low-byte of G channel of AFE in every pixel.

Offset 56h …….. Default value = 8'h00

X	X	X	BHI4	BHI3	BHI2	BHI1	BHI0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

4-0 BHI[4:0] The latch point for high-byte of B channel of AFE in every pixel.

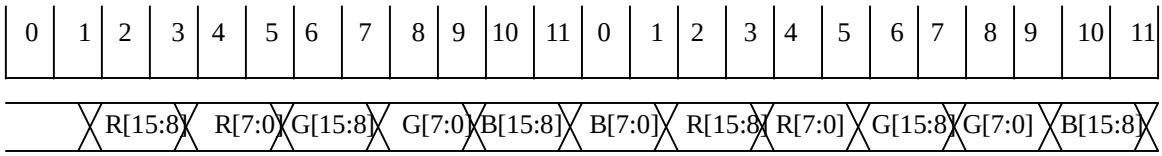
Offset 57h …….. Default value = 8'h00

X	X	X	BLOW4	BLOW3	BLOW2	BLOW1	BLOW0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

4-0 BLOW[4:0] The latch point for low-byte of B channel of AFE in every pixel.

(1). Color, gray or line-art : 12 clocks (phase)/pixel mode



RHI = 01H RLOW = 03H
GHI = 05H GLOW = 07H
BHI = 09H BLOW = 11H

Note: 16 clocks (phase)/pixel and 18 clocks(phase)/pixel modes are similar to 12 clocks(phase)/pixel mode.

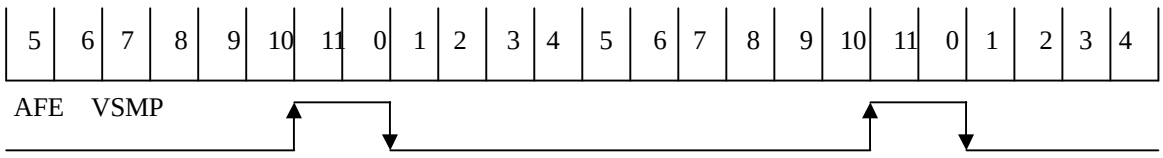
Offset 58h …….. Default value = 8'h00

VSMP4	VSMP3	VSMP2	VSMP1	VSMP0	VSMPW2	VSMPW1	VSMPW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-3 VSMP[4:0] Rising edge position of image sampling for AFE.

2-0 VSMPW[2:0] Pulse width of image sampling.

(1). Color, gray or line-art : 12 clocks (phase)/pixel mode



Reg58=52H : VSMP[4:0]=10H VSMPW[2:0]=2H

Note: 16 clocks (phase)/pixel and 18 clocks(phase)/pixel modes are similar to 12 clocks(phase)/pixel mode.

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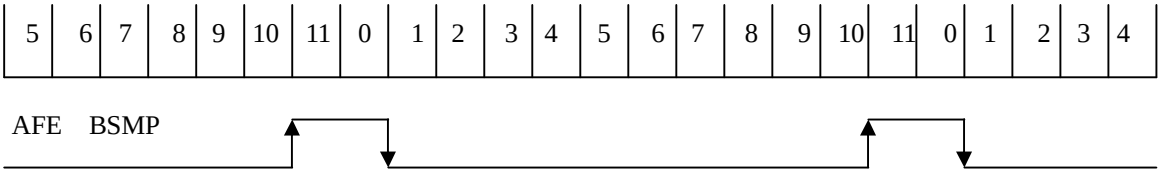
Offset 59h ……..……..……..……..……..……..……..……. Default value = 8'h00

BSMP4	BSMP3	BSMP2	BSMP1	BSMP0	BSMPW2	BSMPW1	BSMPW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-3 BSMP[4:0] Rising edge position of dark voltage sampling for AFE.

2-0 BSMPW[2:0] Pulse width of dark voltage sampling.

(1). Color, gray or line-art : 12 clocks (phase)/pixel mode



Reg59=52H : BSMP[4:0]=10H BSMPW[2:0]=2H

Note: 16 clocks (phase)/pixel and 18 clocks(phase)/pixel modes are similar to 12 clocks(phase)/pixel mode.

Offset 5Ah ……..……..……..……..……..……..……..……. Default value = 8'h00

ADCLKINV	RLCSEL	CDSREF1	CDSREF0	RLC3	RLC2	RLC1	RLC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 ADCLKINV 0 ADC clock in not reversed.
1 ADC clock is reversed.

6 RLCSEL 0 Do not select.
1 Select reset level clamp on a pixel-by-pixel basis.

5-4 CDSREF[1:0] Front-end CDS reference for line rate scanning type.

3-0 RLC[3:0] Front-end RLC for line rate scanning type.

Offset 5Bh ……..……..……..……..……..……..……..……. Default value = 8'h00

X	MTRTBL	GMMADDR13	GMMADDR12	GMMADDR11	GMMADDR10	GMMADDR9	GMMADDR8
X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 RESERVED -

6 MTRTBL 0 To write gamma tables address by GMMADDR[12:0]
1 To write motor tables address by GMMADDR[12:0]

5-0 GMMADDR[13:8] Start address for downloading gamma or motor tables (in word)

Offset 5Ch ……..……..……..……..……..……..……..……. Default value = 8'h00

GMMADDR7	GMMADDR6	GMMADDR5	GMMADDR4	GMMADDR3	GMMADDR2	GMMADDR1	GMMADDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GMMADDR[7:0] Start address for downloading gamma or motor tables (in word)

Offset 5Dh ……..……..……..……..……..……..……..……. Default value = 8'h00

HISPD7	HISPD6	HISPD5	HISPD4	HISPD3	HISPD2	HISPD1	HISPD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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7-0 HISPD[7:0] To change of the speed of motor during moving
Note: It cannot be programmed to logic zero.

Offset 5Eh ……..……..……..……..……..……..……..…….. Default value = 8'h00

DECSEL2	DECSEL1	DECSEL0	STOPTIM4	STOPTIM3	STOPTIM2	STOPTIM1	STOPTIM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-5 DECSEL[2:0] Deceleration steps number after touching home sensor.
000 1 steps deceleration
001 2 steps deceleration
010 4 steps deceleration
011 8 steps deceleration
100 16 steps deceleration
101 32 steps deceleration
110 64 steps deceleration
111 128 steps deceleration

4-0 STOPTIM[4:0] Stop time between forward and backward direction in backtracking.

Note: In ASIC simulation process, STOPTIM has to be set to tgtime=6,7.
It cannot be programmed to logic zero.

Offset 5Fh ……..……..……..……..……..……..……..…….. Default value = 8'h00

FMOVDEC7	FMOVDEC6	FMOVDEC5	FMOVDEC4	FMOVDEC3	FMOVDEC2	FMOVDEC1	FMOVDEC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FMOVDEC[7:0] Deceleration steps in table 5 for auto-go-home.
Note: 1.It cannot be programmed to logic zero.
2.It can be multiplied by 2 $*^{STEPTIM}$

Offset 60h ……..……..……..……..……..……..……..…….. Default value = 8'h00

X	X	X	Z1MOD20	Z1MOD19	Z1MOD18	Z1MOD17	Z1MOD16
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -
4-0 Z1MOD[20:16] "remainder value" of MOD operation in acceleration/deceleration tables.
ASIC calculate the moving time by MOD operation when buffer-full occurs.
Note: It should be less than LPERIOD.

Offset 61h ……..……..……..……..……..……..……..…….. Default value = 8'h00

Z1MOD15	Z1MOD14	Z1MOD13	Z1MOD12	Z1MOD11	Z1MOD10	Z1MOD7	Z1MOD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 Z1MOD[15:8] "remainder value" of MOD operation in acceleration/deceleration tables.
ASIC calculate the moving time by MOD operation when buffer-full occurs.
Note: It should be less than LPERIOD.

Offset 62h ……..……..……..……..……..……..……..…….. Default value = 8'h00

Z1MOD7	Z1MOD6	Z1MOD5	Z1MOD4	Z1MOD3	Z1MOD2	Z1MOD1	Z1MOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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7-0 Z1MOD[7:0] "remainder value" of MOD operation in acceleration/deceleration tables.
ASIC calculate the moving time by MOD operation when buffer-full occurs.
Note: It should be less than LPERIOD.

Offset 63h ……..……..……..……..……..……..…..…..…. Default value = 8'h00

X	X	X	Z2MOD20	Z2MOD19	Z2MOD18	Z2MOD17	Z2MOD16
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

7-0 Z2MOD[20:16] "remainder value" of MOD operation in acceleration/deceleration tables.
ASIC calculate the moving time by MOD operation when scanner start to move.
Note: It should be less than LPERIOD.

Note:for ACDCDIS=1,designer must subtract any small offset value from Z2MOD to solve the first time start/stop motor position problem.

Offset 64h ……..……..……..……..……..……..…..…..…. Default value = 8'h00

Z2MOD15	Z2MOD14	Z2MOD13	Z2MOD12	Z2MOD11	Z2MOD10	Z2MOD9	Z2MOD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 Z2MOD[15:8] "remainder value" of MOD operation in acceleration/deceleration tables.
ASIC calculate the moving time by MOD operation when scanner start to move.
Note: It should be less than LPERIOD.

Note:for ACDCDIS=1,designer must subtract any small offset value from Z2MOD to solve the first time start/stop motor position problem.

Offset 65h ……..……..……..……..……..……..…..…..…. Default value = 8'h00

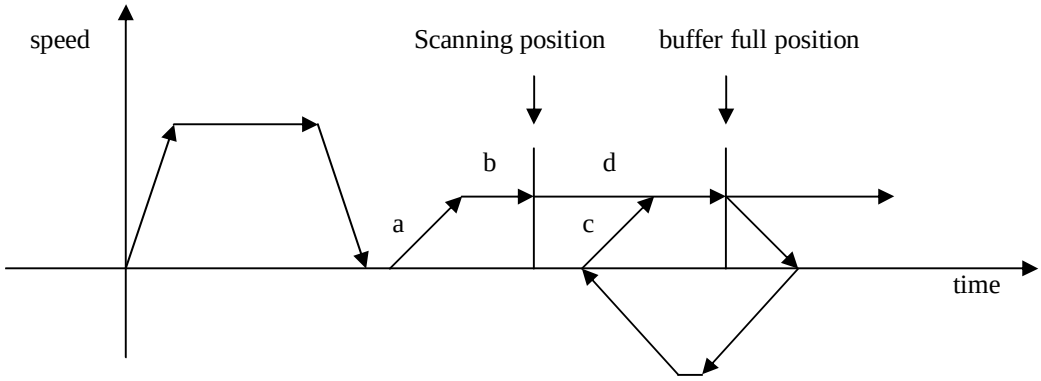
Z2MOD7	Z2MOD6	Z2MOD5	Z2MOD4	Z2MOD3	Z2MOD2	Z2MOD1	Z2MOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 Z2MOD[7:0] "remainder value" of MOD operation in acceleration/deceleration tables.
ASIC calculate the moving time by MOD operation when scanner start to move.
Note: It should be less than LPERIOD.

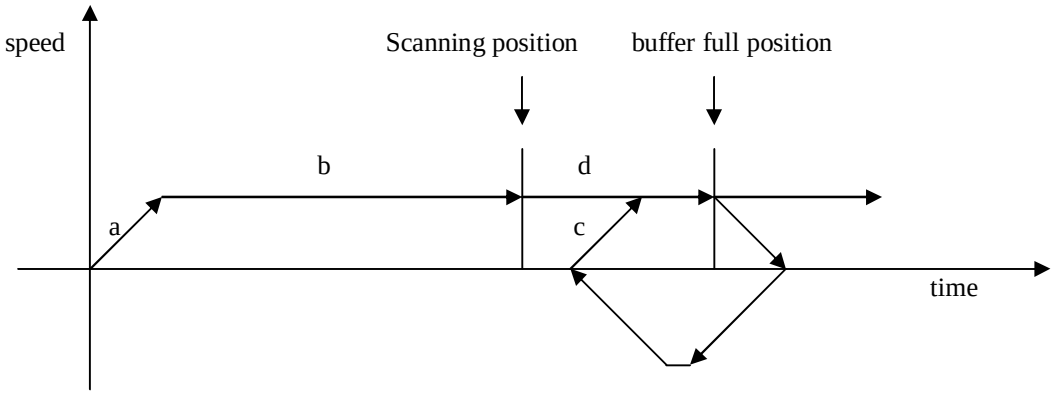
Note:for ACDCDIS=1,designer must subtract any small offset value from Z2MOD to solve the first time start/stop motor position problem.

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(1). Two table moving :



(2). One table moving :



{a+(b-1)} mode LPERIOD = Z2MOD
{c+(d-1)} mode LPERIOD = Z1MOD
For example, c (STEPNO = 4 steps for table 1) = 60H,48H,30H,18H
d (FWDSTEP = 3 steps for moving) = 18H,18H,18H
LPERIOD = 30H
Then Z1MOD = {(60H + 48H + 30H + 18H) + (18H +18H)} MOD {30H} = 00H

Note: If MCNTSET[1:0]=01 or 10 or 11,then (each step curve value + 1)/VCNT.
VCNT= system clocks per pixel / (MCNTSET+1).

Offset 66h …….. Default value = 8'h00

PHFREQ7	PHFREQ6	PHFREQ5	PHFREQ4	PHFREQ3	PHFREQ2	PHFREQ1	PHFREQ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 PHFREQ[7:0] PWM frequency for motor phase of unipolar motors
Frequency: (system clock frequency)/[(PHFREQ+1)*4

Offset 67h …….. Default value = 8'h7F

STEPSEL1	STEPSEL0	MTRPWM5	MTRPWM4	MTRPWM3	MTRPWM2	MTRPWM1	MTRPWM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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7-6 STEPSEL[1:0] For type selection of table one, table two and table three in scanning mode.
(1) For bipolar motors:
00 Full step (for 1939, 1940, 2916, 6219, 3955, 3967).
01 Half step (for 1939, 1940, 2916, 6219, 3955, 3967).
10 Quarter step (for 2916, 6219, 3955, 3967).
11 Eighth step (for 3955, 3967).
(2) For unipolar motors:
00 Two-phase-on full step.
01 Half step.
10 Reserved.
11 Single-phase-on full step.

5-0 MTRPWM[5:0] PWM duty cycle selection of table one, table two and table three of motor phase of unipolar motors in scanning mode.
MTRPWM = 0 1/64 duty
= 1 2/64 duty
= 2 3/64 duty
……
= 63 64/64 duty
Note: If PHFREQ < 0FH,then PWM setting must < (PHFREQ+1)*4

Offset 68h ……..……..……..……..……..……..……..…… Default value = 8'h7F

FSTPSEL1	FSTPSEL0	FASTPWM5	FASTPWM4	FASTPWM3	FASTPWM2	FASTPWM1	FASTPWM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 FSTPSEL[1:0] For type selection of table four and table five in command mode.
(1) For bipolar motors:
00 Full step (for 1939, 1940, 2916, 6219, 3955, 3967).
01 Half step (for 1939, 1940, 2916, 6219, 3955, 3967).
10 Quarter step (for 2916, 6219, 3955, 3967).
11 Eighth step (for 3955, 3967).
(2) For unipolar motors:
00 Two-phase-on full step.
01 Half step.
10 Reserved.
11 Single-phase-on full step.

5-0 FASTPWM[5:0] PWM duty cycle selection of table four and table five of motor phase of unipolar motors in scanning mode.
FASTPWM = 0 1/64 duty
= 1 2/64 duty
= 2 3/64 duty
……
= 63 64/64 duty
Note: If PHFREQ < 0FH,then PWM setting must < (PHFREQ+1)*4

Offset 69h ……..……..……..……..……..……..……..…… Default value = 8'h00

FSHDEC7	FSHDEC6	FSHDEC5	FSHDEC4	FSHDEC3	FSHDEC2	FSHDEC1	FSHDEC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FSHDEC[7:0] Deceleration steps after scanning finished (table three).
Note: It cannot be programmed to logic zero.

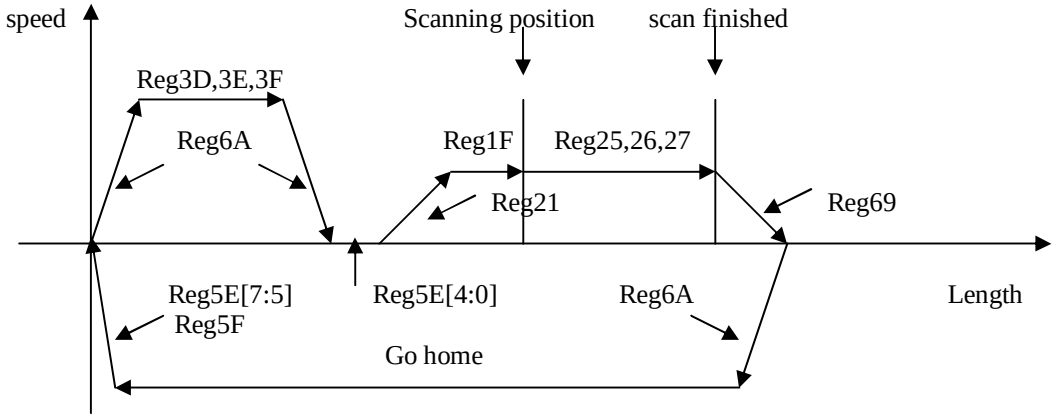
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Offset 6Ah ……..……..……..……..……..……..…….. Default value = 8'h00

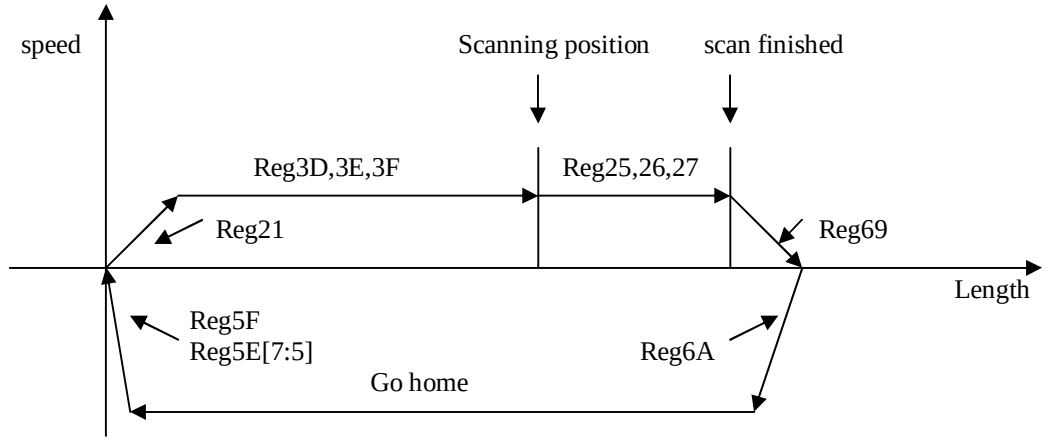
FMOVNO7	FMOVNO6	FMOVNO5	FMOVNO4	FMOVNO3	FMOVNO2	FMOVNO1	FMOVNO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FMOVNO[7:0] Acceleration/deceleration steps for fast moving (table four).
Note: 1.It cannot be programmed to logic zero.
2.It can be multiplied by 2* STEPTIM

(1). Two table type:



(2). One table type:



Offset 6Bh ……..……..……..……..……..……..…….. Default value = 8'h00

MULTFILM	GPOM13	GPOM12	GPOM11	GPOCK4	GPOCP	GPOLEDB	GPOADF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 MULTFILM 0 Disable multi-film scanning mode.
1 Enable multi-film scanning mode. Motor power will not be turned off in this mode.

6 GPOM 13 0 Select GPIO13 as general purpose I/O.
1 Select GPIO13 as V-ref control of bipolar motor driver IC to control Imax.

5 GPOM12 0 Select GPIO12 as general purpose I/O.
1 Select GPIO12 as V-ref control of bipolar motor driver IC to control Imax.

4 GPOM11 0 Select GPIO11 as general purpose I/O..
1 Select GPIO11 as V-ref control of bipolar motor driver IC to control Imax.

Note: GPIO12: 1. Add a pull up resistor on GPIO12 will indicate ASIC to turn on lamp power in power-on initial state. This behavior is independent to setting of GPOM12.

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2. Add a pull down resistor on GPIO12 will indicate ASIC to turn off lamp power in power-on initial state. This behavior is independent to setting of GPOM12.
3. This pin can control bipolar motor driver IC (2916,6219,3955 or 3967) Vref for controlling Imax current when GPOM12 is set to '1'.

GPIO11: This pin can control bipolar motor driver IC (2916,6219,3955 or 3967) Vref for controlling Imax current when GPOM11 is set to '1'.

3 GPOCK4
0 Select pin62 as CCD_CK4X
1 Select CCD_CK4X as GPO33

2 GPOCP
0 Select this pin68 as CCD_CPX.
1 CCD_CPX as GPO32.

1 GPOLEDB
0 Select this pin as LED_B for CIS.
1 Select LED_B as GPO28.

0 GPOADF
0 Select normal function for GPIO6 and GPO28.
1 Select GPIO6 as motor STEP output of 3967 and GPO28(LED_B) as DIR output of 3967.

Offset 6Ch …….. Default value = 8'h00

GPIO16	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPIO[16:9] GPIO16~9 input/output ports

Offset 6Dh …….. Default value = 8'h00

GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPIO[8:1] GPIO8~1 input/output ports

Offset 6Eh …….. Default value = 8'h00

GPOE16	GPOE15	GPOE14	GPOE13	GPOE12	GPOE11	GPOE10	GPOE9
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPOE[16:9] Select directions of GPIO16~9 ports. They can be set to different values independently.
0 Set as input port.
1 Set as output port.

Offset 6Fh …….. Default value = 8'h00

GPOE8	GPOE7	GPOE6	GPOE5	GPOE4	GPOE3	GPOE2	GPOE1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPOE[8:1] Select directions of GPIO8~1 ports. They can be set to different values independently.
0 Set as input port.
1 Set as output port.

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Offset 70h ……..…….……..……..……..……..……..…….. Default value = 8'h06

X	X	X	RSH4	RSH3	RSH2	RSH1	RSH0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

4-0 RSH[4:0] Rising edge position of CCD RS.

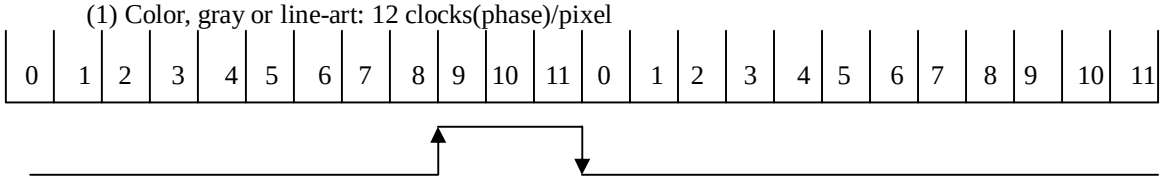
Offset 71h ……..…….……..……..……..……..……..…….. Default value = 8'h08

X	X	X	RSL4	RSL3	RSL2	RSL1	RSL0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

4-0 RSL[4:0] Falling edge position of CCD RS.

(1) Color, gray or line-art: 12 clocks(phase)/pixel



CCD RS : RSH=08H RSL=0BH

Note: 16 clocks(phase)/pixel and 18 clocks(phase)/pixel modes are similar to 12 clocks(phase)/pixel mode.

Offset 72h ……..…….……..……..……..……..……..…….. Default value = 8'h08

X	X	X	CPH4	CPH3	CPH2	CPH1	CPH0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

4-0 CPH[4:0] Rising edge position of CCD CP.

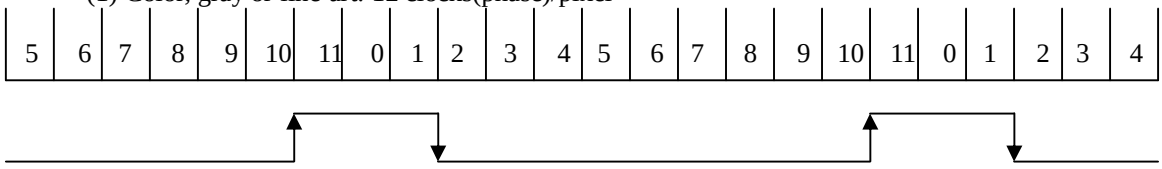
Offset 73h ……..…….……..……..……..……..……..…….. Default value = 8'h0A

X	X	X	CPL4	CPL3	CPL2	CPL1	CPL0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

4-0 CPL[4:0] Falling edge position of CCD CP.

(1) Color, gray or line-art: 12 clocks(phase)/pixel



CCD CP : CPH=0AH CPL=01H

Note: 16 clocks(phase)/pixel and 18 clocks(phase)/pixel modes are similar to 12 clocks(phase)/pixel mode.

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Offset 74h ……..……..……..……..……..……..……..…….. Default value = 8'h00

X	X	X	X	X	X	CK1MAP17	CK1MAP16
X	X	X	X	X	X	R/W	R/W

7-2 RESERVED -

1-0 CK1MAP[17:16] Bits mapping setting for CCD clock 1 or 2.

Offset 75h ……..……..……..……..……..……..……..…….. Default value = 8'h00

CK1MAP15	CK1MAP14	CK1MAP13	CK1MAP12	CK1MAP11	CK1MAP10	CK1MAP9	CK1MAP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 CK1MAP[15:8] Bits mapping setting for CCD clock 1 or 2.

Offset 76h ……..……..……..……..……..……..……..…….. Default value = 8'h00

CK1MAP7	CK1MAP6	CK1MAP5	CK1MAP4	CK1MAP3	CK1MAP2	CK1MAP1	CK1MAP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 CK1MAP[7:0] Bits mapping setting for CCD clock 1 or 2.

Offset 77h ……..……..……..……..……..……..……..…….. Default value = 8'h00

X	X	X	X	X	X	CK3MAP17	CK3MAP16
X	X	X	X	X	X	R/W	R/W

7-2 RESERVED -

1-0 CK3MAP[17:16] Bits mapping setting for CCD clock 3.

Offset 78h ……..……..……..……..……..……..……..…….. Default value = 8'h00

CK3MAP15	CK3MAP14	CK3MAP13	CK3MAP12	CK3MAP11	CK3MAP10	CK3MAP9	CK3MAP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 CK3MAP[15:8] Bits mapping setting for CCD clock 3.

Offset 79h ……..……..……..……..……..……..……..…….. Default value = 8'h00

CK3MAP7	CK3MAP6	CK3MAP5	CK3MAP4	CK3MAP3	CK3MAP2	CK3MAP1	CK3MAP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 CK3MAP[7:0] Bits mapping setting for CCD clock 3.

Offset 7Ah ……..……..……..……..……..……..……..…….. Default value = 8'h00

X	X	X	X	X	X	CK4MAP17	CK4MAP16
X	X	X	X	X	X	R/W	R/W

7-2 RESERVED -

1-0 CK4MAP[17:16] Bits mapping setting for CCD clock 4.

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Offset 7Bh ……..……..……..……..……..……..……..……..…. Default value = 8'h00

CK4MAP15	CK4MAP14	CK4MAP13	CK4MAP12	CK4MAP11	CK4MAP10	CK4MAP9	CK4MAP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 CK4MAP[15:8] Bits mapping setting for CCD clock 4.

Offset 7Ch ……..……..……..……..……..……..……..……..…. Default value = 8'h00

CK4MAP7	CK4MAP6	CK4MAP5	CK4MAP4	CK4MAP3	CK4MAP2	CK4MAP1	CK4MAP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 CK4MAP[7:0] Bits mapping setting for CCD clock 4.

Offset 7Dh ……..……..……..……..……..……..……..……..…. Default value = 8'h00

CK1NEG	CK3NEG	CK4NEG	RSNEG	CPNEG	BSMPNEG	VSMPNEG	DLYSET
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 CK1NEG
0 CCD clock1,clock2 output are synchronized with rising edge of system clock.
1 CCD clock1 & clock2 output are synchronized with falling edge of system clock.

6 CK3NEG
0 CCD clock3 output is synchronized with rising edge of system clock.
1 CCD clock3 output is synchronized with falling edge of system clock.

5 CK4NEG
0 CCD clock4 output is synchronized with rising edge of system clock.
1 CCD clock4 output is synchronized with falling edge of system clock.

4 RSNEG
0 CCD RS output is synchronized with rising edge of system clock.
1 RS output is synchronized with falling edge of system clock.

3 CPNEG
0 CCD CP output is synchronized with rising edge of system clock.
1 CCD CP output is synchronized with falling edge of system clock.

2 BSMPNEG
0 AFE video sample output is synchronized with rising edge of system clock.
1 AFE video sample output is synchronized with falling edge of system clock.

1 VSMPNEG
0 AFE dark sample output is synchronized with rising edge of system clock.
1 AFE dark sample output is synchronized with falling edge of system clock.

0 DLYSET
0 The function is disabled.
1 To enable VSMP and BSMP to delay output by 8.33ns unit. Please refer to Reg 7F.

Offset 7Eh ……..……..……..……..……..……..……..……..…. Default value = 8'h00

GPOLED25	GPOLED24	GPOLED23	GPOLED22	GPOLED21	GPOLED10	GPOLED9	GPOLED8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 GPOLED25
0 Set GPIO25 as general purpose I/O.
1 Set GPIO25 as LED output.

6 GPOLED24
0 Set GPIO24 as general purpose I/O.
1 Set GPIO24 as LED output.

5 GPOLED23
0 Set GPIO23 as general purpose I/O.
1 Set GPIO23 as LED output.

4 GPOLED22
0 Set GPIO22 as general purpose I/O.
1 Set GPIO22 as LED output.

3 GPOLED21
0 Set GPIO21 as general purpose I/O.
1 Set GPIO21 as LED output.

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2 GPOLED10 0 Set GPIO10 as general purpose I/O.
1 Set GPIO10 as LED output.

1 GPOLED9 0 Set GPIO9 as general purpose I/O.
1 Set GPIO9 as LED output.

0 GPOLED8 0 Set GPIO8 as general purpose I/O.
1 Set GPIO8 as LED output.

Offset 7Fh …….……..……...……..……..…..……..…..…. Default value = 8'h00

BSMPDLY1	BSMPDLY0	VSMPDLY1	VSMPDLY0	LEDCNT3	LEDCNT2	LEDCNT1	LEDCNT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 BSMPDLY[1:0] BSMP output delay.
00 No delay.
01 Delay 8.33ns
10 Delay 16.67ns
11 Delay 25ns.

5-4 VSMPDLY[1:0] VSMP output delay.
00 No delay.
01 Delay 8.33ns
10 Delay 16.67ns
11 Delay 25ns.

3-0 LEDCNT[1:0] LED blinking period = (LEDCNT)*(100ms on + 100ms off).
LED will not blink if LEDCNT=0.

Offset 80h ……..……..……...……..……..…..……..…..…. Default value = 8'h00

VRHOME1	VRHOME0	VRMOVE1	VRMOVE0	VRBACK1	VRBACK0	VRSCAN1	VRSCAN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 VRHOME[1:0] Vref. of the motor driver IC for go-home moving.

5-4 VRMOVE[1:0] Vref. of the motor driver IC for fast forward moving.

3-2 VRBACK[1:0] Vref. of the motor driver IC for backward moving when the image buffer is full.

1-0 VRSCAN[1:0] Vref. of the motor driver IC forward scanning moving.

Offset 81h ……..……..……...……..……..…..……..…..…. Default value = 8'h00

X	X	X	LOADSET4	LOADSET3	LOADSET2	LOADST1	LOADSET0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

4-0 LOADSET[4:0] set the data types for downloading data.

Offset 82h ……..……..……...……..……..…..……..…..…. Default value = 8'h00

CONTB3	CONTB2	CONTB1	CONTB0	CONTA3	CONTA2	CONTA1	CONTA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-4 CONTB[7:4] Set flow control counter mode (count method) for flatbed

3-0 CONTA [3:0] Set flow control counter mode (count method) for ADF

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Offset 83h ……..……..……..……..……..……..……..……..…. Default value = 8'h00

IMGSET7	IMGSET6	IMGSET5	IMGSET4	IMGSET3	IMGSET2	IMGSET1	IMGSET0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 IMGSET[7:0] Set flow-control to control image process and motor controls.

Offset 84h ……..……..……..……..……..……..……..……..…. Default value = 8'h00

PACK1	PACK0	PACKCNT5	PACKCNT4	PACKCNT3	PACKCNT2	PACKCNT1	PACKCNT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 PACK[7:6] Set data packing methods.

5-0 PACKCNT [5:0] Set packing count.

Offset 87h ……..……..……..……..……..……..……..……..…. Default value = 8'h00

X	YENB	YBIT	ACYCNRLC	ENOFFSET	LEDADD	CK4ADC	AUTOCONF
X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 RESERVED -

6 YENB
0 Disable PH_Y output of the YBIT.
1 Enable PH_Y output of the YBIT to improve half-step operation of motor control.

5 YBIT Output port of PH_Y control signal.

4 ACYCNRLC
0 Disable this function.
1 Generate RLC/ACYC pulse through BSMP pin to trigger WM8199 auto-cycling for line-by-line color scanning.

3 ENOFFSET
0 To disable this function.
1 To select automatic offset configuration for CIS color scanning.

2 LEDADD
0 Normal gray by controlling CIS single color LED array.
1 Enable true gray weighting in CIS by separately controlling the exposure times of R, G, B LED array. Please refer to Reg 10~15.

1 CK4ADC
0 Select MCLK (ADCCLK) to output default timing for specified AFE.
1 Select MCLK (ADCCLK) pin to output according to pattern defined by CK4MAP (Reg 7A,7B,7C).

0 AUTOCONF
0 To disable these functions.
1 Enable automatic channel switching and offset configuration for CIS color scanning.

Note: If YBIT=1, then YENB=1 => PH_Y=1; YENB=0 => PH_Y=0.
If YBIT=0, then YENB=1 => PH_Y=0; YENB=0 => PH_Y=1.

Offset 88h ……..……..……..……..……..……..……..……..…. Default value = 8'h00

X	X	X	RDNUM4	RDNUM3	RDNUM2	RDNUM1	RDNUM0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -

4-0 RDNUM[4:0] Set the receiving length in bytes of RS232 interface.

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Offset 89h

RS232WD7	RS232WD6	RS232WD5	RS232WD4	RS232WD3	RS232WD2	RS232WD1	RS232WD0
-	-	-	-	-	-	-	-

7-0 RS232WD[7:0] This port is for designers to write data to RS232 interface.

Offset 8Ah

RS232RD7	RS232RD6	RS232RD5	RS232RD4	RS232RD3	RS232RD2	RS232RD1	RS232RD0
-	-	-	-	-	-	-	-

7-0 RS232RD[7:0] This port is for designers to read data to RS232 interface.

Offset 8Bh ……..……...……...……..……...……...…... Default value = 8'h00

ROMADDR7	ROMADDR6	ROMADDR5	ROMADDR4	ROMADDR3	ROMADDR2	ROMADDR1	ROMADDR0
-	-	-	-	-	-	-	-

7-0 ROMADDR[7:0] This port is for designers to write address and commands to 93C46.

Offset 8Ch

ROMWD15	ROMWD14	ROMWD13	ROMWD12	ROMWD11	ROMWD10	ROMWD9	ROMWD8
-	-	-	-	-	-	-	-

7-0 ROMWD[15:8] This port is for designers to write data to 93C46.

Offset 8Dh

ROMWD7	ROMWD6	ROMWD5	ROMWD4	ROMWD3	ROMWD2	ROMWD1	ROMWD0
-	-	-	-	-	-	-	-

7-0 ROMWD[7:0] This port is for designers to write data to 93C46.

Offset 8Eh

ROMRD15	ROMRD14	ROMRD13	ROMRD12	ROMRD11	ROMRD10	ROMRD9	ROMRD8
-	-	-	-	-	-	-	-

7-0 ROMRD[15:8] This port is for designers to read data to 93C46.

Offset 8Fh

ROMRD7	ROMRD6	ROMRD5	ROMRD4	ROMRD3	ROMRD2	ROMRD1	ROMRD0
-	-	-	-	-	-	-	-

7-0 ROMRD[7:0] This port is for designers to read data to 93C46.

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Offset 90h ……..……..……..……..……..……..……..…. Default value = 8'h00

X	X	X	X	RREFED11	RREFED10	RREFED9	RREFED8
X	X	X	X	R/W	R/W	R/W	R/W

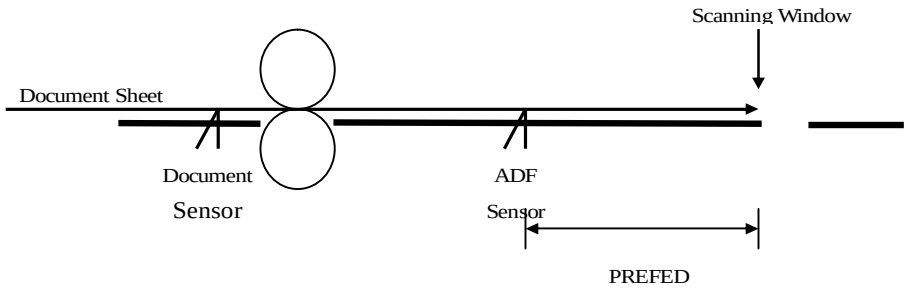
7-4 RESERVED -

4-0 RREFED[11:8] Pre-feed steps for ADF (or sheetfed scanner).

Offset 91h ……..……..……..……..……..……..……..…. Default value = 8'h00

RREFED7	RREFED6	RREFED5	RREFED4	RREFED3	RREFED2	RREFED1	RREFED0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 RREFED[7:0] Pre-feed steps for ADF (or sheetfed scanner).



Note: If the DPI9600 control bit is set to "1", the STRPIXEL is doubled.

Offset 92h ……..……..……..……..……..……..……..…. Default value = 8'h00

PSTFED15	PSTFED14	PSTFED13	PSTFED12	PSTFED11	PSTFED10	PSTFED9	PSTFED8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

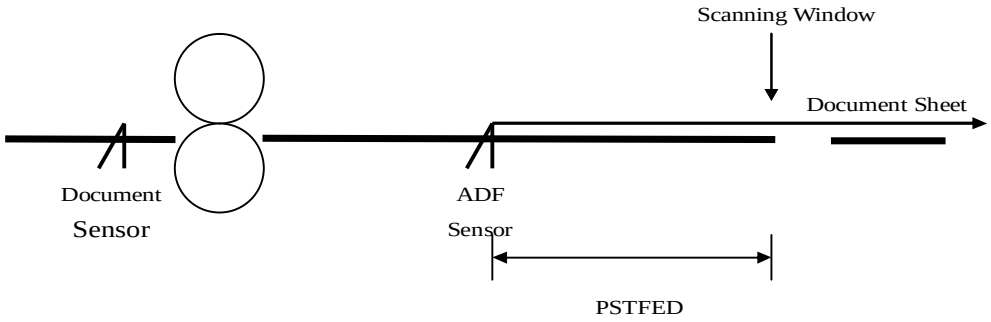
7-0 PSTFED[15:8] Past scanning steps for ADF (or sheetfed scanner).

Offset 93h ……..……..……..……..……..……..……..…. Default value = 8'h00

PSTFED7	PSTFED6	PSTFED5	PSTFED4	PSTFED3	PSTFED2	PSTFED1	PSTFED0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 PSTFED[7:0] Past scanning steps for ADF (or sheetfed scanner).

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Offset 94h ……..……..……..……..……..……..…….. Default value = 8'h00

MTRPLS7	MTRPLS6	MTRPLS5	MTRPLS4	MTRPLS3	MTRPLS2	MTRPLS1	MTRPLS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 MTRPLS[7:0] Pulse width of ADF motor trigger signal (GPIO6). It's valid when ADFSEL = 1.

Offset 95h ……..……..……..……..……..……..…….. Default value = 8'h00

X	X	X	X	SCANLEN19	SCANLEN18	SCANLEN17	SCANLEN16
X	X	X	X	R/W	R/W	R/W	R/W

7-4 RESERVED -

4-0 SCANLEN[19:16] Scanning length limitation of ADF (or sheetfed scanner). If the scanned lines are lager than this value but document sensor is still active (DOC_SENR is high), the paper-jam bit (bit 3 in Reg 40) will be set.

Offset 96h ……..……..……..……..……..……..…….. Default value = 8'h00

SCANLEN15	SCANLEN14	SCANLEN13	SCANLEN12	SCANLEN11	SCANLEN10	SCANLEN9	SCANLEN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 SCANLEN[8:15] Scanning length limitation of ADF (or sheetfed scanner). If the scanned lines are lager than this value but document sensor is still active (DOC_SENR is high), the paper-jam bit (bit 3 in Reg 40) will be set.

Offset 97h ……..……..……..……..……..……..…….. Default value = 8'h00

SCANLEN7	SCANLEN6	SCANLEN5	SCANLEN4	SCANLEN3	SCANLEN2	SCANLEN1	SCANLEN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 SCANLEN[7:0] Scanning length limitation of ADF (or sheetfed scanner). If the scanned lines are lager than this value but document sensor is still active (DOC_SENR is high), the paper-jam bit (bit 3 in Reg 40) will be set.

Offset 98h ……..……..……..……..……..……..…….. Default value = 8'h00

ONDUR15	ONDUR14	ONDUR13	ONDUR12	ONDUR11	ONDUR10	ONDUR9	ONDUR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 ONDUR[15:8] On duration (in system clock) of PWM for LAMP control.

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Offset 99h …….……..……..……..……..……..……..…… Default value = 8'h00

ONDUR7	ONDUR6	ONDUR5	ONDUR4	ONDUR3	ONDUR2	ONDUR1	ONDUR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 ONDUR[7:0] On duration (in system clock) of PWM for LAMP control.

Offset 9Ah …….……..……..……..……..……..……..…… Default value = 8'h00

OFFDUR15	OFFDUR14	OFFDUR13	OFFDUR12	OFFDUR11	OFFDUR10	OFFDUR9	OFFDUR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 OFFDUR[15:8] Off duration (in system clock) of PWM for LAMP control.

Offset 9Bh …….……..……..……..……..……..……..…… Default value = 8'h00

OFFDUR7	OFFDUR6	OFFDUR5	OFFDUR4	OFFDUR3	OFFDUR2	OFFDUR1	OFFDUR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 OFFDUR[7:0] Off duration (in system clock) of PWM for LAMP control.

Offset 9Ch

LCMWD7	LCMWD6	LCMWD5	LCMWD4	LCMWD3	LCMWD2	LCMWD1	LCMWD0
-	-	-	-	-	-	-	-

7-0 LCMWD[7:0] This port is for designers to write data to LCM.

Offset 9Dh …….……..……..……..……..……..……..…… Default value = 8'h00

RAMDLY1	RAMDLY0	MOTLAG	CMODE	STEPTIM1	STEPTIM0	MULDMYLN	IFRS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RAMDLY[1:0] Select timing delay for SCLK of SDRAM.

5 MOTLAG
0 Do not force the trigger position of motor trigger.
1 Force motor to locate its trigger at the end of line when dummy lines function is activated.

4 CMODE
0 Select two-pin type control for COM1 & COM2 of LCD (GPO29&30).
1 Select three-pin type control for COM1 & COM2 of LCD (GPIO10, GPO29&30).

3-2 STEPTIM[1:0] Select the multiplier of slope table. For Reg 21, 24, 5F, 69, 6A, the real slope steps are register values multiplied by STEPTIM.
STEPTIM[1:0] =00 : Slope steps = register values
=01 : Slope steps = register values * 2
=10 : Slope steps = register values * 4
=11 : Reserved

1 MULDMYLN
0 Set dummy lines are equal to LINESEL.
1 Set dummy lines are equal to LINESEL*2

0 IFRS
0 Select data writing for LCM.
1 Select address writing for LCM.

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Offset 9Eh ……..……..……..……..……..……..…….. Default value = 8'h00

X	SEL3INV	TGSTIME2	TGSTIME1	TGSTIME0	TGWTIME2	TGWTIME1	TGWTIME0
X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 RESERVED -
6 SEL3INV To invert SEL3 signals for NEC8884.
5-3 TGSTIME[2:0] To set the times of TGSHLD[4:0] . So , the width is TGSHLD[4:0]* $2^{TGSTIME}$
2-0 TGWTIME[2:0] To set the times of TGW[5:0] . So, the width is TGW[5:0]* $2^{TGWTIME}$

Offset 9Fh ……..……..……..……..……..……..…….. Default value = 8'h00

LCDCTL	LCMCTL	EPROMCTL	TGCTL	MPUCTL	MOTMPU	NEC8884	DPI960
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 LCDCTL To control LCD timing when LCD function is enabled.
6 LCMCTL To control LCD timing when LCM function is enabled.
5 EPROMCTL To control LCD timing when EEPROM function is enabled.
4 TGCTL To enable special CCD TG modes.
3 MPUCTL To enable work styles when designer use internal RISC CPU.
2 MOTMPU To select motor trigger output to MPU. The MPU can process the trigger signal.
Note: If designer set MOTMPU=1 then he must set ACDCDIS=1.
1 NEC8884 To enable NEC8884 SEL3 function.
0 DPI9600 To enable 9600d resolution.

Offset A0h ……..……..……..……..……..……..…….. Default value = 8'h00

X	X	LNOFSET5	LNOFSET4	LNOFSET3	LNOFSET2	LNOFSET1	LNOFSET0
X	X	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RESERVED -
5-0 LNOFSET[5:0] Line difference of R, G, B in packing three channels to one color line.

Offset A1h ……..……..……..……..……..……..…….. Default value = 8'h00

X	X	X	STGSET4	STGSET3	STGSET2	STGSET1	STGSET0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -
4-0 STGSET[4:0] Line difference of stagger CCD between even and odd lines in packing them to the same color line.

Offset A2h ……..……..……..……..……..……..…….. Default value = 8'h00

X	X	X	RFHSET4	RFHSET3	RFHSET2	RFHSET1	RFHSET0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -
4-0 RFHSET[4:0] Refresh time of SDRAM.
The unit is 2us.

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Offset A3h ……..……..……..……..……..……..…….. Default value = 8'h00

TRUER7	TRUER6	TRUER5	TRUER4	TRUER3	TRUER2	TRUER1	TRUER0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 TRUER[7:0] Weighting of R channel in true gray scanning.

Offset A4h ……..……..……..……..……..……..…….. Default value = 8'h00

TRUEG7	TRUEG6	TRUEG5	TRUEG4	TRUEG3	TRUEG2	TRUEG1	TRUEG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 TRUEG[7:0] Weighting of G channel in true gray scanning.

Offset A5h ……..……..……..……..……..……..…….. Default value = 8'h00

TRUEB7	TRUEB6	TRUEB5	TRUEB4	TRUEB3	TRUEB2	TRUEB1	TRUEB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 TRUEB[7:0] Weighting of B channel in true gray scanning.

Offset A6h ……..……..……..……..……..……..…….. Default value = 8'h00

GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPIO[24:17] GPIO24~17 input/output ports.

Offset A7h ……..……..……..……..……..……..…….. Default value = 8'h00

GPOE24	GPOE23	GPOE22	GPOE21	GPOE20	GPOE19	GPOE18	GPOE17
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPOE[24:17] Select directions of GPIO24~17 ports. They can be set to different values independently.
0 Set as input port.
1 Set as output port.

Offset A8h ……..……..……..……..……..……..…….. Default value = 8'h00

X	X	GPOE27	GPOE26	GPOE25	GPIO27	GPIO26	GPIO25
X	X	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RESERVED -

5-3 GPOE[27:25] Select directions of GPIO27~25 ports. They can be set to different values independently.
0 Set as input port.
1 Set as output port.

2-0 GPIO[27:25] GPIO27~25 input/output ports.

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Offset A9h ……..……..……..……..……..……..…….. Default value = 8'h00

X	X	GPO33	GPO32	GPO31	GPO30	GPO29	GPO28
X	X	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RESERVED -

5-0 GPO[33:28] GPO33~28 output ports.

Offset ABh ……..……..……..……..……..……..…….. Default value = 8'h00

GPOM9	MULSTOP2	MULSTOP1	MULSTOP0	NODECEL	TB3TB1	TB5TB2	FIX16CLK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 GPOM9 0 Select GPIO9 as general purpose I/O.
1 Select GPIO9 as V-ref control of bipolar motor driver IC to control Imax

6-4 MULSTOP[2:0] Select stop time of motor start/stop. The stop time = STOPTIM * $2^{MULSTOP}$

3 NODECEL 0 Motor decelate when carriage touch home sensor
1 Motor doesn't decelerate when carriage touch home sensor

2 TB3TB1 0 Don't replace.
1 Use table 1 of motor table to replace table 3.

1 TB5TB2 0 Don't replace.
1 Use table 2 of motor table to replace table 5.

0 FIX16CLK To enable 16 system clocks/pixel recover function

Offset ACh ……..……..……..……..……..……..…….. Default value = 8'h00

VRHOME3	VRHOME2	VRMOVE3	VRMOVE2	VRBACK3	VRBACK2	VRSCAN3	VRSCAN2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 VRHOME[3:2] Vref of the motor driver IC for go-home moving
5-4 VRMOVE[3:2] Vref of the motor driver IC for fast forward moving
3-2 VRBACK[3:2] Vref of the motor driver IC for backward moving when the image buffer is full

Offset ADh ……..……..……..……..……..……..…….. Default value = 8'h00

X	X	ADFTYP1	ADFTYP0	CCDTYP3	CCDTYP2	CCDTYP1	CCDTYP0
X	X	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RESERVED -
5-4 ADFTYP[5:4] Set ADF types like one pass, U-turn, forward & backward.
3-0 CCDTYP[3:0] Set 600 * 2 , 1200 * 2 , 2400 * 2 , 1200 * 4 , 1200 * 2 + 600 , 1200 * 4 + 600 CCD types.

Offset AEh ……..……..……..……..……..……..…….. Default value = 8'h00

X	X	MOTSET2	MOTSET1	MOTSET0	PROCESS2	PROCESS1	PROCESS0
X	X	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RESERVED -

5-3 MOTSET[5:3] Set the working methods of motor motor driver IC under ADF feeding.

2-0 PROCESS[2:0] Set data flow process under scanning.

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Offset AFh ……..……..……...……..……...……..…….. Default value = 8'h00

SCANTYP2	SCANTYP1	SCANTYP0	FEDTYP1	FEDTYP0	ADFMOVE2	ADFMOVE1	ADFMOVE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-5 SCANTYP[2:0] Set scanning types under ADF working.

4-3 FEDTYP [4:3] Set feeding types for ADF fast moving.

2-0 ADFMOVE [2:0] Set document-in moving types for ADF.

4.3 Register Mapping

4.3.1 Shading Mapping (Chunky for Single Bank)

Table 4.2 - Shading Mapping (Chunky for Single Bank)

Attribute	Resolution	Address[24:0]
Shading Mapping	600dpi (DPIHW=00)	0000000H~00083FFH SIZE : 33k
	1200dpi (DPIHW=01)	0000000H~00107FFH SIZE : 66k
	2400dpi (DPIHW=10)	0000000H~0020FFFH SIZE : 132k
	4800dpi (DPIHW=11)	0000000H~0041FFFH SIZE : 264k

4.3.2 Shading Mapping (Chunky for Double Bank)

Table 4.3 - Shading Mapping (Chunky for Double Bank)

Attribute	Resolution	Address[24:0]	
Shading Mapping	600dpi (DPIHW=00)	BABK0	0000000H~00041FFH SIZE : 16.5K
		BANK1	0004200H~00083FFH SIZE : 16.5K
	1200dpi (DPIHW=01)	BANK0	0000000H~00083FFH SIZE : 33K
		BANK1	0008400H~00107FFH SIZE : 33K
	2400dpi (DPIHW=10)	BANK0	0000000H~00107FFH SIZE : 66K
		BANK1	0010800H~0020FFFH SIZE : 66K
	4800dpi (DPIHW=11)	BANK0	0000000H~0020FFFH SIZE : 132K
		BANK1	0021000H~0041FFFH SIZE : 132K

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4.3.3 Image Buffer Mapping

Table 4.4 - Image Buffer Mapping

Attribute	Resolution	Address[24:0]	
SDRAM 16M BITS X 1 [19:0]	600DPI (DPIHW=00)	R_odd	0008400H~00317FFH(165k)
		R_even	0031800H~005ABFFH(165k)
		G_odd	005AC00H~0083FFFH(165k)
		G_even	0084000H~00AD3FFH(165k)
		B_odd	00AD400H~00D67FFH(165k)
		B_even	00D6800H~00FFBFFH(165k)
		Dummy	00FFC00H~00FFFFFH(1k)
	1200DPI (DPIHW=01)	R_odd	0010800H~00383FFH(159k)
		R_even	0038400H~005FFFFH(159k)
		G_odd	0060000H~0087BFFH(159k)
		G_even	0087C00H~00AF7FFH(159k)
		B_odd	00AF800H~00D73FFH(159k)
		B_even	00D7400H~00FEFFFH(159k)
		Dummy	00FF000H~00FFFFFH(4k)
	2400DPI (DPIHW=10)	R_odd	0021000H~0045FFFH(148k)
		R_even	0046000H~006AFFFH(148k)
		G_odd	006B000H~008FFFFH(148k)
		G_even	0090000H~00B4FFFH(148k)
		B_odd	00B5000H~00D9FFFH(148k)
		B_even	00DA000H~00FEFFFH(148k)
		Dummy	00FF000H~00FFFFFH(4k)
	4800DPI (DPIHW=11)	R_odd	0042000H~00617FFH(126k)
		R_even	0061800H~0080FFFH(126k)
		G_odd	0081000H~00A07FFH(126k)
		G_even	00A0800H~00BFFFFH(126k)
		B_odd	00C0000H~00DF7FFH(126k)
		B_even	00DF800H~00FEFFFH(126k)
		Dummy	00FF000H~00FFFFFH(4k)
SDRAM 64M BITS X 1 [21:0]	600DPI (DPIHW=00)	R_odd	0008400H~00B17FFH(677k)
		R_even	00B1800H~015ABFFH(677k)
		G_odd	015AC00H~0203FFFH(677k)
		G_even	0204000H~02AD3FFH(677k)
		B_odd	02AD400H~03567FFH(677k)
		B_even	0356800H~03FFBFFH(677k)
		Dummy	03FFC00H~03FFFFFH(1k)
	1200DPI (DPIHW=01)	R_odd	0010800H~0B83FFH(671k)
		R_even	00B8400H~15FFFFH(671k)
		G_odd	0160000H~207BFFH(671k)
		G_even	0207C00H~2AF7FFH(671k)
		B_odd	02AF800H~3573FFH(671k)
		B_even	0357400H~3FEFFFH(671k)
		Dummy	03FF000H~3FFFFFH(4k)
	2400DPI (DPIHW=10)	R_odd	0021000H~00C5FFFH(660k)
		R_even	00C6000H~016AFFFH(660k)
		G_odd	016B000H~020FFFFH(660k)
		G_even	0210000H~02B4FFFH(660k)
		B_odd	02B5000H~0359FFFH(660k)
		B_even	035A000H~03FEFFFH(660k)
		Dummy	03FF000H~03FFFFFH(4k)
	4800DPI	R_odd	0042000H~00E17FFH(638k)

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	(DPIHW=11)	R_even	00E1800H~0180FFFH(638k)
		G_odd	0181000H~02207FFH(638k)
		G_even	0220800H~02BFFFH(638k)
		B_odd	02C0000H~035F7FFH(638k)
		B_even	035F800H~03FEFFFH(638k)
		Dummy	03FF000H~03FFFFH(4k)
SDRAM 128M BITS X 1 [22:0]	600DPI (DPIHW=00)	R_odd	0010800H~0162FFFH(1354k)
		R_even	0163000H~02B57FFH(1354k)
		G_odd	02B5800H~0407FFFH(1354k)
		G_even	0408000H~055A7FFH(1354k)
		B_odd	055A800H~06ACFFFH(1354k)
		B_even	06AD000H~07FF7FFH(1354k)
		Dummy	07FF800H~07FFFFH(2k)
	1200DPI (DPIHW=01)	R_odd	0021000H~0170BFFH(1343k)
		R_even	0170C00H~02C07FFH(1343k)
		G_odd	02C0800H~04103FFH(1343k)
		G_even	0410400H~055FFFFH(1343k)
		B_odd	0560000H~06AFBFFH(1343k)
		B_even	06AFC00H~07FF7FFH(1343k)
		Dummy	07FF800H~07FFFFH(2k)
	2400DPI (DPIHW=10)	R_odd	0042000H~018C3FFH(1321k)
		R_even	018C400H~02D67FFH(1321k)
		G_odd	02D6800H~0420BFFH(1321k)
		G_even	0420C00H~056AFFFH(1321k)
		B_odd	056B000H~06B53FFH(1321k)
		B_even	06B5400H~07FF7FFH(1321k)
		Dummy	07FF800H~07FFFFH(2k)
	4800DPI (DPIHW=11)	R_odd	0010800H~0162FFFH(1354k)
		R_even	0163000H~02B57FFH(1354k)
		G_odd	02B5800H~0407FFFH(1354k)
		G_even	0408000H~055A7FFH(1354k)
		B_odd	055A800H~06ACFFFH(1354k)
		B_even	06AD000H~07FF7FFH(1354k)
		Dummy	07FF800H~07FFFFH(2k)
SDRAM 256M BITS X 1 [23:0]	600DPI (DPIHW=00)	R_odd	0008400H~02B17FFH(2725k)
		R_even	02B1800H~055ABFFH(2725k)
		G_odd	055AC00H~0803FFFH(2725k)
		G_even	0804000H~0AAD3FFH(2725k)
		B_odd	0AAD400H~0D567FFH(2725k)
		B_even	0D56800H~0FFFBFFH(2725k)
		Dummy	0FFFC00H~0FFFFFFH(1k)
	1200DPI (DPIHW=01)	R_odd	0010800H~02B83FFH(2719k)
		R_even	02B8400H~055FFFFH(2719k)
		G_odd	0560000H~0807BFFH(2719k)
		G_even	0807C00H~0AAF7FFH(2719k)
		B_odd	0AAF800H~0D573FFH(2719k)
		B_even	0D57400H~0FFEFFFH(2719k)
		Dummy	0FFFF000H~0FFFFFFH(4k)
	2400DPI (DPIHW=10)	R_odd	0021000H~02C5FFFH(2708k)
		R_even	02C6000H~056AFFFH(2708k)
		G_odd	056B000H~080FFFFH(2708k)
		G_even	0810000H~0AB4FFFH(2708k)
		B_odd	0AB5000H~0D59FFFH(2708k)
		B_even	0D5A000H~0FFEFFFH(2708k)
		Dummy	0FFFF000H~0FFFFFFH(4k)

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	4800DPI (DPIHW=11)	R_odd	0042000H~02E17FFH(2686k)
		R_even	02E1800H~0580FFFH(2686k)
		G_odd	0581000H~08207FFH(2686k)
		G_even	0820800H~0ABFFFFH(2686k)
		B_odd	0AC0000H~0D5F7FFH(2686k)
		B_even	0D5F800H~0FFEFFFH(2686k)
		Dummy	0FFFF000H~0FFFFFFH(4k)
SDRAM 512M BITS X 1 [24:0]	600DPI (DPIHW=00)	R_odd	0008400H~055BFFFH(5455k)
		R_even	055C000H~0AAFBFFH(5455k)
		G_odd	0AAFC00H~10037FFH(5455k)
		G_even	1003800H~15573FFH(5455k)
		B_odd	1557400H~1AAAFFFH(5455k)
		B_even	1AAB000H~1FFEBFFH(5455k)
		Dummy	1FFEC00H~1FFFFFFH(5k)
	1200DPI (DPIHW=01)	R_odd	0010800H~0562FFFH(5450k)
		R_even	0563000H~0AB57FFH(5450k)
		G_odd	0AB5800H~1007FFFH(5450k)
		G_even	1008000H~155A7FFH(5450k)
		B_odd	155A800H~1AACFFFH(5450k)
		B_even	1AAD000H~1FFF7FFH(5450k)
		Dummy	1FFF800H~1FFFFFFH(2k)
	2400DPI (DPIHW=10)	R_odd	0021000H~0570BFFH(5439k)
		R_even	0570C00H~0AC07FFH(5439k)
		G_odd	0AC0800H~10103FFH(5439k)
		G_even	1010400H~155FFFFH(5439k)
		B_odd	1560000H~1AAFBFFH(5439k)
		B_even	1AAFC00H~1FFF7FFH(5439k)
		Dummy	1FFF800H~1FFFFFFH(2k)
	4800DPI (DPIHW=11)	R_odd	0042000H~058C3FFH(5417k)
		R_even	58C400H~0AD67FFH(5417k)
		G_odd	AD6800H~1020BFFH(5417k)
		G_even	1020C00H~156AFFFH(5417k)
		B_odd	156B000H~1AB53FFH(5417k)
		B_even	1AB5400H~1FFF7FFH(5417k)
		Dummy	1FFF800H~1FFFFFFH(2k)

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CHAPTER 5 BLOCK DIAGRAM

5.1 USB2.0 System Block Diagram

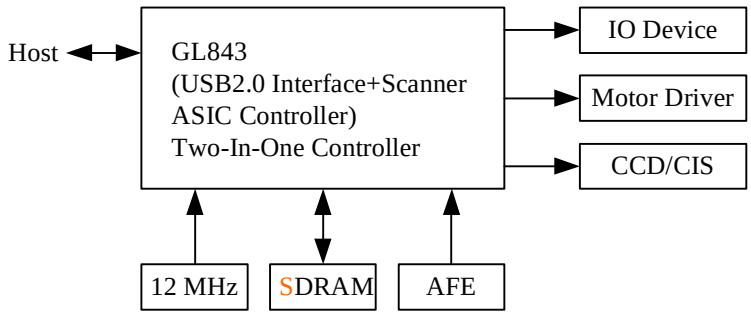


Figure 5.1 - USB2.0 System Block Diagram

5.2 Function Block Diagram

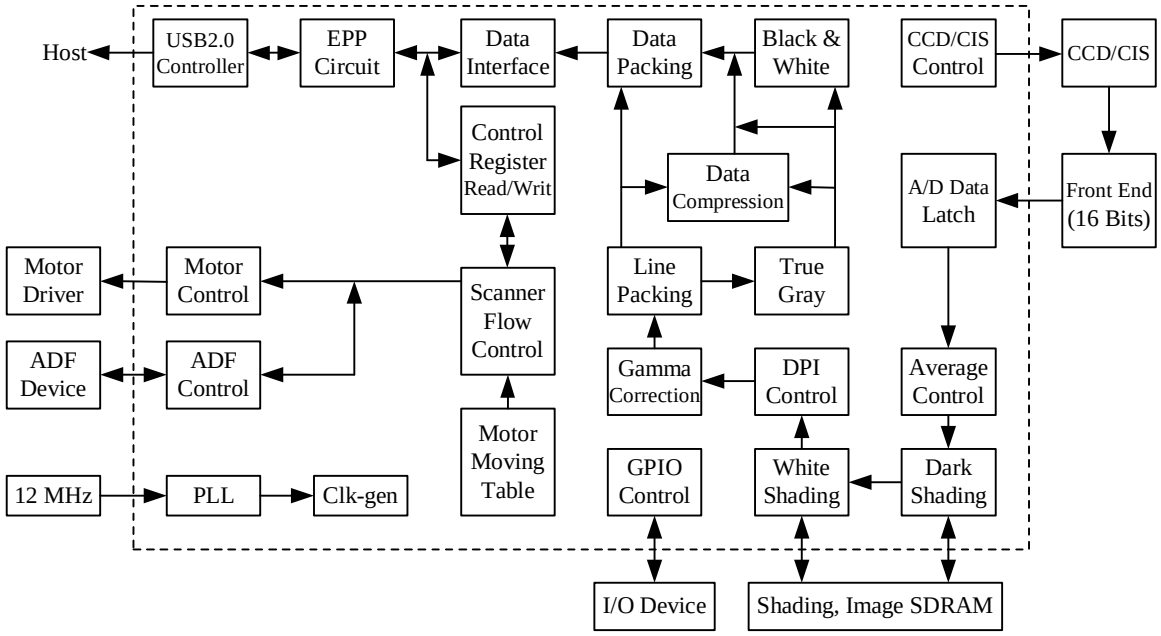


Figure 5.2 - Function Block Diagram

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CHAPTER 6 FUNCTIONAL DESCRIPTION

1 System Clock

Internal PLL.

A. Input: 12MHz crystal.

B. Output: 12, 24, 30, 40, 48 or 60 MHz to scanner controller system.

2 Pixel Clock

A. Normal mode

Scan mode 0:
- a. 12 system clock/pixel.
- b. Chunky color (three line in), gray or art scanning for CCD.
- c. Planar color scan (one line in) or Monochrome scanning for CIS.

B. Scan mode 7
- a. 16 system clock/pixel.
- b. Chunky color (three line in), gray or line-art scanning for CCD.
- c. Planar color scan (one line in) or Monochrome scanning for CIS.

C. Scan mode 6
- a. 18 system clock/pixel
- b. Chunky color (three line in), gray or art scanning for CCD.
- c. Planar color scan (one line in) or Monochrome scan for CIS.

Note: Chunky Color is R1G1B1, R2G2B2, R3G3B3,……(three-line-in or pixel rate).
Planar Color is R1, R2, R3,…..; G1, G2, G3,…….; B1, B2, B3,……..(one-line-in or line rate).
CCD: Chunky color or planar color.
CIS: Planar color.

3 Scan Speed

A. System clock = 30MHz:

a. Normal Mode: Chunky color, fine gray or fine line art scan.
(scan mode 0) 12x33.333ns/pixel = 0.4us/pixel.
(1). 600dpi: 2.160ms/line, 15.163s/page.
(2). 1200dpi: 4.320ms/line, 60.653s/page.

B. System clock = 40MHz:

a. Normal Mode: Chunky color, fine gray or fine line art scan.
12x25ns/pixel = 0.3us/pixel
(1). 600dpi: 1.620ms/line, 11.372s/page.
(2). 1200dpi: 3.240ms/line, 45.488s/page.

4 Fast Scan for Low Resolutions

Designers are allowed to increase CCD clock rates to up scanning speed in low resolutions, such as 2, 4, 8, …times..

5 Scanning Type

GL843 supports three-line-in (parallel) for CCD and one-line-in for CIS.

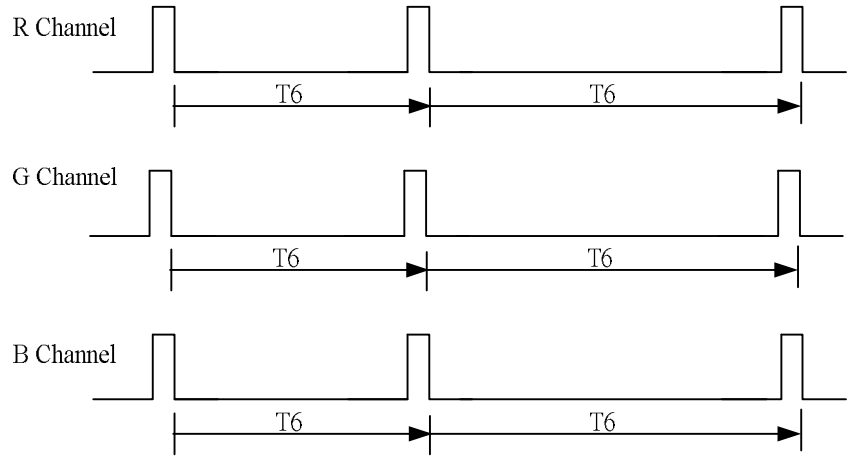
A. CCD Type

CCD Exposure control

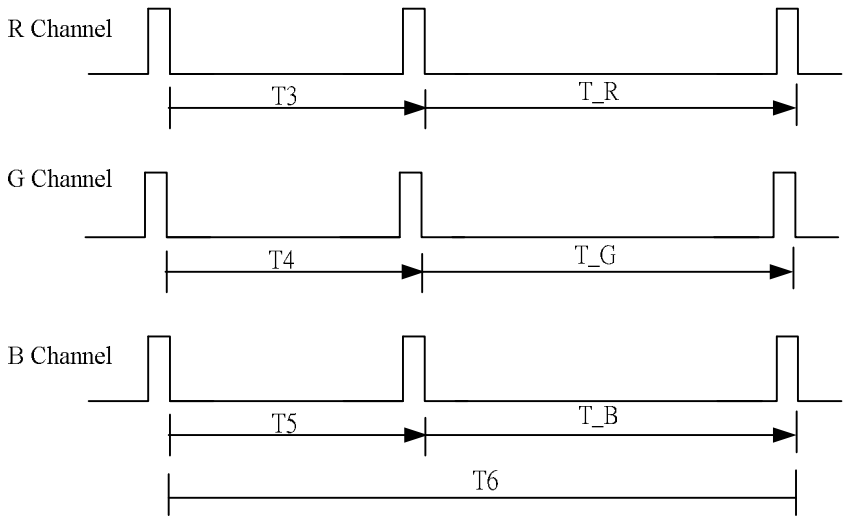
There are three modes to control CCD TG by TGMODE control bits.
Mode 0: single exposure time for R, G and B channels.
Mode 1, 2: different exposure times for R, G and B channels .

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Timing diagrams:
a.TGMODE=00
T6 is the exposure time for each color.



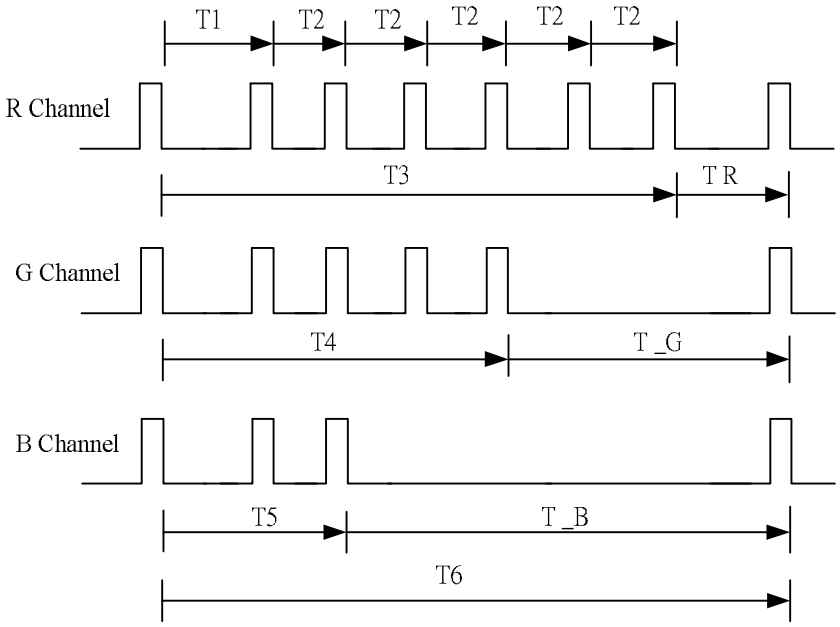
b. TGMODE=01
T3.T4 and T5 is the shift time of image data.
T_R is the exposure time of R channel.
T_G is the exposure time of G channel.
T_B is the exposure time of B channel..



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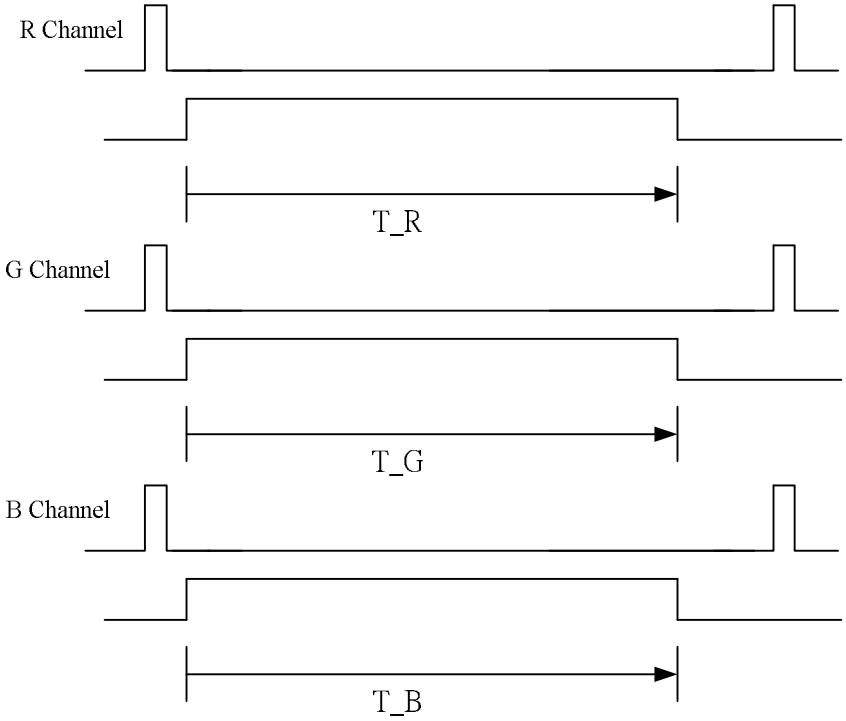
c. TGMODE=10

T1 is the shift time of image data.
T2 is for dummy lines.
T_R is the exposure time of R channel.
T_G is the exposure time of G channel.
T_B is the exposure time of B channel..



d. TGMODE=00

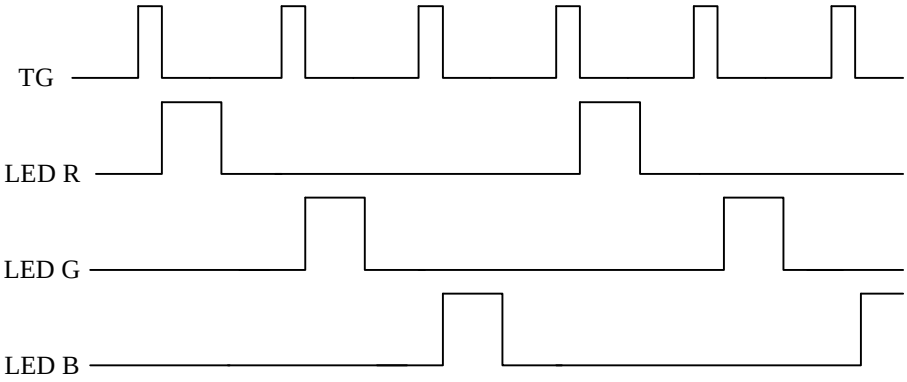
T_R , T_G and T_B are the exposure times for three channels.



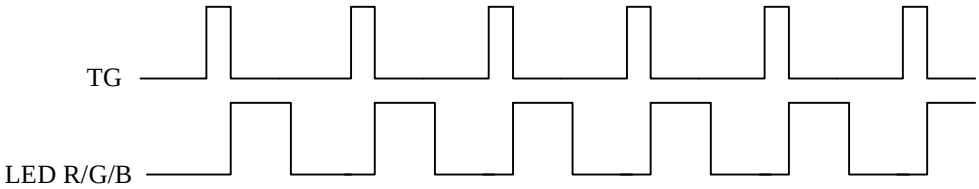
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B. CIS Type

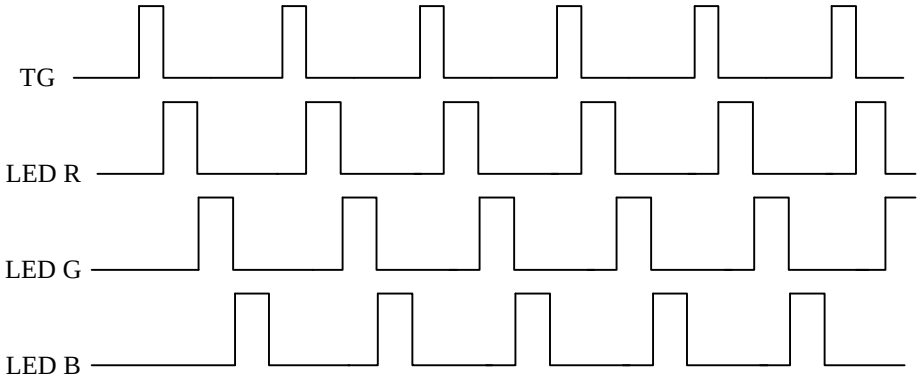
a. Color scan:



b. Gray scan:



c. True gray scan:



6 Image Sensor Timing

Image sensor timings can be programmed by S/W.

A. For CCD: Support 600, 1200, 2400, 3200, 3600 ,4800dpi ~ 9600dpi CCD such as NEC, TOSHIBA, Sony ……etc.

B. For CIS: Support 600, 1200, 2400, 3200, 3600,4800dpi ~ 9600dp CIS such as TOSHIBA, Canon ……etc.

7 Dummy Line

GL843 supports programmable dummy lines to resolve (overcome) start/stop problem.
Designers can insert dummy lines to reduce scanner start/stop events (buffer full).

A. Line base of dummy lines:

The range of dummy lines is 0~30 lines.

B. Adjustable dummy line:

The range is from the minimum shift time of CCD/CIS up to 2096K pixel time, with 1 pixel time resolution.

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8 Support Analog Front End Timing

GL843 supports external 16 bits front-end.
Wolfson: WM8192, WM8199, …etc.
Analog device: AD9826, …etc.

9 Image Type

A. Supports color, gray and line art scanning.
B. Supports color filters options (R, G or B channels) in gray or line art scanning.
C. Supports true gray with programmable R, G and B weightings.

10 Bits Depth

16*3 bits color, 16 bits gray level and 1 bit line art (Black & White).
Image data type: 16 bits, 8 bits and 1 bit.

11 Shading & Correction

a. White Shading & Dark Shading:

White shading and dark shading are pixel-by-pixel corrections with 16-bit solution and can be enabled or disabled by S/W. The white shading curve is calculated by S/W.

Data arrangement: three line in mode: dark R1, white R1, dark G1, white G1, dark B1, white B1,
dark R2, white R2, dark G2, white G2, dark B2, white B2,
dark R3, white R3, dark G3, white G3, dark B3, white B3,
one line in mode: dark R1, white R1, dark R2, white R2, dark R3, white R3…
dark G1, white G1, dark G2, white G2, dark G3, white G3…
dark B1, white B1, dark B2, white B2, dark B3, white B3…

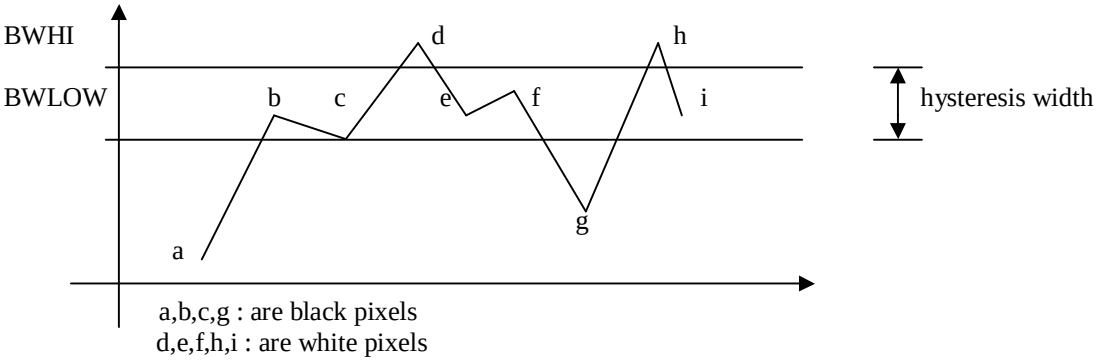
White shading formula: 2000H * Target / (Wn-Dn) = White Gain data ----- for 8 times system
White shading formula: 4000H * Target / (Wn-Dn) = White Gain data ----- for 4 times system
For example: Target = 3FFFH, Wn = 2FFFH, Dn = 0040H and 8 times system operation
then White Gain = 2000H * 3FFFH / (2FFFH-0040H) = 2AE4H (1.34033 times)

b. Gamma Correction:

16-bit GAMMA correction table is programmed by S/W.
Range: 0 ~ 64k (16 bits) input mapping to 0 ~ 255 (8 bits) output.
Style: increment or decrement gamma curve
Note: 16 bits image data will be mapped to 8 bits data by gamma table. Designer can get 16 bit image data by disabling gamma table.

12 Threshold Setting for Line-Art

Threshold can be programmed by S/W.
Range: 0 ~ 255 adjustable.
The threshold with hysteresis characteristic is for reducing image noise.



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13 Exposure Time

Maximum: 2096k pixels time
Adjustment step: 1 pixel time.
For transparency scanning, the exposure time can be up to 2096k pixels time.

14 Scan Width control for Horizontal Line

a. Supports start and end pixels assignment in setting scan width.

b. Scanning width= end pixels - start pixels
Maximum length: 128K pixels.
Minimum length: 1 pixel.

15 Support built-in USB 2.0 Controller

2-in-1 USB2.0 controller + scanner controller.

16 SDRAM Timing

Supports 16M Bits (1M*16), 64M Bits (4M*16), 128M Bits (8M*16), 256M Bits (16M*16) and 512 M Bits (32M*16) SDRAM as image buffer and calibration buffer.

17 Horizontal Resolution Adjustable for DPI Function

A. Digital deletion type:
Software adjustable resolutions range from 9600 to 1 dpi with 1 dpi decrement.

B. Digital average type:

Supports 1/2, 1/3, 1/4, 1/5, 1/6, 1/8, 1/10, 1/12, 1/15 digital average function.
For example, options for 1200dpi scanner are:

1200dpi, 600dpi, 400dpi, 300dpi, 240dpi, 200dpi, 150dpi,120dpi, 100dpi, 80dpi by average function.

C. Support stagger CCD:

Supports 1/2, 1/4, 1/8 resolutions, such as NEC Toshiba and Sony stagger CCD.

18 Vertical Resolution Adjustable for DPI Function

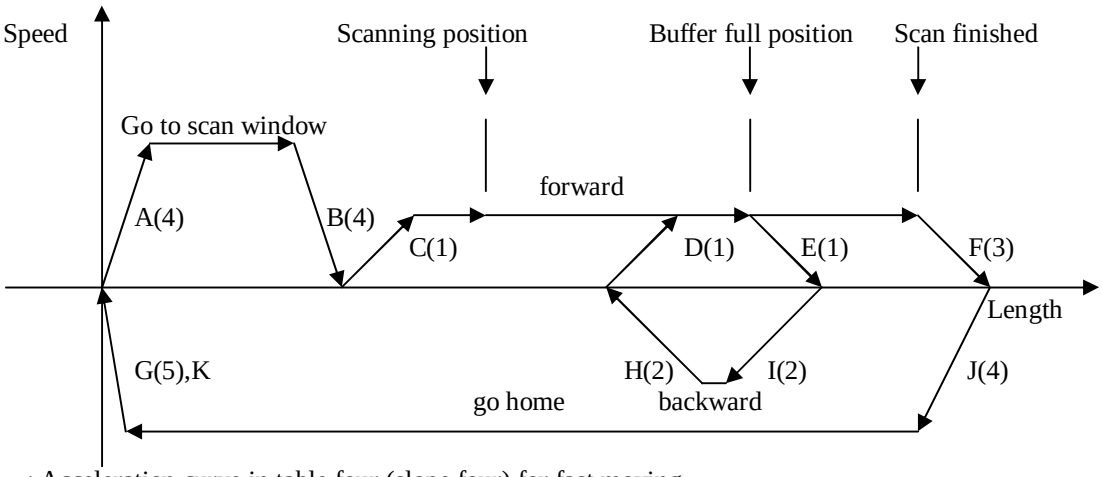
The resolution of motor moving is 16 bits wide and is flexibly controlled by motor tables.
The resolution can be up to 4800 dpi for 1200 dpi scanners, 9600 dpi for 2400 dpi scanners and 19200 dpi for 4800 dpi scanners.
Note: The resolution of vertical direction of quarter step can up to four times resolution.

19 Five Acceleration/Deceleration Tables

The acceleration/deceleration tables are stored in internal SRAM and can be downloaded by S/W.
And the resolution is 16 bits in pixel-time. The number of table steps is from 1 to 1020 steps for arbitrary curves. There are five tables for motor moving. Three tables are for scanning and the others are for fast moving. The forward and backward steps can be programmed by S/W separately.
Note: “Fast move” means move back to home position or move forward to scan window in any position.

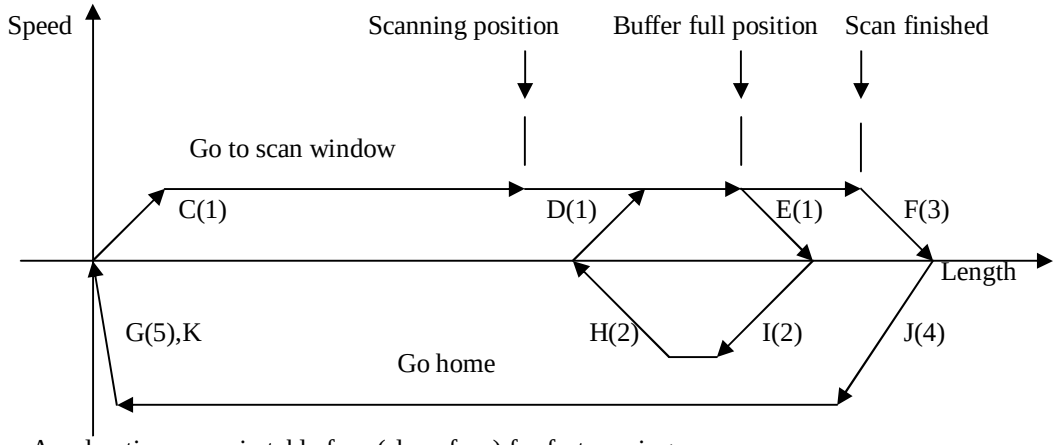
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(1) Two tables type:



A,J : Acceleration curve in table four (slope four) for fast moving.
B : Deceleration curve in table four (slope four) for fast moving.
C,D : Acceleration curve in table one (slope one) for scanning.
E : Deceleration curve in table one (slope one) for scanning.
F : Deceleration curve in table three (slope three) for scanning finished to protect wall hitting.
I : Acceleration curve in table two (slope two) for back-track when image buffer full.
H : Deceleration curve in table two (slope two) for back-track when image buffer full.
G : Deceleration curve in table five (slope five) for go-home to protect wall hitting.
K : Touch home sensor deceleration curve for go-home.

(2) One tables type:



J : Acceleration curve in table four (slope four) for fast moving.
C,D : Acceleration curve in table one (slope one) for forward scanning.
E : Deceleration curve in table one (slope one) for scanning.
F : Deceleration curve in table three (slope three) for scanning finished to protect wall hitting.
I : Acceleration curve in table two (slope two) for back-track when image buffer full.
H : Deceleration curve in table two (slope two) for back-track when image buffer full.
G : Deceleration curve in table five (slope five) for go-home to protect wall hitting.
K : Touch home sensor deceleration curve for go-home.

20 Trigger Position Control

Designers can select to move motor first then capture image; or capture image first then move motor.

21 Stepping Motor Phase Control

There are 8 output control pins to control stepping motors:

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MTR_PH 0~7 for bipolar motors MTR_PH 0~3 for unipolar motors

A. Bipolar motors:

a. Supports 2916 motor driver timing and 2916 compatible driver IC, such as L6219.
Include full, half and quarter steps control.

b. Supports 3955 motor driver timing.
Include full, half, quarter and eighth steps control.

c. Supports 3967 motor driver timing.
Include full, half, quarter and eighth steps control.

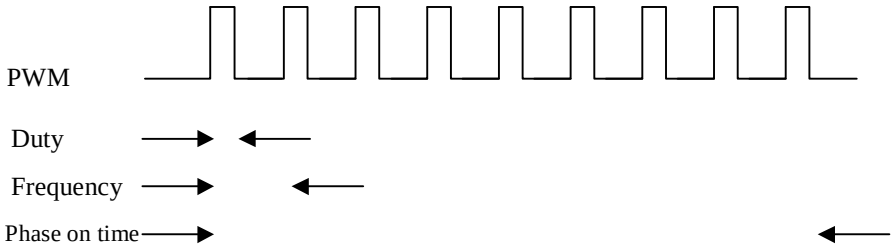
d. Supports LB1939, 1940 motor driver timing.
Include full and half steps control

B. Unipolar motors:

a. Supports 2003 motor driver timing and 2003 compatible driver IC.

b. Include full step two phases on, full step single phase on and half step.

c. PWM control, include frequency and duty controls.



22 Watchdog Protection

This function can automatically reset the system to initial state when the system is hanged (no access signal) beyond the time limit. It can be enabled or disabled by S/W.
This function can protect motor power, lamp power and ASIC system.
Calculation formula: (30sec.) * (times setting) * (setting number.).

The range of setting number is from 1 to 15; the range of times setting is 0 or 1.

23 Lamp Time-out Control

This circuitry can automatically turn off the lamp power when this function is enabled. It can be enabled or disabled by S/W.
Calculation formula: (60sec.) * (times setting) * (setting number).
The range of setting number is from 1 to 7;the range of times setting is 0 to 3.

24 Lamp Power Control

These are two power control ports for lamp. One is for Flatbed and the other is for XPA (Transparency or film). These control ports have PWM function. According to the system clock, designers can flexibly adjust their frequency and duty by S/W. And the resolution of PWM is 16 bits.

25 Sensors

The system supports home sensor for flatbed; ADF sensor, document sensor and cover sensor for ADF module.

26 GPIO Ports

Designers can separately assign input or output direction for each GPIO pin of GPIO1~20 and GPIO27. Some GPIO can be designed for keypads, document sensor of sheetfed or motor power control…etc.
Designers can assign GPIO27 as general-purpose input/output port or as ADF sensor input.
Note : There are two pins for special function. One is GPIO12 and the other is GPIO11.

GPIO12: 1. Pull up by resistor to indicate ASIC to turn on lamp power in power-on initial state.
2. Pull down by resistor to indicate ASIC to turn off lamp power in power-on initial state..

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3. This pin can control bipolar motor driver IC (2916,6219,3955 or 3967) Vref for controlling Imax current.

GPIO11: This pin can control bipolar motor driver IC (2916,6219,3955 or 3967) Vref for control Imax current.

27 GPO28~33 Ports

GL843 provides 6 ports for general-purpose output. They exist in both 128 and 208 pins packages.

28 Power on Check

The default status of the PWRBIT control bit is reset. Programmers can set the PWRBIT control bit before controlling the ASIC. GL843 will keep the status until power is turn off. This operation is to check if the power had been turned off or not.

29 Extended GPIO

GPIO21~26 is only available in 208 pins QFP package.

30 LED Blinking

GL843 supports LED -blinking function. It is implemented in GPIO15~16 pins and GPIO21~26.

31 Support Back Scanning

GL843 supports forward or backward scanning.

32 Support LCD Interface

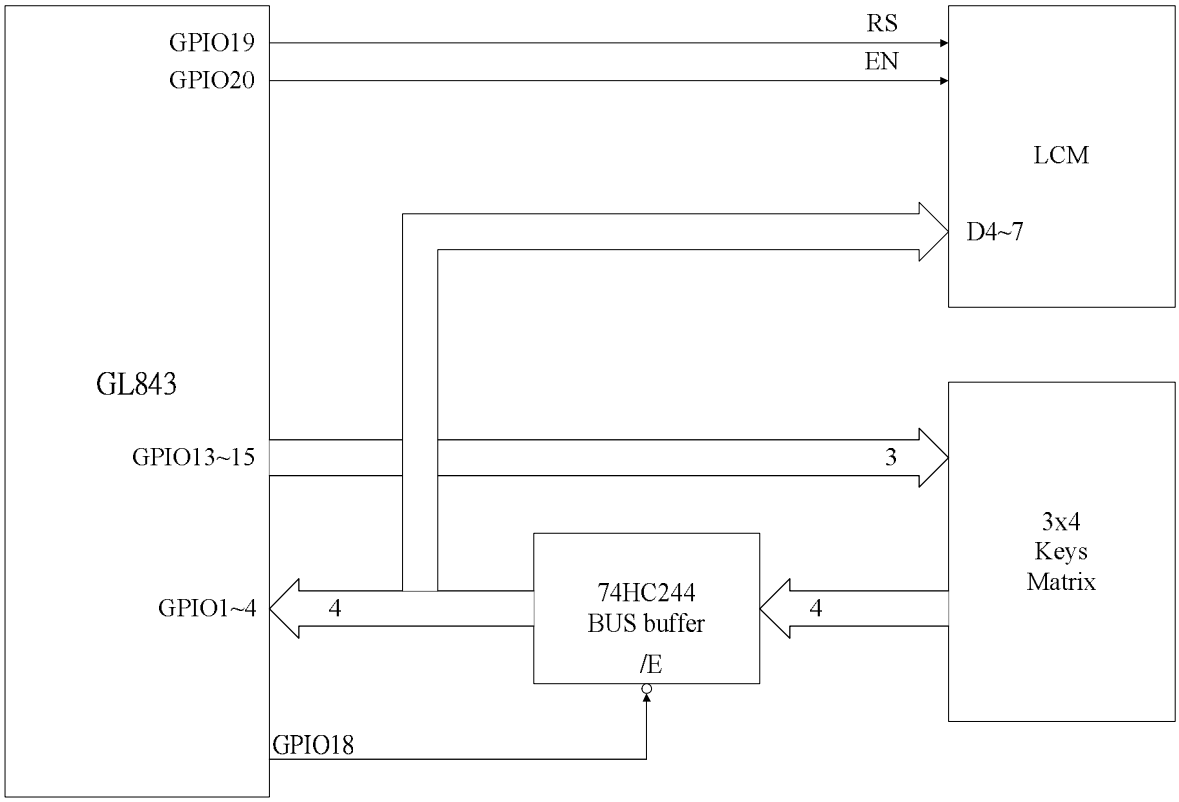
GL843 supports LCD display interface via internal logic circuitry. Programmers need to set the LCDSEL control bit to logic '1'.

33 Support LCM Interface

GL843 supports LCM display interface via internal logic circuitry. Programmers need to set the LCMSEL control bit to logic '1'. GPIO19 controls RS of LCM. GPIO20 controls EN of LCM.
GPIO1~4 control the data bus of LCM and share the input of keys matrix. GPIO18 controls the /E of external 74HC244.
The 74HC244 is a bus buffer to share keys matrix and LCM data bus.

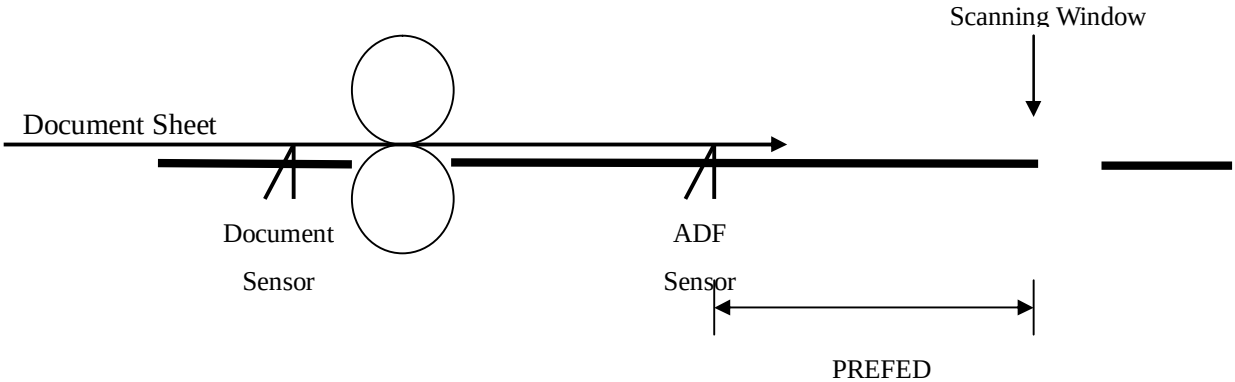
Following is the application of keys matrix & LCM display.

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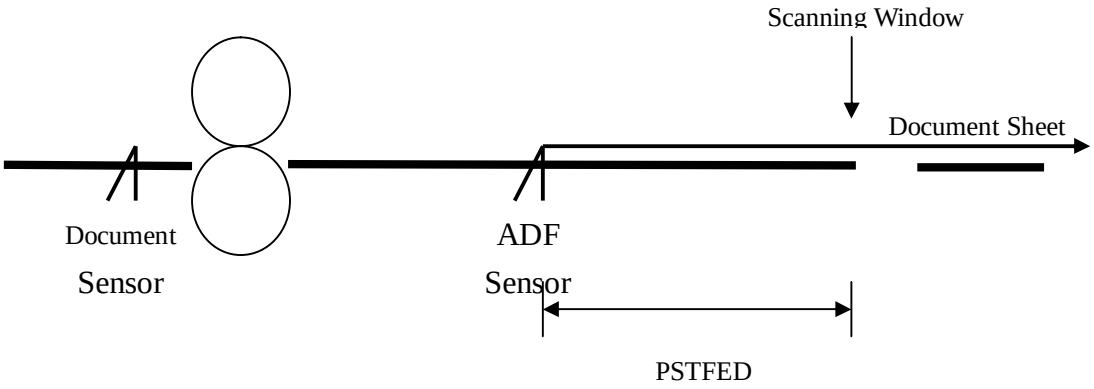
34 Supports ADF Function

GL843 supports ADF (Auto-document-feeder) function via internal logic circuitry. Programmers need to set the ADFSEL control bit to logic '1'. GPIO6 controls the motor pulse trigger if the motor moving of ADF module is implemented by trigger pulse, otherwise the motor moving is driven by motor phases. GPO28 controls the moving direction of motor if ADF module is necessary. GPIO16 is the cover sensor input, GPIO27 is the ADF sensor input and HOME is document sensor input under ADF mode.



GL843 can feed document sheets automatically to scanning window. After sensing the present of document by document sensor, software should issue feed command to GL843 for paper feeding. After document sheet reaches ADF sensor, scanning process will be started after PREFED motor steps.

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When document sheet keeps moving forward, after sensing the absent of document by ADF sensor, scanning process will be terminated after PSTFED scanning lines.

35 Supports RS232 Interface

GL843 supports RS232 interface via internal logic circuitry. Programmers need to set the RS232SEL control bit to logic '1'. GPIO6 transmits the data of RS232 and GPIO28 receives the data of RS232 under RS232 mode. The baud rate can be programmed to 2400,4800, 9600 and 19200 bps by S/W.

36 Supports EEPROM (93C46) Interface

GL843 supports EEPROM interface via internal logic circuitry. Programmers need to set the EPROMSEL control bit to logic '1'. GPIO1 controls SK of external EEPROM, GPIO2 controls DI/DO of EEPROM and GPIO17 controls CS of external EEPROM under EEPROM mode.

37 Embedded RISC CPU for Scanning, Run-in and Diagnostic Tests

GL843 embeds a powerful RISC CPU. It has timers, counters and interrupt ports. Designers can use the embedded CPU to do the run-in, diagnostic tests and anything he wants to do.

38 Supports External 24Kbytes flash ROM or Internal 24Kbyte mask ROM

Designers can use 24K bytes embedded mask ROM or external flash ROM. Firmware can be downloaded to flash ROM directly by PC S/W. It provides a flexible development environment to design the firmware.

39 Supports Key-Matrix with Latch Function

Designers need to set MATRIXEN control bit to logic '1' to enable key-matrix function. GPIO13~15 are the scanning output of key-matrix and GPIO1~4 are the scanning input of key-matrix. Designers can select 1*4, 2*4 or 3*4 matrix for different applications.
By resetting MATRIXEN to logic '0', designers can directly use GPIO1~4 as four hot keys inputs.
Any hot key status is latched into key buffer until it is read out.

40 "True gray" with R,G and B weightings

Designers can obtain the "true gray" image data by enabling "true gray" function. Image data is generated by R,G and B outputs and multiplied by weightings.
Formula of true gray value = R*(TRUER [7:0]) + G*(TRUEG [7:0]) + B*(TRUEB [7:0])

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41 Lossless Data Compression

GL843 use Huffman coding method to implement the lossless data compression.

42 Lines Packing for Stagger CCD or R/G/B Line Differences

GL843 packs R, G and B lines together for CCD sensors by hardware. And it also packs the same color lines of stagger CCD together.

43 Fine CDS Sampling Adjustment

Designers can fine-tune the CDS sampling position to avoid the digital noise influence (8.33ns adjustment). The image noise may come from the digital noise of PCB.

44 Wall-Hitting Protection

Designers can use table five of motor moving to protect the wall hitting. The LONGCURV control bit has to be set to logic '1' to enable the long-curve function. The first several steps are used to decelerate the carriage moving; the other slower steps are focused on touching the home sensor.
Due to the special table five, designers can replace the photo-sensor by simple, cheaper mechanical-type sensors.

45 Motor Driver IC Setting

Designers add pull up/pull down resistors on MTR_SEL1~3 will indicate ASIC to generate the timing of specified motor driver IC. Please refer to section 5.2.
MTR_SEL1 share in CCD_CH4X pin.
MTR_SEL2 share in CCD_TGG pin.
MTR_SEL3 share in CCD_TGB pin.

46 Operation Mode Setting

Designers add pull down resistors on TSTSEL1~2 will indicate ASIC to work on normal mode.Please refer to section 5.2.
TSTSEL1 share in CCD_CK2X pin.
TSTSEL2 share in CCD_RSX.

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CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings (Voltage Referenced to GND)

Table 7.1 - Absolute Maximum Ratings (Voltage Referenced to GND)

Symbol	Description	Min	Max
DVCC0 DVCC1 AVDD AVCC1 VccCore1~4	DC supply voltage	-0.5V	+3.6V
VccIO1~6	DC supply voltage	-0.5V	+3.6V or +5.5V
V_I	DC input voltage	-0.5V	VCC+0.5V
$V_{I/O}$	DC input voltage range for I/O	-0.5V	VCC+0.5V
$V_{AI/O}$	DC input voltage for USB D+/D- pins	-0.5V	VCC+0.5V
$V_{I/OZ}$	DC voltage applied to outputs in High Z state	-0.5V	VCC+0.5V
T_{STQ}	Storage temperature range	-60˚C	+150˚C
T_{amb}	Operating ambient temperature	0˚C	70˚C

Note: VCC: VccCore, VccIO, DVCC, AVDD or AVCC1

7.2 DC Characteristics (Digital Pins): 3.3 V Logic Core or Pads

Table 7.2 - DC Characteristics (Digital Pins): 3.3 V Logic Core or Pads

SYMBOL	Description	Min	Typ.	Max	Unit
P_D	Power Dissipation				mA
DVCC0 DVCC1 AVDD AVCC1 VccCore1~4	Power Supply Voltage	3.1	3.3	3.6	V
VccIO1~6	Power Supply Voltage 3.3V	3	3.3	3.6	V
I_O	DC output sink current excluding D+/D-/VCC/GND	16 or 8			mA
V_{IL}	LOW level input voltage			0.9	V
V_{IH}	HIGH level input voltage	2.0			V
V_{TLH}	LOW to HIGH threshold voltage	1.3	1.43	1.56	V
V_{THL}	HIGH to LOW threshold voltage	1.3	1.43	1.56	V
V_{HYS}	Hysteresis voltage	-	0	-	V
V_{OL}	LOW level output voltage when I_{OL}=16mA			0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=16mA	2.4			V
I_{OLK}	Leakage current for pads with internal pull up or pull down resistor			46	µA
R_{DN}	Pad internal pulldown resister	72.8K	105.7K	167.4K	Ω
R_{UP}	Pad internal pullup resister	135.9K	167.8K	212.4K	Ω

Note: hbd16dhk is internal pulled down; hbd16uhk is internal pulled up; hbd16* is 16mA; hbd8* is for 8mA

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7.3 DC Characteristics (Digital Pins): 5.0 V Pads

Table 7.3 - DC Characteristics (Digital Pins): 5.0 V Pads

SYMBOL	Description	Min	Typ.	Max	Unit
P_D	Power Dissipation				mA
VccIO1~6	Power Supply Voltage 5.0V	4.5	5.0	5.5	V
I_O	DC output sink current excluding D+/D-/VCC/GND	16			mA
V_{IL}	LOW level input voltage			0.9	V
V_{IH}	HIGH level input voltage	2.4			V
V_{TLH}	LOW to HIGH threshold voltage				V
V_{THL}	HIGH to LOW threshold voltage				V
V_{OL}	LOW level output voltage when I_{OL}=8mA			0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=8mA	2.4			V
I_{OLK}	Leakage current for pads with internal pull up or pull down resistor			46	µA
R_{DN}	Pad internal pulldown resister	104.6K	159.5K	206.6K	Ω
R_{UP}	Pad internal pullup resister	81.9K	103.2K	254.6K	Ω

7.4 DC Characteristics (D+/D-)

Table 7.4 - DC Characteristics (D+/D-)

SYMBOL	Description	Min	Typ.	Max	Unit
V_{OL}	D+/D- static output LOW(R_L of 1.5K to 3.6V)			0.3	V
V_{OH}	D+/D- static output HIGH (R_L of 15K to GND)	2.8		3.6	V
V_{DI}	Differential input sensitivity	0.2			V
V_{CM}	Differential common mode range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold	0.2			V
C_{IN}	Transceiver capacitance			20	pF
I_{LO}	Hi-Z state data line leakage	-10		+10	µA
Z_{DRV}	Driver output resistance	28		43	Ω

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CHAPTER 8 PACKAGE DIMENSION

QFP-128L (14*20 mm, F/P: 3.2 mm):

SYMBOLS	MIN(mm)	NOM(mm)	MAX(mm)
A1	0.25	0.35	0.45
A2	2.57	2.72	2.87
b	0.10	0.20	0.30
C	0.10	0.15	0.20
D	13.90	14.00	14.10
E	19.90	20.00	20.10
e	-	0.50	-
Hd	17.00	17.20	17.40
He	23.00	23.20	23.40
L	0.65	0.80	0.95
L1	-	1.60	-
Y	-	-	0.08
Θ	0	-	12

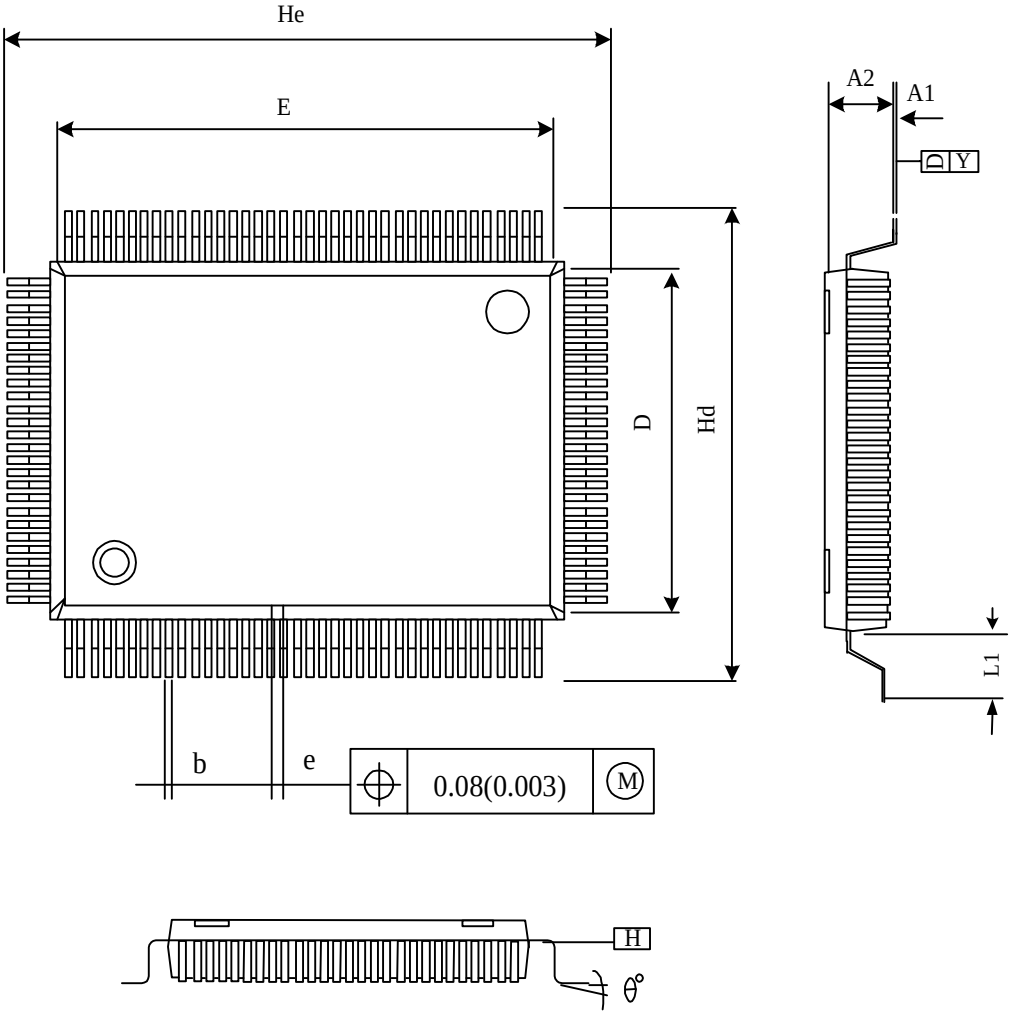
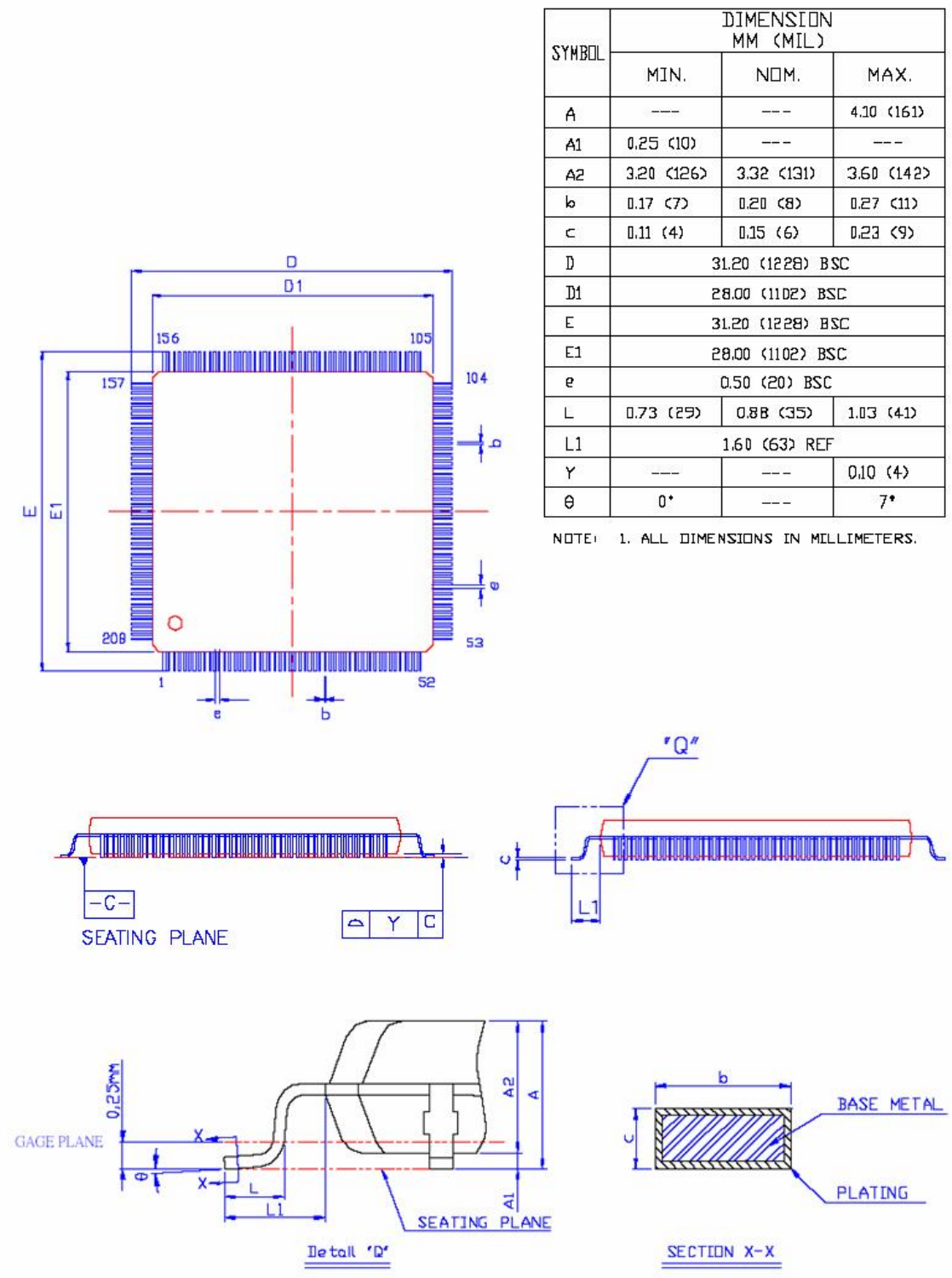


Figure 8.1 - GL843 128 Pin QFP Package

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SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	4.10 (161)
A1	0.25 (10)	---	---
A2	3.20 (126)	3.32 (131)	3.60 (142)
b	0.17 (7)	0.20 (8)	0.27 (11)
c	0.11 (4)	0.15 (6)	0.23 (9)
D	31.20 (1228) BSC		
D1	28.00 (1102) BSC		
E	31.20 (1228) BSC		
E1	28.00 (1102) BSC		
e	0.50 (20) BSC		
L	0.73 (29)	0.88 (35)	1.03 (41)
L1	1.60 (63) REF		
Y	---	---	0.10 (4)
θ	0°	---	7°

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.

Figure 8.2- GL843 208 Pin QFP Package

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