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# OKI Semiconductor

# MSC2323258D-xxBS4/DS4

**2,097,152-word x 32-bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE WITH EDO**

## DESCRIPTION

The MSC2323258D-xxBS4/DS4 is a fully decoded, 2,097,152-word x 32-bit CMOS dynamic random access memory module composed of four 16Mb DRAMs in SOJ packages mounted with eight decoupling capacitors on a 72-pin glass epoxy single-inline package. This module supports any application where high density and large capacity of storage memory are required.

## FEATURES

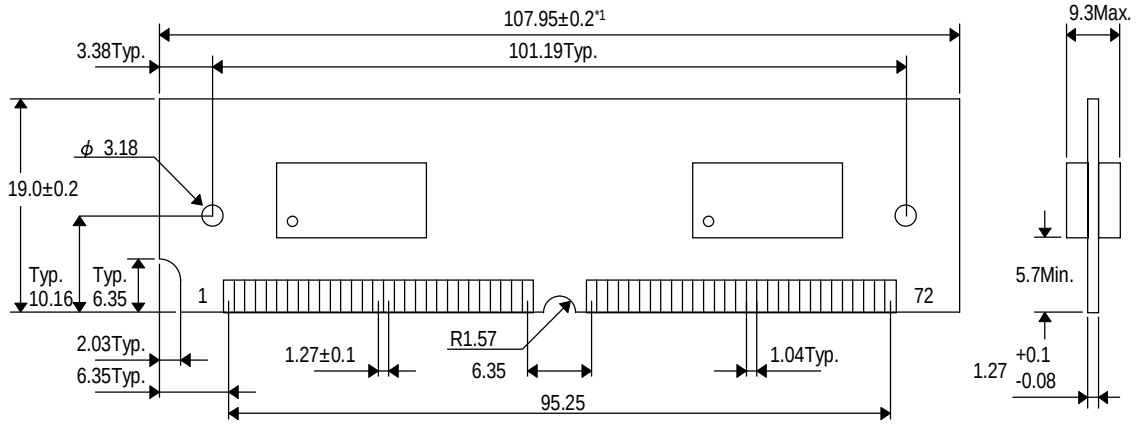
· 2,097,152-word x 32-bit organization
· 72-pin Single Inline Memory Module
  MSC2323258D-xxBS4 : Gold tab
  MSC2323258D-xxDS4 : Solder tab
· Single +5V supply ± 10% tolerance
· Input : TTL compatible
· Output : TTL compatible, 3-state
· Refresh : 1024cycles/16ms
· /CAS before /RAS refresh, hidden refresh, /RAS only refresh capability
· Fast page mode with EDO capability

## PRODUCT FAMILY

| Family | Access Time (Max.) | | | Cycle Time (Min.) | Power Dissipation | |
|---|---|---|---|---|---|---|
| | $t_{RAC}$ | $t_{AA}$ | $t_{CAC}$ | | Operating (Max.) | Standby (Max.) |
| MSC2323258D-60BS4/DS4 | 60ns | 30ns | 15ns | 104ns | 1430mW | 22mW |
| MSC2323258D-70BS4/DS4 | 70ns | 35ns | 20ns | 124ns | 1320mW | |

## MODULE OUTLINE

MSC2323258D-xxBS4/DS4 (Unit : mm)




*1 The common size difference of the board width 12.5mm of its height is specified as ±0.2.
The value above 12.5mm is specified as ±0.5.

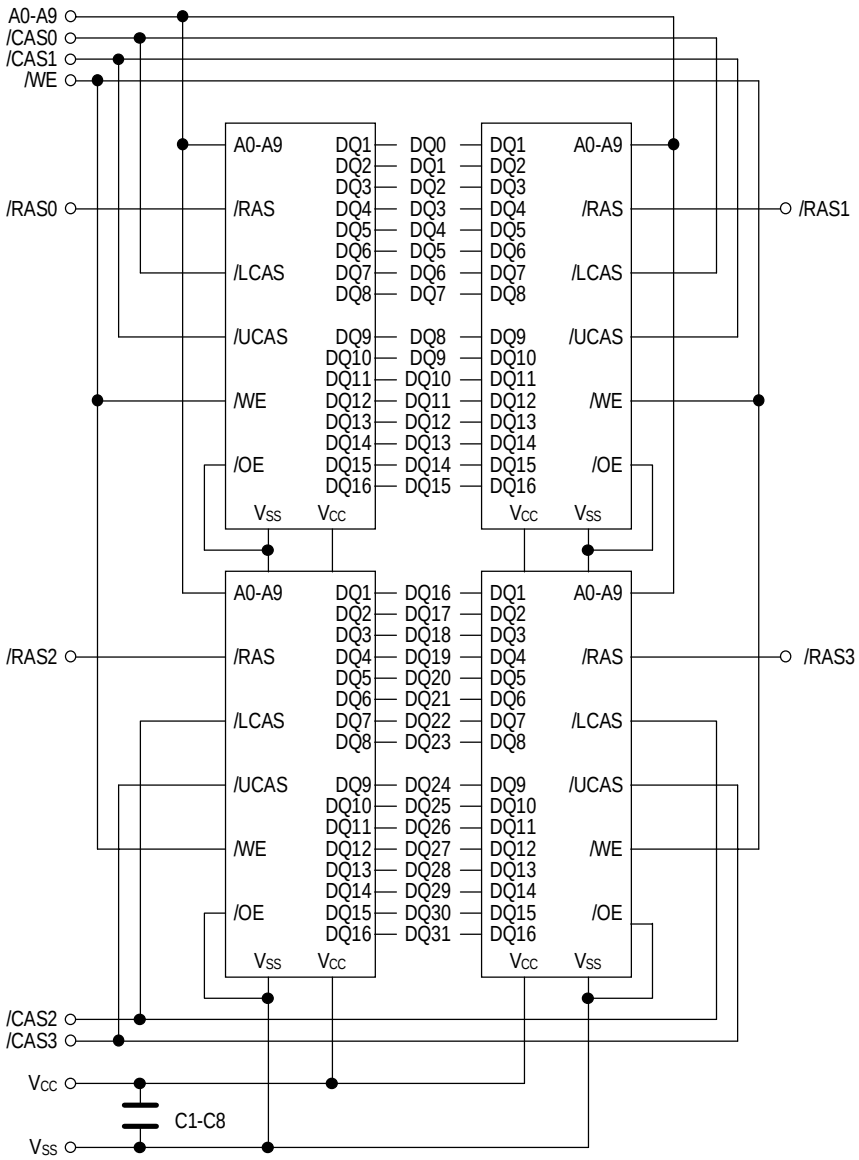
## PIN CONFIGURATION

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 19 | NC | 37 | NC | 55 | DQ11 |
| 2 | DQ0 | 20 | DQ4 | 38 | NC | 56 | DQ27 |
| 3 | DQ16 | 21 | DQ20 | 39 | $V_{SS}$ | 57 | DQ12 |
| 4 | DQ1 | 22 | DQ5 | 40 | /CAS0 | 58 | DQ28 |
| 5 | DQ17 | 23 | DQ21 | 41 | /CAS2 | 59 | $V_{CC}$ |
| 6 | DQ2 | 24 | DQ6 | 42 | /CAS3 | 60 | DQ29 |
| 7 | DQ18 | 25 | DQ22 | 43 | /CAS1 | 61 | DQ13 |
| 8 | DQ3 | 26 | DQ7 | 44 | /RAS0 | 62 | DQ30 |
| 9 | DQ19 | 27 | DQ23 | 45 | /RAS1 | 63 | DQ14 |
| 10 | $V_{CC}$ | 28 | A7 | 46 | NC | 64 | DQ31 |
| 11 | NC | 29 | NC | 47 | /WE | 65 | DQ15 |
| 12 | A0 | 30 | $V_{CC}$ | 48 | NC | 66 | NC |
| 13 | A1 | 31 | A8 | 49 | DQ8 | 67 | PD1 |
| 14 | A2 | 32 | A9 | 50 | DQ24 | 68 | PD2 |
| 15 | A3 | 33 | /RAS3 | 51 | DQ9 | 69 | PD3 |
| 16 | A4 | 34 | /RAS2 | 52 | DQ25 | 70 | PD4 |
| 17 | A5 | 35 | NC | 53 | DQ10 | 71 | NC |
| 18 | A6 | 36 | NC | 54 | DQ26 | 72 | $V_{SS}$ |

### Presence Detect Pins

| Pin No. | Pin Name | MSC2323258D -60BS4/DS4 | MSC2323258D -70BS4/DS4 |
|---|---|---|---|
| 67 | PD1 | NC | NC |
| 68 | PD2 | NC | NC |
| 69 | PD3 | NC | $V_{SS}$ |
| 70 | PD4 | NC | NC |

## BLOCK DIAGRAM



## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Voltage on Any Pin Relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -1.0 to +7.0 | V |
| Voltage on $V_{CC}$ Supply Relative to $V_{SS}$ | $V_{CC}$ | -1.0 to +7.0 | V |
| Short Circuit Output Current | $I_{OS}$ | 50 | mA |
| Power Dissipation | $P_D$ * | 4 | W |
| Operating Temperature | $T_{OPR}$ | 0 to +70 | °C |
| Storage Temperature | $T_{STG}$ | -40 to +125 | °C |

* Ta = 25°C

### Recommended Operating Conditions

( Ta = 0°C to +70°C )

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| | $V_{SS}$ | 0 | 0 | 0 | V |
| Input High Voltage | $V_{IH}$ | 2.4 | - | 6.5 | V |
| Input Low Voltage | $V_{IL}$ | -1.0 | - | 0.8 | V |

### Capacitance

( $V_{CC}$ = 5V ± 10%, Ta = 25°C, f = 1 MHz )

| Parameter | Symbol | Typ. | Max. | Unit |
|---|---|---|---|---|
| Input Capacitance (A0 - A9) | $C_{IN1}$ | - | 32 | pF |
| Input Capacitance (/WE) | $C_{IN2}$ | - | 35 | pF |
| Input Capacitance (/RAS0- /RAS3) | $C_{IN3}$ | - | 13 | pF |
| Input Capacitance (/CAS0- /CAS3) | $C_{IN4}$ | - | 20 | pF |
| I/O Capacitance (DQ0 - DQ31) | $C_{DQ}$ | - | 25 | pF |

Note: Capacitance measured with Boonton Meter.

## DC Characteristics

($V_{CC}$ = 5V ± 10%, Ta = 0°C to +70°C )

| Parameter | Symbol | Condition | MSC2323258D -60BS4/DS4 | | MSC2323258D -70BS4/DS4 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | | |
| Input Leakage Current | $I_{LI}$ | 0V ≤ $V_{IN}$ ≤ 6.5V; All other pins not under test = 0V | -40 | 40 | -40 | 40 | µA | |
| Output Leakage Current | $I_{LO}$ | DQ disable 0V ≤ $V_{OUT}$ ≤ 5.5V | -20 | 20 | -20 | 20 | µA | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -5.0mA | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 4.2mA | 0 | 0.4 | 0 | 0.4 | V | |
| Average Power Supply Current (Operating) | $I_{CC1}$ | /RAS, /CAS cycling, $t_{RC}$ = Min. | - | 260 | - | 240 | mA | 1, 2 |
| Power supply current (Standby) | $I_{CC2}$ | /RAS, /CAS = $V_{IH}$ | - | 8 | - | 8 | mA | 1 |
| | | /RAS, /CAS ≥ $V_{CC}$ -0.2V | - | 4 | - | 4 | mA | 1 |
| Average Power Supply Current (/RAS only refresh) | $I_{CC3}$ | /RAS cycling, /CAS = $V_{IH}$, $t_{RC}$ = Min. | - | 260 | - | 240 | mA | 1, 2 |
| Average Power Supply Current (/CAS before /RAS refresh) | $I_{CC6}$ | /RAS cycling, /CAS before /RAS | - | 260 | - | 240 | mA | 1, 2 |
| Average Power Supply Current (Fast Page Mode) | $I_{CC7}$ | /RAS = $V_{IL}$, /CAS cycling, $t_{HPC}$ = Min. | - | 260 | - | 240 | mA | 1, 3 |

Notes: 1. $I_{CC}$ Max. is specified as $I_{CC}$ for output open condition.
2. Address can be changed once or less while /RAS = $V_{IL}$.
3. Address can be changed once or less while /CAS = $V_{IH}$.

## AC Characteristics (1/2)

($V_{CC}$ = 5V ± 10%, Ta = 0°C to +70°C ) Note: 1, 2, 3

| Parameter | Symbol | MSC2323258D -60BS4/DS4 | | MSC2323258D -70BS4/DS4 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| Random Read or Write Cycle Time | $t_{RC}$ | 104 | - | 124 | - | ns | |
| Fast Page Mode Cycle Time | $t_{HPC}$ | 25 | - | 30 | - | ns | |
| Access Time from /RAS | $t_{RAC}$ | - | 60 | - | 70 | ns | 4, 5, 6 |
| Access Time from /CAS | $t_{CAC}$ | - | 15 | - | 20 | ns | 4, 5 |
| Access Time from Column Address | $t_{AA}$ | - | 30 | - | 35 | ns | 4, 6 |
| Access Time from /CAS Precharge | $t_{CPA}$ | - | 35 | - | 40 | ns | 4 |
| Output Low Impedance Time from /CAS | $t_{CLZ}$ | 0 | - | 0 | - | ns | 4 |
| Data Output Hold After /CAS Low | $t_{DOH}$ | 5 | - | 5 | - | ns | |
| /CAS to Data Output Buffer Turn-off Delay Time | $t_{CEZ}$ | 0 | 15 | 0 | 20 | ns | 7, 8 |
| /RAS to Data Output Buffer Turn-off Delay Time | $t_{REZ}$ | 0 | 15 | 0 | 20 | ns | 7, 8 |
| /WE to Data Output Buffer Turn-off Delay Time | $t_{WEZ}$ | 0 | 15 | 0 | 20 | ns | 7 |
| Transition Time | $t_T$ | 1 | 50 | 1 | 50 | ns | 3 |
| Refresh Period | $t_{REF}$ | - | 16 | - | 16 | ms | |
| /RAS Precharge Time | $t_{RP}$ | 40 | - | 50 | - | ns | |
| /RAS Pulse Width | $t_{RAS}$ | 60 | 10K | 70 | 10K | ns | |
| /RAS Pulse Width (Fast Page Mode with EDO) | $t_{RASP}$ | 60 | 100K | 70 | 100K | ns | |
| /RAS Hold Time | $t_{RSH}$ | 10 | - | 13 | - | ns | |
| /CAS Precharge Time (Fast Page Mode with EDO) | $t_{CP}$ | 10 | - | 10 | - | ns | |
| /CAS Pulse Width | $t_{CAS}$ | 10 | 10K | 13 | 10K | ns | |
| /CAS Hold Time | $t_{CSH}$ | 40 | - | 45 | - | ns | |
| /CAS to /RAS Precharge Time | $t_{CRP}$ | 5 | - | 5 | - | ns | |
| /RAS Hold Time from /CAS Precharge | $t_{RHCP}$ | 35 | - | 40 | - | ns | |
| /RAS to /CAS Delay Time | $t_{RCD}$ | 14 | 45 | 14 | 50 | ns | 5 |
| /RAS to Column Address Delay Time | $t_{RAD}$ | 12 | 30 | 12 | 35 | ns | 6 |
| Row Address Set-up Time | $t_{ASR}$ | 0 | - | 0 | - | ns | |
| Row Address Hold Time | $t_{RAH}$ | 10 | - | 10 | - | ns | |
| Column Address Set-up Time | $t_{ASC}$ | 0 | - | 0 | - | ns | |
| Column Address Hold Time | $t_{CAH}$ | 10 | - | 13 | - | ns | |
| Column Address to /RAS Lead Time | $t_{RAL}$ | 30 | - | 35 | - | ns | |
| Read Command Set-up Time | $t_{RCS}$ | 0 | - | 0 | - | ns | |
| Read Command Hold Time | $t_{RCH}$ | 0 | - | 0 | - | ns | 9 |
| Read Command Hold Time referenced to /RAS | $t_{RRH}$ | 0 | - | 0 | - | ns | 9 |

## AC Characteristics (2/2)

($V_{CC}$ = 5V ± 10%, Ta = 0°C to +70°C ) Note: 1, 2, 3

| Parameter | Symbol | MSC2323258D -60BS4/DS4 | | MSC2323258D -70BS4/DS4 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| Write Command Set-up Time | $t_{WCS}$ | 0 | - | 0 | - | ns | |
| Write Command Hold Time | $t_{WCH}$ | 10 | - | 13 | - | ns | |
| Write Command Pulse Width | $t_{WP}$ | 10 | - | 10 | - | ns | |
| /WE Pulse Width (DQ Disable) | $t_{WPE}$ | 10 | - | 10 | - | ns | |
| Write Command to /RAS Lead Time | $t_{RWL}$ | 10 | - | 13 | - | ns | |
| Write Command to /CAS Lead Time | $t_{CWL}$ | 10 | - | 13 | - | ns | |
| Data-in Set-up Time | $t_{DS}$ | 0 | - | 0 | - | ns | |
| Data-in Hold Time | $t_{DH}$ | 10 | - | 13 | - | ns | |
| /CAS Active Delay Time from /RAS Precharge | $t_{RPC}$ | 5 | - | 5 | - | ns | |
| /RAS to /CAS Set-up Time (/CAS before /RAS) | $t_{CSR}$ | 5 | - | 5 | - | ns | |
| /RAS to /CAS Hold Time (/CAS before /RAS) | $t_{CHR}$ | 10 | - | 10 | - | ns | |

Notes: 1. A start-up delay of 200µs is required after power-up, followed by a minimum of eight initialization cycles (/RAS only refresh or /CAS before /RAS refresh) before proper device operation is achieved.

2. The AC characteristics assumes $t_T$ = 2ns.

3. $V_{IH}$(Min.) and $V_{IL}$(Max.) are reference levels for measuring input timing signals. Transition time ($t_T$) are measured between $V_{IH}$ and $V_{IL}$.

4. This parameter is measured with a load circuit equivalent to 2TTL loads and 100pF.

5. Operation within the $t_{RCD}$(Max.) limit ensures that $t_{RAC}$(Max.) can be met.
$t_{RCD}$(Max.) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$(Max.) limit, then the access time is controlled by $t_{CAC}$.

6. Operation within the $t_{RAD}$(Max.) limit ensures that $t_{RAC}$(Max.) can be met.
$t_{RAD}$(Max.) is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$(Max.) limit, then the access time is controlled by $t_{AA}$.

7. $t_{CEZ}$(Max.), $t_{REZ}$(Max.) and $t_{WEZ}$(Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

8. $t_{CEZ}$ and $t_{REZ}$ must be satisfied for open circuit condition.

9. $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.