TIBPAL22V10-5C
HIGH-PERFORMANCE *IMPACT-XL*™ PROGRAMMABLE ARRAY LOGIC CIRCUIT

- **High-Performance Operation:**
  f_{max} **(External Feedback) . . . 117 MHz**
  Propagation Delay . . . 5 ns Max

- **Increased Logic Power – Up to 22 Inputs and 10 Outputs**

- **Increased Product Terms – Average of 12 Per Output**

- **Variable Product Term Distribution Allows More Complex Functions to Be Implemented**

- **Each Output Is User Programmable for Registered or Combinational Operation, Polarity, and Output Enable Control**

- **Power-Up Clear on Registered Outputs**

- **TTL-Level Preload for Improved Testability**

- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**

- **Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses**

- **AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features**

- **JEDEC Approved Revolutionary Power and Ground Pinout for 28-Pin Chip Carrier Reduces Cross Talk and Ground Bounce**

- **JEDEC File Compatibility Allows Previous '22V10 Designs to be Programmed Into the TIBPAL22V10-5C Without Modifications**

FN PACKAGE
(TOP VIEW)
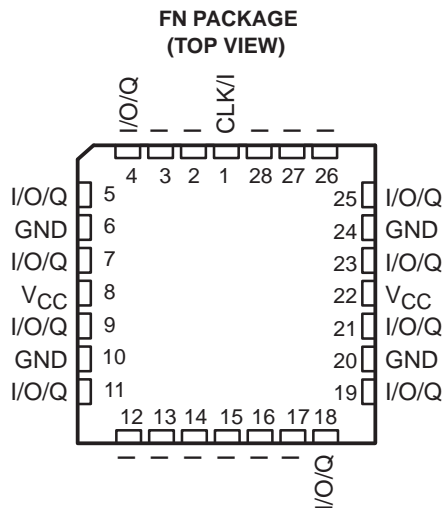
description

The TIBPAL22V10-5C is a programmable array logic device featuring high speed and functional equivalency when compared to presently available devices. The TIBPAL22V10-5C is implemented with the familiar sum-of-products (AND-OR) logic structure featuring programmable output logic macrocells. These IMPACT-XL™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic.

This device contains up to 22 inputs and 10 outputs. It incorporates the unique capability of defining and programming the architecture of each output on an individual basis. Outputs can be registered or nonregistered and inverting or noninverting as shown in the output logic macrocell diagram. The ten potential outputs are enabled through the use of individual product terms.

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

This device is covered by U.S. Patent 4,410,987.
IMPACT-XL is a trademark of Texas Instruments Incorporated.

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description (continued)

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22V10-5C offers quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins can be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power up with their outputs high. Registered outputs selected as active-high power up with their outputs low.

A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will verify as open.

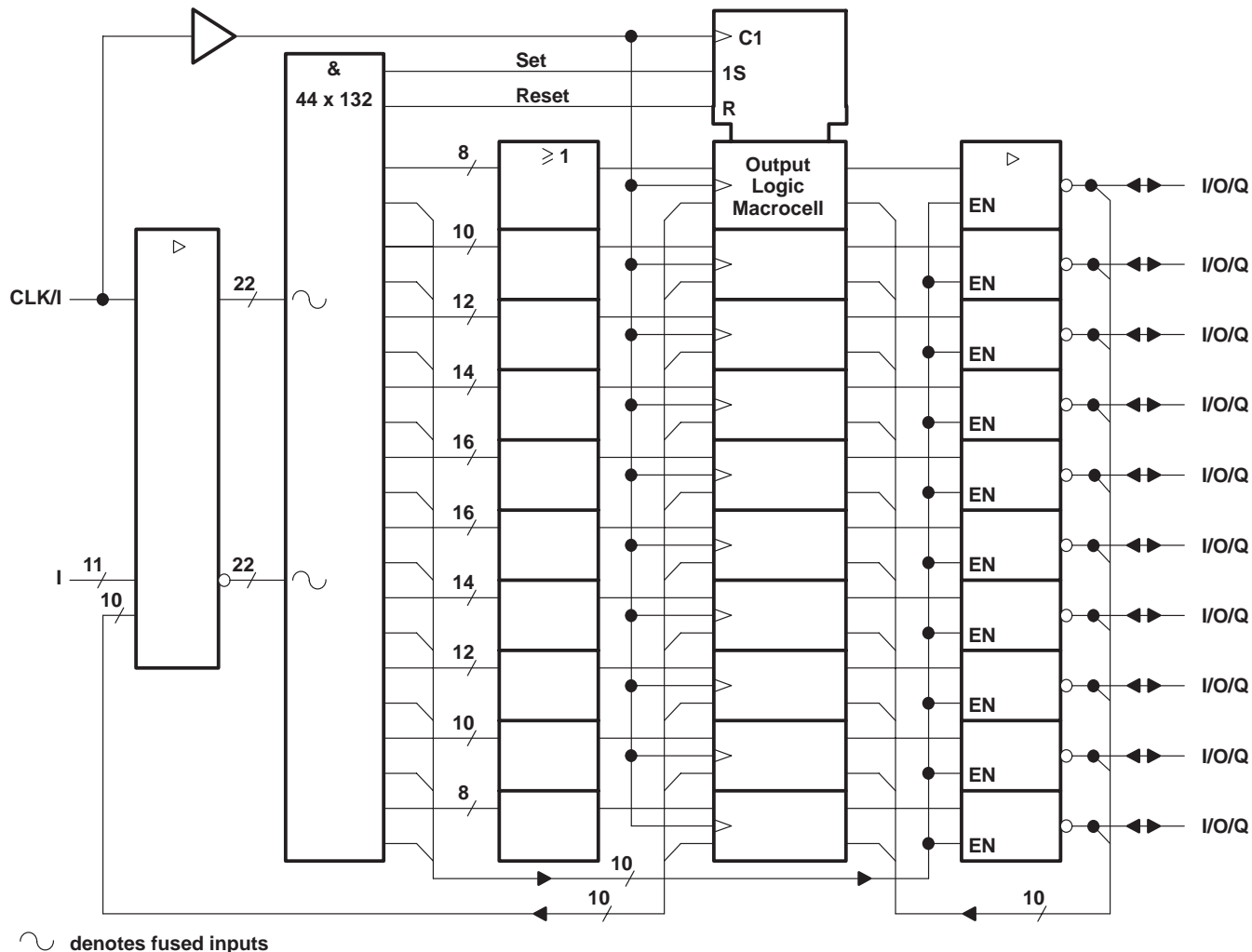The TIBPAL22V10-5C is characterized for operation from 0°C to 75°C.

functional block diagram (positive logic)

$\curvearrowright$ **denotes fused inputs**

logic diagram (positive logic)

Increment

0 4 8 12 16 20 24 28 32 36 40

CLK/I 1

2

3

First Fuse Numbers → 0

28

27

26

Asynchronous Reset
(to all registers)

I/O/Q 4

Macro-cell
P = 5808
R = 5809

396

440

880

Macro-cell
P = 5810
R = 5811

25 I/O/Q

924

I/O/Q 5

Macro-cell
P = 5812
R = 5813

1452

1496

Macro-cell
P = 5814
R = 5815

23 I/O/Q

2112

2156

I/O/Q 7

Macro-cell
P = 5816
R = 5817

2860
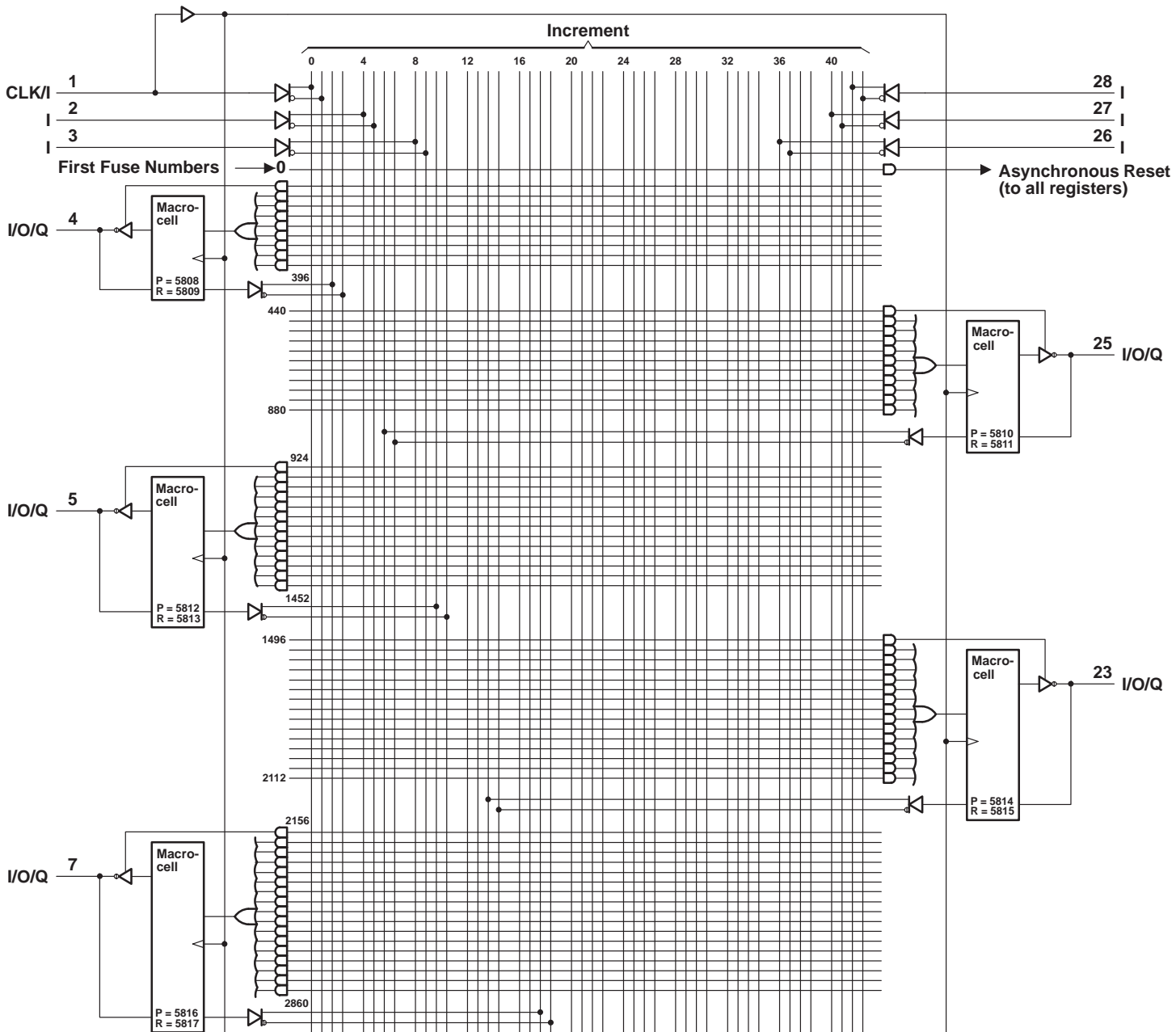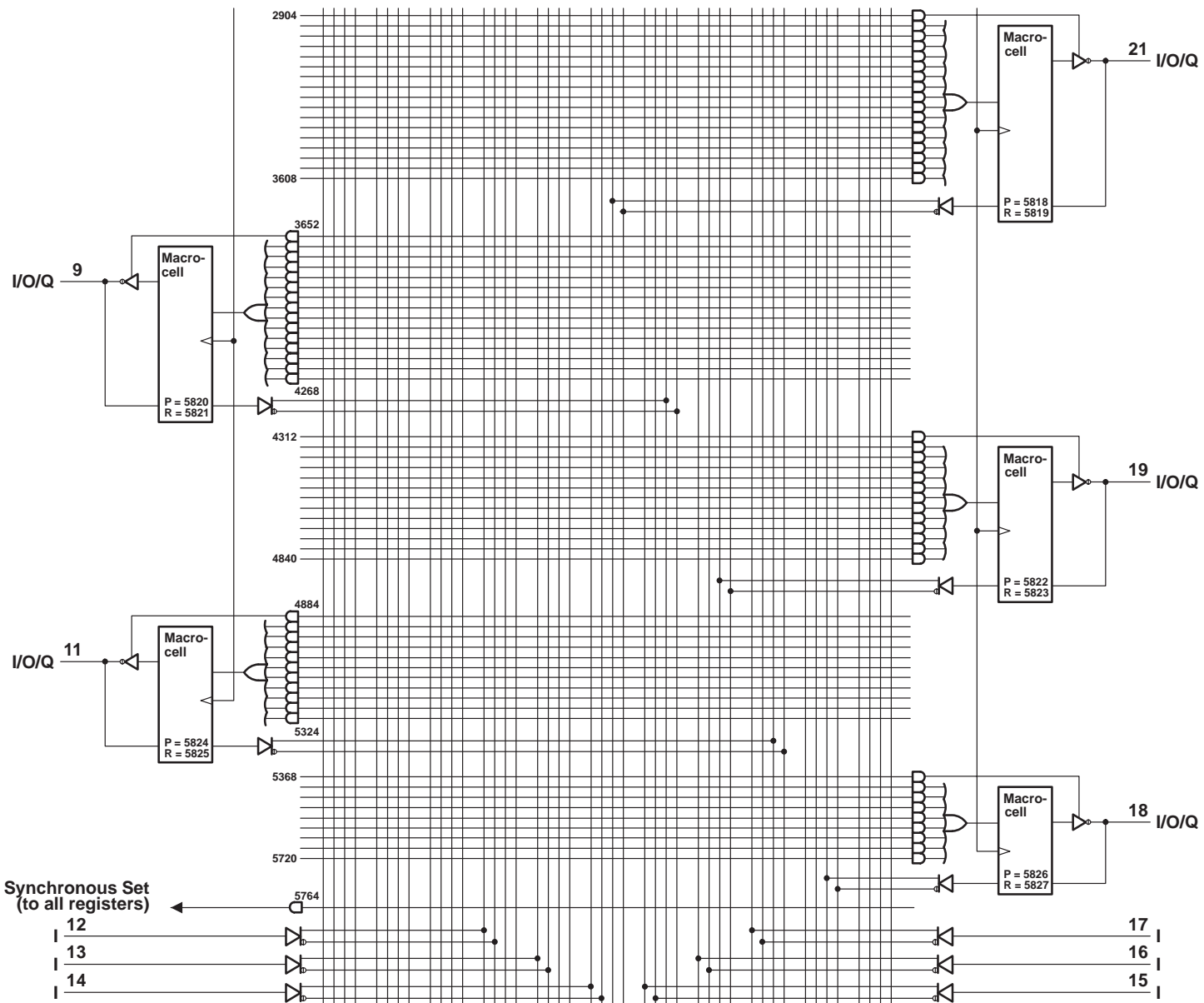
Fuse number = First fuse number + Increment
Inside each MACROCELL the "P" fuse is the polarity fuse and the "R" fuse is the register fuse.

output logic macrocell diagram

Output Logic Macrocell

From Clock Buffer

AR = asynchronous reset
SS = synchronous set

REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT

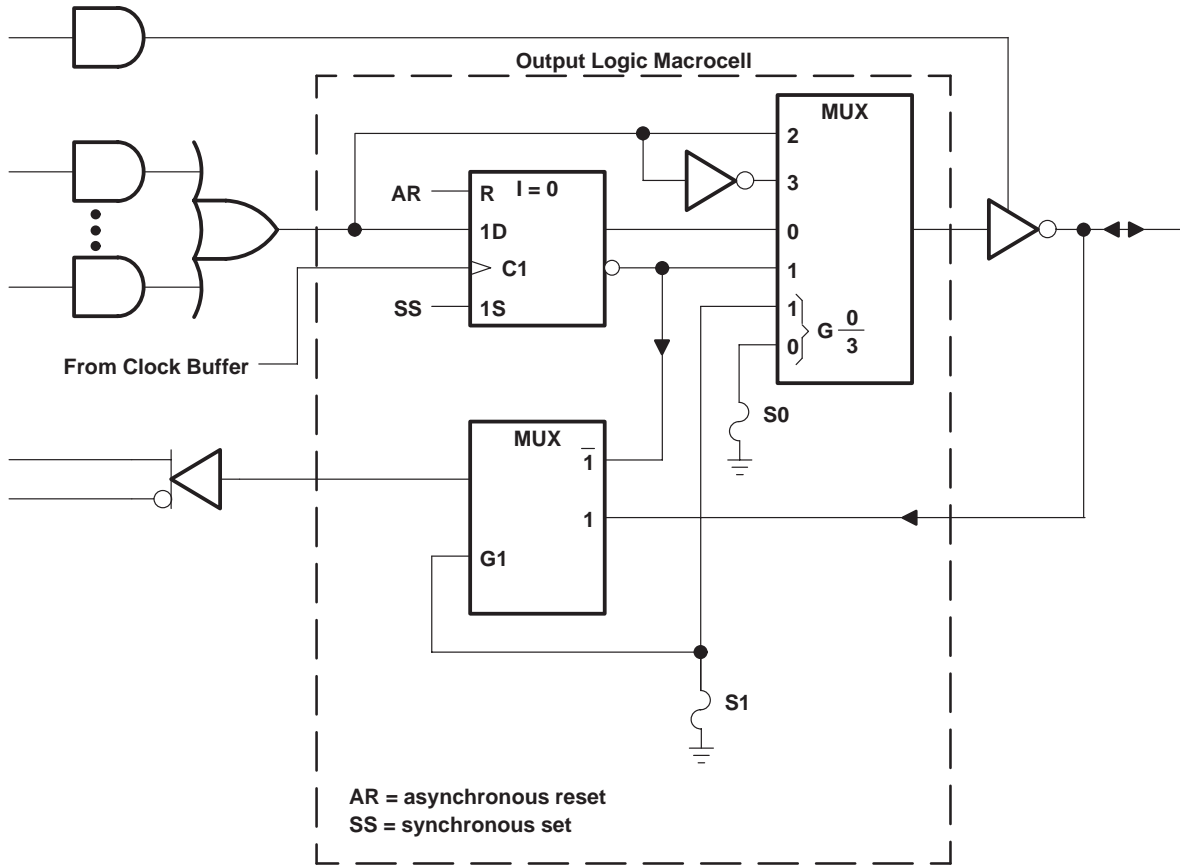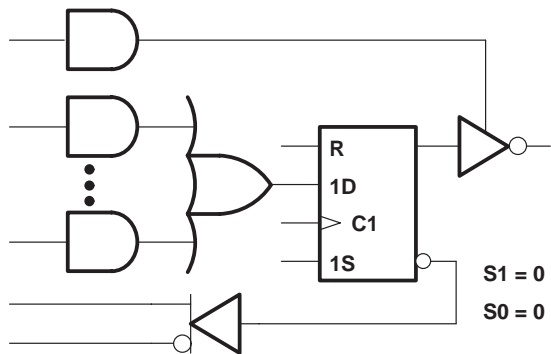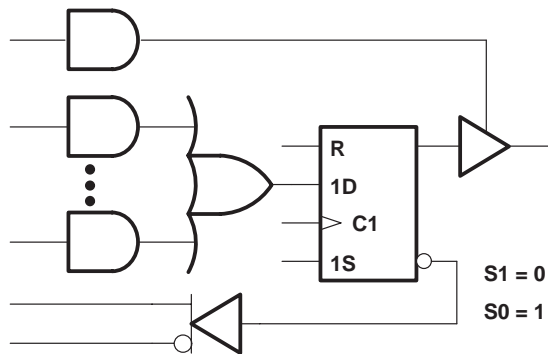**REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT**
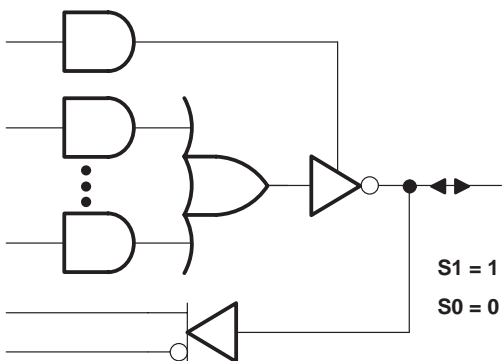
I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT
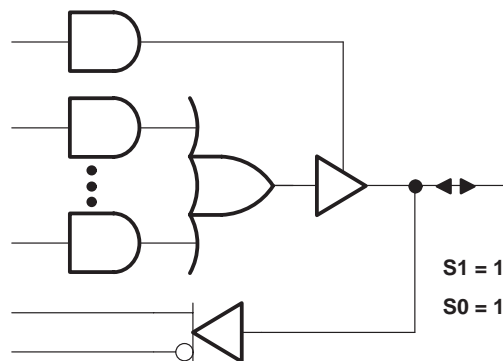
I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	**S0**			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse
S1 and S0 are select-function fuses as shown in the output logic macrocell
diagram.

Figure 1. Resultant Macrocell Feedback and Output Logic After Programming

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage range (see Note 1) . . . . −1.2 V to V_{CC} +0.5 V
Voltage range applied to disabled output (see Note 1) . . . . −0.5 V to V_{CC} +0.5 V
Operating free-air temperature range . . . . 0°C to 75°C
Storage temperature range . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				16	mA
t_w	Pulse duration	Clock high or low	3.5			ns
		Asynchronous reset high or low	5			
t_{su}	Setup time before clock↑	Input	4.5			ns
		Feedback	4.5			
		Synchronous preset (active)	7			
		Synchronous preset (inactive)	7			
		Asynchronous reset (inactive)	6			
t_h	Hold time, input, set, or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0		75	°C

NOTE 2: These are absolute voltage levels with respect to the ground terminal of the device and includes all overshoots due to system and/or
tester noise. Testing these parameters should not be attempted without suitable equipment.

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electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	$I_I = -18$ mA				−1.2	V
V_{OH}		V_{CC} = 4.75 V,	$I_{OH} = -3.2$ mA		2.4			V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 16 mA			0.35	0.5	V
I_{OZH}‡		V_{CC} = 5.25 V,	V_O = 2.7 V				0.1	mA
I_{OZL}‡		V_{CC} = 5.25 V,	V_O = 0.4 V				−0.1	mA
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V				25	µA
I_{IL}	CLK	V_{CC} = 5.25 V,	V_I = 0.4 V				−0.3	mA
	All others						−0.1	
I_{OS}§		V_{CC} = 5.25 V,	V_O = 0.5 V		−30		−130	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = GND,	Outputs open			210	mA
C_i	I	f = 1 MHz,	V_I = 2 V				7	pF
	CLK						8	
C_O		f = 1 MHz,	V_O = 2 V				10	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}¶	Without feedback			143		MHz
	With internal feedback (counter configuration)			133		
	With external feedback			117		
t_{pd}	I, I/O	I/O	R1 = 300 Ω,	1	5	ns
t_{pd}	I, I/O (reset)	Q	R2 = 300 Ω,		10	ns
t_{pd}	CLK	Q	See Figure 4	0.5	4	ns
t_{pd}#	CLK	Feedback			3	ns
t_{en}	I, I/O	I/O, Q			6.5	ns
t_{dis}	I, I/O	I/O, Q			6	ns

¶ f_{max} (without feedback) $= \dfrac{1}{t_{w(low)} \ + \ t_{w(high)}}$

f_{max} (with internal feedback) $= \dfrac{1}{t_{su} \ + \ t_{pd}\text{(CLK to feedback)}}$

f_{max} (with external feedback) $= \dfrac{1}{t_{su} \ + \ t_{pd}\text{(CLK to Q)}}$

This parameter is calculated from the measured f_{max} with internal feedback in the counter configuration.

preload procedure for registered outputs (see Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below:

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 14 to V_{IHH}.

Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.

Step 3. Pulse pin 1, clocking in preload data.

Step 4. Remove output voltage, then lower pin 14 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.
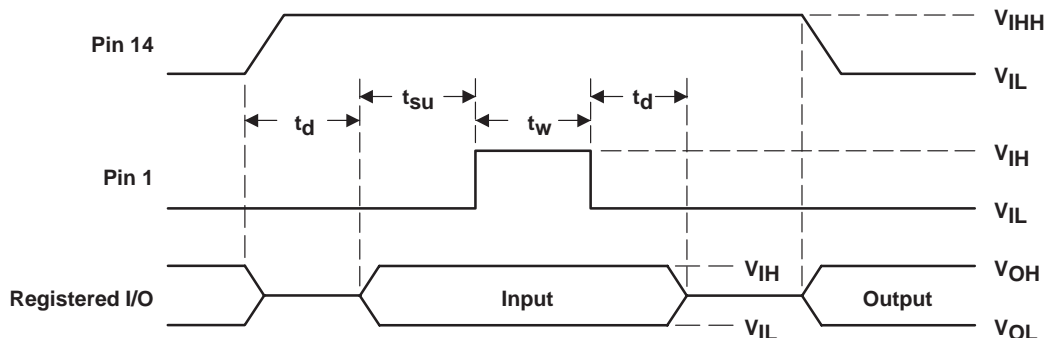

Figure 2. Preload Waveforms

NOTE 3: $t_d = t_{su} = t_w = 100$ ns to 1000 ns. $V_{IHH} = 10.25$ V to 10.75 V.

power-up reset

Following power up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.
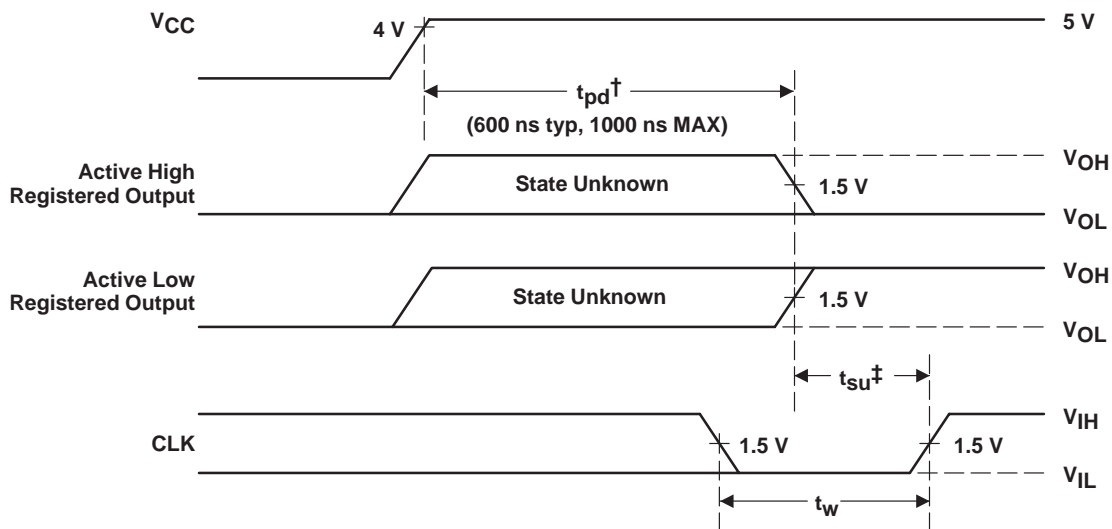
† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 3. Power-Up Reset Waveforms

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

PARAMETER MEASUREMENT INFORMATION

**LOAD CIRCUIT FOR
3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PULSE DURATIONS**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**
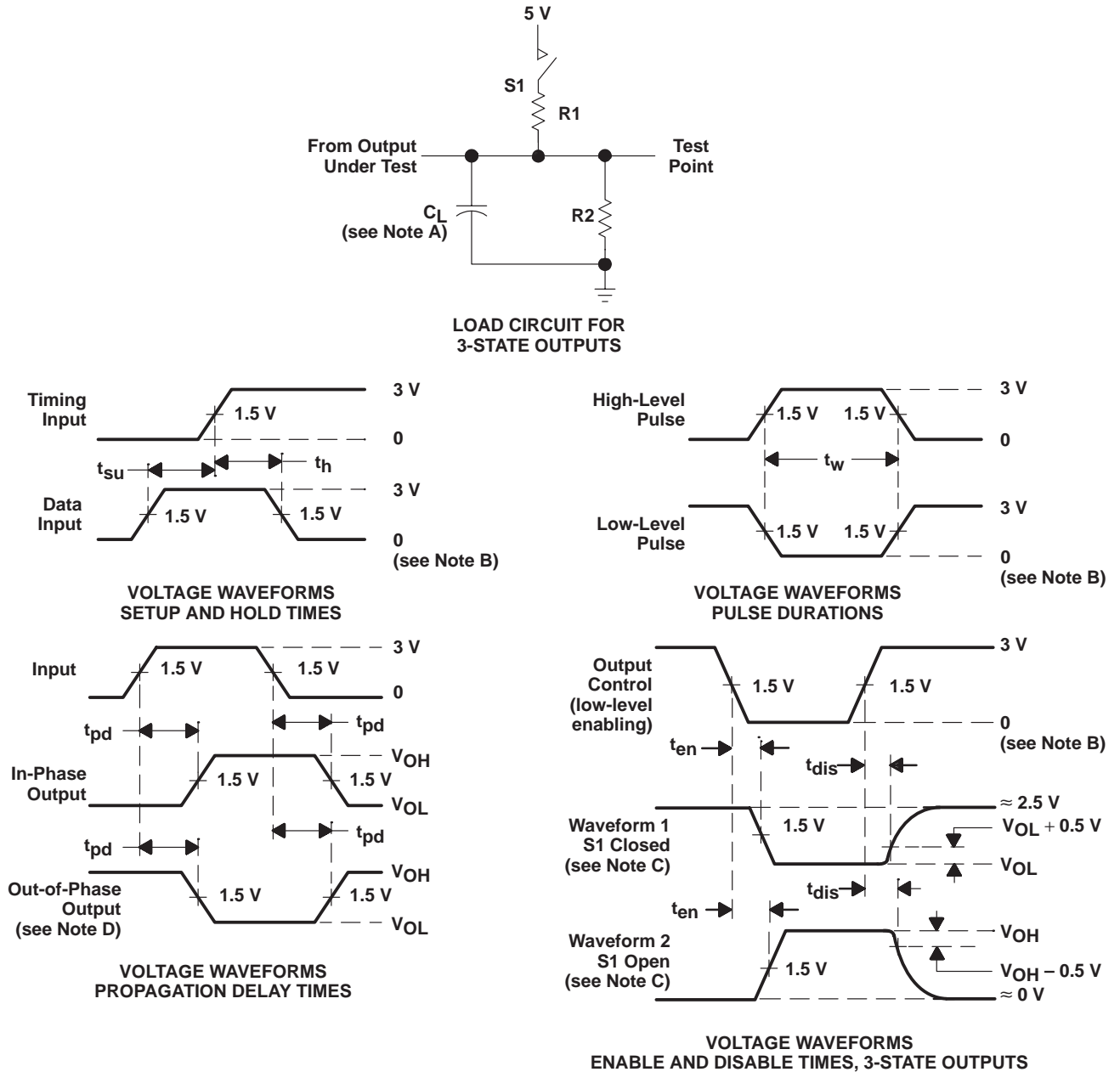
NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
  B. All input pulses have the following characteristics: PRR $\leq$ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
  C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
  E. Equivalent loads may be used for testing.

Figure 4. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 5

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

Figure 6

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

Figure 7

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

Figure 8

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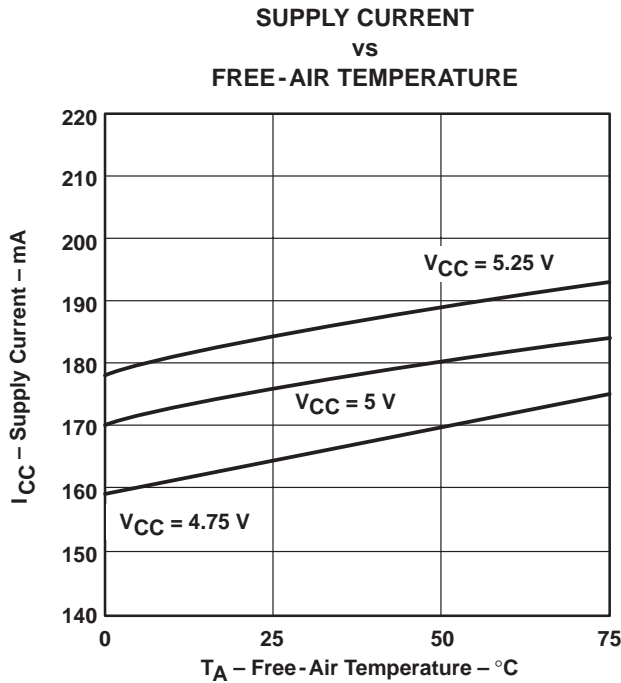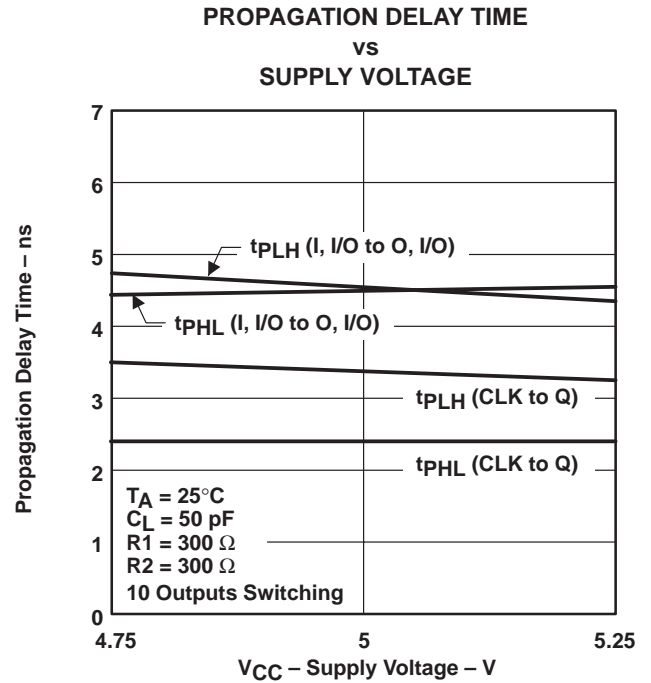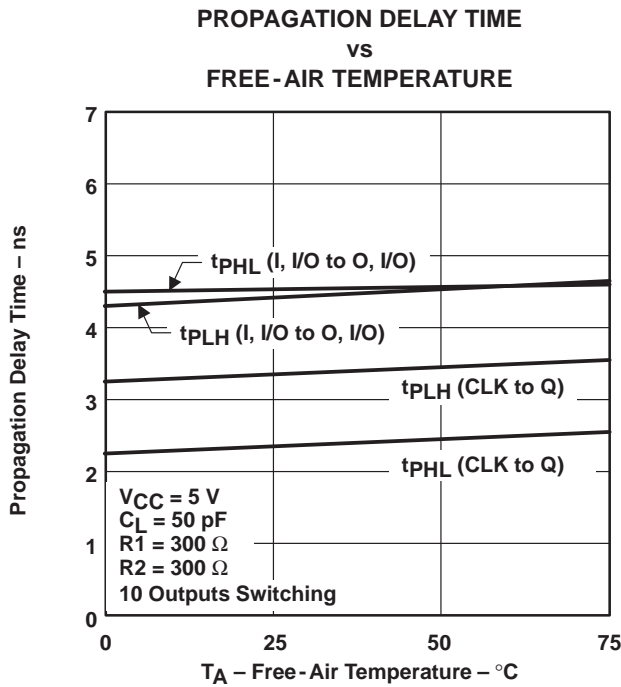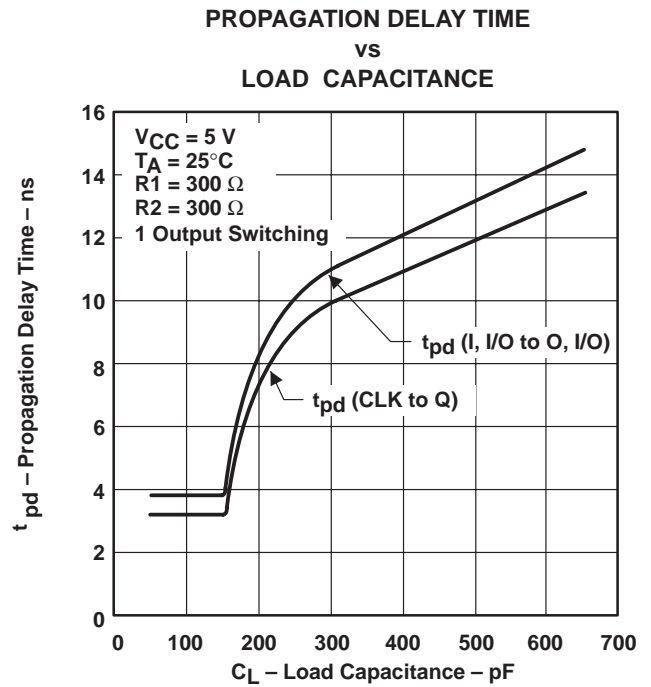
TYPICAL CHARACTERISTICS

WORST-CASE PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

Figure 9

POWER DISSIPATION
vs
FREQUENCY
10-BIT COUNTER MODE

Figure 10

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ARIZONA: Phoenix: 8825 N. 23rd Avenue, Suite 100, Phoenix, AZ 85021, (602) 995-1007.
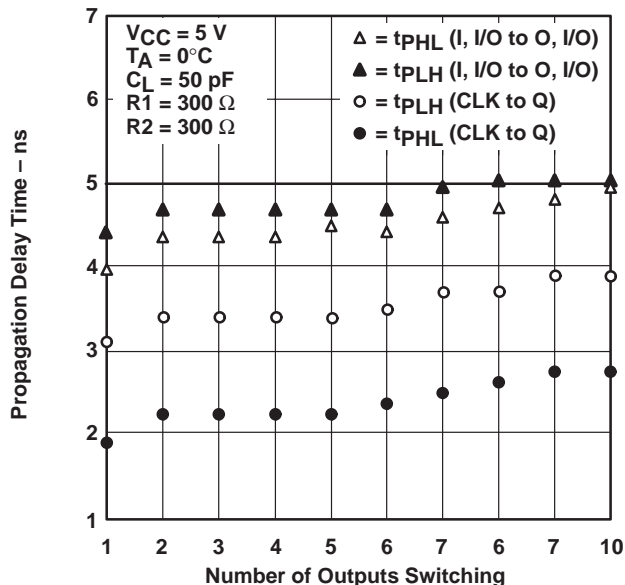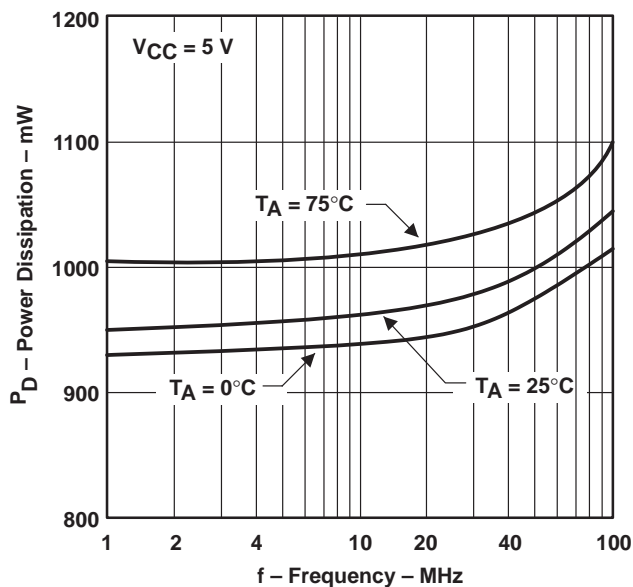**CALIFORNIA: Irvine:** 1920 Main Street, Suite 900, Irvine, CA 92714, (714) 660-1200;
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JAPAN: Texas Instruments Japan Ltd., Aoyama Fuji Building 3-6-12 Kita-Aoyama Minato-ku, Tokyo, Japan 107, 03-498-2111; MS Shibaura Building 9F, 4-13-23 Shibaura, Minato-ku, Tokyo, Japan 108, 03-769-8700; Nissho-iwai Building 5F, 2-5-8 Imabashi, Chuou-ku, Osaka, Japan 541, 06-204-1881; Dai-ni Toyota Building Nishi-kan 7F, 4-10-27 Meieki, Nakamura-ku, Nagoya, Japan 450, 052-583-8691; Kanazawa Oyama-cho Daiichi Seimei Building 6F, 3-10 Oyama-cho, Kanazawa-shi, Ishikawa, Japan 920, 0762-23-5471; Matsumoto Showa Building 6F, 1-2-11 Fukashi, Matsumoto-shi, Nagano, Japan 390 0263-33-1060; Daiichi Olympic Tachikawa Building 6F, 1-25-12, Akebono-cho, Tachikawa-shi, Tokyo, Japan 190, 0425-27-6760; Yokohama Business Park East Tower 10F, 134 Goudo-cho Hodogaya-ku, Yokohama-shi, Kanagawa, Japan 240, 045-338-1220; Nihon Seimei Kyoto Yasaka Building 5F, 843-2, Higashi-Shiokohji-cho, Higashi-iru, Nishinotoh-in, Shiokohji-dori, Shimogyo-ku, Kyoto, Japan 600, 075-341-7713; Sumitomo Seimei Kumagaya Bldg. 8F, 2-44 Yayoi, Kumagaya-shi, Saitama, Japan 360, 0485-22-2440; 2597-1, Aza Harudai, Oaza Yasaka, Kitsuki-shi, Oita, Japan 873, 09786-3-3211.
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