# TPS54010 3V 至 4V 输入、14A 同步降压转换器

## 1 特性

- 单独的低压电源总线
- 14A 持续输出时，用于实现高效率的 8mΩ 金属氧化物半导体场效应晶体管 (MOSFET) 开关
- 输出电压可调低至 0.9V
- 具有 1% 内部基准精度的外部补偿
- 快速瞬态响应
- 宽 PWM 频率：280kHz 至 700kHz 可调
- 受到峰值电流限制和热关断保护的负载
- 集成解决方案减少了电路板面积和总体成本

## 2 应用

- 可在 2.5V，3.3V 上配电的低压、高密度系统
- 针对高性能数字信号处理器 (DSP)、现场可编程栅极阵列 (FPGA)、特定用途集成电路 (ASIC)、和微处理器的负载点调节
- 宽带、网络互联及光纤通信基础设施

## 3 说明

直流/直流稳压器中的 TPS54010 低输入电压、高输出电流、同步降压 PWM 转换器集成了所有必需的有源组件。除了所列的特性 之外， 基板还包含一个真正的高性能电压误差放大器（可在瞬态条件下实现高性能，并且可灵活选择输出滤波器 L 和 C 组件）；一个欠压锁定电路（用于防止在输入电压达到 3V 之前启动）；一个内部和外部设置的慢速启动电路（用于限制浪涌电流）；以及一个电源正常状态输出（用于处理器/逻辑复位、故障信令和电源定序）。

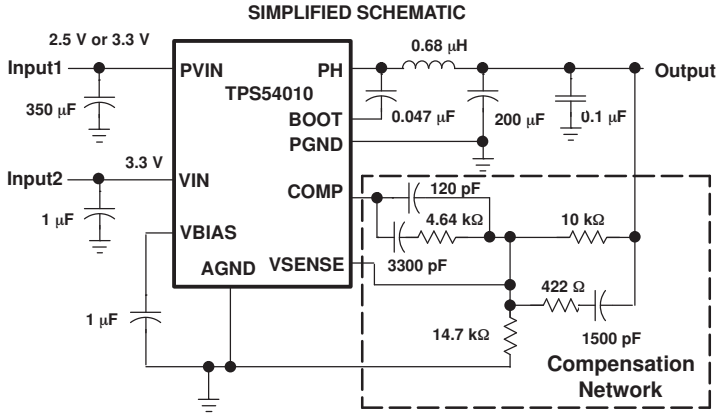
TPS54010 采用耐热增强型 28 引脚薄型小尺寸 (TSSOP)(PWP) PowerPAD™封装，无需大型散热器。

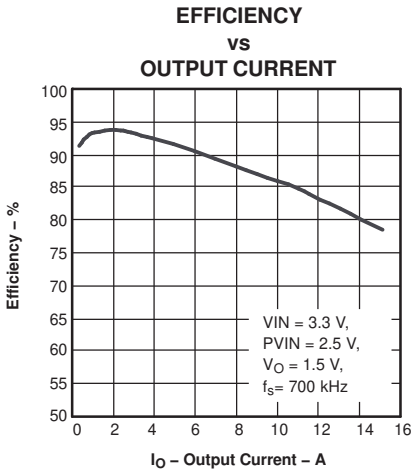
器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TPS54010 | HTSSOP (28) | 9.70mm × 4.40mm |

(1) 如需了解所有可用封装，请参阅产品说明书书末尾的可订购产品附录。

典型应用和效率曲线



# 目录



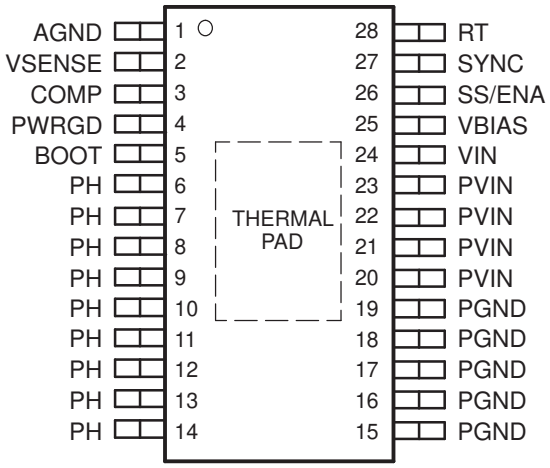
## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| Changes from Revision B (June 2005) to Revision C | Page |
|---|---|
| • 仅有编辑更改，无技术性修订； | 1 |
| • 删除“订购信息”表和 POA 中的信息 | 1 |

# 5 Pin Configuration and Functions

**PWP Package**
**28-Pin HTSSOP**
**Top View**




**Pin Functions**

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| AGND | 1 | Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, and RT resistor. If using the PowerPAD, connect it to AGND. See the *Application Information* section for details. |
| BOOT | 5 | Bootstrap output. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver. |
| COMP | 3 | Error amplifier output. Connect frequency compensation network from COMP to VSENSE |
| PGND | 15, 16, 17, 18, 19 | Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single point connection to AGND is recommended. |
| PH | 6-14 | Phase output. Junction of the internal high-side and low-side power MOSFETs, and output inductor. |
| PVIN | 20, 21, 22, 23 | Input supply for the power MOSFET switches and internal bias regulator. Bypass the PVIN pins to the PGND pins close to device package with a high-quality, low-ESR 10-µF ceramic capacitor. |
| PWRGD | 4 | Power-good open-drain output. High when VSENSE > 90% $V_{ref}$, otherwise PWRGD is low. Note that output is low when SS/ENA is low or the internal shutdown signal is active. |
| RT | 28 | Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, $f_s$. |
| SS/ENA | 26 | Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time. |
| SYNC | 27 | Synchronization input. Dual function pin which provides logic input to synchronize to an external oscillator or pin select between two internally set switching frequencies. When used to synchronize to an external signal, a resistor must be connected to the RT pin. |
| VBIAS | 25 | Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high-quality, low-ESR 0.1-µF to 1.0-µF ceramic capacitor. |
| VIN | 24 | Input supply for the internal control circuits. Bypass the VIN pin to the PGND pins close to device package with a high-quality, low-ESR 1-µF ceramic capacitor. |
| VSENSE | 2 | Error amplifier inverting input. Connect to output voltage compensation network/output divider. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | | MINIMUM to MAXIMUM | UNIT |
|---|---|---|---|---|
| $V_I$ | Input voltage range | SS/ENA, SYNC | –0.3 to 7 | V |
| | | RT | –0.3 to 6 | |
| | | VSENSE | –0.3 to 4 | |
| | | PVIN, VIN | –0.3 to 4.5 | |
| | | BOOT | –0.3 to 10 | |
| $V_O$ | Output voltage range | VBIAS, COMP, PWRGD | –0.3 to 7 | V |
| | | PH | –0.6 to 6 | |
| $V_O$ | Source current | PH | Internally limited | |
| | | COMP, VBIAS | 6 | mA |
| $I_S$ | Sink current | PH | 25 | A |
| | | COMP | 6 | mA |
| | | SS/ENA, PWRGD | 10 | |
| | Voltage differential | AGND to PGND | ±0.3 | V |
| $T_J$ | Operating junction temperature range | | –40 to 125 | °C |
| $T_{stg}$ | Storage temperature range | | –65 to 150 | °C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 300 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | 1500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 (2) | 750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_I$ | Input voltage, VIN | 3 | | 4 | V |
| | Power Input voltage, PVIN | 2.2 | | 4 | V |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

## 6.4 Dissipation Ratings (1) (2)

| PACKAGE | THERMAL IMPEDANCE JUNCTION-TO-AMBIENT | $T_A$ = 25°C POWER RATING | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|
| 28-Pin PWP with solder | 14.4°C/W | 6.94 W (3) | 3.81 W | 2.77 W |
| 28-Pin PWP without solder | 27.9°C/W | 3.58 W | 1.97 W | 1.43 W |

(1) For more information on the PWP package, refer to TI technical brief, literature number SLMA002.
(2) Test board conditions:
  (a) 3 inch × 3 inch, 4 layers, thickness: 0.062 inch
  (b) 1.5-oz. copper traces located on the top of the PCB
  (c) 1.5-oz. copper ground plane on the bottom of the PCB
  (d) 0.5-oz. copper ground planes on the 2 internal layers
  (e) 12 thermal vias (see Recommended Land Pattern in applications section of this data sheet)
(3) Maximum power dissipation may be limited by over current protection.

## 6.5 Electrical Characteristics

$T_J$ = –40°C to 125°C, $V_{IN}$ = 3 V to 4 V, $P_{VIN}$ = 2.2 V to 4 V (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE, VIN** | | | | | | | |
| $V_I$ | Input voltage, VIN | | | 3 | | 4 | V |
| | Supply voltage range, PVIN | | Output = 1.8 V | 2.2 | | 4 | V |
| $I_Q$ | Quiescent current | VIN | $f_s$ = 350 kHz, RT open, PH pin open, PVIN = 2.5 V, SYNC = 0 V | | 6.3 | 10 | mA |
| | | | $f_s$ = 550 kHz, RT open, PH pin open, SYNC ≥ 2.5 V, PVIN = 2.5 V | | 8.3 | 13 | mA |
| | | | SHUTDOWN, SS/ENA = 0 V, PVIN = 2.5 V | | 1 | 1.4 | mA |
| | | PVIN | $f_s$ = 350 kHz, RT open, PH pin open, PVIN = 3.3 V, SYNC = 0 V | | 6 | 8 | mA |
| | | | $f_s$ = 550 kHz, RT open, PH pin open, SYNC ≥ 2.5 V, PVIN = 2.5 V, VIN = 3.3 V | | 6 | 9 | mA |
| | | | SHUTDOWN, SS/ENA = 0 V, VIN = 3.3 V | | <140 | | µA |
| **UNDERVOLTAGE LOCKOUT (VIN)** | | | | | | | |
| | Start threshold voltage, UVLO | | | | 2.95 | 3 | V |
| | Stop threshold voltage, UVLO | | | 2.7 | 2.8 | | V |
| | Hysteresis voltage, UVLO | | | | 0.11 | | V |
| | Rising and falling edge deglitch, UVLO(1) | | | | 2.5 | | µs |
| **BIAS VOLTAGE** | | | | | | | |
| | Output voltage, VBIAS | | $I_{(VBIAS)}$ = 0 | 2.7 | 2.8 | 2.9 | V |
| | Output current, VBIAS(2) | | | | | 100 | µA |
| **CUMULATIVE REFERENCE** | | | | | | | |
| $V_{ref}$ | Accuracy | | | 0.882 | 0.891 | 0.900 | V |
| **REGULATION** | | | | | | | |
| | Line regulation(1)(3) | | $I_L$ = 7 A, $f_s$ = 350 kHz, $T_J$ = 85°C | | 0.05 | | %/V |
| | Load regulation(1)(3) | | $I_L$ = 0 A to 14 A, $f_s$ = 350 kHz, $T_J$ = 85°C PVIN = 2.5 V, VIN = 3.3 V | | 0.013 | | %/A |
| **OSCILLATOR** | | | | | | | |
| | Internally set—free running frequency | | RT open(1), SYNC ≤ 0.8 V | 280 | 350 | 420 | kHz |
| | | | RT open(1), SYNC ≥ 2.5 V | 440 | 550 | 660 | |
| | Externally set—free running frequency range | | RT = 180 kΩ (1% resistor to AGND)(1) | 252 | 280 | 308 | kHz |
| | | | RT = 100 kΩ (1% resistor to AGND) | 460 | 500 | 540 | |
| | | | RT = 68 kΩ (1% resistor to AGND)(1) | 663 | 700 | 762 | |
| | High-level threshold voltage, SYNC | | | 2.5 | | | V |
| | Low-level threshold voltage, SYNC | | | | | 0.8 | V |
| | Pulse duration, SYNC(1) | | | 50 | | | ns |
| | Frequency range, SYNC | | | 300 | | 700 | kHz |
| | Ramp valley(1) | | | | 0.75 | | V |
| | Ramp amplitude (peak-to-peak)(1) | | | | 1 | | V |
| | Minimum controllable on time(1) | | | | | 200 | ns |
| | Maximum duty cycle(1) | | | 90% | | | |

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 11

## Electrical Characteristics (continued)

$T_J$ = –40°C to 125°C, $V_{IN}$ = 3 V to 4 V, $P_{VIN}$ = 2.2 V to 4 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ERROR AMPLIFIER** | | | | | | |
| | Error amplifier open-loop voltage gain | 1 kΩ COMP to AGND(1) | 90 | 110 | | dB |
| | Error amplifier unity gain bandwidth | Parallel 10 kΩ, 160 pF COMP to AGND(1) | 3 | 5 | | MHz |
| | Error amplifier common mode input voltage range | Powered by internal LDO(1) | 0 | | VBIAS | V |
| | Input bias current, VSENSE | VSENSE = $V_{ref}$ | | 60 | 250 | nA |
| | Output voltage slew rate (symmetric), COMP | | 1 | 1.4 | | V/µs |
| **PWM COMPARATOR** | | | | | | |
| | PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime) | 10-mV overdrive(1) | | 70 | 85 | ns |
| **SLOW-START/ENABLE** | | | | | | |
| | Enable threshold voltage, SS/ENA | | 0.82 | 1.2 | 1.4 | V |
| | Enable hysteresis voltage, SS/ENA(1) | | | 0.03 | | V |
| | Falling edge deglitch, SS/ENA(1) | | | 2.5 | | µs |
| | Internal slow-start time | | 2.6 | 3.35 | 4.1 | ms |
| | Charge current, SS/ENA | SS/ENA = 0 V | 2 | 5 | 8 | µA |
| | Discharge current, SS/ENA | SS/ENA = 0.2 V, VIN = 2.7 V, PVIN = 2.5 V | 1.3 | 2.3 | 4 | mA |
| **POWER GOOD** | | | | | | |
| | Power-good threshold voltage | VSENSE falling | | 93 | | %$V_{ref}$ |
| | Power-good hysteresis voltage(1) | | | 3 | | %$V_{ref}$ |
| | Power-good falling edge deglitch(1) | | | 35 | | µs |
| | Output saturation voltage, PWRGD | $I_{(sink)}$ = 2.5 mA | | 0.18 | 0.3 | V |
| | Leakage current, PWRGD | VIN = 3.3 V, PVIN = 2.5 V | | | 1 | µA |
| **CURRENT LIMIT** | | | | | | |
| | Current limit | VIN = 3.3 V, PVIN = 2.5 V (1), Output shorted | 14.5 | 21 | | A |
| | Current limit leading edge blanking time(1) | | | 100 | | ns |
| | Current limit total response time(1) | | | 200 | | ns |
| **THERMAL SHUTDOWN** | | | | | | |
| | Thermal shutdown trip point(1) | | 135 | 165 | | °C |
| | Thermal shutdown hysteresis(1) | | | 10 | | °C |
| **OUTPUT POWER MOSFETS** | | | | | | |
| $r_{DS(on)}$ | Power MOSFET switches | VIN = 3 V, PVIN = 2.5 V | | 8 | 21 | mΩ |
| | | VIN = 3.6 V, PVIN = 2.5 V | | 8 | 18 | |

## 6.6 Typical Characteristics

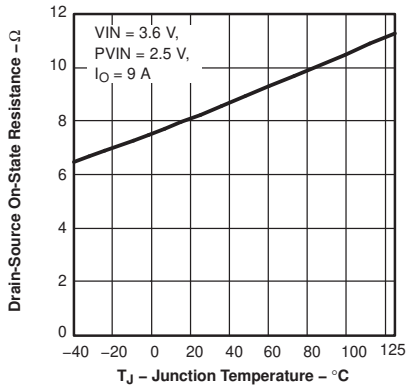



**Figure 1. Drain-Source On-State Resistance vs Junction Temperature**

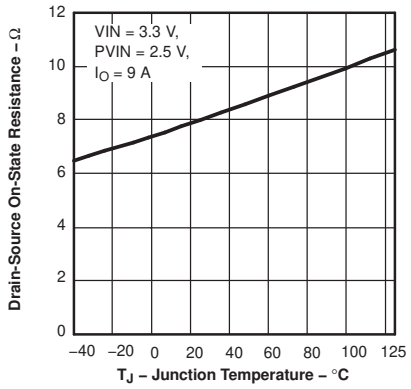



**Figure 2. Drain-Source On-State Resistance vs Junction Temperature**

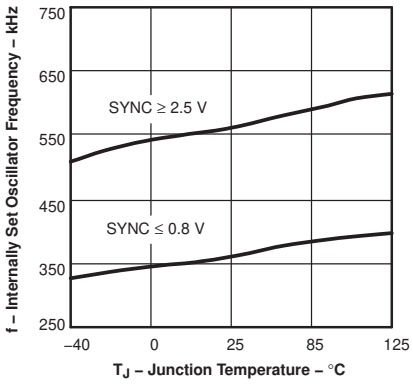



**Figure 3. Internally Set Oscillator Frequency vs Junction Temperature**

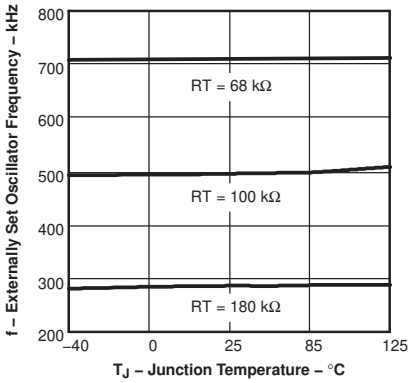



**Figure 4. Externally Set Oscillator Frequency vs Junction Temperature**

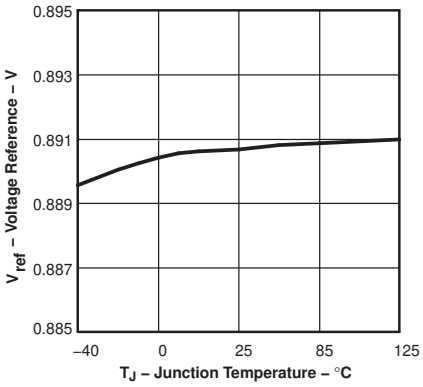



**Figure 5. Voltage Reference vs Junction Temperature**

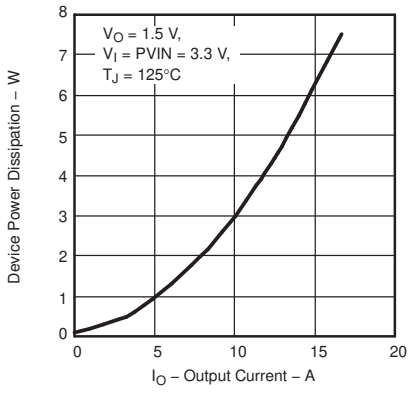



**Figure 6. Device Power Dissipation vs Output Current**

## Typical Characteristics (continued)

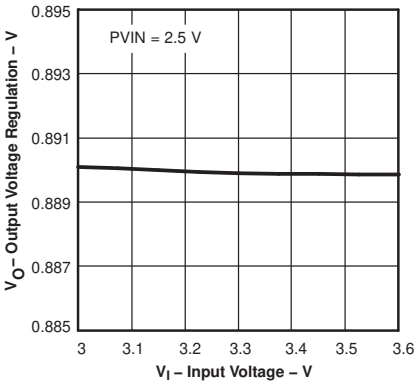



**Figure 7. Reference Voltage vs Input Voltage**

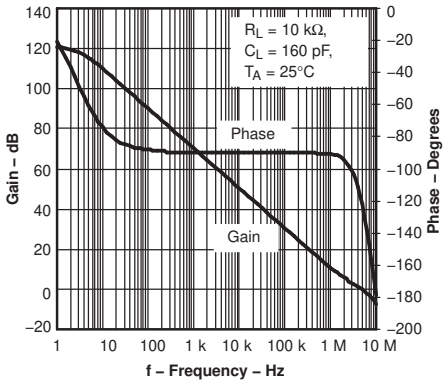



**Figure 8. Error Amplifier Open-Loop Response**

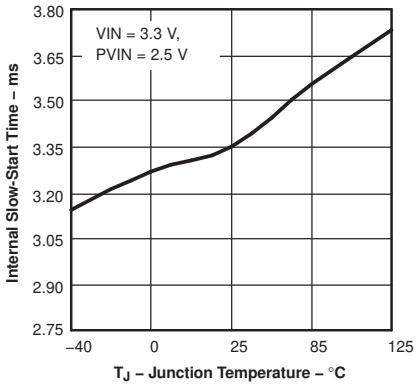


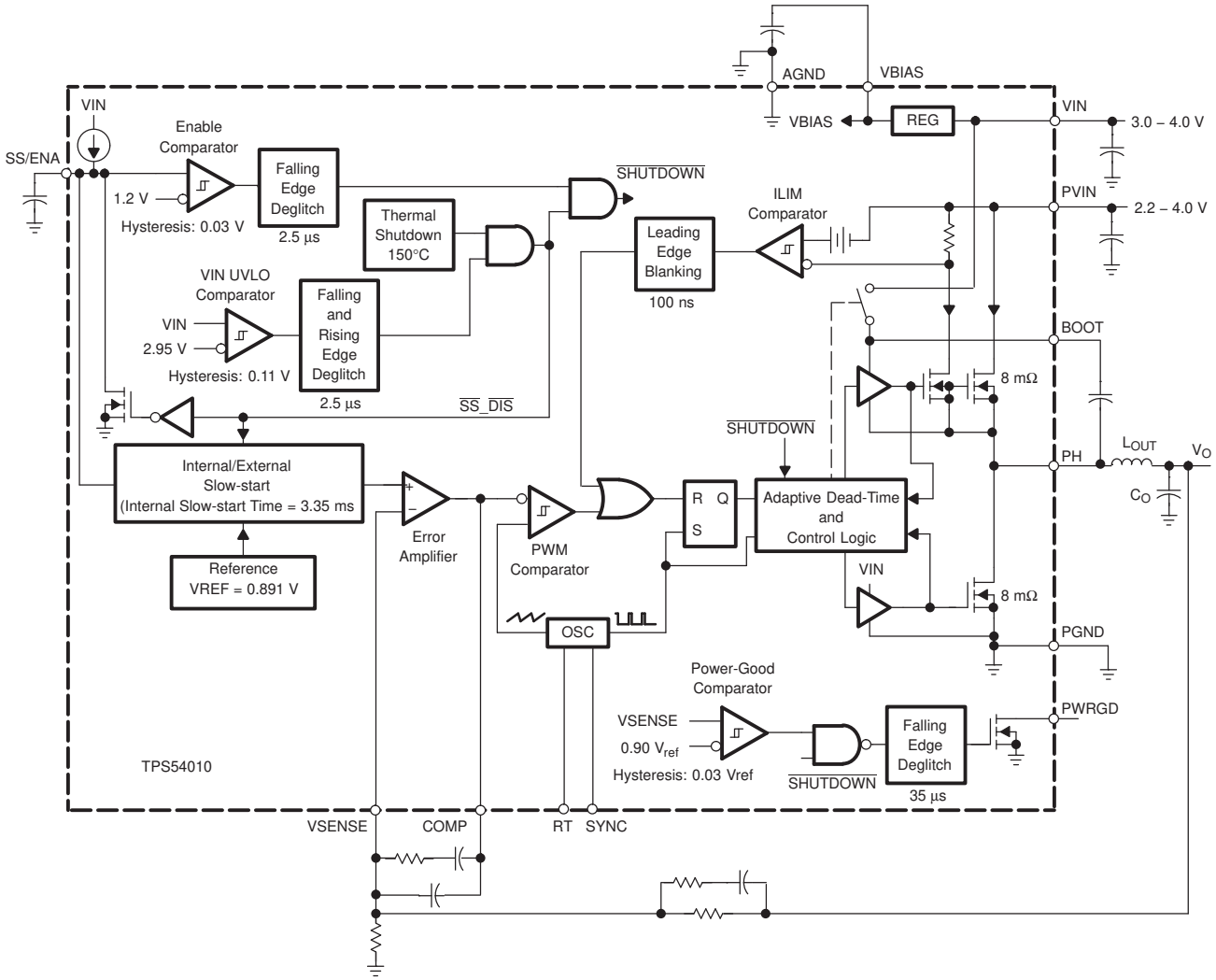

**Figure 9. Internal Slow-Start Time vs Junction Temperature**

# 7 Detailed Description

## 7.1 Overview

The TPS54010 low-input voltage, high-output current synchronous buck PWM converter in a dc/dc regulator integrating all required active components. Included on the substrate with the listed features are a true, high-performance, voltage error amplifier that enables maximum performance under transient conditions and flexibility in choosing the output filter L and C components; an undervoltage-lockout circuit to prevent start-up until the VIN input voltage reaches 3 V; an internally and externally set slowstart circuit to limit in-rush currents; and a power-good output useful for processor/logic reset, fault signaling, and supply sequencing.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Operating With Separate Pvin

The TPS54010 is designed to operate with the power stage (high-side and low-side MOSFETs) and the PVIN input connected to a separate power source from VIN. The primary intended application has VIN connected to a 3.3-V bus and PVIN connected to a 2.5-V bus. The TPS54010 cannot be damaged by any sequencing of these voltages. However, the UVLO (see Undervoltage Lockout (UVLO)) is referenced to the VIN input. Some conditions may cause undesirable operation.

## Feature Description (continued)

If PVIN is absent when the VIN input is high, the slow-start is released, and the PWM circuit goes to maximum duty factor. When the PVIN input ramps up, the output of the TPS54010 follows the PVIN input until enough voltage is present to regulate to the proper output value.

**NOTE**

If the PVIN input is controlled via a fast bus switch, it results in a hard-start condition and may damage the load (that is, whatever is connected to the regulated output of the TPS54010). If a power-good signal is not available from the 2.5-V power supply, one can be generated using a comparator and hold the SS/ENA pin low until the 2.5-V bus power is good. An example of this is shown in Figure 10. This circuit can also be used to prevent the TPS54010 output from following the PVIN input while the PVIN power supply is ramping up.

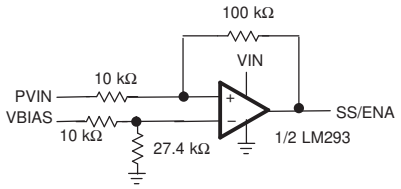



**Figure 10. Undervoltage Lockout Circuit For Pvin Using Open-Collector or Open-Drain Comparator**

PVIN and VIN can be tied together for 3.3-V bus operation.

### 7.3.2 Maximum Output Voltage

The maximum attainable output voltage is limited by the minimum voltage at the PVIN pin. Nominal maximum duty cycle is limited to 90% in the TPS54010; so, maximum output voltage is:

$$V_{O(max)} = PVIN_{(min)} \times 0.9 \quad (1)$$

Care must be taken while operating when nominal conditions cause duty cycles near 90%. Load transients can require momentary increases in duty cycle. If the required duty cycle exceeds 90%, the output may fall out of regulation.

### 7.3.3 Grounding and PowerPAD Layout

The TPS54010 has two internal grounds (analog and power). Inside the TPS54010, the analog ground ties to all of the noise-sensitive signals, whereas the power ground ties to the noisier power signals. The PowerPAD must be tied directly to AGND. Noise injected between the two grounds can degrade the performance of the TPS54010, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground planes are recommended. These two planes must tie together directly at the IC to reduce noise between the two grounds. The only components that must tie directly to the power ground plane are the input capacitor, the output capacitor, the input voltage decoupling capacitor, and the PGND pins of the TPS54010.

### 7.3.4 Slow-Start/Enable (SS/ENA)

The slow-start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start-up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-ms falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND.

Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start-up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

## Feature Description (continued)

$$t_d = C_{(SS)} \times \frac{1.2\ V}{5\ \mu A} \quad (2)$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ V}{5\ \mu A} \quad (3)$$

The actual slow-start time is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

### 7.3.5 Undervoltage Lockout (UVLO)

The TPS54010 incorporates an undervoltage-lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-ms rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN. UVLO is with respect to VIN and not PVIN, see the *Application Information* section.

### 7.3.6 VBIAS Regulator (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high-quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor must be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.7 V, and external loads on VBIAS with ac or digital-switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits. VBIAS is derived from the VIN pin; see the functional block diagram of this data sheet.

### 7.3.7 Voltage Reference

The voltage reference system produces a precise $V_{ref}$ signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high-precision regulation of the TPS54010, because it cancels offset errors in the scale and error amplifier circuits.

### 7.3.8 Oscillator and PWM Ramp

The oscillator frequency is set to an internally fixed value of 350 kHz. The oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor between the RT pin to ground. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100\ k\Omega}{R} \times 500\ [kHz] \quad (4)$$

External synchronization of the PWM ramp is possible over the frequency range of 330 kHz to 700 kHz by driving a synchronization signal into SYNC and connecting a resistor from RT to AGND. Choose a resistor between the RT and AGND which sets the free running frequency to 80% of the synchronization signal. The following table summarizes the frequency selection configurations:

## Feature Description (continued)

| SWITCHING FREQUENCY | SYNC PIN | RT PIN |
|---|---|---|
| 350 kHz, internally set | Float or AGND | Float |
| 550 kHz, internally set | ≥ 2.5 V | Float |
| Externally set 280 kHz to 700 kHz | Float | R = 180 kΩ to 68 kΩ |
| Externally synchronized frequency | Synchronization signal | R = RT value for 80% of external synchronization frequency |

### 7.3.9 Error Amplifier

The high-performance, wide bandwidth, voltage error amplifier sets the TPS54010 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type-2 or Type-3 compensation can be employed using external compensation components.

### 7.3.10 PWM Control

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control-logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp. During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54010 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

### 7.3.11 Dead-Time Control and MOSFET Drivers

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turn-on times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side FET is below 2 V. While the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V.

The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, whereas the high-side driver is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

### 7.3.12 Overcurrent Protection

The cycle-by-cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and comparing this signal to a preset overcurrent threshold. The high-side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading-edge blanking circuit prevents current limit false tripping. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

### 7.3.13 Thermal Shutdown

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the slow-start circuit, heating up due to the fault condition, and then shutting down on reaching the thermal shutdown trip point. This sequence repeats until the fault condition is removed.

### 7.3.14 Power-Good (PWRGD)

The power-good circuit monitors for undervoltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold or SS/ENA is low. When VIN, UVLO threshold, SS/ENA, enable threshold, and VSENSE > 90% of Vref, the open-drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of $V_{ref}$ and a 35-µs falling-edge deglitch circuit prevent tripping of the power-good comparator due to high-frequency noise.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The following design procedure can be used to select component values for the TPS54010. This section presents a simplified discussion of the design process.

## 8.2 Typical Application

Figure 11 shows the schematic for a typical TPS54010 application. The TPS54010 can provide up to 14-A output current at a nominal output voltage of 1.5 V. Nominal input voltages are 2.5 V for $P_{VIN}$ and 3.3 V for $V_{IN}$. For proper thermal performance, the exposed PowerPAD underneath the device must be soldered down to the printed-circuit board.

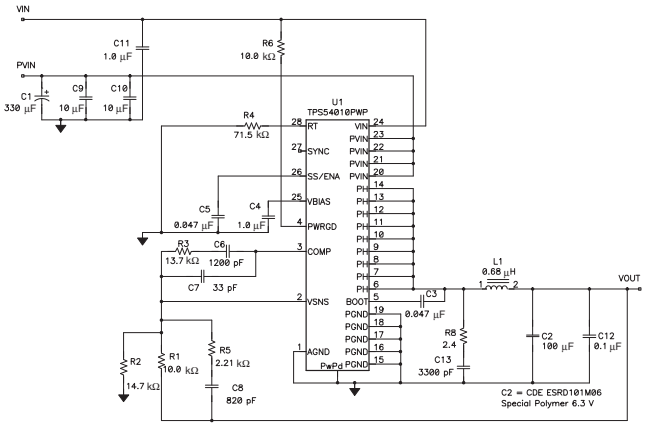



**Figure 11. Application Circuit, 2.5 V to 1.5 V**

### 8.2.1 Design Requirements

To begin the design process, a few parameters must be decided:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

For this design example, use the following as the input parameters:

**Table 1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage (VIN) | 3.3 V |
| Input voltage range (PVIN) | 2.2 to 3.5 V |
| Output voltage | 1.5 V |
| Input ripple voltage | 300 mV |
| Output ripple voltage | 50 mV |
| Output current rating | 14 A |
| Operating frequency | 700 kHz |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Switching Frequency*

The switching frequency can be set to either one of two internally programmed frequencies or set to a externally programmed frequency. With the RT pin open, setting the SYNC pin at or above 2.5 V selects 550-kHz operation, whereas grounding or leaving the SYNC pin open selects 350-kHz operation. For this design, the switching frequency is externally programmed using the RT pin. By connecting a resistor (R4) from RT to AGND, any frequency in the range of 250 to 700 kHz can be set. Use Equation 5 to determine the proper value of RT.

$$R4(k\Omega) = \frac{500\ kHz}{fs(kHz)} \times 100\ k\Omega \quad (5)$$

In this example circuit, R4 is calculated to be 71.5 kΩ and the switching frequency is set at 700 kHz.

#### 8.2.2.2 Input Capacitors

The TPS54010 requires an input de-coupling capacitor and, depending on the application, a bulk input capacitor. The minimum value for the de-coupling capacitor, C9, is 10 µF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. Additionally, some bulk capacitance may be needed, especially if the TPS54010 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but it also should be rated to handle the maximum input voltage including ripple voltage, and should filter the output so that input ripple voltage is acceptable.

This input ripple voltage can be approximated by Equation 6:

$$\Delta V_{PVIN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} + \left( I_{OUT(MAX)} \times ESR_{MAX} \right) \quad (6)$$

Where $I_{OUT(MAX)}$ is the maximum load current.

The TPS54010 requires an input de-coupling capacitor and, depending on the application, a bulk input capacitor. $f_{sw}$ is the switching frequency, $C_{(BULK)}$ is the bulk capacitor value and $ESR_{MAX}$ is the maximum series resistance of the bulk capacitor.

The maximum RMS ripple current also must be checked. For worst-case conditions, this can be approximated by Equation 7:

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \quad (7)$$

In this case, the input ripple voltage would be 155 mV and the RMS ripple current would be 7 A. The maximum voltage across the input capacitors would be Vin max plus delta Vin/2. The chosen bulk capacitor, a Sanyo POSCAP 6TPD330M is rated for 6.3 V and 4.4 A of ripple current; two bypass capacitors, TDK C3225X5R1C106M are each rated for 16 V, and the ripple current capacity is greater than 3 A at the operating frequency of 700 kHz. Total ripple current handling is in excess of 10.4 A. It is important that the maximum ratings for voltage and current are not exceeded under any circumstance.

#### 8.2.2.3 Output Filter Components

Two components need to be selected for the output filter, L1 and C2. Because the TPS54010 is an externally compensated device, a wide range of filter component types and values can be supported.

##### 8.2.2.3.1 Inductor Selection

To calculate the minimum value of the output inductor, use Equation 8

$$L_{MIN} = \frac{V_{OUT} \times \left( V_{in(MAX)} - V_{OUT} \right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{sw}} \quad (8)$$

$K_{IND}$ is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. For designs using low ESR output capacitors such as ceramics, use $K_{IND}$ = 0.3. When using higher ESR output capacitors, $K_{IND}$ = 0.2 yields better results.

For this design example, use $K_{IND}$ = 0.2 to keep the inductor ripple current small. The minimum inductor value is calculated to be 0.44 µH.

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from Equation 9:

$$I_{L(RMS)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times \left[ V_{OUT} \times \frac{\left( V_{in(MAX)} - V_{OUT} \right)}{V_{IN(MAX)} \times L_{OUT} \times F_{sw} \times 0.8} \right]^2} \quad (9)$$

and the peak inductor current can be found from Equation 10

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{in(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{sw}} \quad (10)$$

For this design, the RMS inductor current is 15.4 A, and the peak inductor current is 15.1 A. For this design, a Vishay IHLP2525CZ-01 style output inductor is specified. The largest value greater than 0.44 µH that meets these current requirements is 0.68 µH. Increasing the inductor value decreases the ripple current and the corresponding output ripple voltage. The inductor value can be decreased if more margin in the RMS current is required. In general, inductor values for use with the TPS54010 falls in the range of 0.47 to 2.2 µH.

#### 8.2.2.3.2 Capacitor Requirements

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed-loop crossover frequency of the design and LC corner frequency of the output filter. In general, it is desirable to keep the closed-loop crossover frequency at less than 1/5 of the switching frequency. With high switching frequencies such as the 500 kHz frequency of this design, internal circuit limitations of the TPS54010 limit the practical maximum crossover frequency to about 70 kHz. To allow for adequate phase gain in the compensation network, the LC corner frequency should be about one decade or so below the closed-loop crossover frequency. This limits the minimum capacitor value for the output filter to:

$$C_{OUT(MIN)} = \frac{1}{L_{OUT}} \times \left(\frac{K}{2\pi \ f_{CO}}\right)^2 \quad (11)$$

Where K is the frequency multiplier for the spread between $f_{LC}$ and $f_{CO}$. K should be between 5 and 15, typically 10 for one decade difference. For a desired crossover of 100-kHz and a 0.68-µH inductor, the minimum value for the output capacitor is 93 µF using a minimum K factor of 5. Increasing the K factor would require using a larger capacitance as 100 kHz is approaching the maximum practical closed-loop crossover frequency for this device. The selected output capacitor must be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any de-rating amount must also be included. The maximum RMS ripple current in the output capacitors is given by Equation 12:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left\{\frac{V_{OUT} \times \left(V_{PVIN(MAX)} - V_{OUT}\right)}{V_{PVIN(MAX)} \times L_{OUT} \times F_{sw}}\right\} \quad (12)$$

The calculated RMS ripple current is 780 mA in the output capacitors.

The maximum ESR of the output capacitor is determined by the amount of allowable output ripple as specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter; therefore, the maximum specified ESR as listed in the capacitor data sheet is given by Equation 13 :

$$ESR_{MAX} = N_C \times \left\{\frac{V_{IN(MAX)} \times L_{OUT} \times F_{sw} \times 0.8}{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}\right\} \times \Delta V_{P-P(MAX)} \quad (13)$$

and the maximum ESR required is 22.2 mΩ. A capacitor that meets these requirements is a Cornell Dubilier Special Polymer (SP) ESRD101M06 rated at 6.3 V with a maximum ESR of 0.015 Ω and a ripple current rating of 2 A. An additional small 0.1-µF ceramic bypass capacitor C13 is a also used.

Other capacitor types work well with the TPS54010, depending on the needs of the application.

#### 8.2.2.3.3 Compensation Components

The external compensation used with the TPS54010 allows for a wide range of output filter configurations. A large range of capacitor values and types of dielectric are supported. The design example uses Type-3 compensation consisting of R1, R3, R5, C6, C7, and C8. Additionally, R2 along with R1 forms a voltage divider network that sets the output voltage. These component reference designators are the same as those used in the SWIFT Designer Software. There are a number of different ways to design a compensation network. This procedure outlines a relatively simple procedure that produces good results with most output filter combinations. Use the SWIFT Designer Software for designs with unusually high closed-loop crossover frequencies, low value, low ESR output capacitors such as ceramics or if you are unsure about the design procedure.

When designing compensation networks for the TPS54010, a number of factors must be considered. The gain of the compensated error amplifier should not be limited by the open-loop amplifier gain characteristics and should not produce excessive gain at the switching frequency. Also, the closed-loop crossover frequency should be set less than one-fifth of the switching frequency, and the phase margin at crossover must be greater than 45 degrees. The general procedure outlined here produces results consistent with these requirements without going into great detail about the theory of loop compensation.

First, calculate the output filter LC corner frequency using Equation 14:

$$f_{LC} = \frac{1}{2\pi \sqrt{L_{OUT} C_{OUT}}} \tag{14}$$

For the design example, $f_{LC}$ = 19.3 kHz.

Choose the closed-loop crossover frequency to be greater than $f_{LC}$ and less than one-fifth of the switching frequency. Also, the crossover frequency should not exceed 150 kHz, as the error amplifier may not provide the desired gain. For this design, a crossover frequency of 100 kHz was chosen. This value is chosen for comparatively wide loop bandwidth while still allowing for adequate phase boost to insure stability.

Next, calculate the R2 resistor value for the output voltage of 1.5 V using Equation 15:

$$R2 = \frac{R1 \times 0.891}{V_{OUT} - 0.891} \tag{15}$$

For any TPS54010 design, start with an R1 value of 10 kΩ. R2 is 14.7 kΩ.

Now, the values for the compensation components that set the poles and zeros of the compensation network can be calculated. Assuming that R1 >> than R5 and C6 >> C7, the pole and zero locations are given by Equation 16 through Equation 22:

$$f_{Z1} = \frac{1}{2\pi R3C6} \tag{16}$$

$$f_{Z2} = \frac{1}{2\pi R1C8} \tag{17}$$

$$f_{P1} = \frac{1}{2\pi R5C8} \tag{18}$$

$$f_{P2} = \frac{1}{2\pi R3C7} \tag{19}$$

Additionally, there is a pole at the origin, which has unity gain at a frequency:

$$f_{INT} = \frac{1}{2\pi R1C6} \tag{20}$$

This pole is used to set the overall gain of the compensated error amplifier and determines the closed-loop crossover frequency. Because R1 is given as 1 kΩ and the crossover frequency is selected as 100 kHz, the desired $f_{INT}$ can be calculated from Equation 21:

$$f_{INT} = \frac{f_{CO}}{V_{IN(MAX)} \times 2} \tag{21}$$

And the value for C6 is given by Equation 22:

$$C6 = \frac{1}{2\pi R1 f_{INT}} \quad (22)$$

The first zero, $f_{Z1}$ is located at one-half the output filter LC corner frequency; so, R3 can be calculated from:

$$R3 = \frac{1}{\pi C6 f_{LC}} \quad (23)$$

The second zero, $f_{Z2}$ is located at the output filter LC corner frequency; so, C8 can be calculated from:

$$C8 = \frac{1}{2\pi R1 f_{LC}} \quad (24)$$

The first pole, $f_{P1}$ is located to coincide with output filter ESR zero frequency. This frequency is given by:

$$f_{ESR0} = \frac{1}{2\pi R_{ESR} C_{OUT}} \quad (25)$$

where $R_{ESR}$ is the equivalent series resistance of the output capacitor.

In this case, the ESR zero frequency is 88.4 kHz, and R5 can be calculated from:

$$R5 = \frac{1}{2\pi C8 f_{ESR}} \quad (26)$$

The final pole is placed at a frequency above the closed-loop crossover frequency high enough to not cause the phase to decrease too much at the crossover frequency while still providing enough attenuation so that there is little or no gain at the switching frequency. The $f_{P2}$ pole location for this circuit is set to 3.5 times the closed-loop crossover frequency and the last compensation component value C7 can be derived:

$$C7 = \frac{1}{7\pi R3 f_{CO}} \quad (27)$$

Note that capacitors are only available in a limited range of standard values, so the nearest standard value has been chosen for each capacitor. The measured closed-loop response for this design is shown in Figure 5.

#### 8.2.2.4 Bias and Bootstrap Capacitors

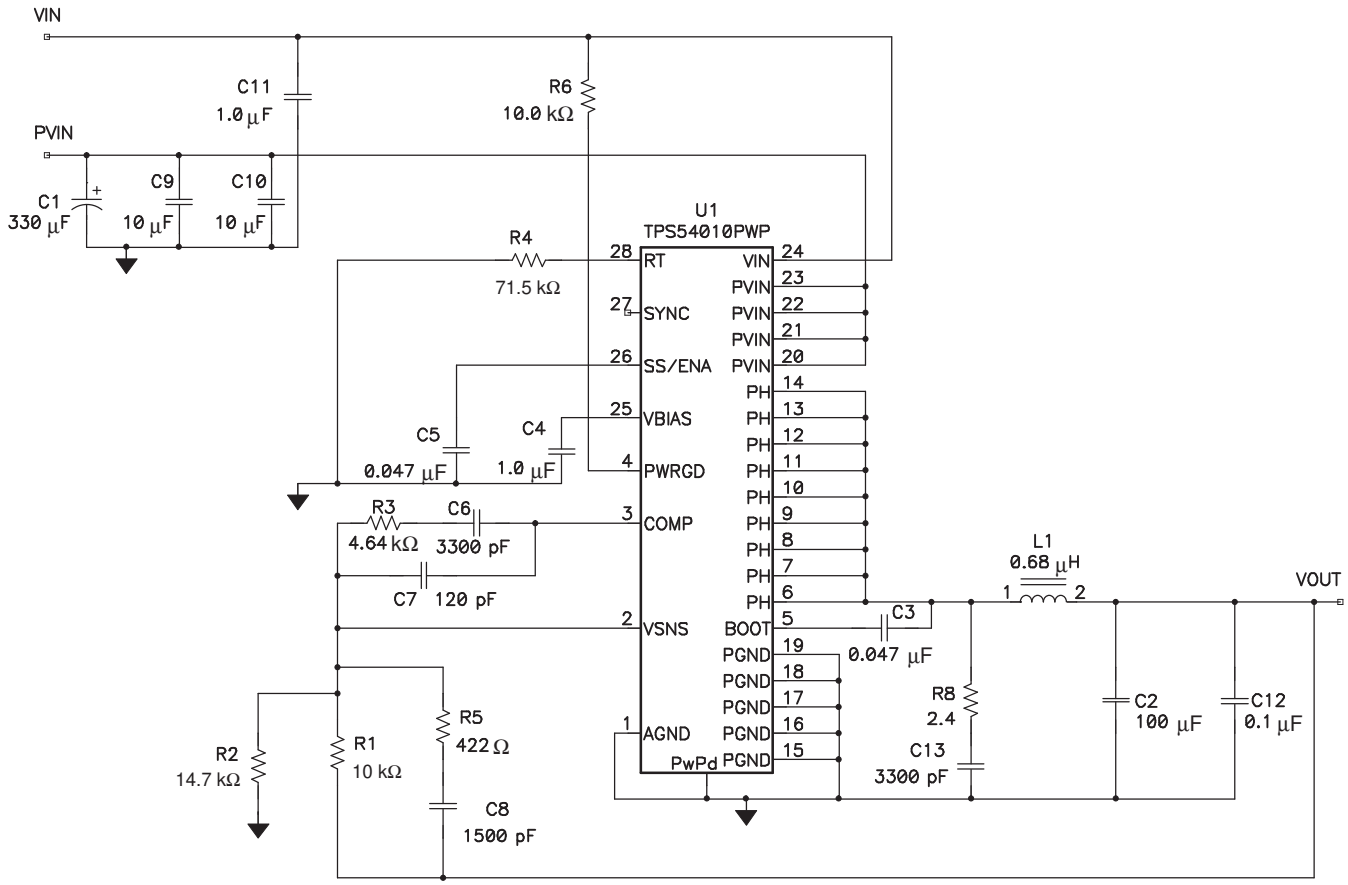
Every TPS54010 design requires a bootstrap capacitor, C3, and a bias capacitor, C4. The bootstrap capacitor must be a 0.1 µF. The bootstrap capacitor is located between the PH pins and BOOT. The bias capacitor is connected between the VBIAS pin and AGND. The value should be 1.0 µF. Both capacitors should be high-quality ceramic types with X7R or X5R grade dielectric for temperature stability. They should be placed as close to the device connection pins as possible.

#### 8.2.2.5 Power Good

The TPS54010 is provided with a power-good output pin PWRGD. This output is an open-drain output and is intended to be pulled up to a 3.3-V or 5-V logic supply. A 10-kΩ pullup works well in this application.

#### 8.2.2.6 Snubber Circuit

R10 and C11 of the application schematic comprise a snubber circuit. The snubber is included to reduce overshoot and ringing on the phase node when the internal high-side FET turns on. Because the frequency and amplitude of the ringing depends to a large degree on parasitic effects, it is best to choose these component values based on actual measurements of any design layout. See literature number SLUP100 for more detailed information on snubber design.




The following part numbers are used for test purposes:
C1 = T520D337M0O4ASE015 (Kemet)
C2 = TDK C3225X5R0J107M ceramic 6.3 V X5R
L1 = IHLP2525CZ–01 0.68 µH (Vishay Dale)

**Figure 12. 1.5-V Power Supply With Ceramic Output Capacitors**

Figure 12 shows an application where all ceramic capacitors, including the main output filter capacitor, are used. The compensation network components were calculated using SWIFT Designer Software. See Figure 21 through Figure 29 for loop response, performance graphs, and switching waveforms for this circuit.

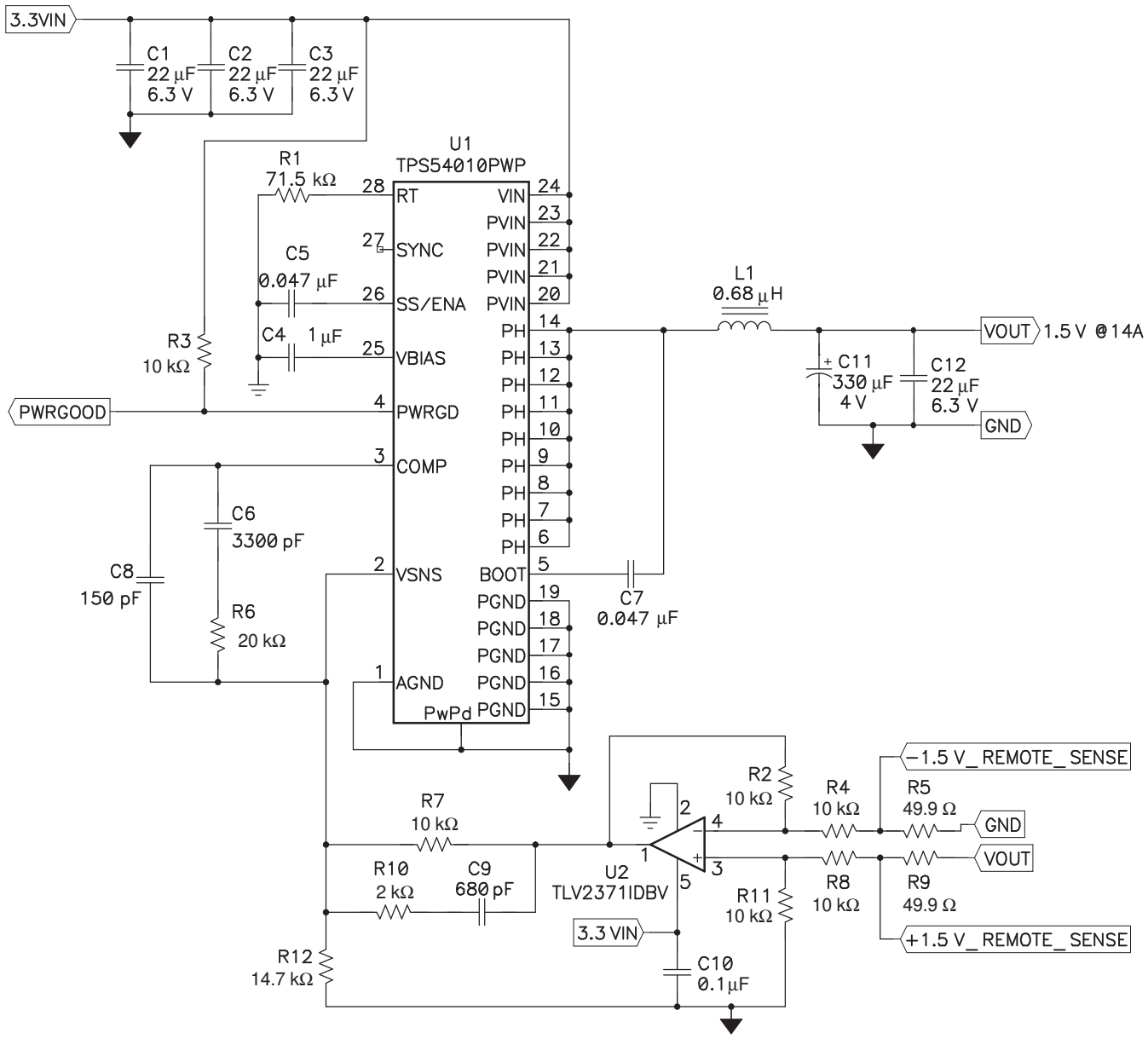



**Figure 13. 1.5-V Power Supply With Remote Sense**

With an output current of 14 A, if the load is located far from the dc/dc converter circuit, it may be beneficial to include a remote sense capability. Figure 13 is an example of a power supply incorporating active differential remote sensing. As the TPS54010 only has a positive VSENSE input, this circuit compensates for voltage drops in both the output voltage rail and the return (GND). The difference amplifier of U2 forces the output of the TPS54010 to generate an output voltage that maintains a constant 1.5-V difference between +1.5V_REMOTE_SENSE and –1.5V_REMOTE_SENSE.

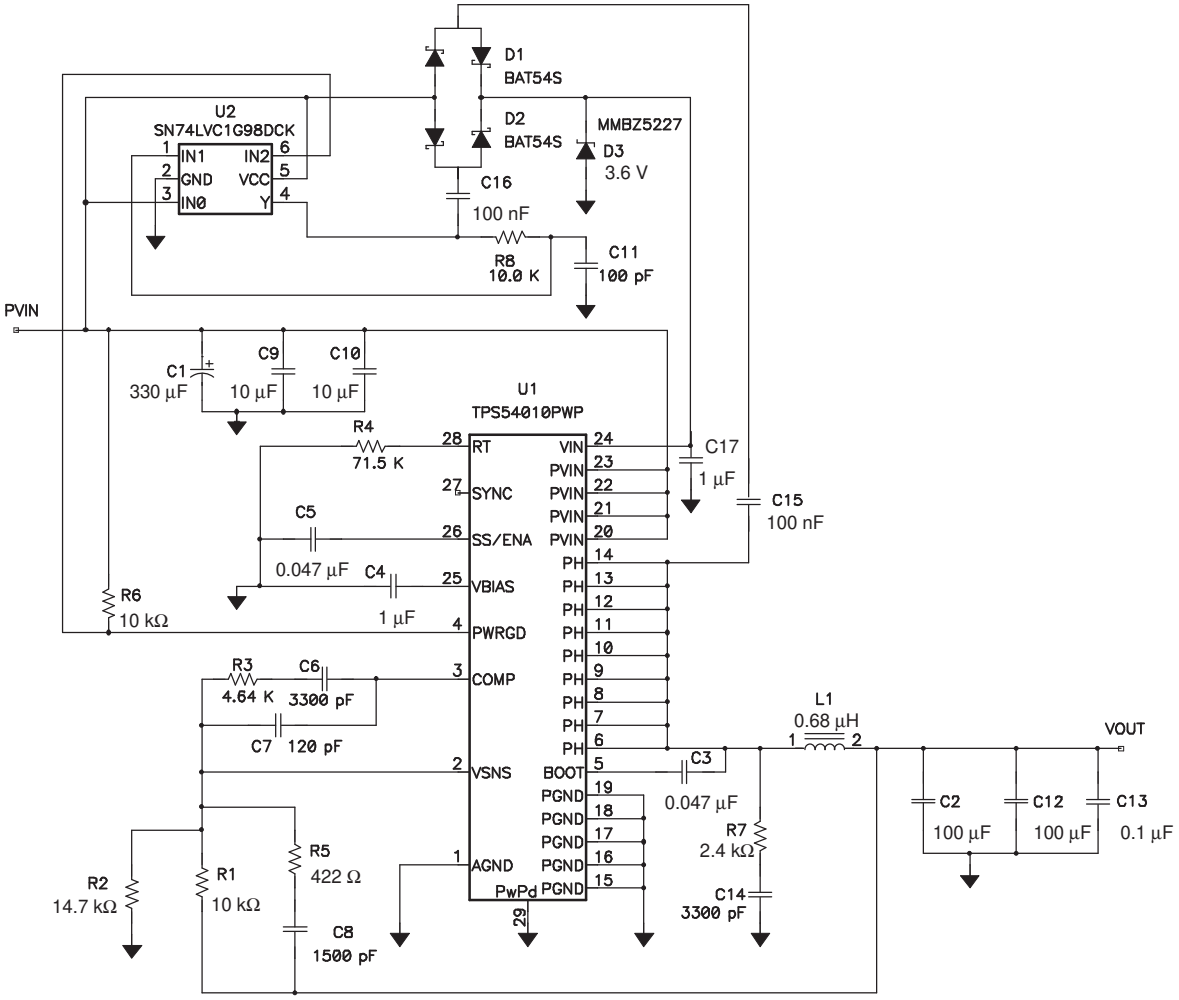



**Figure 14. 2.5 V To 1.5 V Power Supply With Charge Pump**

If a suitable 3-V to 4-V source is not available for the VIN supply, a charge pump may be used to boost the PVIN voltage. In this circuit, the charge pump is used to boost a 2.5-V source to a nominal 3.6 V.

### 8.2.3 Application Curves: Circuit in Figure 11

The performance data for Figure 15 through Figure 23 are for the circuit in Figure 11. Conditions are $P_{VIN}$ = 2.5 V, $V_{IN}$ = 3.3 V, $V_O$ = 1.5 V, $f_s$ = 700 kHz, and $I_O$ = 7 A, $T_A$ = 25°C, unless otherwise specified.

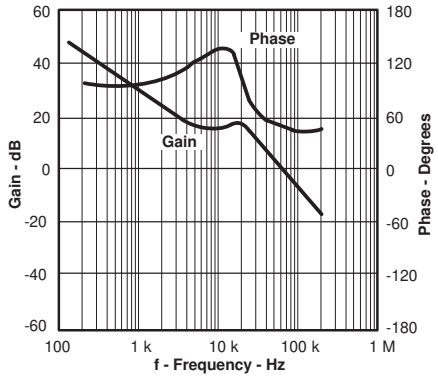



**Figure 15. Measured Loop Response vs Frequency**

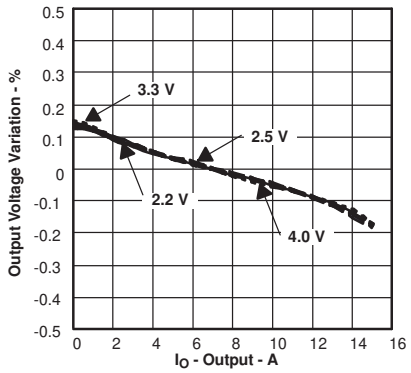



**Figure 16. Load Regulation vs Output Current**

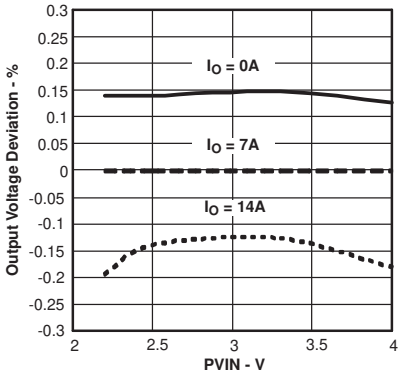



**Figure 17. Line Regulation vs Input Voltage**

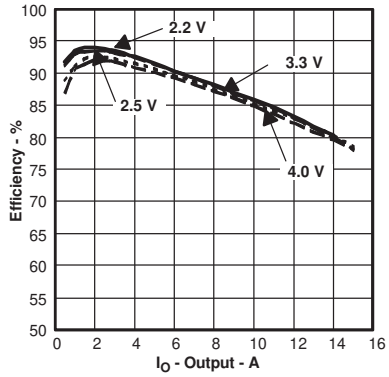



**Figure 18. Efficiency vs Output Current**

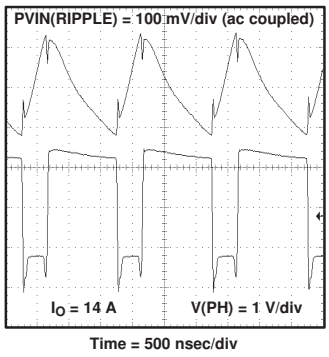



**Figure 19. Input Ripple Voltage**

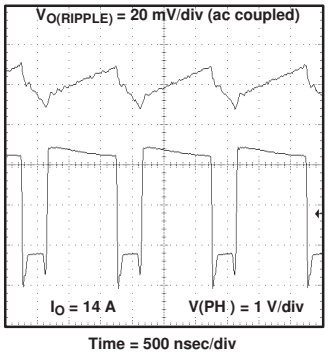



**Figure 20. Output Voltage Ripple**

The performance data for Figure 15 through Figure 23 are for the circuit in Figure 11. Conditions are $P_{VIN}$ = 2.5 V, $V_{IN}$ = 3.3 V, $V_O$ = 1.5 V, $f_s$ = 700 kHz, and $I_O$ = 7 A, $T_A$ = 25°C, unless otherwise specified.

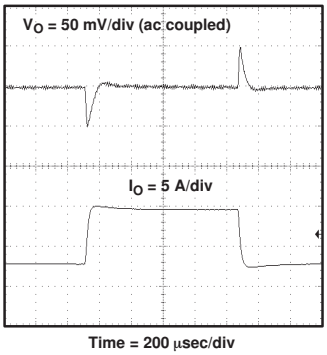



**Figure 21. Load Transient Response**

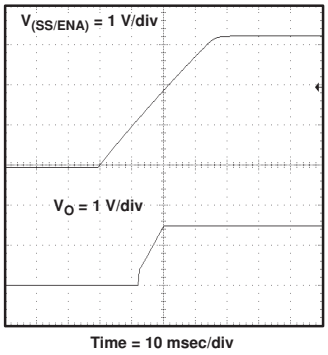



**Figure 22. Start-Up Waveform Output Voltage Relative To Enable**

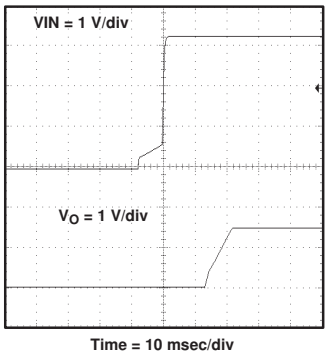
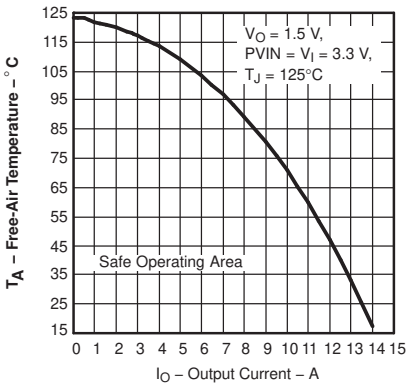



**Figure 23. Start-Up Waveform Output Voltage Relative To VIN**

The performance data for Figure 15 through Figure 23 are for the circuit in Figure 11. Conditions are $P_{VIN}$ = 2.5 V, $V_{IN}$ = 3.3 V, $V_O$ = 1.5 V, $f_s$ = 700 kHz, and $I_O$ = 7 A, $T_A$ = 25°C, unless otherwise specified.

### 8.2.4 Application Curves: Circuit in Figure 12

The performance data for Figure 24 through Figure 33 are for the circuit in Figure 12. Conditions are $P_{VIN}$ = 2.5 V, $V_{IN}$ = 3.3 V, $V_O$ = 1.5 V, $f_s$ = 700 kHz, and $I_O$ = 7 A, $T_A$ = 25°C, unless otherwise specified.




Note: Figure 25 applies to the application circuit (Figure 13) installed on a 3 inch x 3 inch x 0.062 inch four-layer PCB.

**Figure 24. Free-Air Temperature vs Maximum Output Current**

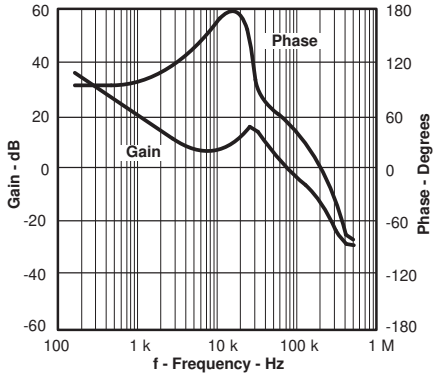



**Figure 25. Measured Loop Response vs Frequency**

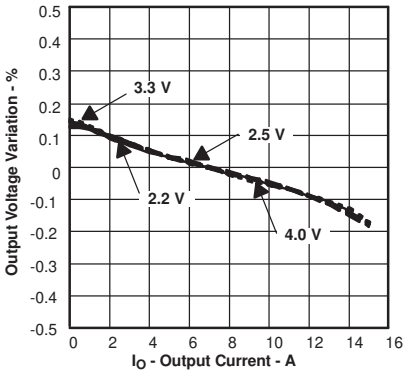



**Figure 26. Load Regulation vs Output Current**

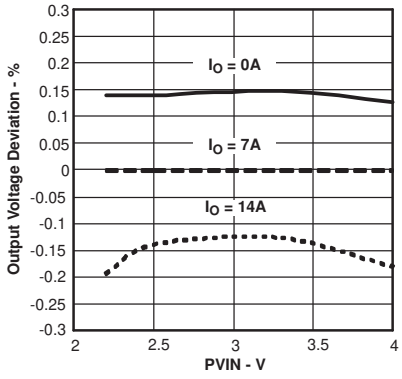



**Figure 27. Line Regulation vs Pvin**

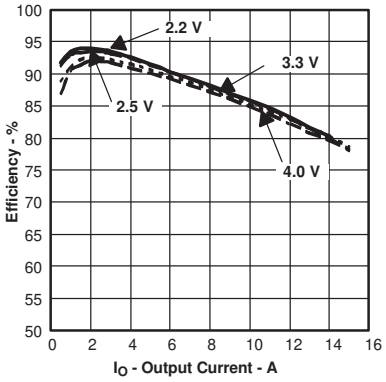



**Figure 28. Efficiency vs Output Current**

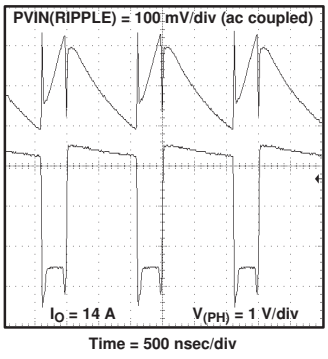



**Figure 29. Input Ripple Voltage**

The performance data for Figure 24 through Figure 33 are for the circuit in Figure 12. Conditions are $P_{VIN}$ = 2.5 V, $V_{IN}$ = 3.3 V, $V_O$ = 1.5 V, $f_s$ = 700 kHz, and $I_O$ = 7 A, $T_A$ = 25°C, unless otherwise specified.

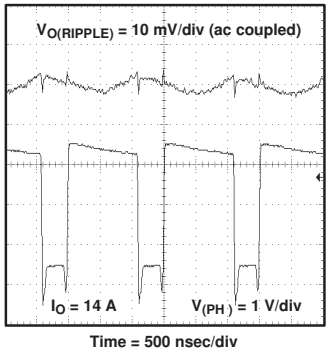



**Figure 30. Output Voltage Ripple**

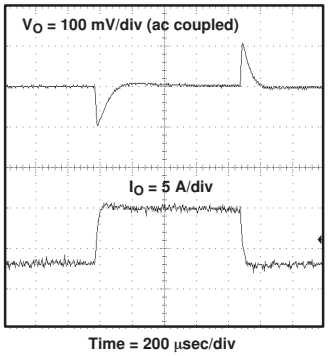



**Figure 31. Load Transient Response**

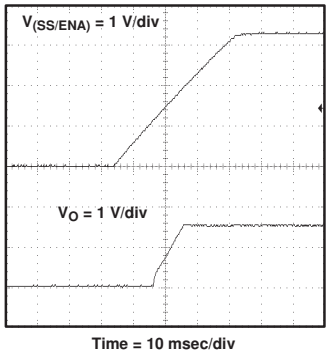



**Figure 32. Start-Up Waveform Output Voltage Relative to Enable**

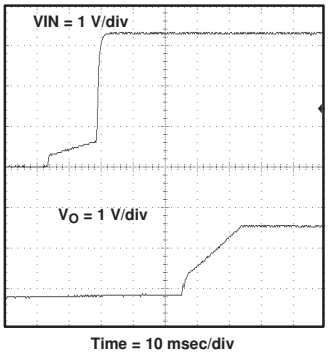



**Figure 33. Start-Up Waveform Output Voltage Relative to Enable**

# 9 Layout

## 9.1 PCB Layout

The PVIN pins are connected together on the printed- circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Take care to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the TPS54010 ground pins. The minimum recommended bypass capacitance is a 10-µF ceramic capacitor with a X5R or X7R dielectric. The optimum placement is as close as possible to the PVIN pins, the AGND, and PGND pins. See Figure 35 for an example of a board layout. If the VIN is connected to a separate source supply, it is bypassed with its own capacitor. There is an area of ground on the top layer of the PCB, directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors. The AGND and PGND pins are tied to the PCB ground by connecting them to the ground area under the device as shown in Figure 35. Use a separate wide trace for the analog ground signal path. This analog ground is used for the voltage set point divider, timing resistor RT, slow-start capacitor, and bias capacitor grounds. The PH pins are tied together and routed to the output inductor. Because the PH connection is the switching node, an inductor is located close to the PH pins, and the area of the PCB conductor is minimized to prevent excessive capacitive coupling. Connect the boot capacitor between the phase node and the BOOT pin as shown in Figure 35. Keep the boot capacitor close to the IC, and minimize the conductor trace lengths. Connect the output filter capacitor(s) between the VOUT trace and PGND. It is important to keep the loop formed by the PH pins, Lout, Cout, and PGND as small as is practical. Place the compensation components from the VOUT trace to the VSENSE and COMP pins. Do not place these components too close to the PH trace. Due to the size of the IC package and the device pinout, they must be routed close, but maintain as much separation as possible while keeping the layout compact. Connect the bias capacitor from the VBIAS pin to analog ground using the isolated analog ground trace. If a slow-start capacitor or RT resistor is used, or if the SYNC pin is used to select 350-kHz operating frequency, connect them to this trace.

For operation at full rated load current, the analog ground plane must provide an adequate heat-dissipating area. A 3-inch by 3-inch plane of 1-ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD must be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available must be used when 6-A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer must be made using 0.013-inch diameter vias to avoid solder wicking through the vias.

Eight vias must be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the twelve recommended that enhance thermal performance must be included in areas not under the device package.

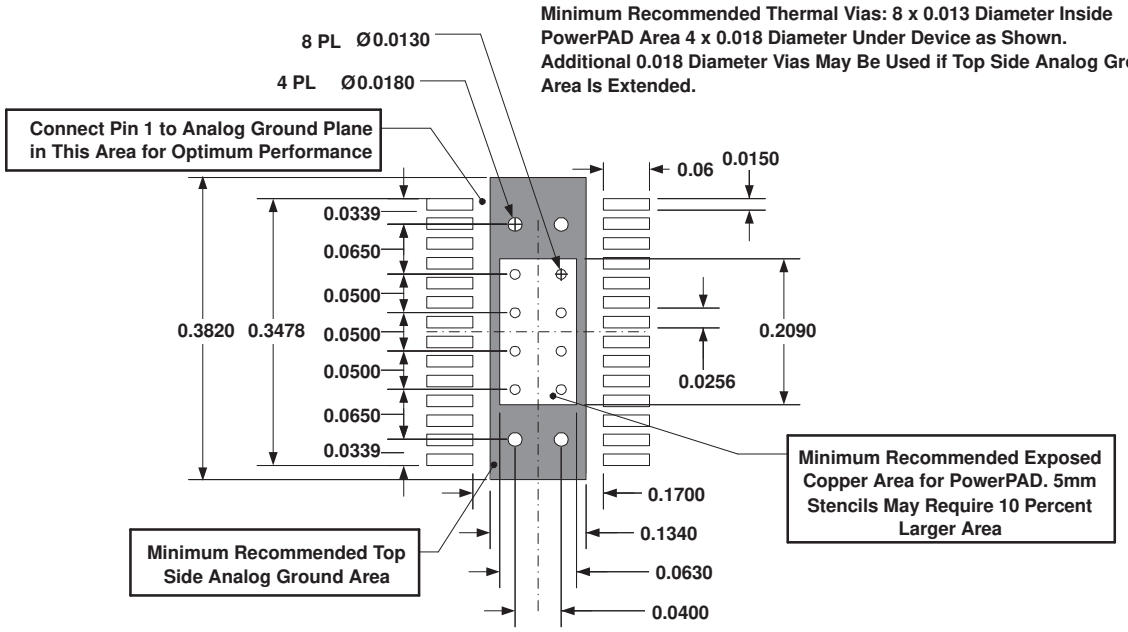



**Figure 34. Recommended Land Pattern for 28-Pin PWP PowerPAD**

## 9.2 Layout Example

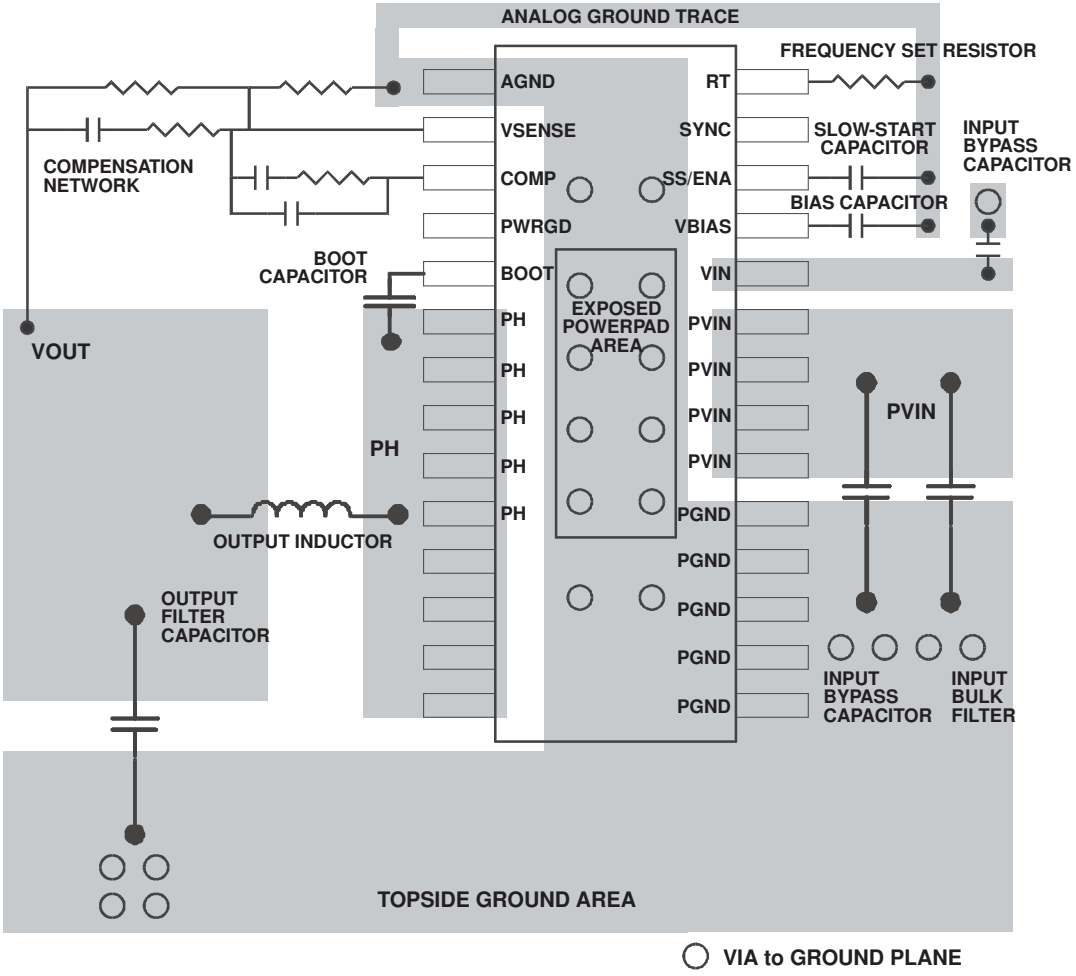



**Figure 35. TPS54010 Layout**

# 10 器件和文档支持

## 10.1 器件支持

### 10.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

## 10.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 10.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 10.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.

## 10.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS54010PWP | ACTIVE | HTSSOP | PWP | 28 | 50 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS54010 | Samples |
| TPS54010PWPG4 | ACTIVE | HTSSOP | PWP | 28 | 50 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS54010 | Samples |
| TPS54010PWPR | ACTIVE | HTSSOP | PWP | 28 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS54010 | Samples |
| TPS54010PWPRG4 | ACTIVE | HTSSOP | PWP | 28 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS54010 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

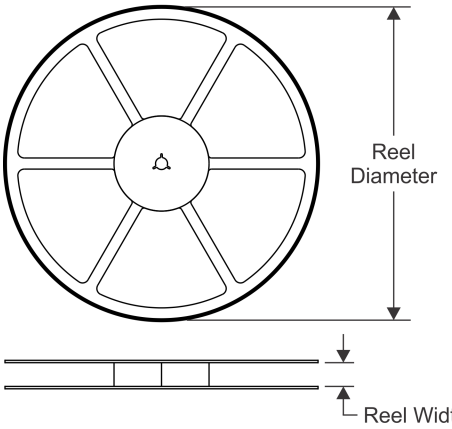
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

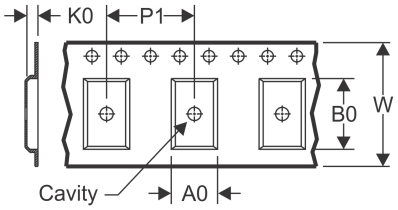
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

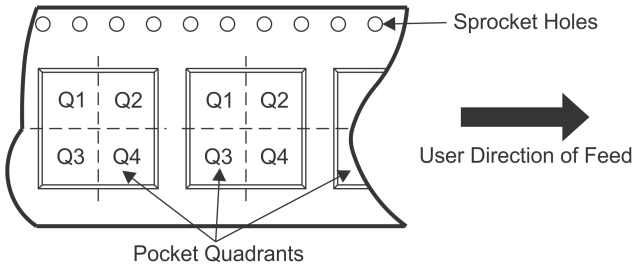



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

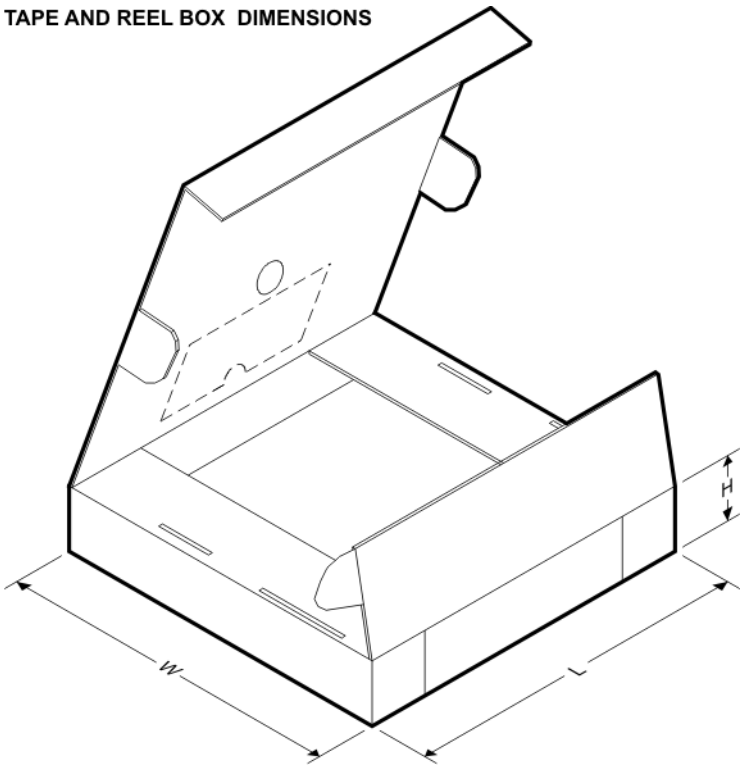
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS54010PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

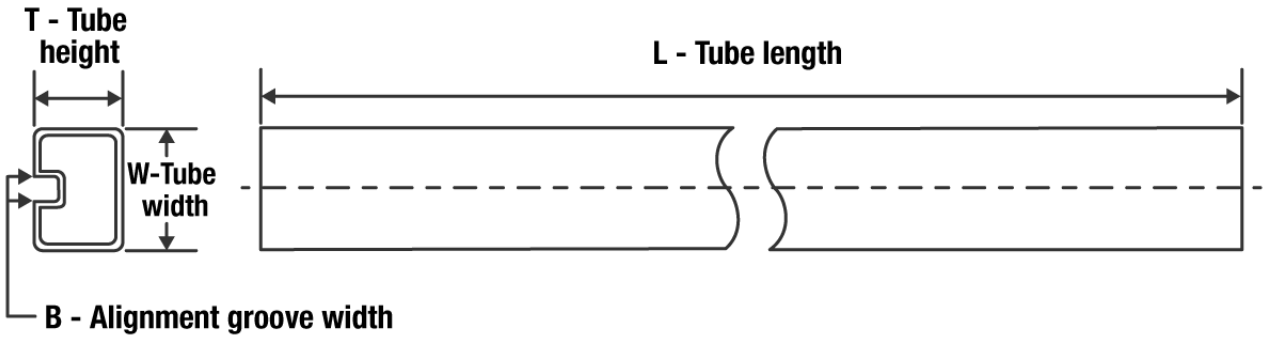
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS54010PWPR | HTSSOP | PWP | 28 | 2000 | 350.0 | 350.0 | 43.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TPS54010PWP | PWP | HTSSOP | 28 | 50 | 530 | 10.2 | 3600 | 3.5 |
| TPS54010PWPG4 | PWP | HTSSOP | 28 | 50 | 530 | 10.2 | 3600 | 3.5 |

# GENERIC PACKAGE VIEW

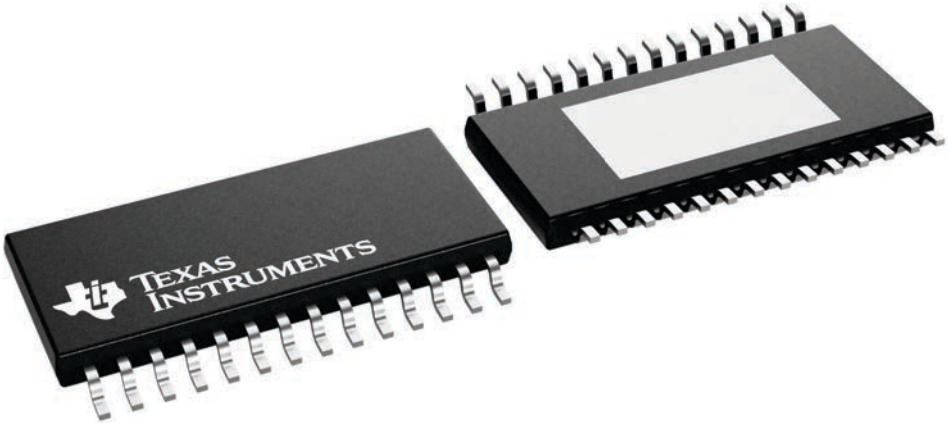
## PWP 28

## PowerPAD™ TSSOP - 1.2 mm max height

**4.4 x 9.7, 0.65 mm pitch**

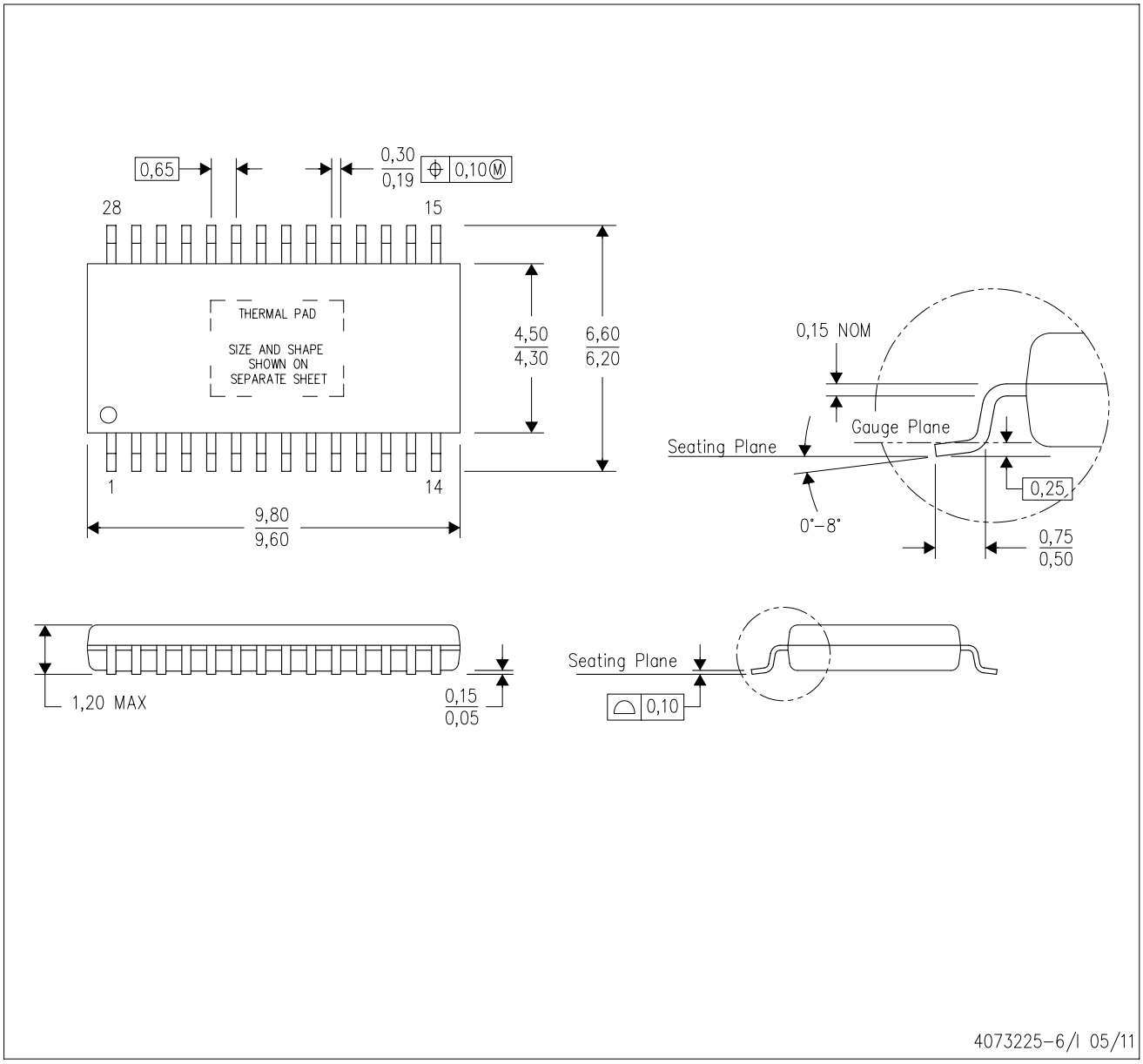
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

**PowerPAD is a trademark of Texas Instruments.**

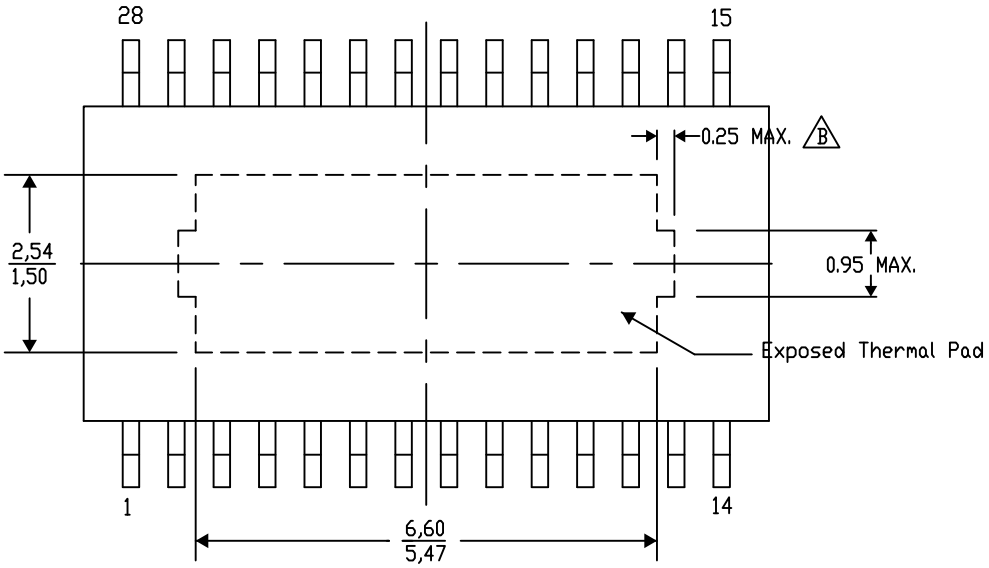
# PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

4206332–40/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

# 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265