Multioutput Power Management Solution with Four Buck Switching and Three LDO Linear Regulators with I²C

FEATURES

- **Quad I²C Adjustable High Efficiency Step-Down DC/DC Converters: 2.5A, 2.5A, 1.5A, 1.5A**
- **Three 300mA LDO Regulators (Two Adjustable)**
- **Independent Enable Pin-Strap or I²C Sequencing**
- **Programmable Autonomous Power-Down Control**
- Warnings and Faults
- $\overline{IRQ}$ Pin and IRQ Status Register
- Power Good Pin and Status Register
- 150°C T_J Operation (LT3380H)
- Dynamic Voltage Scaling
- Selectable 2.25MHz or 1.12MHz Switching Frequency
- 12µA Standby Current
- Side Wettable 40-Lead 6mm × 6mm QFN Package

APPLICATIONS

- Automotive
- Industrial
- Communications
- General Purpose Multichannel Power Supplies

DESCRIPTION

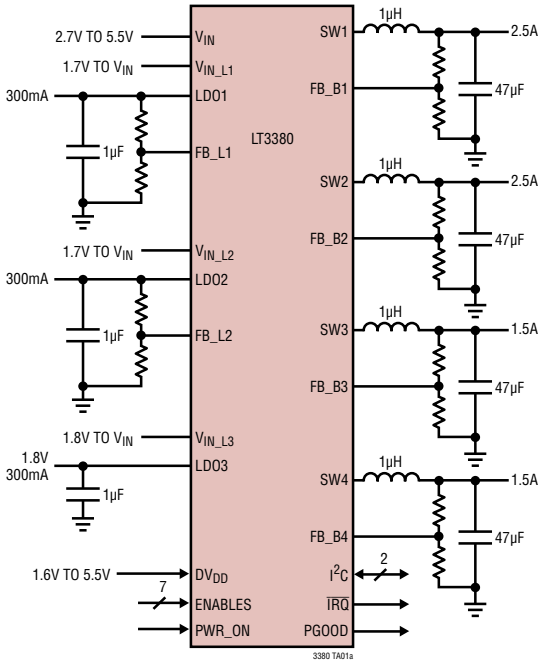
The LT®3380 is a complete power management solution for advanced portable application processor-based systems. The device contains four synchronous step-down DC/DC converters for core, memory, I/O, and system on-chip (SoC) rails and three 300mA LDO regulators for low noise analog supplies. An I²C serial port may be used to control regulator enables, power-down sequencing, output voltage levels, dynamic voltage scaling, operating modes, and status reporting.

Regulator start-up is sequenced by connecting outputs to enable pins in the desired order or via the I²C port. The LT3380 outputs may be sequenced off in one of four time slots selected using I²C command registers.

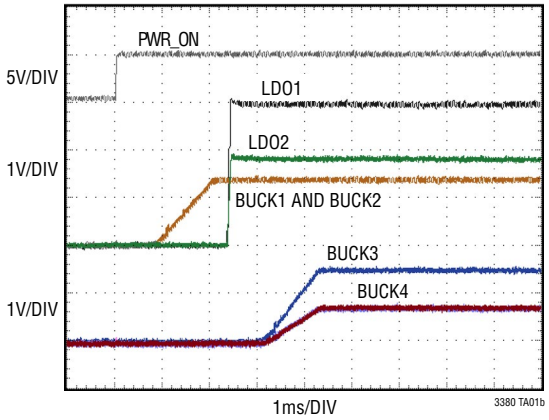
The device is available in a 40-lead 6mm × 6mm QFN with wettable flanks for optical inspection.

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TYPICAL APPLICATION



Start-Up Sequence

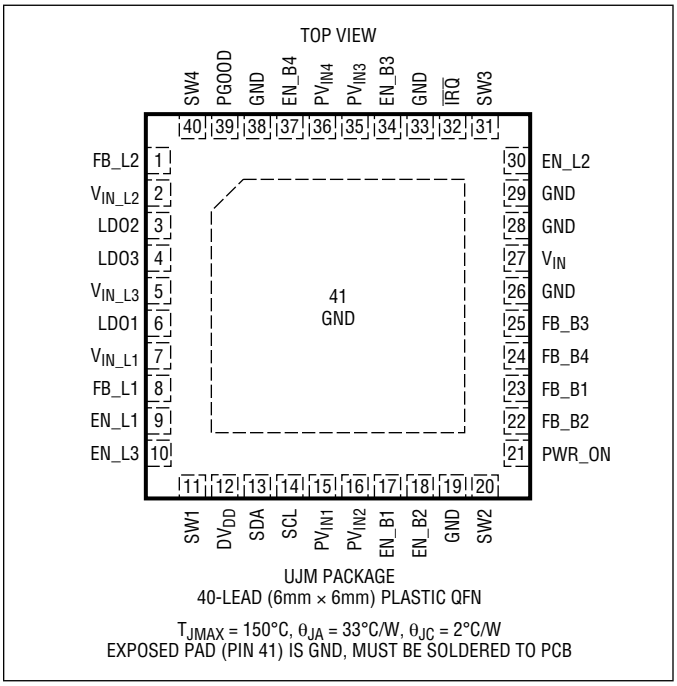


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, DV_{DD} ..... –0.3V to 6V
PV_{IN1}, PV_{IN2}, PV_{IN3}, PV_{IN4} ..... V_{IN} – 0.3V to V_{IN} + 0.3V
V_{IN_L1}, V_{IN_L2}, V_{IN_L3} ..... –0.3V to V_{IN} + 0.3V
LDO1, FB_L1, LDO2, FB_L2, LDO3, FB_B1, FB_B2, FB_B3, FB_B4, PGOOD, EN_B1, EN_B2, EN_B3, EN_B4, EN_L1, EN_L2, EN_L3, PWR_ON, $\overline{IRQ}$ ..... –0.3V to 6V
SDA, SCL ..... –0.3V to DV_{DD} + 0.3V
Operating Junction Temperature Range (Notes 2, 3) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UJM PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 33°C/W, θ_{JC} = 2°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3380EUJM#PBF	LT3380EUJM#TRPBF	LT3380UJM	40-Lead Plastic Side Wettable QFN (6mm × 6mm)	–40°C to 125°C
LT3380IUJM#PBF	LT3380IUJM#TRPBF	LT3380UJM	40-Lead Plastic Side Wettable QFN (6mm × 6mm)	–40°C to 125°C
LT3380HUJM#PBF	LT3380HUJM#TRPBF	LT3380UJM	40-Lead Plastic Side Wettable QFN (6mm × 6mm)	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT3380IUJM#WPBF	LT3380IUJM#WTRPBF	LT3380UJM	40-Lead Plastic Side Wettable QFN (6mm × 6mm)	–40°C to 125°C
LT3380HUJM#WPBF	LT3380HUJM#WTRPBF	LT3380UJM	40-Lead Plastic Side Wettable QFN (6mm × 6mm)	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = PV_{IN1} = PV_{IN2} = PV_{IN3} = PV_{IN4} = V_{IN_L1} = V_{IN_L2} = V_{IN_L3} = DV_{DD} = 3.8V. All regulators disabled unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Input Supply Voltage, V_{IN}		●	2.7		5.5	V
V_{IN} Standby Current	PWR_ON = 0V	●		12	21	µA
V_{IN} Undervoltage Fault Rising (Note 7) V_{IN} Undervoltage Fault Falling		● ●	 2.35	2.55 2.45	2.65	V V
V_{IN} Undervoltage Warning Falling	CNTRL[4:2] = 000 (POR Default) CNTRL[4:2] = 001 CNTRL[4:2] = 010 CNTRL[4:2] = 011 CNTRL[4:2] = 100 CNTRL[4:2] = 101 CNTRL[4:2] = 110 CNTRL[4:2] = 111			2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4		V V V V V V V V
Step-Down Switching Regulators 1, 2, 3 and 4						
Output Voltage Range		●	V_{FB}		PV_{IN}	V
Burst Mode® V_{IN} Quiescent Current Pulse-Skipping Mode V_{IN} Quiescent Current Forced Continuous V_{IN} Quiescent Current	V_{FB_Bx} = 850mV (Note 5) V_{FB_Bx} = 850mV (Note 5) V_{FB_Bx} = 0V (Note 5)	● ● ●		23 120 170	50 200 300	µA µA µA
Feedback Pin Input Current	V_{FB_Bx} = 850mV		–0.05		0.05	µA
Maximum Duty Cycle	V_{FB_Bx} = 0V	●	100			%
Minimum Duty Cycle		●		18	24	%
SW Pull-Down Resistance	Regulator Disabled			625		Ω
Feedback Reference Soft-Start Rate	(Note 6)			0.8		V/ms
High Feedback Regulation Voltage (V_{FB})	DVBxA[4:0] = DVBxB[4:0] = 11111, V_{IN} = 2.7V to 5.5V	●	788	800	812	mV
Default Feedback Regulation Voltage (V_{FB})	DVBxA[4:0] = DVBxB[4:0] = 11001, V_{IN} = 2.7V to 5.5V	●	714	725	736	mV
Low Feedback Regulation Voltage (V_{FB})	DVBxA[4:0] = DVBxB[4:0] = 00000, V_{IN} = 2.7V to 5.5V	●	404	412.5	421	mV
Feedback LSB Step Size				12.5		mV
Switching Frequency	BUCKx[2] = 0 BUCKx[2] = 1	● ●	1.7 0.85	2.25 1.125	2.7 1.35	MHz MHz
1.5A Step-Down Switching Regulators 3 and 4						
PMOS Current Limit		●	2.0			A
PMOS On-Resistance				160		mΩ
NMOS On-Resistance				80		mΩ
2.5A Step-Down Switching Regulators 1 and 2						
PMOS Current Limit		●	3.0			A
PMOS On-Resistance				120		mΩ
NMOS On-Resistance				70		mΩ
LDO Regulators 1, 2 and 3						
Feedback Reference Soft-Start Rate				10		V/ms
Output Pull-Down Resistance	Regulator Disabled			625		Ω
LDO Regulators 1 and 2						
V_{IN_Lx} Input Voltage		●	1.7		V_{IN}	V
Output Voltage Range	I_{LDO} = 0mA		V_{FB}		V_{IN_Lx}	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = PV_{IN1} = PV_{IN2} = PV_{IN3} = PV_{IN4} = V_{IN_L1} = V_{IN_L2} = V_{IN_L3} = DV_{DD} = 3.8V. All regulators disabled unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Available Output Current		●	300			mA
V_{IN_Lx} Quiescent Current V_{IN_Lx} Shutdown Current	Regulator Enabled, I_{LDO} = 0A Regulator Disabled	● ●		12 0	25 1	µA µA
V_{IN} Quiescent Current	Regulator Enabled	●		50	85	µA
Feedback Regulation Voltage		●	0.707	0.725	0.743	V
Line Regulation	I_{LDO} =1mA, V_{IN} = 2.7V to 5.5V			0.01		%/V
Load Regulation	I_{LDO} = 1mA to 300mA			0.01		%
Short-Circuit Current Limit					770	mA
Dropout Voltage (Note 4)	I_{LDO} = 300mA, V_{LDO} = 2.5V I_{LDO} = 300mA, V_{LDO} = 1.2V			210 450	260 615	mV mV
Feedback Pin Input Current	V_{FB_Lx} = 725mV		–0.05		0.05	µA
LDO Regulator 3						
V_{IN_L3} Input Voltage		●	2.35		V_{IN}	V
Output Voltage	I_{LDO} = 1mA	●	1.746	1.8	1.854	V
Available Output Current		●	300			mA
V_{IN_L3} Quiescent Current V_{IN_L3} Shutdown Current	Regulator Enabled, I_{LDO} = 0A Regulator Disabled	● ●		14 0	25 1	µA µA
V_{IN} Quiescent Current	Regulator Enabled	●		50	85	µA
Line Regulation	I_{LDO} =1mA, V_{IN} = 2.7V to 5.5V			0.01		%/V
Load Regulation	I_{LDO} = 1mA to 300mA			0.05		%
Short-Circuit Current Limit					770	mA
Dropout Voltage (Note 4)	I_{LDO} = 300mA, V_{LDO} = 1.8V			280	350	mV
Enable Inputs						
Threshold Rising	All Enables Low	●		0.75	1.2	V
Threshold Falling	One Enable High	●	0.4	0.7		V
Precision Threshold	One or More Regulators Previously Enabled	●	0.370	0.400	0.430	V
Input Pull-Down Resistance				4.5		MΩ
PWR_ON						
Threshold		●	0.370	0.400	0.430	V
Pull-Down Resistance				4.5		MΩ
PWR_ON High to Allow Enables Delay				3		ms
PWR_ON High to Inhibit Enables Delay				3		ms
Inhibit Enable Time from PWR_ON Low				1		s
Status Output Pins (PGOOD, $\overline{IRQ}$)						
$\overline{IRQ}$ Output Low Voltage	$I_{\overline{IRQ}}$ = 3mA			0.1	0.4	V
$\overline{IRQ}$ Output High Leakage Current	$I_{\overline{IRQ}}$ = 3.8mA		–0.1		0.1	µA
PGOOD Output Low Voltage	I_{PGOOD} = 3mA			0.1	0.4	V
PGOOD Output High Leakage Current	V_{PGOOD} = 3.8V		–0.1		0.1	µA
PGOOD Threshold Rising PGOOD Threshold Falling				–6 –8		% %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = PV_{IN1} = PV_{IN2} = PV_{IN3} = PV_{IN4} = V_{IN_L1} = V_{IN_L2} = V_{IN_L3} = DV_{DD} = 3.8V. All regulators disabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I²C Port							
DV_{VDD}	DV_{DD} Input Supply Voltage		●	1.6		5.5	V
I_{DVDD}	DV_{DD} Quiescent Current	SCL/SDA = 0kHz			0.3	1	µA
DV_{VDD_UVLO}	DV_{DD} UVLO Level				1		V
ADDRESS	LT3380 Device Address				0111100[R/$\overline{W}$]		
V_{IH}	SDA/SCL Input Threshold Rising				70		$\%DV_{DD}$
V_{IL}	SDA/SCL Input Threshold Falling				30		$\%DV_{DD}$
I_{IH}	SDA/SCL High Input Current	SDA = SCL = 5.5V		–1	0	1	µA
I_{IL}	SDA/SCL Low Input Current	SDA = SCL = 0V		–1	0	1	µA
V_{OL_SDA}	SDA Output Low Voltage	I_{SDA} = 3mA				0.4	V
f_{SCL}	Clock Operating Frequency					400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition			1.3			µs
$t_{HD, STA}$	Hold Time After Repeated Start Condition			0.6			µs
$t_{SU, STA}$	Repeated Start Condition Setup Time			0.6			µs
$t_{SU, STO}$	Stop Condition Setup Time			0.6			µs
$t_{HD, DAT(0)}$	Data Hold Time Output			0		900	ns
$t_{SU, DAT}$	Data Setup Time			100			ns
t_{LOW}	SCL Clock Low Period			1.3			µs
t_{HIGH}	SCL Clock High Period			0.6			µs
t_f	Clock/Data Fall Time	C_B = Capacitance of BUS Line (pF)		$20 + 0.1C_B$		300	ns
t_r	Clock/Data Rise Time	C_B = Capacitance of BUS Line (pF)		$20 + 0.1C_B$		300	ns
t_{SP}	Input Spike Suppression Pulse Width					50	ns

Note 1: Stresses beyond those listed Under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3380 is tested under pulsed load conditions such that $T_J \approx T_A$. The LT3380E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3380I is guaranteed over the –40°C to 125°C operating junction temperature range and the LT3380H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D, in Watts), and package to junction ambient thermal impedance (θJ_A in Watts/°C) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$.

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The LT3380 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Dropout voltage is defined as ($V_{IN_Lx} – V_{LDOx}$) when V_{LDOx} is 3% lower than V_{LDOx} measured with V_{IN} = V_{IN_Lx} = 4.3V.

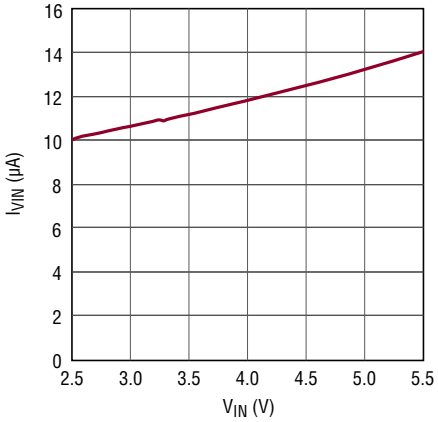
Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 6: Soft-Start measured in test mode with regulator error amplifier in unity-gain mode.

Note 7: The LT3380 will operate before V_{IN} has risen higher than V_{IN} undervoltage fault rising (2.65V max) but will shutdown if V_{IN} does not cross the rising threshold in less than 5 seconds. Please refer to the Operation section.

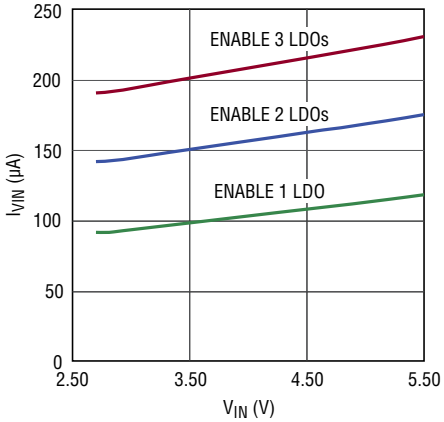
TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.8V, T_A = 25°C unless otherwise noted

Standby I_{VIN} vs V_{IN}



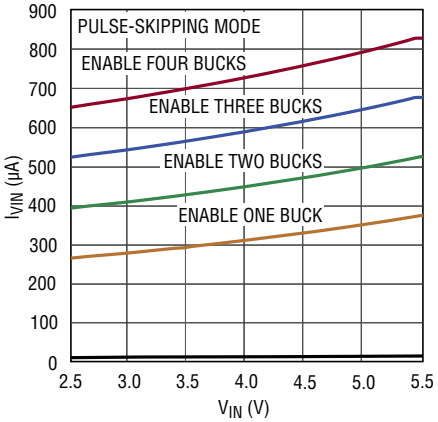
3380 G01

LDO1 to LDO3 I_{VIN} vs V_{IN}



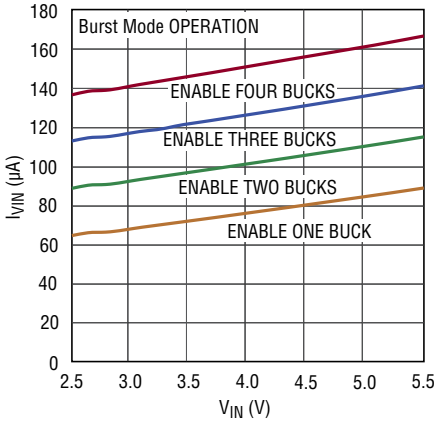
3380 G02

Step-Down Switching Regulator I_{VIN} vs V_{IN}



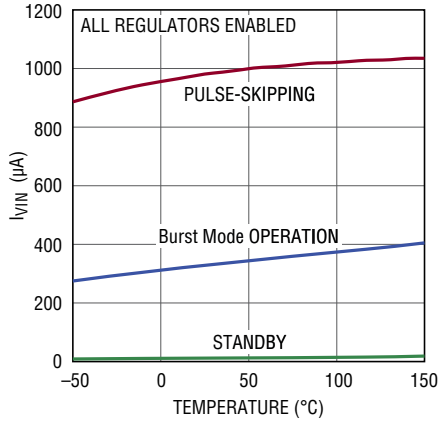
3380 G03

Step-Down Switching Regulator I_{VIN} vs V_{IN}



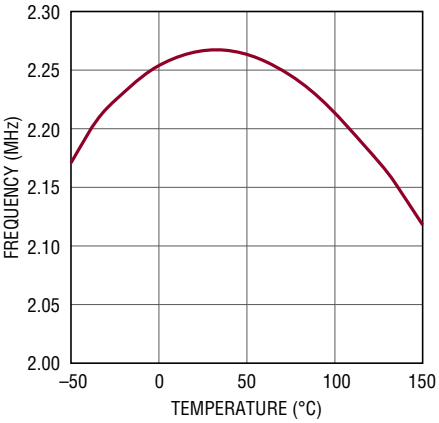
3380 G04

Input Supply Current vs Temperature



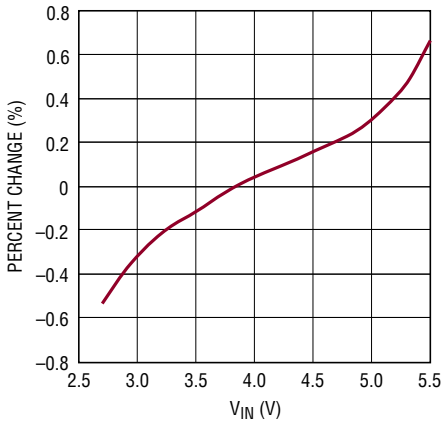
3380 G05

Oscillator Frequency vs Temperature



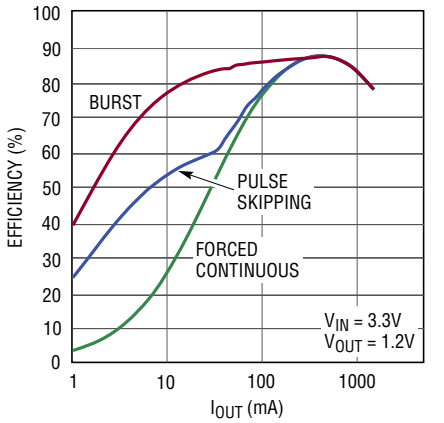
3380 G06

Oscillator Frequency Change vs V_{IN}



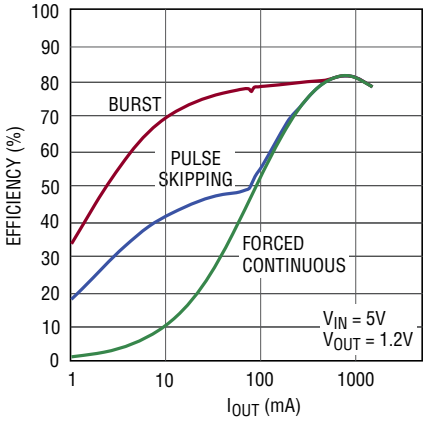
3380 G07

Step-Down Switching Regulators 3 and 4 Efficiency vs I_{OUT}



3380 G08

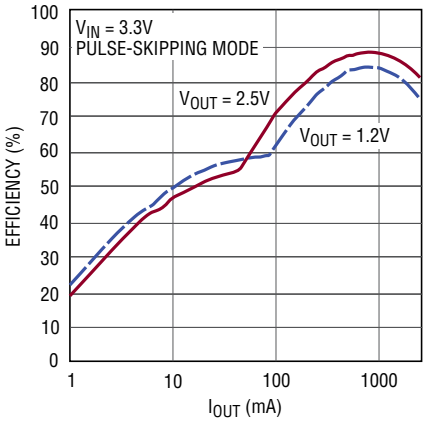
Step-Down Switching Regulators 3 and 4 Efficiency vs I_{OUT}



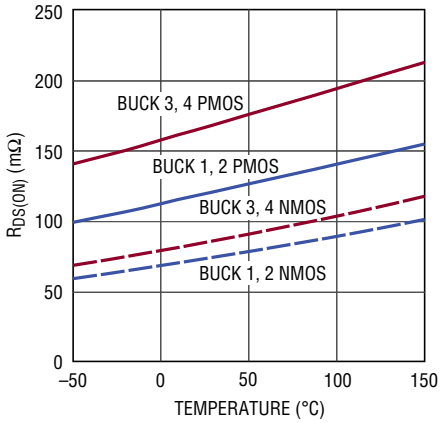
3380 G09

TYPICAL PERFORMANCE CHARACTERISTICS

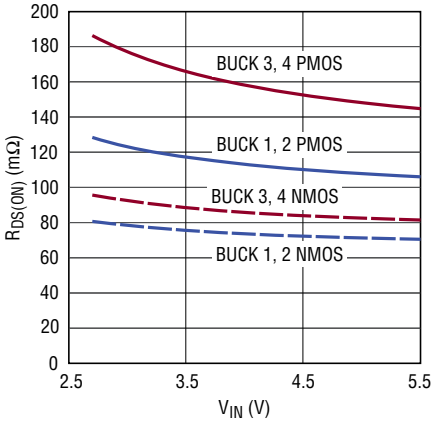
Step-Down Switching Regulators 1 and 2 Efficiency vs I_{OUT}



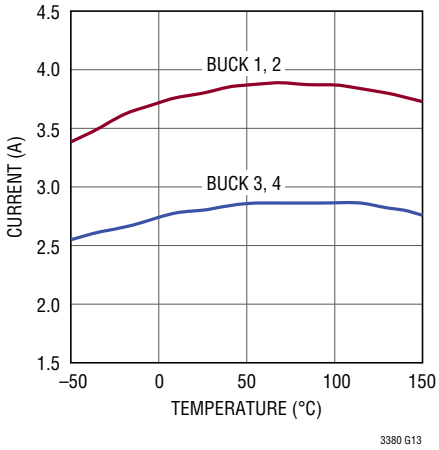
Buck $R_{DS(ON)}$ vs Temperature



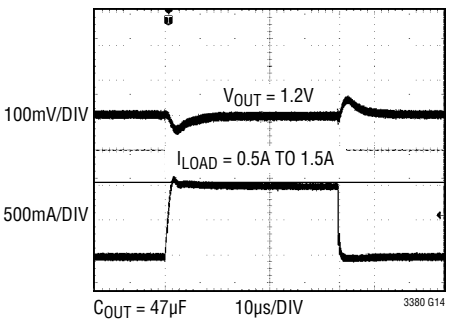
Buck $R_{DS(ON)}$ vs V_{IN}



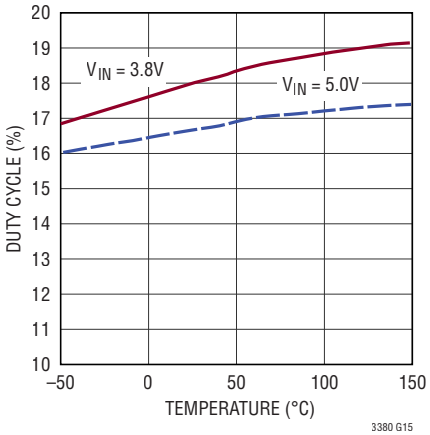
Step-Down Switching Regulator Current Limit vs Temperature



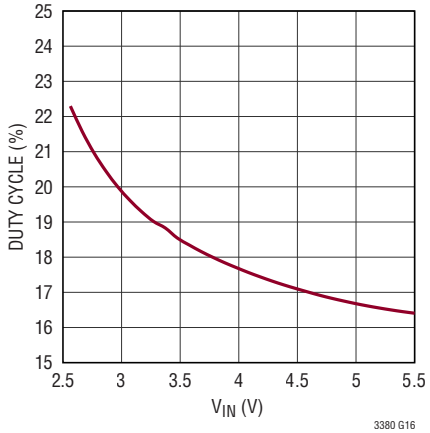
Step-Down Switching Regulator Load Step



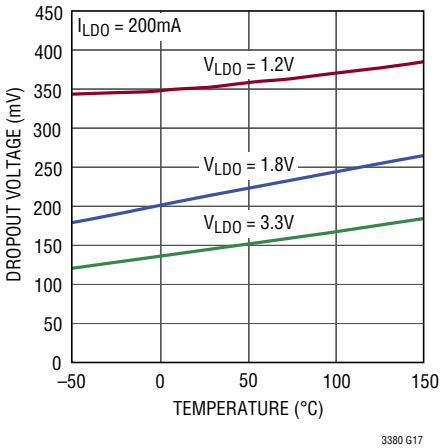
Buck Minimum Duty Cycle vs Temperature



Buck Minimum Duty Cycle vs V_{IN}

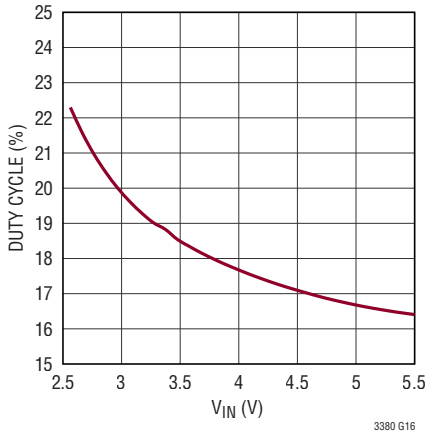


LDO1 to LDO3 Dropout Voltage vs Temperature

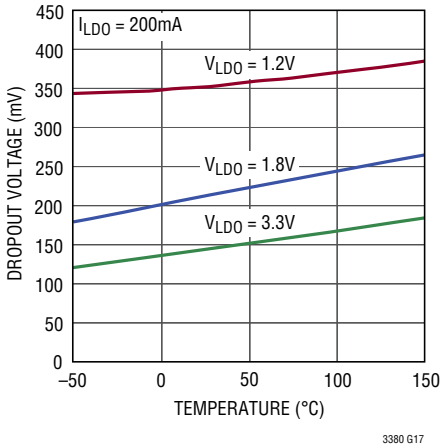


TYPICAL PERFORMANCE CHARACTERISTICS

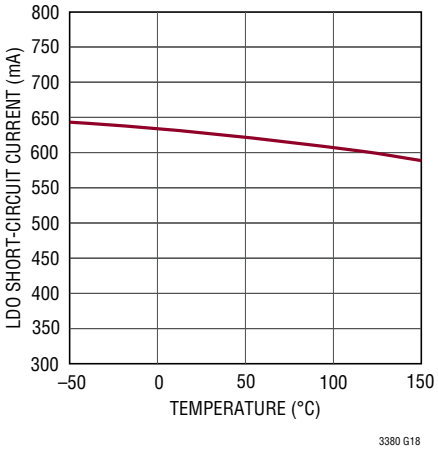
Buck Minimum Duty Cycle vs V_{IN}



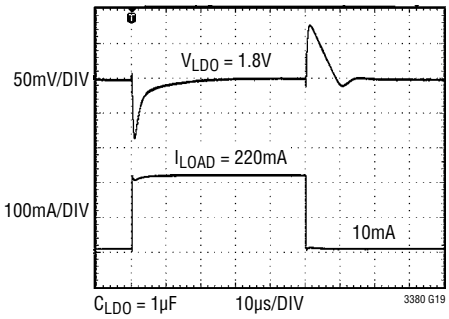
LDO1 to LDO3 Dropout Voltage vs Temperature



LDO1 to LDO3 Short-Circuit Current vs Temperature



LDO1 to LDO3 Load Step Response



PIN FUNCTIONS

FB_L2 (Pin 1): Feedback Input for LDO2. Set output voltage using a resistor divider connected from LDO2 to this pin to ground.

V_{IN_L2} (Pin 2): Power Input for LDO2. This pin should be bypassed to ground with a 1µF or greater ceramic capacitor. Voltage on V_{IN_L2} should not exceed voltage on V_{IN} pin.

LDO2 (Pin 3): Output Voltage of LDO2. Nominal output voltage is set with a resistor feedback divider that servos to a fixed 725mV reference. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

LDO3 (Pin 4): Output Voltage of LDO3. Nominal output voltage is a fixed 1.8V. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

V_{IN_L3} (Pin 5): Power Input for LDO3. This pin should be bypassed to ground with a 1µF or greater ceramic capacitor. Voltage on V_{IN_L3} should not exceed voltage on V_{IN} pin.

LDO1 (Pin 6): Output Voltage of LDO1. Nominal output voltage is set with a resistor feedback divider that servos to a fixed 725mV reference. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

V_{IN_L1} (Pin 7): Power Input for LDO1. This pin should be bypassed to ground with a 1µF or greater ceramic capacitor. Voltage on V_{IN_L1} should not exceed voltage on V_{IN} pin.

FB_L1 (Pin 8): Feedback Input for LT3380 LDO1. Set output voltage using a resistor divider connected from LDO1 to this pin to ground.

EN_L1 (Pin 9): Enable LDO1 Input for LT3380. Active high enables LDO1. A weak pull-down pulls EN_L1 low when left floating.

EN_L3 (Pin 10): Enable LDO3 Input. Active high enables LDO3. A weak pull-down pulls EN_L3 low when left floating.

SW1 (Pin 11): Switch Pin for Step-Down Switching Regulator 1. Connect one side of step-down switching regulator 1 inductor to this pin.

DV_{DD} (Pin 12): Supply Voltage for I^2C Serial Port. This pin sets the logic reference level of SCL and SDA I^2C pins. DV_{DD} resets I^2C registers to power-on state when driven to <1V. SCL and SDA logic levels are scaled to DV_{DD}. Connect a 0.1µF decoupling capacitor from this pin to ground.

SDA (Pin 13): Data Pin for the I^2C Serial Port. The I^2C logic levels are scaled with respect to DV_{DD}.

SCL (Pin 14): Clock Pin for the I^2C Serial Port. The I^2C logic levels are scaled with respect to DV_{DD}.

PV_{IN1} (Pin 15): Power Input for Step-Down Switching Regulator 1. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 10µF or greater ceramic capacitor.

PV_{IN2} (Pin 16): Power Input for Step-Down Switching Regulator 2. Tie this pin to the V_{IN} supply. This pin should be bypassed to ground with a 10µF or greater ceramic capacitor.

EN_B1 (Pin 17): Enable Step-Down Switching Regulator 1. Active high input enables step-down switching regulator 1. A weak pull-down pulls EN_B1 low when left floating.

EN_B2 (Pin 18): Enable Step-Down Switching Regulator 2. Active high input enables step-down switching regulator 2. A weak pull-down pulls EN_B2 low when left floating.

GND (Pins 19/26/28/29/33/38): Ground.

SW2 (Pin 20): Switch Pin for Step-Down Switching Regulator 2. Connect one side of step-down switching regulator 2 inductor to this pin.

PWR_ON (Pin 21): Power On. PWR_ON is a master enable and disable input. When low, PWR_ON inhibits the regulator enable pins. When high, PWR_ON allows enable pin operation.

FB_B2 (Pin 22): Feedback Input for Step-Down Switching Regulator 2. Set output voltage using resistor divider connected from the output of step-down switching regulator 2 to this pin to ground.

PIN FUNCTIONS

FB_B1 (Pin 23): Feedback Input for Step-Down Switching Regulator 1. Set output voltage using resistor divider connected from the output of step-down switching regulator 1 to this pin to ground.

FB_B4 (Pin 24): Feedback Input for Step-Down Switching Regulator 4. Set output voltage using resistor divider connected from the output of step-down switching regulator 4 to this pin to ground.

FB_B3 (Pin 25): Feedback Input for Step-Down Switching Regulator 3. Set output voltage using resistor divider connected from the output of step-down switching regulator 3 to this pin to ground.

V_{IN} (Pin 27): Supply Voltage Input. This pin should be bypassed to ground with a 1µF or greater ceramic capacitor. All switching regulator PV_{IN} supplies should be tied to V_{IN}.

EN_L2 (Pin 30): Enable LDO2 Input. Active high enables LDO2. A weak pull-down pulls EN_L2 low when left floating.

SW3 (Pin 31): Switch Pin for Step-Down Switching Regulator 3. Connect one side of step-down switching regulator 3 inductor to this pin.

$\overline{IRQ}$ (Pin 32): Interrupt Request Output. Open-drain driver is pulled low for power good, undervoltage, and overtemperature warning and fault conditions. Clear $\overline{IRQ}$ by writing to the I^2C CLIRQ command register.

EN_B3 (Pin 34): Enable Step-Down Switching Regulator 3. Active high input enables step-down switching regulator 3. A weak pull-down pulls EN_B3 low when left floating.

PV_{IN3} (Pin 35): Power Input for Step-Down Switching Regulator 3. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 10µF or greater ceramic capacitor.

PV_{IN4} (Pin 36): Power Input for Step-Down Switching Regulator 4. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 10µF or greater ceramic capacitor.

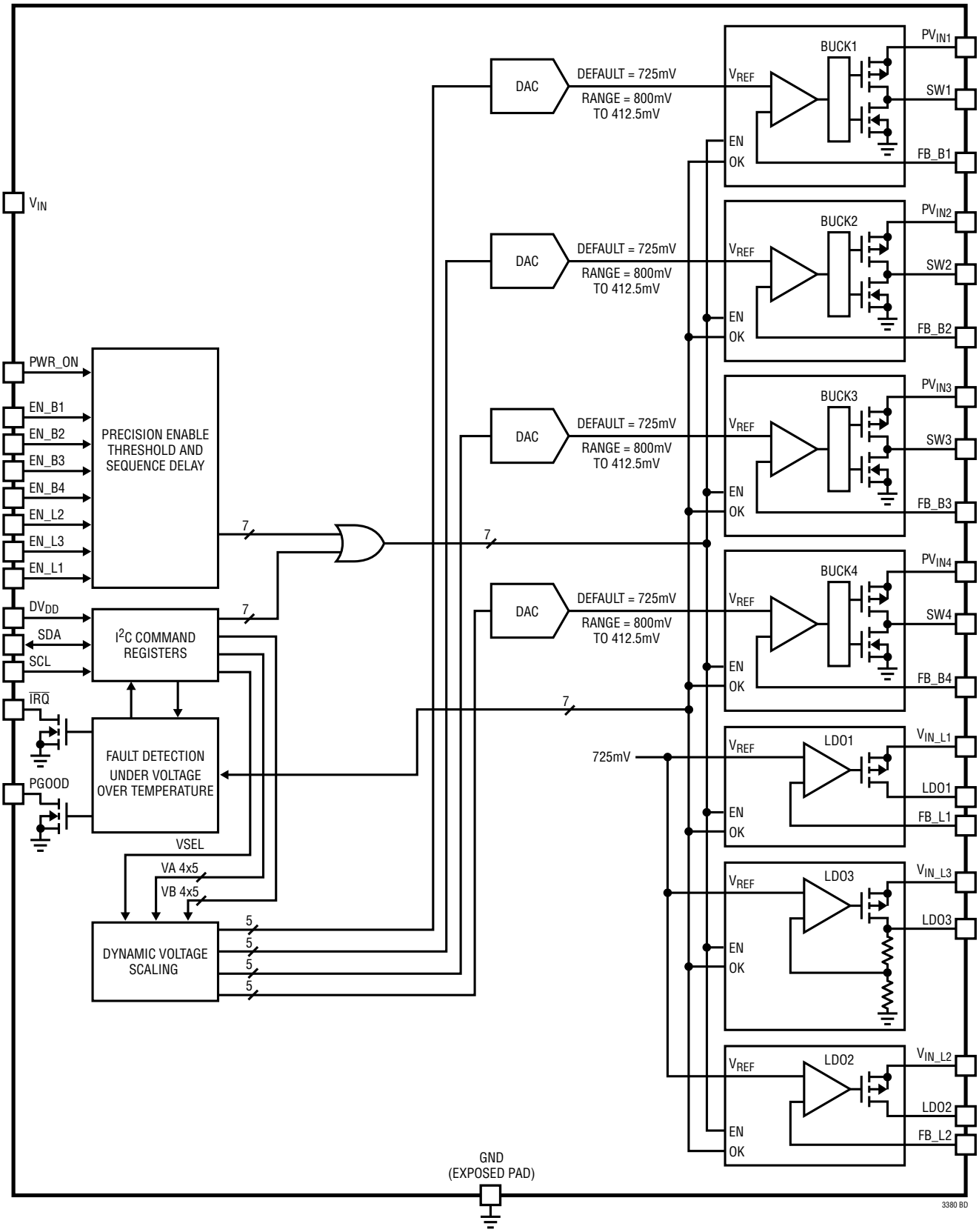
EN_B4 (Pin 37): Enable Step-Down Switching Regulator 4. Active high enables step-down switching regulator 4. A week pull-down pulls EN_B4 low when left floating.

PGOOD (Pin 39): Power Good Output. Open-drain output pulls low when any enabled regulator falls below power good threshold or during dynamic voltage slew unless disabled in command register. Pulls low when all regulators are disabled.

SW4 (Pin 40): Switch Pin for Step-Down Switching Regulator 4. Connect one side of step-down switching regulator 4 inductor to this pin.

GND (Exposed Pad Pin 41): Ground. The exposed pad must be connected to a continuous ground plane of the printed circuit board by multiple interconnect vias directly under the LT3380 to maximize electrical and thermal conduction.

BLOCK DIAGRAM



OPERATION

INTRODUCTION

The LT3380 is a multi-topology, multiple output voltage regulator. It generates a total of seven voltage rails. Supplying the voltage rails are, two 2.5A step-down regulators, two 1.5A step-down regulators, and three 300mA low dropout regulators. Supporting the multiple regulators is a highly configurable power-on sequencing capability, dynamic voltage scaling DAC output voltage control, and extensive status and interrupt outputs.

300mA Low Dropout Regulators

Three LDO regulators on the LT3380 will each deliver up to 300mA output. Each LDO regulator has a separate input supply to help manage power loss in the LDO output devices. The LDO regulators are enabled by pin input or I²C command register. When disabled, the regulator outputs are pulled to ground through a 625Ω resistor. A low ESR 1µF ceramic capacitor should be tied from the LDO output to ground. The 300mA LDO regulators have current limit control circuits. The LDO input voltages, V_{IN_L1}, V_{IN_L2}, and V_{IN_L3} must be at a potential of V_{IN} or less.

The LDO regulator I²C command register controls are shown in Table 1.

LT3380 Resistor Programmable LDO1 and LDO2

LDO1 and LDO2 output voltages are programmed by resistor dividers tied from the LDO output pin to the feedback pin as shown in Figure 1. The output voltage is calculated using the following formula:

$$V_{LDO} = \left(1 + \frac{R1}{R2}\right) \bullet (725)\,(mV)$$

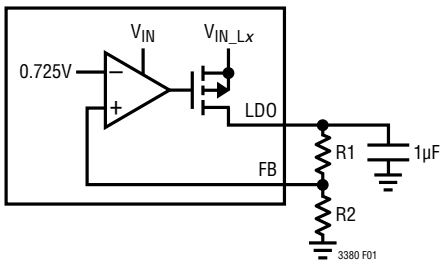


Figure 1. LDO1 and LDO2 Application Circuit

Table 1. LDO Control Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
LDOA[0]	0* 1	Do Not Keep Alive LDO2 in Standby Keep Alive LDO2 in Standby
LDOA[1]	0* 1	Enable LDO2 at Any Output Voltage Enable LDO2 Only if Output Voltage is <300mV
LDOA[2]	0* 1	LDO2 Disabled if EN_L2 is Low LDO2 Enable
LDOA[3]	0* 1	Do Not Keep Alive LDO3 in Standby Keep Alive LDO3 in Standby
LDOA[4]	0* 1	Enable LDO3 at Any Output Voltage Enable LDO3 Only if Output Voltage is <300mV
LDOA[5]	0* 1	LDO3 Disabled if EN_L3 is Low LDO3 Enabled
LDOB[0]	0* 1	Do Not Keep Alive LDO1 in Standby Keep Alive LDO1 in Standby
LDOB[1]	0* 1	Enable LDO1 at Any Output Voltage Enable LDO1 Only if Output Voltage is <300mV
LDOB[2]	0* 1	LDO1 Disabled if EN_L1 is Low LDO1 Enabled

*denotes default power-on value

STEP-DOWN SWITCHING REGULATORS

The LT3380 contains four buck regulators. Two of the buck regulators are capable of delivering up to 2.5A load current and the other two can deliver up to 1.5A each. The regulators have forward and reverse current limiting, soft-start, and switch slew rate control for lower radiated EMI.

The LT3380 buck regulators are capable of 100% duty cycle, or dropout, regulation. When in dropout the regulator output voltage is equal to PV_{IN} minus the load current times $R_{DS(ON)}$ of the converters PMOS device and inductor DCR.

Each buck regulator is enabled using its enable pin or I²C command register control. Operating modes, start-up option, reference voltage, and switch slew rate are controlled using the I²C port.

The buck converter I²C command register controls are shown in Table 2, Table 3, Table 4, and Table 5.

OPERATION

Table 2. Buck1 Control Command Register

COMMAND REGISTER[BIT]	VALUE	SETTING
BUCK1[0]	0* 1	Switch Slew Rate Normal Switch Slew Rate Fast
BUCK1[1]	0* 1	Do Not Keep Enabled in Device Standby Keep Enabled in Device Standby
BUCK1[2]	0* 1	Switching Frequency 2.25MHz Switching Frequency 1.125MHz
BUCK1[3]	0* 1	Clock Phase 1 Clock Phase 2
BUCK1[4]	0* 1	Enable at Any Output Voltage Enable Only if Output Voltage Is <300mV
BUCK1[6:5]	00* 01 10	Pulse-Skipping Mode Burst Mode Operation Forced Continuous Mode
BUCK1[7]	0* 1	Buck1 Disabled if EN_B1 Pin Is Low Buck1 Enabled

*denotes default power-on value

Table 3. Buck2 Control Command Register

COMMAND REGISTER[BIT]	VALUE	SETTING
BUCK2[0]	0* 1	Switch Slew Rate Normal Switch Slew Rate Fast
BUCK2[1]	0* 1	Do Not Keep Enabled in Device Standby Keep Enabled in Device Standby
BUCK2[2]	0* 1	Switching Frequency 2.25MHz Switching Frequency 1.125MHz
BUCK2[3]	0* 1	Clock Phase 1 Clock Phase 2
BUCK2[4]	0* 1	Enable at Any Output Voltage Enable Only if Output Voltage Is <300mV
BUCK2[6:5]	00* 01 10	Pulse-Skipping Mode Burst Mode Operation Forced Continuous Mode
BUCK2[7]	0* 1	Buck2 Disabled if EN_B2 Pin Is Low Buck2 Enabled

*denotes default power-on value

Table 4. Buck3 Control Command Register

COMMAND REGISTER[BIT]	VALUE	SETTING
BUCK3[0]	0* 1	Switch Slew Rate Normal Switch Slew Rate Fast
BUCK3[1]	0* 1	Do Not Keep Enabled in Device Standby Keep Enabled in Device Standby
BUCK3[2]	0* 1	Switching Frequency 2.25MHz Switching Frequency 1.125MHz
BUCK3[3]	0* 1	Clock Phase 1 Clock Phase 2
BUCK3[4]	0* 1	Enable at Any Output Voltage Enable Only if Output Voltage Is <300mV
BUCK3[6:5]	00* 01 10	Pulse-Skipping Mode Burst Mode Operation Forced Continuous Mode
BUCK3[7]	0* 1	Buck3 Disabled if EN_B3 Pin Is Low Buck3 Enabled

*denotes default power-on value

Table 5. Buck4 Control Command Register

COMMAND REGISTER[BIT]	VALUE	SETTING
BUCK4[0]	0* 1	Switch Slew Rate Normal Switch Slew Rate Fast
BUCK4[1]	0* 1	Do Not Keep Enabled in Device Standby Keep Enabled in Device Standby
BUCK4[2]	0* 1	Switching Frequency 2.25MHz Switching Frequency 1.125MHz
BUCK4[3]	0* 1	Clock Phase 1 Clock Phase 2
BUCK4[4]	0* 1	Enable at Any Output Voltage Enable Only if Output Voltage Is <300mV
BUCK4[6:5]	00* 01 10	Pulse-Skipping Mode Burst Mode Operation Forced Continuous Mode
BUCK4[7]	0* 1	Buck4 Disabled if EN_B4 Pin Is Low Buck4 Enabled

*denotes default power on-value

OPERATION

Operating Modes

The buck regulators operate in either pulse-skipping, Burst Mode operation, or forced continuous mode. In pulse-skipping mode the regulator will skip pulses at light load but operates at constant frequency at higher loads. When set in Burst Mode operation, the regulator runs in PWM mode at high current load and Burst Mode operation at lower current load. In forced continuous setting the inductor current is allowed to be less than zero over the full range of duty cycles. In forced continuous operation the buck regulator has the ability to sink output current. Because the regulator is switching every cycle regardless of output load, forced continuous mode results in the least output voltage ripple at light load.

Output Voltage Programming

Each of the step-down converters uses a dynamically slewing DAC for its reference. The output voltage of the DAC reference is selectable using a 5-bit I²C command register. The output voltage is set by using a resistor divider connected from the step-down switching regulator output to its feedback pin as shown in Figure 2. The output voltage is calculated using the following formula:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \bullet (DVBx \bullet 12.5 + 412.5)\ (mV)$$

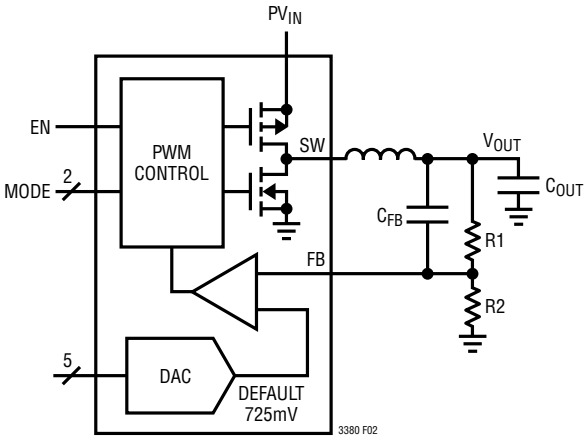


Figure 2. Step-Down Switching Regulator Application Circuit

DVBx is the decimal value of the 5-bit binary number in the I²C command registers. The default DAC input code is 11001 (25 in decimal) which corresponds to a reference voltage of 725mV. Typical values for R1 are in the range of 40k to 1M. Capacitor C_{FB} cancels the pole created by the feedback resistors and the input capacitance on the FB pin and helps to improve load step transient response. A value of 10pF is recommended.

Inductor Selection

The choice of step-down switching regulator inductor influences the efficiency and output voltage ripple of the converter. A larger inductor improves efficiency since the peak current is closer to the average output current. Larger inductors generally have higher series resistance that counters the efficiency advantage of reduced peak current.

Inductor ripple current is a function of switching frequency, inductance, V_{IN}, and V_{OUT} as shown in this equation:

$$\Delta I_L = \frac{1}{f \bullet L} \bullet V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A good starting design point is to use an inductor that gives ripple equal to 30% of the maximum output current. Select an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure the inductor does not saturate.

Input and Output Capacitor Selection

Low ESR ceramic capacitors should be used at both the output and input supply of the switching regulators. Only X5R or X7R ceramic capacitors should be used since they have better temperature and voltage stability than other ceramic types.

Operating Frequency

The switching frequency of each of the LT3380 switching regulators may be set using the I²C command registers. The default switching frequency is 2.25MHz and the selectable frequency is 1.125MHz. Operation at lower frequency improves efficiency by reducing internal gate charge and switching losses at the expense of a larger inductor.

OPERATION

The maximum V_{IN} to V_{OUT} ratio at which the step-down converter can maintain constant frequency operation in regulation is determined by the minimum duty cycle. If the duty cycle required falls below the minimum duty cycle of the converter, the output voltage ripple will increase as the converter skips cycles to maintain regulation. By setting LT3380 command register bits BUCK1[2], BUCK2[2], BUCK3[2], or BUCK4[2], the switching frequency of a regulator may be halved to accommodate a high V_{IN} to V_{OUT} ratio.

Phase Selection

To reduce the cycle-by-cycle peak current drawn by the switching regulators, the clock phase at which each of the LT3380 buck's PMOS switch turns on can be set using I^2C command register settings (see Figure 3).

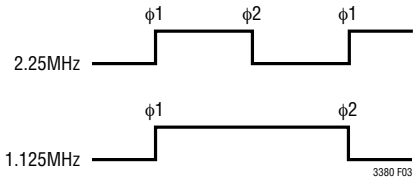


Figure 3. Phase Settings Full- and Half-Speed Buck Clock

Switch Slew Rate Control

To help reduce EMI the switch rise time of each buck regulator is slew limited by default. A faster setting is selectable using the I^2C buck command registers. The faster setting will improve efficiency if limited edge rate is not required.

Soft-Start

To reduce inrush current at start-up each buck regulator soft starts when enabled. When enabled the internal reference voltage is ramped from ground to the level of the slewing DAC output at a rate of 0.8V/ms. During soft-start the converter is forced to pulse-skipping mode regardless of command register mode settings.

SLEWING DAC REFERENCE OPERATION

Each LT3380 step-down switching regulators error amplifier reference voltage is supplied by a 5-bit DAC with an output voltage range of 412.5mV to 800mV in 12.5mV steps. One of two 5-bit codes stored in I^2C command registers is selected for input to the DAC. When a change in code is detected by the DAC control circuits, the output of the DAC is slewed at 3.5mV/µs to the new value.

Dynamic Voltage Scaling

Table 6 shows the command registers used to control dynamic voltage scaling (DVS) of the step-down switching regulators input reference DAC. The command register bits DVB1A[4:0] and DVB1B[4:0] store two 5-bit inputs to the DAC reference for Buck1. The bit stored in command register DVB1A[5] selects either the 5 bits stored in DVB1A[4:0] or DVB1B[4:0] DAC as input to the DAC reference. Buck2, Buck3, and Buck4 operate the same way using their assigned "A" and "B" command registers shown in Table 6.

Table 6. Buck1, Buck2, Buck3, and Buck4 Slewing DAC Control Command Registers

COMMAND REGISTER[BIT]	VALUE	SETTING
DVB1A[4:0]	bbbbb	Buck1 Reference DAC Input A
DVB1A[5]	0* 1	Select DVB1A[4:0] Select DVB1B[4:0]
DVB1B[4:0]	bbbbb	Buck1 Reference DAC Input B
DVB1B[5]	0* 1	Pull PGOOD Low Slewing Buck1 Do Not Pull PGOOD Slewing Buck1
DVB2A[4:0]	bbbbb	Buck2 Reference DAC Input A
DVB2A[5]	0* 1	Select DVB2A[4:0] Select DVB2B[4:0]
DVB2B[4:0]	bbbbb	Buck2 Reference DAC Input B
DVB2B[5]	0* 1	Pull PGOOD Low Slewing Buck2 Do Not Pull PGOOD Slewing Buck2
DVB3A[4:0]	bbbbb	Buck3 Reference DAC Input A
DVB3A[5]	0* 1	Select DVB3A[4:0] Select DVB3B[4:0]
DVB3B[4:0]	bbbbb	Buck3 Reference DAC Input B
DVB3B[5]	0* 1	Pull PGOOD Low Slewing Buck3 Do Not Pull PGOOD Slewing Buck3
DVB4A[4:0]	bbbbb	Buck4 Reference DAC Input A
DVB4A[5]	0* 1	Select DVB4A[4:0] Select DVB4B[4:0]
DVB4B[4:0]	bbbbb	Buck4 Reference DAC Input B
DVB4B[5]	0* 1	Pull PGOOD Low Slewing Buck4 Do Not Pull PGOOD Slewing Buck4

*denotes default power-on value

OPERATION

Command register bits DVB1B[5], DVB2B[5], DVB3B[5], and DVB4B[5] control whether the PGOOD status pin is pulled low while the DAC output is slewing. The default command register setting is to pull the PGOOD pin low during DAC slew. As shown in Figure 4, during the DVS, PGOOD will be held low for just the duration of the DVS and the PGSTAT register is not affected.

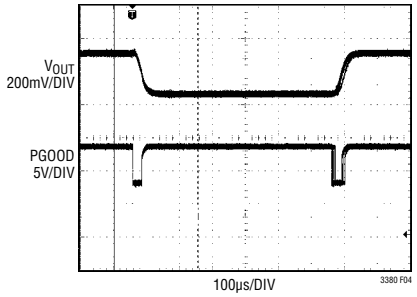


Figure 4. Dynamic Voltage Scaling

Operating Mode State Diagram

Figure 5 shows the state diagram of the LT3380 enable and sequence controller. First application of power to the V_{IN} pin brings the controller to the power-on reset/hard reset (POR/HRST) state. In this state the I^2C command registers have been set to their default values, and the device is waiting for PWR_ON inputs. Regulator enable pins and command register enable bits are ignored in the POR/HRST state. In the POR/HRST state V_{IN} draws typically 12µA.

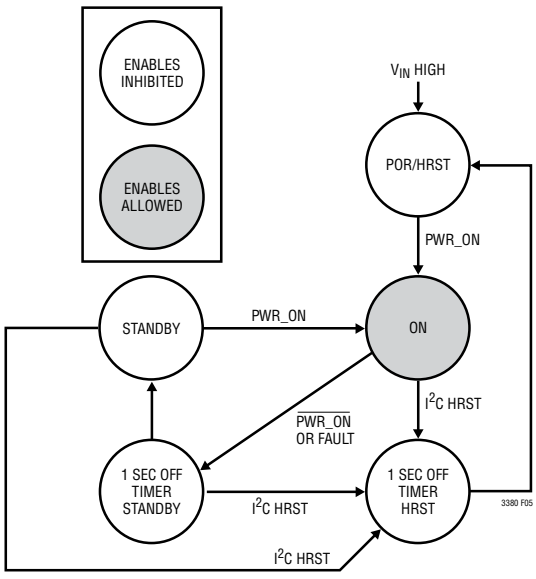


Figure 5. LT3380 Operating Mode State Diagram

PWR_ON Enable Control

The PWR_ON pin acts as a master enable pin by inhibiting or allowing all the individual regulator enable pins. A typical use is to drive PWR_ON with a power good status pin from a pre-regulator. Figure 6 shows the timing relationship between PWR_ON and inhibition of the enable pins.

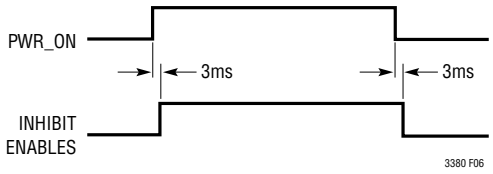


Figure 6. Power Up and Down with PWR_ON

POWER ON SEQUENCING

Enable Pin Operation

The LT3380 enable pins facilitate pin-strapping output rails to enable pins to up-sequence the LT3380 regulators in any order. Figure 7 shows an example of pin-strapped sequence connections. The enable pins normally have a 0.75V (typical) input voltage threshold.

If any enable is driven high, the remaining enable input thresholds switch to an accurate 400mV threshold. To ensure separation of the sequenced rails, there is a built-in 450µs delay from the enable pin threshold crossing to the internal enable of the regulator. Figure 8 shows the start-up timing of the example shown in Figure 7.

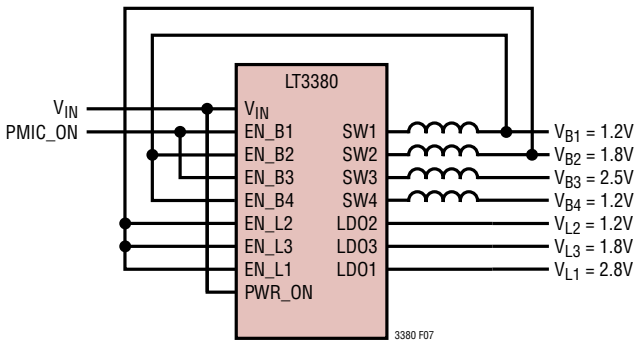


Figure 7. Pin-Strapped Power-On Sequence Application

OPERATION

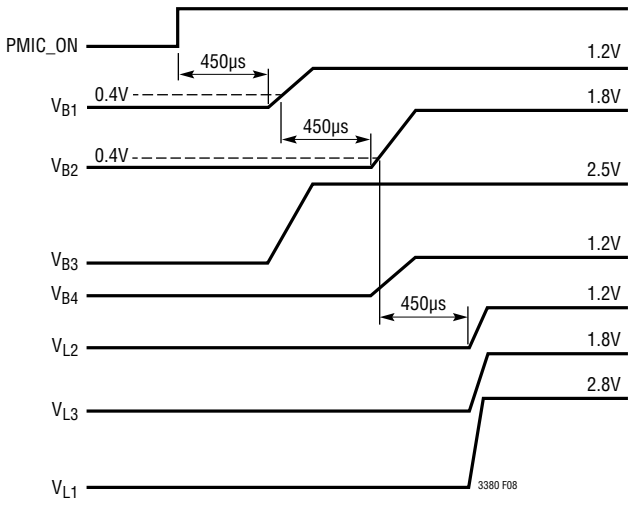


Figure 8. Pin-Strapped Power-On Sequence

Software Control Mode

Once a power-up sequence is completed, each regulator may be enabled and disabled individually by the system as needed for power management requirements by using the command register bit CNTRL[5]. When CNTRL[5] is set high the regulators ignore the state of their enable pins and respond only to I^2C command register bit settings. The software control mode bit is reset in the one second standby and hard reset timer states so a pin strapped sequence begins at the next LT3380 power on.

Keep Alive Operation

Each regulator has a dedicated command register keep alive bit that, when set, forces a regulator to be enabled regardless of the enable pins, command register enable bits, or the operating state of the LT3380. A hard reset or fault shutdown resets the keep alive bits.

POWER OFF SEQUENCING

Sequence down command registers SQD1 and SQD2 are used to set the time, relative to PWR_ON falling, that a regulator is disabled. Table 7 shows register settings for SQD1 and SQD2.

Table 7. Sequence Down Control Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
SQD1[1:0]	00*	Disable Buck4 at Falling PWR_ON
	01	Disable Buck4 at Falling PWR_ON + 100ms
	10	Disable Buck4 at Falling PWR_ON + 200ms
	11	Disable Buck4 at Falling PWR_ON + 300ms
SQD1[3:2]	00*	Disable Buck3 at Falling PWR_ON
	01	Disable Buck3 at Falling PWR_ON + 100ms
	10	Disable Buck3 at Falling PWR_ON + 200ms
	11	Disable Buck3 at Falling PWR_ON + 300ms
SQD1[5:4]	00*	Disable Buck2 at Falling PWR_ON
	01	Disable Buck2 at Falling PWR_ON + 100ms
	10	Disable Buck2 at Falling PWR_ON + 200ms
	11	Disable Buck2 at Falling PWR_ON + 300ms
SQD1[7:6]	00*	Disable Buck1 at Falling PWR_ON
	01	Disable Buck1 at Falling PWR_ON + 100ms
	10	Disable Buck1 at Falling PWR_ON + 200ms
	11	Disable Buck1 at Falling PWR_ON + 300ms
SQD2[1:0]	00*	Disable LDO2 at Falling PWR_ON
	01	Disable LDO2 at Falling PWR_ON + 100ms
	10	Disable LDO2 at Falling PWR_ON + 200ms
	11	Disable LDO2 at Falling PWR_ON + 300ms
SQD2[3:2]	00*	Disable LDO3 at Falling PWR_ON
	01	Disable LDO3 at Falling PWR_ON + 100ms
	10	Disable LDO3 at Falling PWR_ON + 200ms
	11	Disable LDO3 at Falling PWR_ON + 300ms
SQD2[5:4]	00*	Disable LDO1 at Falling PWR_ON
	01	Disable LDO1 at Falling PWR_ON + 100ms
	10	Disable LDO1 at Falling PWR_ON + 200ms
	11	Disable LDO1 at Falling PWR_ON + 300ms

*denotes default power-on value

Figure 9 shows an example of a shutdown sequence. In this example, the bits in command registers SQD1 and SQD2 are set so that LDO2, LDO3, and LDO1 shut off at the same time as PWR_ON. Buck2 and Buck4 shut off 100ms after PWR_ON. Buck3 shuts off 200ms after PWR_ON and Buck1 shuts off 300ms after PWR_ON.

FAULT DETECTION AND REPORTING

The LT3380 has fault detection circuits that monitor for V_{IN} undervoltage, die overtemperature, and regulator output undervoltage. Status of the fault detect circuits is indicated by the $\overline{IRQ}$ and PGOOD pins and the IRQSTAT and PGSTAT status registers.

An overtemperature or V_{IN} undervoltage fault initiates a power-down sequence and moves the control circuit into

OPERATION

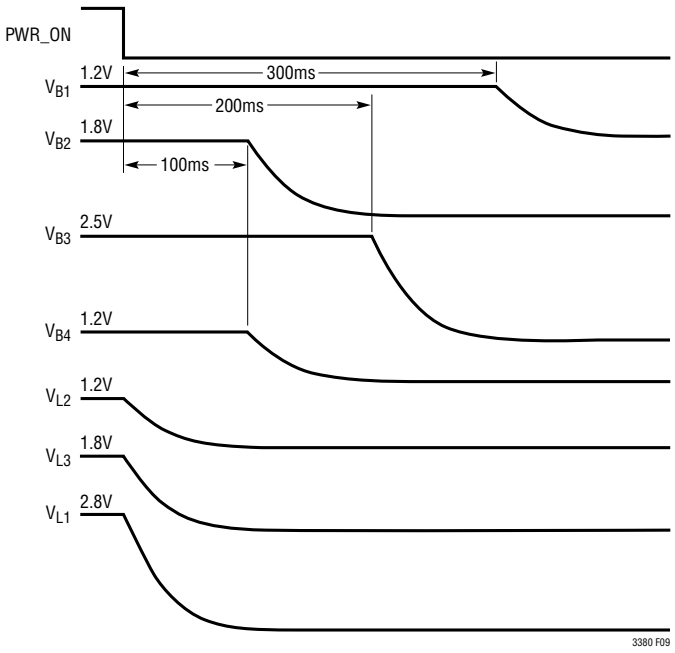


Figure 9. Power-Down Sequence

the STANDBY state. If the PWR_ON pin is held high during the one second STANDBY time the controller will move to the ON state and the LT3380 will start-up immediately.

V_{IN} Undervoltage

The undervoltage (UV) circuit monitors the input supply voltage, V_{IN}, and when the voltage falls below 2.45V creates a FAULT condition that forces the LT3380 into the standby state. The LT3380 also provides a (UV) warning that is triggered at user programmable V_{IN} voltages as shown in Table 8.

The V_{IN} undervoltage fault rising (2.65V max) defines the voltage at which V_{IN} rising undervoltage fault is detected. The LT3380 will respond to PWR_ON and regulator enable pins when V_{IN} is less than the V_{IN} undervoltage fault rising threshold at initial application of V_{IN}. An internal timer will inhibit all enables if V_{IN} does not cross the rising fault threshold within 5 seconds. PWR_ON and enables should be asserted only when the application has applied V_{IN} greater than the minimum V_{IN} input of 2.7V. A power good signal from a V_{IN} preregulator or voltage divider from V_{IN} to the 400mV (Typ) PWR_ON input threshold may be used to ensure V_{IN} is above 2.7V.

Table 8. Undervoltage Warning Threshold Command Register Settings

COMMAND REGISTER[BIT]	VALUE	FALLING V_{IN} THRESHOLD
CNTRL[4:2]	000*	2.7V
	001	2.8V
	010	2.9V
	011	3.0V
	100	3.1V
	101	3.2V
	110	3.3V
	111	3.4V

*denotes default power-on value.

Overtemperature

To prevent thermal damage the LT3380 incorporates an overtemperature (OT) circuit. When the die temperature reaches 155°C the OT circuits create a FAULT condition that forces the LT3380 into standby. When the OT circuit detects the temperature falls below 140°C the FAULT condition is cleared. The LT3380 also has an OT warning circuit that indicates the die temperature is approaching the OT fault threshold. The OT warning threshold is user programmable as shown in Table 9.

Table 9. Overtemperature Warning Threshold Command Register Settings

COMMAND REGISTER[BIT]	VALUE	OT WARNING THRESHOLD
CNTRL[1:0]	00*	10°C Below OT Fault
	01	20°C Below OT Fault
	10	30°C Below OT Fault
	11	40°C Below OT Fault

*denotes default power-on value

PGOOD Status Pin

The PGOOD open-drain status pin is pulled low when all regulators are disabled. PGOOD is released when all enabled regulator outputs are above 94% of their programmed value. When any enabled regulator output falls below 92% of its programmed value for longer than 50µs the PGOOD pin is pulled low. The 50µs transient filter on PGOOD prevents PGOOD glitches due to transients. If the error condition persists for longer than 20ms, the $\overline{IRQ}$ pin is pulled low and status register IRQSTAT bit 2 is set to indicate a persistent low output voltage. The PGOOD pin is held low for the duration of the low output condition plus 1ms. Figure 10 shows the timing of PGOOD during enable and low output voltage events.

OPERATION

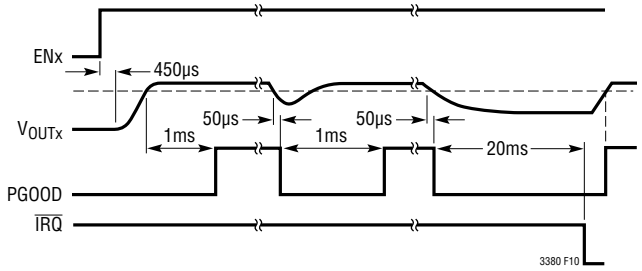


Figure 10. Output Low Voltage PGOOD and $\overline{IRQ}$ Timing

PGOOD Status and Mask PGOOD Registers

The power good status of each regulator is accessible through the LT3380 I²C interface by reading the contents of the PGOOD status registers. Table 10 shows the PGSTATL and PGSTATRT register contents. The data in the PGSTATL register is held for a minimum of 1ms. The data in the PGSTATRT register is held only for the duration of the low voltage condition.

Table 10. Power Good Status Registers

STATUS REGISTER[BIT]	VALUE	REGULATOR OUTPUT LOW STATUS
PGSTAT[0]	0 1	Buck4 Output Low Buck4 Output OK
PGSTAT[1]	0 1	Buck3 Output Low Buck3 Output OK
PGSTAT[2]	0 1	Buck2 Output Low Buck2 Output OK
PGSTAT[3]	0 1	Buck1 Output Low Buck1 Output OK
PGSTAT[5]	0 1	LDO2 Output Low LDO2 Output OK
PGSTAT[6]	0 1	LDO3 Output Low LDO3 Output OK
PGSTAT[7]	0 1	LDO1 Output Low LDO1 Output OK

Each regulator has a corresponding bit in the MSKPG register. (see Table 11) When a MSKPG it is set low, the PGOOD pin is prevented from pulling down when an output undervoltage occurs from its matching regulator. The PGOOD pin is allowed to pull-down when undervoltage output is detected on the regulator output when its matching MSKPG bit is high. The values in the PGSTATL and PGSTATRT status registers are not masked by the MSKPG bits.

Table 11. Power Good Status Masking Command Register

COMMAND REGISTER[BIT]	VALUE	
MSKPG [0]	0 1*	Mask Buck4 PGOOD Status Pass Buck4 PGOOD Status
MSKPG [1]	0 1*	Mask Buck3 PGOOD Status Pass Buck3 PGOOD Status
MSKPG [2]	0 1*	Mask Buck2 PGOOD Status Pass Buck2 PGOOD Status
MSKPG [3]	0 1*	Mask Buck1 PGOOD Status Pass Buck1 PGOOD Status
MSKPG [5]	0 1*	Mask LDO2 PGOOD Status Pass LDO2 PGOOD Status
MSKPG [6]	0 1*	Mask LDO3 PGOOD Status Pass LDO3 PGOOD Status
MSKPG [7]	0 1*	Mask LDO1 PGOOD Status Pass LDO1 PGOOD Status

*denotes default power-on value

$\overline{IRQ}$ Status Pin

The $\overline{IRQ}$ pin is pulled and latched low when undervoltage, overtemperature or persistent PGOOD events occur. The $\overline{IRQ}$ pin is cleared by addressing the CLIRQ command register.

Table 12. Interrupt Request Status Register

STATUS REGISTER[BIT]	VALUE	IRQSTAT REGISTER BIT MEANING
IRQSTAT [1]	0 1	Hard Reset Occurred
IRQSTAT [2]	0 1	PGOOD Timeout Occurred
IRQSTAT [3]	0 1	Undervoltage Warning
IRQSTAT [4]	0 1	Undervoltage Standby Occurred
IRQSTAT [5]	0 1	Overtemperature Warning
IRQSTAT [6]	0 1	Overtemperature Standby Occurred

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IRQSTAT and MSKIRQ Registers

The bits in the MSKIRQ command register (see Table 13) are set to mask the warning and fault events reported by the $\overline{IRQ}$ pin. When set to mask, the $\overline{IRQ}$ pin is not pulled low as a result of a fault or warning. Even though the $\overline{IRQ}$ pin is not pulled low the masked bit is set in the IRQSTAT (see Table 12) register. When undervoltage, overtemperature faults, and hard reset signals are masked, the $\overline{IRQ}$ pin is not pulled low but the LT3380 state controller is pushed into the STANDBY or POR/HRST state. Accessing the CLIRQ status register clears the latched bits in the IRQSTAT status register and releases the $\overline{IRQ}$ pin.

Table 13. Interrupt Request Mask Command Register

COMMAND REGISTER[BIT]	VALUE	
MSKIRQ [2]	0* 1	Pass PGOOD Timeout Mask PGOOD Timeout
MSKIRQ [3]	0* 1	Pass Undervoltage Warning Mask Undervoltage Warning
MSKIRQ [4]	0* 1	Pass Undervoltage Shutdown Mask Undervoltage Shutdown
MSKIRQ [5]	0* 1	Pass Overtemperature Warning Mask Overtemperature Warning
MSKIRQ [6]	0* 1	Pass Overtemperature Shutdown Mask Overtemperature Shutdown

*denotes default power-on value

IRQ and IRQSTAT are not cleared by hard reset or fault shutdown. If V_{IN} remains applied while the LT3380 is in STANDBY or POR/HRST then IRQSTAT may be read on the subsequent power up to determine if a fault or hard reset occurred.

Hard Reset

A hard reset can be initiated by writing to the HRST command register. A hard reset sets all I^2C command register bits to their default power-on state.

A hard reset command will push the LT3380 state controller through the 1 second HRST timer state and into the POR/HRST state.

I^2C OPERATION

The LT3380 communicates with a bus master using the standard I^2C 2-wire interface. The timing diagram in Figure 11 shows the relationship of the signals on the bus. The two bus lines, SDA and SCL must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on SDA and SCL. The LT3380 is both a slave receiver and slave transmitter. The I^2C control signals, SDA and SCL, are scaled internally to the DV_{DD} supply. DV_{DD} must be connected to the same power supply as the bus pull-up resistors.

The I^2C port has an undervoltage lockout on the DV_{DD} pin. When DV_{DD} is below approximately 1V, the I^2C serial port is cleared and the command registers are set to default POR values.

The complete I^2C command register table is shown in Table 15 and Table 16.

I^2C Bus Speed

The I^2C port operates at speeds up to 400kHz. It has built in timing delays to ensure correct operation when addressed from an I^2C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

I^2C START and STOP Conditions

A bus master signals the beginning of communications by transmitting a START condition. A START condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The master may transmit either the slave write or the slave read address. Once data is written to the LT3380, the master may transmit a STOP condition which commands the LT3380 to act upon its new command set. A STOP condition is sent by the master by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is then free for communication with another I^2C device.

OPERATION

I²C Byte Format

Each byte sent to or received from the LT3380 must be 8 bits long followed by an extra clock cycle for the acknowledge bit. The data should be sent to the LT3380 most significant bit (MSB) first.

I²C Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. When the LT3380 is written to, it acknowledges its write address and subsequent data bytes. When it is read from, the LT3380 acknowledges its read address only. The bus master should acknowledge data returned from the LT3380.

An acknowledge generated by the LT3380 lets the master know that the latest byte of information was received. The master generates the acknowledge related clock and releases the SDA line during the acknowledge clock cycle. The LT3380 pulls down the SDA line during the write acknowledge clock pulse so that it is a stable LOW during the HIGH period of this clock pulse.

At the end of a byte of data transferred from the LT3380 during a READ operation, the LT3380 releases the SDA line to allow the master to acknowledge receipt of the data. Failure of the master to acknowledge data from the LT3380 has no effect on the operation of the I²C port.

I²C Slave Address

The LT3380 responds to factory programmed read and write addresses. The least significant bit of the address byte is 0 when writing data and 1 when reading data. Table 14 shows read and write addresses for the LT3380 options.

Table 14. LT3380 I²C Read and Write Addresses

LTC PART NUMBER	R/$\overline{W}$	ADDRESS
LT3380	$\overline{W}$	0111 1000, 0x78
LT3380	R	0111 1001, 0x79

I²C Write Operation

The LT3380 has twenty-two command registers for control input. They are accessed by the I²C port via a sub-addressed writing system.

A single write cycle of the LT3380 consists of exactly three bytes except when a clear interrupt or hard reset command is written. The first byte is always the LT3380 write address. The second byte represents the LT3380 sub-address. The sub-address is a pointer which directs the subsequent data byte within the LT3380. The third byte consists of the data to be written to the location pointed to by the sub-address.

As shown in Figure 12, the LT3380 supports multiple sub-addressed write operations. Data pairs sent following the chip write address are interpreted as sub-address and data. Any number of sub-address and data pairs may be sent. The data in the command registers is not acted on by the LT3380 until a STOP signal is issued.

The LT3380 will keep interim writes to the registers when a repeat START condition occurs. A repeat start may be used to set up other devices on the I²C bus prior to sending a STOP condition. The LT3380 will act on the data written prior to the repeat start when a STOP condition is detected.

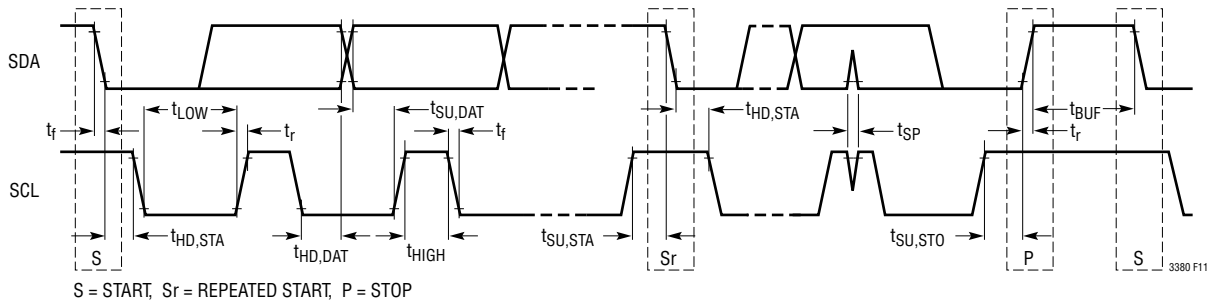


Figure 11. LT3380 I²C Serial Port Timing

OPERATION

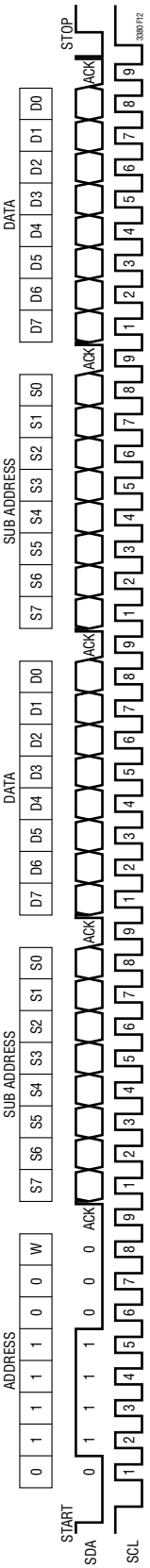


Figure 12. LT3380 I²C Serial Port Multiple Write Pattern



Figure 13. LT3380 I²C Serial Port Read Pattern

OPERATION

I²C Read Operation

Figure 13 shows the LT3380 command register read sequence. The bus master reads a byte of data from a LT3380 command or status register by first writing the LT3380 write address followed by the sub-address to be read from. The LT3380 acknowledges each of the two bytes. Next, the bus master initiates a new START condition and sends the LT3380 read address. Following the acknowledge of the read address by the LT3380, the LT3380 pushes data onto the I²C bus for the 8 clock cycles. The bus master then acknowledges the data on its ninth clock.

The last read sub-address that is written to the LT3380 is stored. This allows repeated polling of a command or status register without the need to re-write its sub-address. Additionally, the last register written may be immediately read by issuing a START condition followed by read address and clocking out the data.

Reserved Bits

The bits marked as reserved in command registers cannot be written to and will return inconsistent data when read. These bits must be considered invalid and masked by software when reading.

Table 15. LT3380 Command Registers

REG	NAME	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	DEFAULT
0x01	BUCK4	Enable: 0 = Disabled if EN_B4 Low 1 = Enabled	Mode: 00 = Pulse-Skipping 01 = Burst 10 = Forced Continuous		Start-Up: 0 = Enable at Any Output Voltage 1 = Enable Only if Output <300mV	Phase Select: 0 = Clock Phase 1 1 = Clock Phase 2	Clock Rate: 0 = 2.25MHz 1 = 1.125MHz	Keep Alive Buck4: 0 = Do Not Keep Alive 1= Keep Alive in Shutdown.	Switch DV/DT Control: 0 = Slow 1 = Fast	0000 0000
0x02	BUCK3	Enable: 0 = Disabled if EN_B3 Low 1 = Enabled	Mode: 00 = Pulse-Skipping 01 = Burst 10 = Forced Continuous		Start-Up: 0 = Enable at Any Output Voltage 1 = Enable Only if Output <300mV	Phase Select: 0 = Clock Phase 1 1 = Clock Phase 2	Clock Rate: 0 = 2.25MHz 1 = 1.125MHz	Keep Alive Buck3: 0 = Do Not Keep Alive 1 = Keep Alive in Shutdown	Switch DV/DT Control: 0 = Slow 1 = Fast	0000 0000
0x03	BUCK2	Enable: 0 = Disabled if EN_B2 Low 1 = Enabled	Mode: 00 = Pulse-Skipping 01 = Burst 10 = Forced Continuous		Start-Up: 0 = Enable at Any Output Voltage 1 = Enable Only if Output <300mV	Phase Select: 0 = Clock Phase 1 1 = Clock Phase 2	Clock Rate: 0 = 2.25MHz 1 = 1.125MHz	Keep Alive Buck2: 0 = Do Not Keep Alive 1 = Keep Alive in Shutdown	Switch DV/DT Control: 0 = Slow 1 = Fast	0000 0000
0x04	BUCK1	Enable: 0 = Disabled if EN_B1 Low 1 = Enabled	Mode: 00 = Pulse-Skipping 01 = Burst 10 = Forced Continuous		Start-Up: 0 = Enable at Any Output Voltage 1 = Enable Only if Output <300mV	Phase Select: 0 = Clock Phase 1 1 = Clock Phase 2	Clock Rate: 0 = 2.25MHz 1 = 1.125MHz	Keep Alive Buck1: 0 = Do Not Keep Alive 1 = Keep Alive in Shutdown	Switch DV/DT Control: 0 = Slow 1 = Fast	0000 0000
0x05	LDOA	Reserved	Reserved	Enable LDO3: 0 = Disabled if EN_L3 Low 1 = Enabled	Start-Up LDO3: 0 = Enable at Any Output Voltage 1 = Enable Only if Output <300mV	Keep Alive LDO3: 0 = Do Not Keep Alive 1 = Keep Alive in Shutdown	Enable LDO2: 0 = Disabled if EN_L2 Low 1 = Enabled	Start-Up LDO2: 0 = Enable at Any Output Voltage 1 = Enable Only if Output <300mV	Keep Alive LDO2: 0 = Do Not Keep Alive 1 = Keep Alive in Shutdown	XX00 0000

OPERATION

Table 15. LT3380 Command Registers

REG	NAME	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	DEFAULT
0x06	LDOB	Reserved	Reserved	Reserved	Reserved	Reserved	Enable LDO1: 0 = Disabled if EN_L1 Low 1 = Enabled	Start-Up LDO1: 0 = Enable at Any Output Voltage 1 = Enable Only if Output <300mV	Keep Alive LDO1: 0 = Do Not Keep Alive 1 = Keep Alive in Shutdown	XXXX X000
0x07	SQD1	Sequence Down Buck1: 00 = With PWR_ON 01 = PWR_ON + 100ms 10 = PWR_ON + 200ms 11 = PWR_ON + 300ms		Sequence Down Buck2: 00 = With PWR_ON 01 = PWR_ON + 100ms 10 = PWR_ON + 200ms 11 = PWR_ON + 300ms		Sequence Down Buck3: 00 = With PWR_ON 01 = PWR_ON + 100ms 10 = PWR_ON + 200ms 11 = PWR_ON + 300ms		Sequence Down Buck4: 00 = With PWR_ON 01 = PWR_ON + 100ms 10 = PWR_ON + 200ms 11 = PWR_ON + 300ms		0000 0000
0x08	SQD2	Reserved	Reserved	Sequence Down LD01: 00 = With PWR_ON 01 = PWR_ON + 100ms 10 = PWR_ON + 200ms 11 = PWR_ON + 300ms		Sequence Down LD03: 00 = With PWR_ON 01 = PWR_ON + 100ms 10 = PWR_ON + 200ms 11 = PWR_ON + 300ms		Sequence Down LD02: 00 = With PWR_ON 01 = PWR_ON + 100ms 10 = PWR_ON + 200ms 11 = PWR_ON + 300ms		XX00 0000
0x09	CNTRL	PWR_ON: 0 = Not PWR_ON 1 = PWR_ON "ORed" with PWR_ON PIN	Reserved	Software Control Mode: 0 = Pin or Register Control 1 = Inhibit Pin Control	UV Warning Threshold: 000 = 2.7V 001 = 2.8V 010 = 2.9V 011 = 3.0V 100 = 3.1V 101 = 3.2V 110 = 3.3V 111 = 3.4V			Over temperature Warning Levels: 00 = 10°C Below Overtemperature 01 = 20°C Below Overtemperature 10 = 30°C Below Overtemperature 11 = 40°C Below Overtemperature		0X00 0000
0x0A	DVB4A	Reserved	Reserved	Buck4 Reference Select: 0 = DVB4A[4-0] 1 = DVB4B[4-0]	Buck4 Feedback Reference Input (VA): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size					XX01 1001
0x0B	DVB4B	Reserved	Reserved	PGOOD Mask: 0 = PGOOD Low When Slewing 1 = PGOOD Not Forced Low When Slewing	Buck4 Feedback Reference Input (VB): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size					XX01 1001
0x0C	DVB3A	Reserved	Reserved	Buck3 Reference Select: 0 = DVB3A[4-0] 1 = DVB3B[4-0]	Buck3 Feedback Reference Input (VA): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size					XX01 1001
0x0D	DVB3B	Reserved	Reserved	PGOOD Mask: 0 = PGOOD Low When Slewing 1 = PGOOD Not Forced Low When Slewing	Buck3 Feedback Reference Input (VB): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size					XX01 1001

OPERATION

Table 15. LT3380 Command Registers

REG	NAME	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	DEFAULT
0x0E	DVB2A	Reserved	Reserved	Buck2 Reference Select: 0 = DVB2A[4-0] 1 = DVB2B[4-0]	Buck2 Feedback Reference Input (VA): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size					XX01 1001
0x0F	DVB2B	Reserved	Reserved	PGOOD Mask: 0 = PGOOD Low When Slewing 1 = PGOOD Not Forced Low When Slewing	Buck2 Feedback Reference Input (VB): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size					XX01 1001
0x10	DVB1A	Reserved	Reserved	Buck1 Reference. Select: 0 = DVB1A[4-0] 1 = DVB1B[4-0]	Buck1 Feedback Reference Input (VA): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size					XX01 1001
0x11	DVB1B	Reserved	Reserved	PGOOD Mask: 0 = PGOOD Low When Slewing 1 = PGOOD Not Forced Low When Slewing	Buck1 Feedback Reference Input (VB): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size					XX01 1001
0x12	MSKIRQ	Reserved	Mask Over-temperature Shutdown	Mask Over-temperature Warning	Mask Undervoltage Shutdown	Mask Undervoltage Warning	Mask PGOOD Timeout	Reserved	Reserved	X000 00XX
0x13	MSKPG	Allow LDO1 PGOOD Fault	Allow LDO3 PGOOD Fault	Allow LDO2 PGOOD Fault	Reserved	Allow Buck1 PGOOD Fault	Allow Buck2 PGOOD Fault	Allow Buck3 PGOOD Fault	Allow Buck4 PGOOD Fault	1111 1111
0x14	USER	User Bit 7	User Bit 6	User Bit 5	User Bit 4	User Bit 3	User Bit 2	User Bit 1	User Bit 0	0000 0000
0x1E	HRST	Hard Reset Command. No Data.								
0x1F	CLIRQ	Clear $\overline{IRQ}$ Command. No Data								

Table 16. LT3380 Status Registers

REG	NAME	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
0x15	IRQSTAT	Reserved	Over-temperature Shutdown	Over-temperature Warning	Undervoltage Shutdown	Undervoltage Warning	PGOOD Timeout	Hard Reset	Reserved
0x16	PGSTATL	LDO1 PGOOD Hold 1ms	LDO3 PGOOD Hold 1ms	LDO2 PGOOD Hold 1ms	Reserved	Buck1 PGOOD Hold 1ms	Buck2 PGOOD Hold 1ms	Buck3 PGOOD Hold 1ms	Buck4 PGOOD Hold 1ms
0x17	PGSTATRT	LDO1 PGOOD	LDO3 PGOOD	LDO2 PGOOD	Reserved	Buck1 PGOOD	Buck2 PGOOD	Buck3 PGOOD	Buck4 PGOOD

APPLICATIONS INFORMATION

THERMAL CONSIDERATIONS AND BOARD LAYOUT

Printed Circuit Board Power Dissipation

In order to ensure optimal performance and the ability to deliver maximum output power to any regulator, it is critical that the exposed ground pad on the backside of the LT3380 package be soldered to a ground plane on the board. Correctly soldered to a 2500mm^2 ground plane on a double-sided 1oz copper board, the LT3380 has a thermal resistance(θ_{JA}) of approximately 33°C/W. Failure to make good thermal contact between the exposed pad on the backside of the package and an adequately sized ground plane will result in thermal resistances far greater than 33°C/W. To ensure the junction temperature of the LT3380 die does not exceed the maximum rated limit and to prevent overtemperature faults, the power output of the LT3380 must be managed by the application. The total power dissipation in the LT3380 is approximated by summing the power dissipation in each of the switching regulators and the LDO regulators. The power dissipation in a switching regulator is estimated by:

$$P_{D(SWx)} = V_{OUTx} \bullet I_{OUTx} \bullet \frac{100\text{-}Eff\%}{100} (W)$$

where V_{OUTx} is the programmed output voltage, I_{OUTx} is the load current, and Eff is the % efficiency that can be measured or looked up from the efficiency curves for the programmed output voltage.

The power dissipated by an LDO regulator is estimated by:

$$P_{D(LDOx)} = (V_{IN_Lx} - V_{LDOx}) \bullet I_{LDOx} (W)$$

where V_{LDOx} is the programmed output voltage, $V_{IN(LDOx)}$ is the LDO supply voltage, and I_{LDOx} is the output load current. If one of the switching regulator outputs is used as an LDO supply voltage, remember to include the LDO supply current in the switching regulator load current for calculating power loss.

An example using the equations above with the parameters in Table 17 shows an application that is at a junction temperature of 118°C at an ambient temperature of 55°C. LDO1, LDO2, and LDO3 are powered by step-down Buck2 and Buck4. The total load on Buck2 and Buck4 is the sum of the application load and the LDO load. This example is with the LDO regulators at one-third rated current and the switching regulators at three quarters rated current.

Table 17. LT3380 Power Loss Example

	V_{IN}	V_{OUT}	APPLICATION LOAD (A)	TOTAL LOAD (A)	EFF (%)	P_D (mW)
LDO2	1.8	1.2	0.1	0.100	–	60.00
LDO3	3.3	1.8	0.1	0.100	–	150.00
LDO1	3.3	2.5	0.1	0.100	–	80.00
Buck1	3.8	1.2	1.875	1.875	80	450.00
Buck2	3.8	1.8	1.775	1.875	85	506.25
Buck3	3.8	1.25	1.125	1.125	80	281.25
Buck4	3.8	3.3	0.925	1.125	90	371.25
					Total Power =	1899
				Internal Junction Temperature at 55°C Ambient		118°C

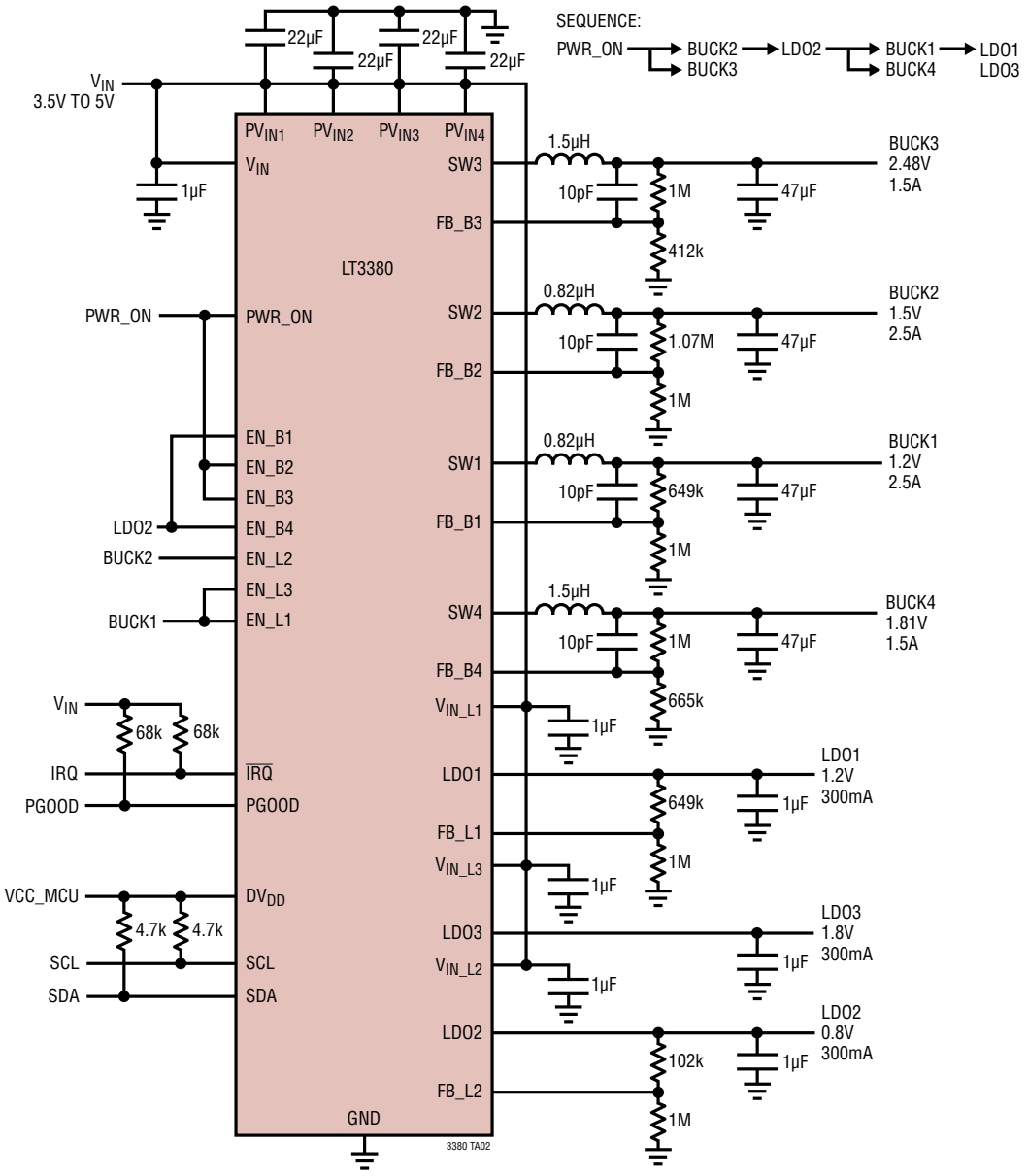
Printed Circuit Board Layout

When laying out the printed circuit board, the following checklist should be followed to ensure proper operation of the LT3380:

1. Connect the exposed pad of the package (Pin 41) directly to a large ground plane to minimize thermal and electrical impedance.
2. The switching regulator input supply traces to their decoupling capacitors should be as short as possible. Connect the GND side of the capacitors directly to the ground plane of the board. The decoupling capacitors provide the AC current to the internal power MOSFETs and their drivers. It is important to minimize inductance from the capacitors to the LT3380 pins.
3. Minimize the switching power traces connecting SW1, SW2, SW3, and SW4 to the inductors to reduce radiated EMI and parasitic coupling. Keep sensitive nodes such as the feedback pins away from or shielded from the large voltage swings on the switching nodes.
4. Minimize the length of the connection between the step-down switching regulator inductors and the output capacitors. Connect the GND side of the output capacitors directly to the thermal ground plane of the board.

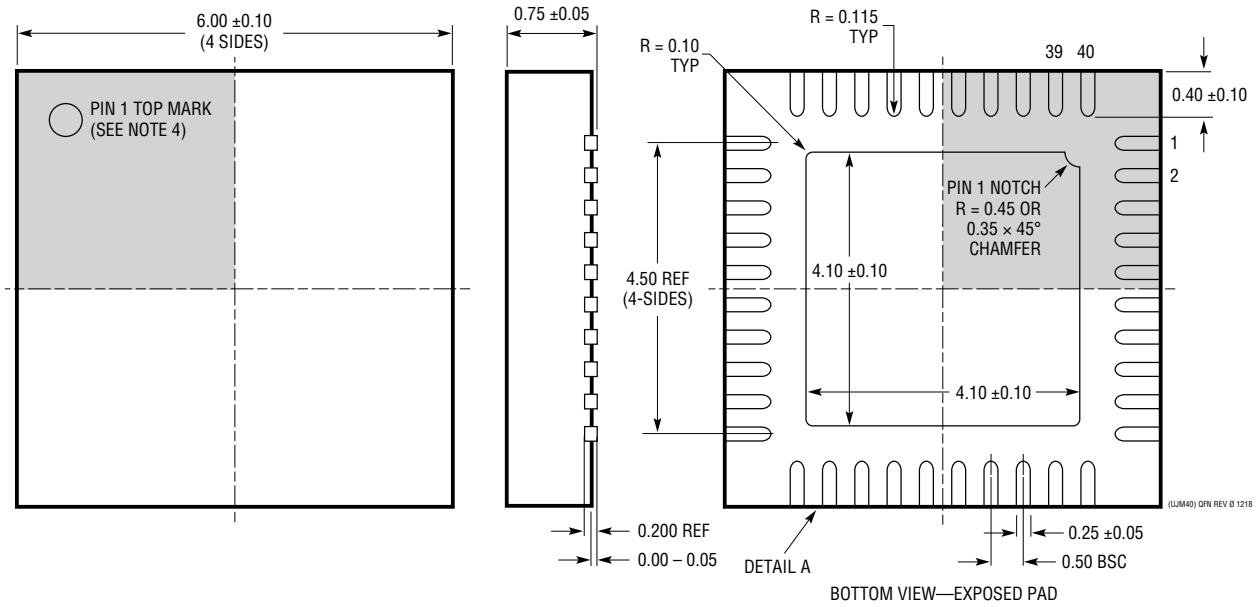
TYPICAL APPLICATIONS

LT3380 Seven Power Rails

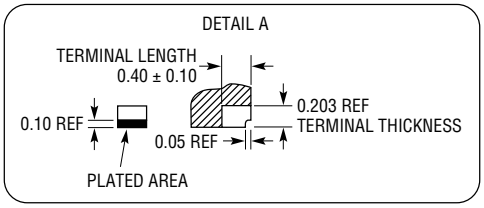


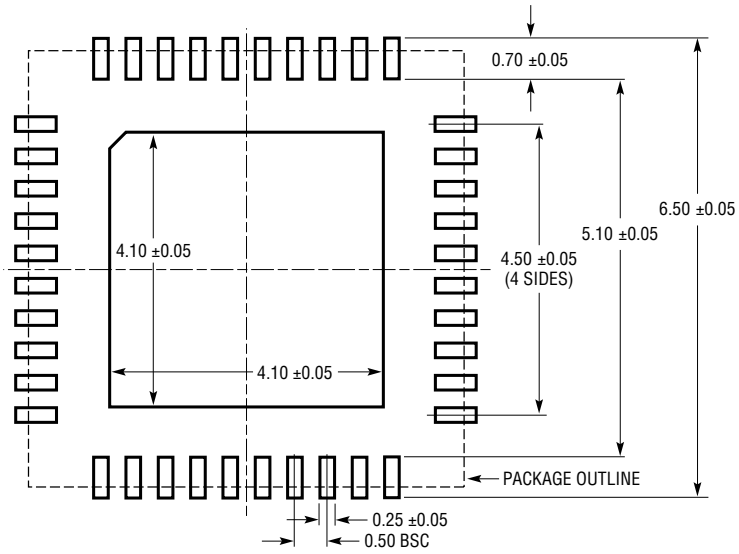
PACKAGE DESCRIPTION

UJM Package
40-Lead Plastic Side Wettable QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1681 Rev Ø)



NOTE:
1. DRAWING NOT TO SCALE
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
4. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE





RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

Rev. A

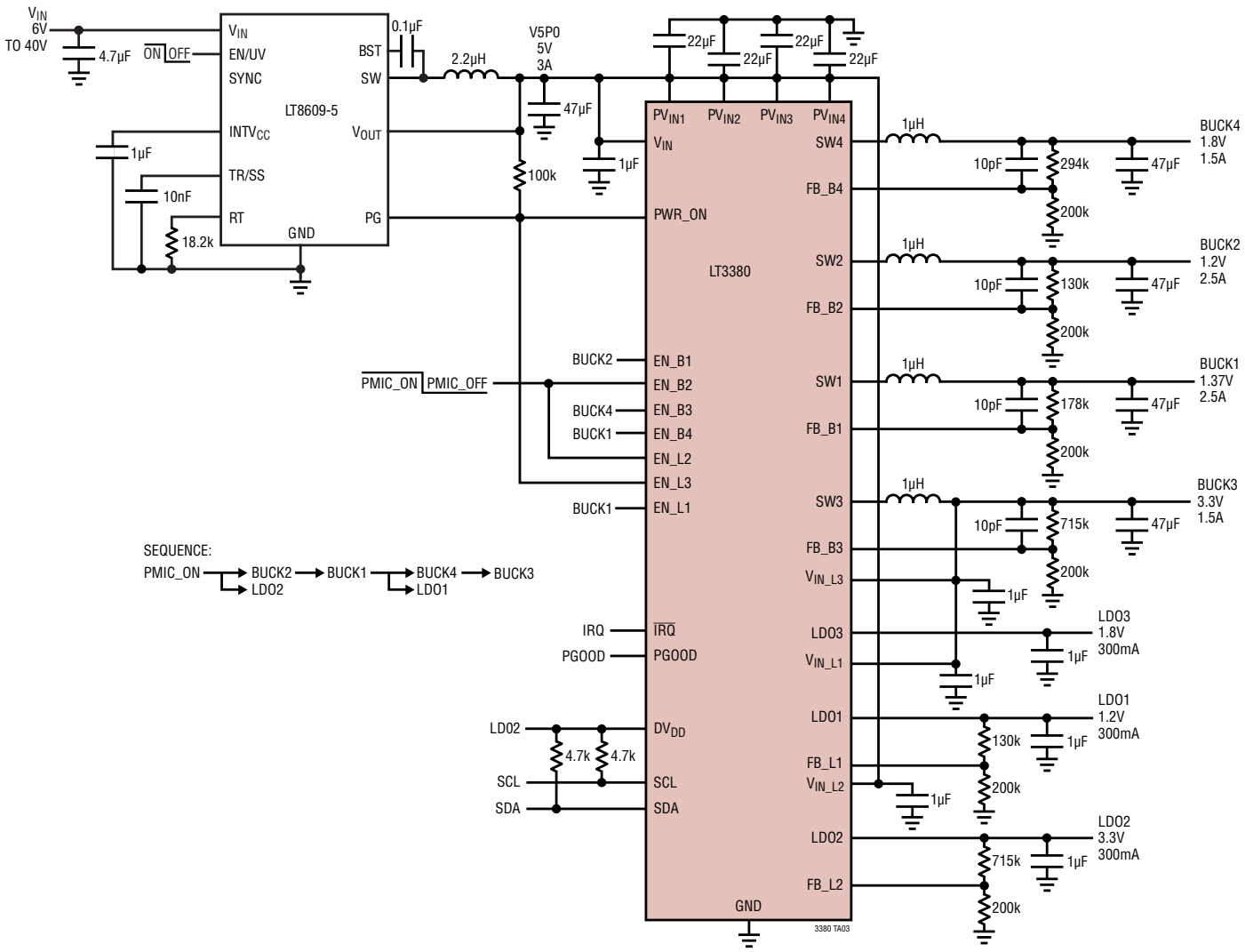
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/21	Add Ordering Information for Automotive Products	2

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TYPICAL APPLICATION

Seven Sequenced Power Rails From 40V Input Using LT8609-5



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3676/ LTC3676-1	PMIC for Application Processors	Quad I²C Adjustable High Efficiency Step-Down DC/DC Converters: 2.5A, 2.5A, 15A, 1.5A, Three 300mA LDO Regulators (Two Adjustable), DDR Power Solutions with VTT and VTTR Reference, Pushbutton ON/OFF Control, LTC3676-1 Supports DDR, 40-Lead 6mm × 6mm × 0.75mm QFN Package.
LTC3375	8-Channel Programmable, Parallelable 1A Buck DC/DCs	8-Channel Independent Step-Down DC/DCs. Master Slave Configurable for Up to 4A per Output Channel with a Single Inductor, Die Temperature Monitor Output, 48-Lead 7mm × 7mm QFN Package
LTC3589/ LTC3589-1/ LTC3589-2	8-Output Regulator with Sequencing and I²C	Triple I²C Adjustable High Efficiency Step-Down DC/DC Converters: 1.6A, 1A, 1A. High Efficiency 1.2A Buck-Boost DC/DC Converter. Triple 250mA LDO Regulators. Pushbutton ON/OFF Control with System Reset. Flexible Pin-Strap Sequencing Operation. I²C and Independent Enable Control Pins, DVS and Slew Rate Control, 40-Lead 6mm × 6mm × 0.75mm QFN Package
LTC3586/ LTC3586-1	Switching USB Power Manager PMIC with Li-Ion/Polymer Charger	Complete Multifunction PMIC: Switching Power Manager, 1A Buck-Boost + 2 Bucks + Boost + LDO, 4mm × 6mm QFN-38 Package, LTC3586-1 Version Has 4.1V V_{FLOAT}.

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