Integrated Circuit Systems, Inc.

ICS9248-96

Frequency Generator & Integrated Buffers for Celeron & PII/III™

Recommended Application:
810/810E type chipset.

Output Features:

- 2- CPUs @ 2.5V, up to 166.5MHz.
- 9 - SDRAM @ 3.3V, up to 155MHz including 1 free running
- 8 - PCICLK @ 3.3V
- 1 - IOAPIC @ 2.5V,
- 2 - 3V66MHz @ 3.3V, 2X PCI MHz
- 2 - 48MHz, @ 3.3V fixed.
- 1 - 24/48MHz, @3.3V selectable by I^2C
- 1 - REF @v3.3V, 14.318MHz.

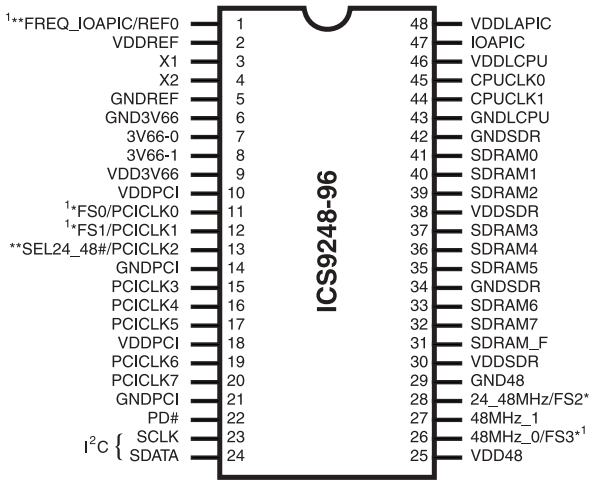
Features:

- Up to 166.5MHz frequency support
- Support FS0-FS3 strapping status bit for I^2C read back.
- Support power management: Through Power down Mode from I^2C programming.
- Spread spectrum for EMI control (± 0.25% center).
- Uses external 14.318MHz crystal

Skew Specifications:

- CPU – CPU: <175ps
- SDRAM - SDRAM: < 250ps
- 3V66 – 3V66: <175ps
- PCI – PCI: <500ps
- CPU-SDRAM<500ps
- For group skew specifications, please refer to group timing relationship table.

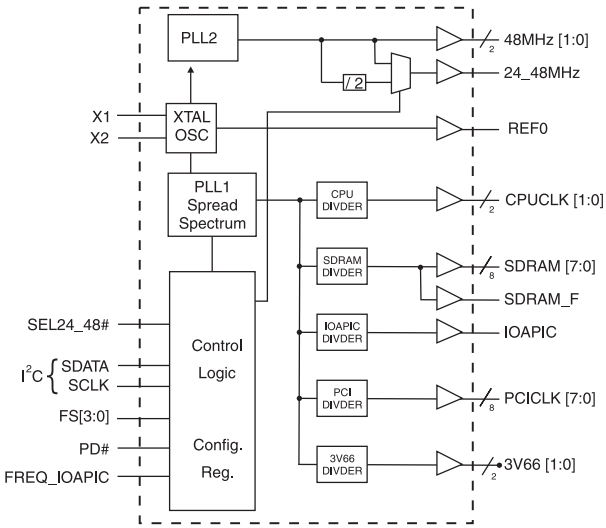
Pin Configuration



48-Pin 300mil SSOP

* These inputs have a 120K pull up to VDD.
** 60K pull-up to VDD on indicated input
1 These are double strength.

Block Diagram



Functionality

FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	3V66 (MHz)	PCICLK (MHz)	IOAPIC 1=PCICLK/2 (MHz)	IOAPIC 0=PCICLK (MHz)
0	0	0	0	66.80	100.20	66.80	33.40	16.70	33.40
0	0	0	1	68.00	102.00	68.00	34.00	17.00	34.00
0	0	1	0	100.30	100.30	66.87	33.43	16.72	33.43
0	0	1	1	103.00	103.00	68.67	34.33	17.17	34.33
0	1	0	0	133.73	100.30	66.87	33.43	16.72	33.43
0	1	0	1	145.00	108.75	72.50	36.25	18.13	36.25
0	1	1	0	133.73	100.30	66.87	33.43	16.72	33.43
0	1	1	1	137.33	103.00	68.67	34.33	17.17	34.33
1	0	0	0	140.00	105.00	70.00	35.00	17.50	35.00
1	0	0	1	140.00	140.00	93.33	46.67	23.33	46.67
1	0	1	0	118.00	118.00	78.67	39.33	19.67	39.33
1	0	1	1	124.00	124.00	82.67	41.33	20.67	41.33
1	1	0	0	133.70	133.70	89.13	44.57	22.28	44.57
1	1	0	1	137.00	137.00	91.33	45.67	22.83	45.67
1	1	1	0	150.00	112.50	75.00	37.50	18.75	37.50
1	1	1	1	72.50	108.75	72.50	36.25	18.13	36.25

Additional frequencies selectable through I^2C programming.

General Description

ICS9248-96 is the single chip clock solution for designs using the 810/810E style chipset. It provides all necessary clock signals for such a system.
Spread spectrum may be enabled through I^2C programming.
Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-96 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.
Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

Power Groups

GNDREF, VDDREF = REF0, X1, X2
GNDPCI , VDDPCI = PCICLK [9:0]
GNDSDR, VDDSDR = SDRAM [7:0], SDRAM_F, supply for PLL core
GND3V66 , VDD3V66 = 3V66
GND48 , VDD48 = 48MHz, 24_48MHz,
VDDLAPIC = IOAPIC
GNDLCPU , VDDLCPU = CPUCLK [1:0]

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FREQ_IOAPIC	IN	If FREQ_APIC = 0, APIC Clock = PCICLK If FREQ_APIC = 1, APIC Clock = PCICLK/2 (default)
	REF0	OUT	14.318 MHz reference clock.
2, 9, 10, 18, 25, 30, 38	VDD	PWR	3.3V Power supply for SDRAM output buffers, PCI output buffers, reference output buffers and 48MHz output
3	X1	IN	Crystal input,nominally 14.318MHz.
4	X2	OUT	Crystal output, nominally 14.318MHz.
5, 6, 14, 21, 29, 34, 42	GND	PWR	Ground pin for 3V outputs.
8, 7	3V66 [1:0]	OUT	3.3V Clocks
11	FS0	IN	Frequency select pin.
	PCICLK0	OUT	PCI clock output
12	FS1	IN	Frequency select pin.
	PCICLK1	OUT	PCI clock output
13	SEL24_48MHz#	IN	Logic inputs frequency select I/O/USB output, When a "0" is latched, output frequency = 48MHz When a "1" is latched, output frequency = 24MHz
	PCICLK2	OUT	PCI clock output
20, 19, 17, 16, 15	PCICLK [7:3]	OUT	PCI clock outputs.
22	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
23	SCLK	IN	Clock input of I2C input, 5V tolerant input
24	SDATA	IN	Data input for I2C serial input, 5V tolerant input
26	FS3	IN	Frequency select pin.
	48MHz_0	OUT	48MHz output clocks
27	48MHz_1	OUT	48MHz output clocks
28	FS2	IN	Frequency select pin.
	24_48MHz	OUT	24 or 48MHz output
31	SDRAM_F	OUT	Free running SDRAM - used for feed back to chipset, should remain on always.
32, 33, 35, 36, 37, 39, 40, 41,	SDRAM [7:0]	OUT	SDRAM clock outputs
43	GNDLCPU	PWR	Ground pin for the CPU clocks.
44, 45	CPUCLK [1:0]	OUT	CPU clock outputs.
46	VDDLCPU	PWR	Power pin for the CPUCLKs. 2.5V
47	IOAPIC	OUT	2.5V clock output
48	VDDLAPIC	PWR	Power pin for the IOAPIC. 2.5V

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General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

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Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description												PWD
	Bit (2, 7:4)					CPUCLK (MHz)	SDRAM (MHz)	3V66 (MHz)	PCICLK (MHz)	FREQ_IOAPIC (MHz)		Spread Precentage	
										1	0		
Bit 2, Bit 7:4	0	0	0	0	0	66.80	100.20	66.80	33.40	16.70	33.40	+/- 0.25% Center	00011 Note1
	0	0	0	0	1	68.00	102.00	68.00	34.00	17.00	34.00	+/- 0.25% Center	
	0	0	0	1	0	100.30	100.30	66.87	33.43	16.72	33.43	+/- 0.25% Center	
	0	0	0	1	1	103.00	103.00	68.67	34.33	17.17	34.33	+/- 0.25% Center	
	0	0	1	0	0	133.73	100.30	66.87	33.43	16.72	33.43	+/- 0.25% Center	
	0	0	1	0	1	145.00	108.75	72.50	36.25	18.13	36.25	+/- 0.25% Center	
	0	0	1	1	0	133.73	100.30	66.87	33.43	16.72	33.43	+/- 0.25% Center	
	0	0	1	1	1	137.33	103.00	68.67	34.33	17.17	34.33	+/- 0.25% Center	
	0	1	0	0	0	140.00	105.00	70.00	35.00	17.50	35.00	+/- 0.25% Center	
	0	1	0	0	1	140.00	140.00	93.33	46.67	23.33	46.67	+/- 0.25% Center	
	0	1	0	1	0	118.00	118.00	78.67	39.33	19.67	39.33	+/- 0.25% Center	
	0	1	0	1	1	124.00	124.00	82.67	41.33	20.67	41.33	+/- 0.25% Center	
	0	1	1	0	0	133.70	133.70	89.13	44.57	22.28	44.57	+/- 0.25% Center	
	0	1	1	0	1	137.00	137.00	91.33	45.67	22.83	45.67	+/- 0.25% Center	
	0	1	1	1	0	150.00	112.50	75.00	37.50	18.75	37.50	+/- 0.25% Center	
	0	1	1	1	1	72.50	108.75	72.50	36.25	18.13	36.25	+/- 0.25% Center	
	1	0	0	0	0	75.00	112.50	75.00	37.50	18.75	37.50	+/- 0.25% Center	
	1	0	0	0	1	83.00	83.00	27.67	13.83	6.92	13.83	+/- 0.25% Center	
	1	0	0	1	0	110.00	110.00	73.33	36.67	18.33	36.67	+/- 0.25% Center	
	1	0	0	1	1	120.00	120.00	80.00	40.00	20.00	40.00	+/- 0.25% Center	
	1	0	1	0	0	125.00	125.00	83.33	41.67	20.83	41.67	+/- 0.25% Center	
	1	0	1	0	1	69.25	103.88	69.25	34.63	17.31	34.63	+/- 0.25% Center	
	1	0	1	1	0	70.00	105.00	70.00	35.00	17.50	35.00	+/- 0.25% Center	
	1	0	1	1	1	76.67	115.00	76.67	38.33	19.17	38.33	+/- 0.25% Center	
	1	1	0	0	0	145.00	145.00	96.67	48.33	24.17	48.33	+/- 0.25% Center	
	1	1	0	0	1	66.50	99.75	66.50	33.25	16.63	33.25	+/- 0.25% Center	
	1	1	0	1	0	150.00	150.00	100.00	50.00	25.00	50.00	+/- 0.25% Center*	
	1	1	0	1	1	99.75	99.75	66.50	33.25	16.63	33.25	+/- 0.25% Center*	
	1	1	1	0	0	155.00	155.00	103.33	51.67	25.83	51.67	+/- 0.25% Center	
	1	1	1	0	1	166.50	166.50	111.00	55.50	27.75	55.50	+/- 0.25% Center	
	1	1	1	1	0	153.33	115.00	76.67	38.33	19.17	38.33	+/- 0.25% Center	
	1	1	1	1	1	133.00	99.75	66.50	33.25	16.63	33.25	+/- 0.25% Center*	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 2, 7:4												0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled ± 0.25% Center Spread												1
Bit 0	0 - Running 1- Tristate all outputs												0

Note 1: Default at power-up will be for latched logic inputs to define frequency (Bit 3 = 0).

* These frequencies with spread enabled are equal to original Intel defined frequencies with -0.5% down spread.

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Byte 1: Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS3#
Bit 6	-	X	FS0#
Bit 5	-	X	FS2#
Bit 4	28	X	24_48MHz, 0 = 24MHz
Bit 3	27	1	48MHz_1
Bit 2	26	1	48MHz_0
Bit 1	-	1	(Reserved)
Bit 0	31	1	SDRAM_F

Byte 2: SDRAM, Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	32	1	SDRAM7
Bit 6	33	1	SDRAM6
Bit 5	35	1	SDRAM5
Bit 4	36	1	SDRAM4
Bit 3	37	1	SDRAM3
Bit 2	39	1	SDRAM2
Bit 1	40	1	SDRAM1
Bit 0	41	1	SDRAM0

Byte 3: PCI, Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	20	1	PCICLK7
Bit 6	19	1	PCICLK6
Bit 5	17	1	PCICLK5
Bit 4	16	1	PCICLK4
Bit 3	15	1	PCICLK3
Bit 2	13	1	PCICLK2
Bit 1	12	1	PCICLK1
Bit 0	11	1	PCICLK0

Byte 4: Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	8	1	3V66_1
Bit 5	7	1	3V66_0
Bit 4	-	X	FREQ_IOAPIC#
Bit 3	47	1	IOAPIC
Bit 2	-	X	FS1#
Bit 1	44	1	CPUCLK1
Bit 0	45	1	CPUCLK0

Byte 5: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	1	Reserved
Bit6	-	1	Reserved
Bit5	-	1	Reserved
Bit4	-	1	Reserved
Bit3	-	1	Reserved
Bit2	-	1	Reserved
Bit1	-	1	Reserved
Bit0	-	1	Reserved

Notes:
1. Disable means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Byte 6: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

Note: Don't write into this register. Writing into this register can cause malfunction

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-96 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, then only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

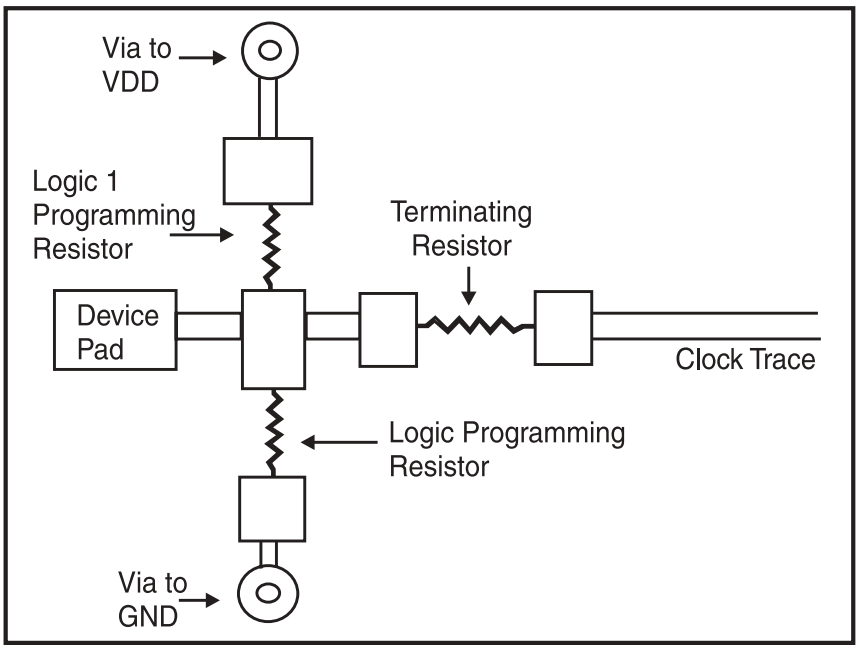
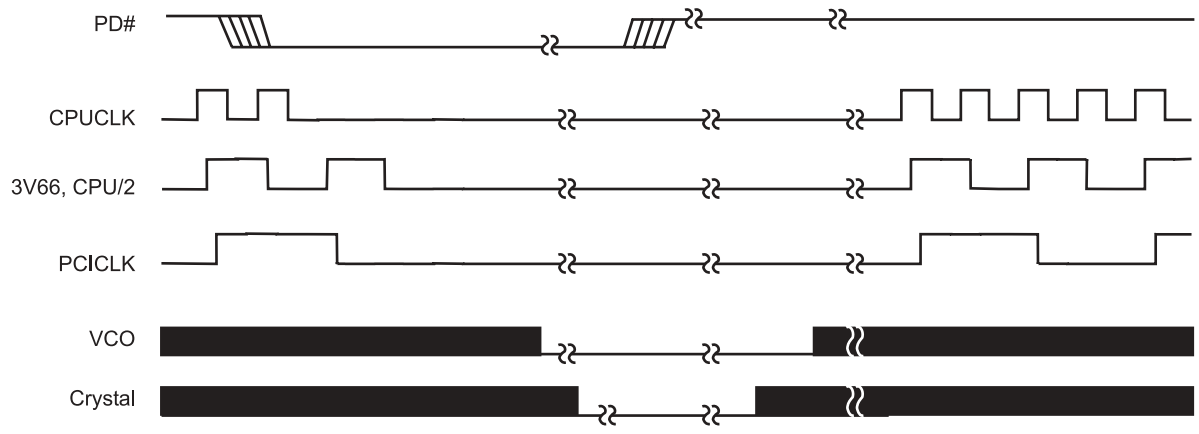


Fig. 1

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low, all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 ms. The power down latency should be as short as possible but conforming to the sequence requirements shown below. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

Absolute Maximum Ratings

Core Supply Voltage . . . . . 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Group Timing Relationship Table

Group	CPU 66MHz		CPU 100MHz		CPU 133MHz	
	Offset	Tolerance	Offset	Tolerance	Offset	Tolerance
CPU to SDRAM	2.5ns	500ps	5.0ns	500ps	0.0ns	500ps
CPU to 3V66	7.5ns	500ps	5.0ns	500ps	0.0ns	500ps
SDRAM to 3V66	0.0ns	500ps	0.0ns	500ps	0.0ns	500ps
3V66 to PCI	1.5-3.5ns	500ps	1.5-3.5ns	500ps	1.5-3.5ns	500ps
PCI to PCI	0.0ns	1.0ns	0.0ns	1.0ns	0.0ns	1.0ns
USB & DOT	Async	N/A	Async	N/A	Async	N/A

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			
Operating Supply Current	$I_{DD3.3OP}$	C_L = Max loads; CPU @ 66 MHz; SDRAM @ 100 MHz		300	340	mA
	$I_{DD2.5OP}$			12	15	
	$I_{DD3.3OP}$	C_L = Max loads; CPU @ 100 MHz; SDRAM @ 100 MHz		300	350	mA
	$I_{DD2.5OP}$			25	30	
	$I_{DD3.3OP}$	C_L = Max loads; CPU @ 133 MHz; SDRAM @ 133 MHz		300	420	mA
	$I_{DD2.5OP}$			35	40	
Power Down Supply Current	$I_{DD3.3PD}$	C_L = Max loads; V_{IN} = V_{DD} or GND		300	600	µA
Input Frequency	F_i	V_{DD} = 3.3 V		14.31818		MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition time[1]	T_{trans}	To 1st crossing of target frequency			3	ms
Settling time[1]	T_s	From 1st crossing to 1% target frequency			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target frequency			3	ms

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70°C; V_{DDL} = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP2B}	$V_O = V_{DD}/2$	13.5	14	45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2	2.5		V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA		0.2	0.4	V
Output High Current	I_{OH}	V_{OH} = 1.0 V		-85	-27	mA
		V_{OH} = 2.375 V	-27	-9		
Output Low Current	I_{OL}	V_{OL} = 1.2 V	27	68		mA
		V_{OL} = 0.3 V		20	30	
Rise Time[1]	t_r	0.4 V to 2.0 V	0.5	1.1	2	ns
Fall Time[1]	t_f	2.0 V to 0.4 V	0.5	1.1	2	ns
Duty Cycle[1]	d_t	V_T = 1.25 V	45	50	55	%
Skew window[1]	t_{sk}	V_T = 1.25 V		50	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc}$	V_T = 1.25 V; 66 MHz < f_{CPU} < 133 MHz f_{SDRAMb}= 100 MHz or 133 MHz Spread ON or OFF		200	250	ps

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP1B}	$V_O = V_{DD}/2$	12	18	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4	3.3		V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA		0.1	0.4	V
Output High Current	I_{OH1}	V_{OH} = 1.0 V		-136	-33	mA
		V_{OH} = 3.135 V	-33	-13		
Output Low Current	I_{OL1}	V_{OL} = 1.95 V	30	115		mA
		V_{OL} = 0.4 V		28	38	
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.2	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.3	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	53.6	55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V		37	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		280	500	ps

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70°C; V_{DDL} = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP2B}	$V_O = V_{DD}/2$	13.5	14	45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2	2.5		V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA		0.2	0.4	V
Output High Current	I_{OH}	V_{OH} = 1.0 V	-27			mA
		V_{OH} = 2.375 V		-9	-27	
Output Low Current	I_{OL}	V_{OL} = 1.2 V	27	68		mA
		V_{OL} = 0.3 V		20	30	
Rise Time[1]	t_r	0.4 V to 2.0 V	0.5	1.1	2	ns
Fall Time[1]	t_f	2.0 V to 0.4 V	0.5	1.1	2	ns
Duty Cycle[1]	d_t	V_T = 1.25 V	45	50	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc4B}$	V_T = 1.25 V		130	500	ps

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 20-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP3}	$V_O = V_{DD}/2$	10		24	Ω
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4	3.3		V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA		0.01	0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V	-54	-124		mA
		V_{OH} = 3.135 V		-20	-46	
Output Low Current	I_{OL3}	V_{OL} = 1.0 V	54	105		mA
		V_{OL} = 0.4 V		46	53	
Rise Time[1]	t_{r3}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1	1.6	ns
Fall Time[1]	t_{f3}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1	1.6	ns
Duty Cycle[1]	d_{t3}	V_T = 1.5 V	45	53	55	%
Skew window[1]	t_{sk3}	V_T = 1.5 V		98	250	ps
Jitter[1]	$t_j$cyc-cyc	V_T = 1.5 V		170	250	ps

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP1B}	$V_O = V_{DD}/2$	11	25	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4	3.2		V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA		0.1	0.55	V
Output High Current	I_{OH1}	V_{OH} = 1.0 V	-33	-136		mA
		V_{OH} = 3.135 V		-13	-33	
Output Low Current	I_{OL1}	V_{OL} = 1.95 V	30	115		mA
		V_{OL} = 0.4 V		38	38	
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.3	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.6	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	51.6	55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V		330	500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		145	500	ps

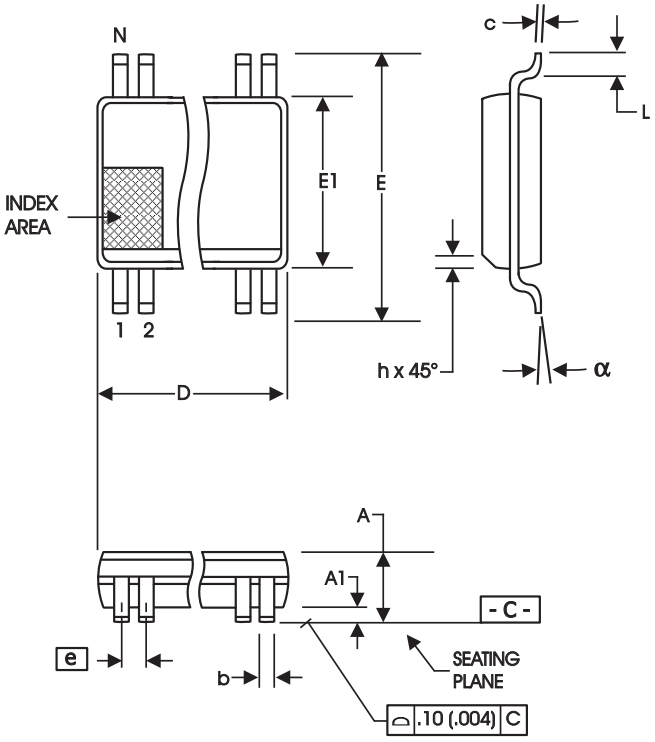
[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - REF, 48MHz_0 (Pin 26)

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP5}	$V_O = V_{DD}/2$	20	22	60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -1 mA	2.4	3.2		V
Output Low Voltage	V_{OL5}	I_{OL} = 1 mA		0.1	0.4	V
Output High Current	I_{OH5}	V_{OH} = 1.0 V	-29	-136		mA
		V_{OH} = 3.135 V		-13	-23	
Output Low Current	I_{OL5}	V_{OL} = 1.95 V	29	115		mA
		V_{OL} = 0.4 V			27	
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.2	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.2	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	53	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V; 48MHz		200	500	ps
		V_T = 1.5 V; REF		780	1000	ps

[1]Guaranteed by design and characterization, not 100% tested in production.



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS9248yF-96LF-T

Example:

ICS XXXX y F LF- T

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0311D—04/23/04