



# FDS86242

## N-Channel PowerTrench® MOSFET

150 V, 4.1 A, 67 mΩ

### Features

- Max  $r_{DS(on)}$  = 67 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 4.1\text{ A}$
- Max  $r_{DS(on)}$  = 98 mΩ at  $V_{GS} = 6\text{ V}$ ,  $I_D = 3.3\text{ A}$
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- 100% UIL Tested
- RoHS Compliant

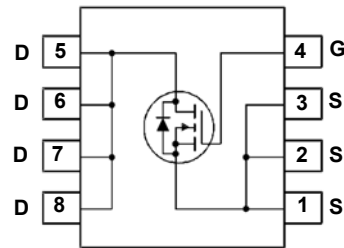
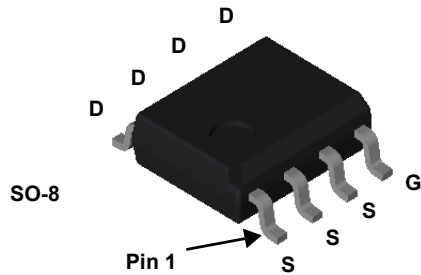


### General Description

This N-Channel MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

### Applications

- DC/DC converters and Off-Line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	4.1	A
	-Pulsed	20	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	40	mJ
$P_D$	Power Dissipation $T_C = 25\text{ °C}$ (Note 1)	5.0	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS86242	FDS86242	SO-8	13 "	12 mm	2500 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		104		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2	3.5	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		-10		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 4.1\ \text{A}$		56.3	67	m $\Omega$
		$V_{GS} = 6\ \text{V}, I_D = 3.3\ \text{A}$		73.8	98	
		$V_{GS} = 10\ \text{V}, I_D = 4.1\ \text{A}, T_J = 125^\circ\text{C}$		107	126	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\ \text{V}, I_D = 4.1\ \text{A}$		11		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 75\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1\ \text{MHz}$		570	760	pF
$C_{oss}$	Output Capacitance			64	85	pF
$C_{rss}$	Reverse Transfer Capacitance			2.9	5	pF
$R_g$	Gate Resistance			0.5		$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\ \text{V}, I_D = 4.1\ \text{A},$ $V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		7.9	16	ns	
$t_r$	Rise Time			1.5	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			13	23	ns	
$t_f$	Fall Time			2.8	10	ns	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\ \text{V to } 10\ \text{V}$		8.9	13	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V to } 5\ \text{V}$	$V_{DD} = 75\ \text{V},$ $I_D = 4.1\ \text{A}$		4.9	7	nC
$Q_{gs}$	Gate to Source Charge				3.0		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				2.0		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 4.1\ \text{A}$ (Note 2)		0.81	1.3	V
		$V_{GS} = 0\ \text{V}, I_S = 2\ \text{A}$ (Note 2)		0.77	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 4.1\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		61	98	ns
$Q_{rr}$	Reverse Recovery Charge			71	114	nC

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $50^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.  
3. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\ \text{mH}$ ,  $I_{AS} = 9\ \text{A}$ ,  $V_{DD} = 135\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$ .

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

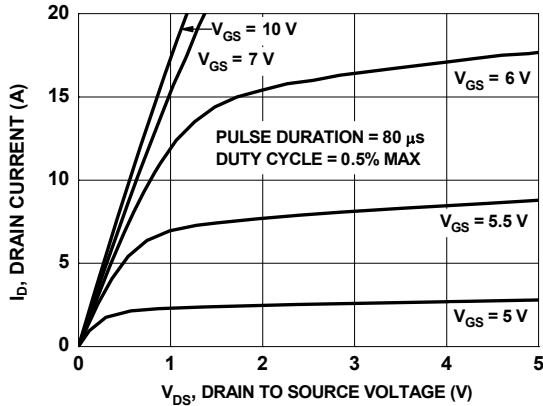


Figure 1. On-Region Characteristics

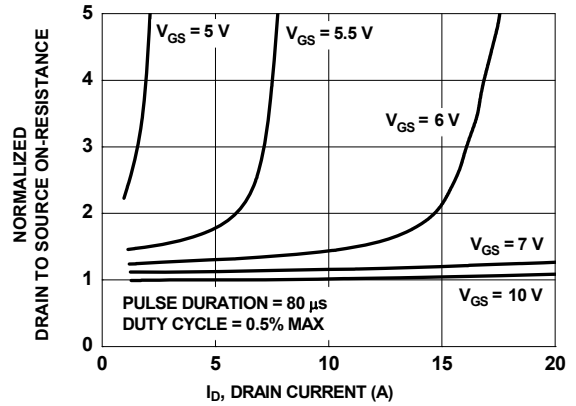


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

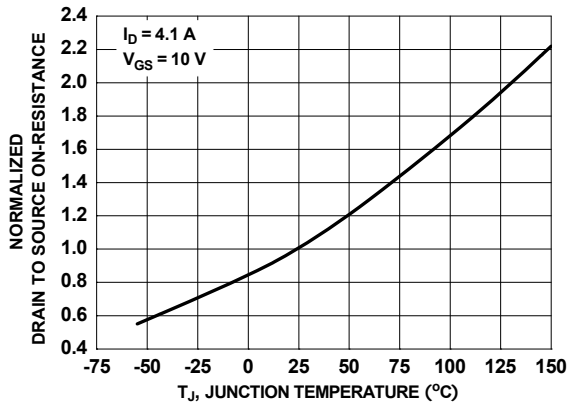


Figure 3. Normalized On-Resistance vs Junction Temperature

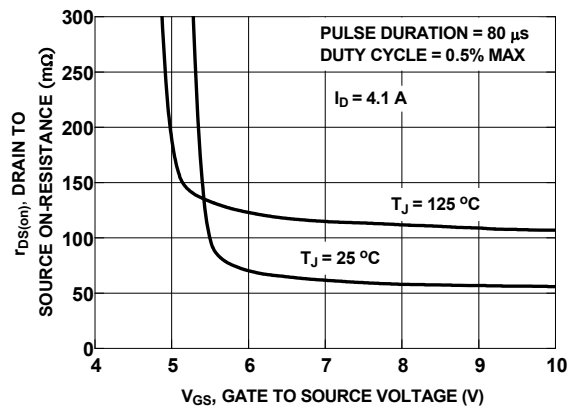


Figure 4. On-Resistance vs Gate to Source Voltage

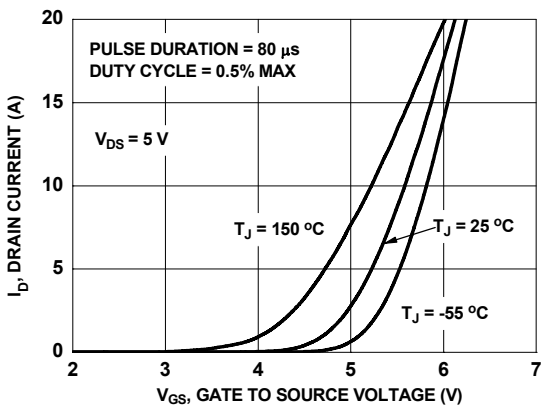


Figure 5. Transfer Characteristics

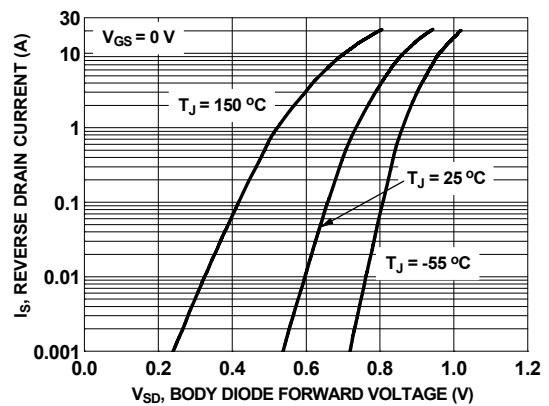
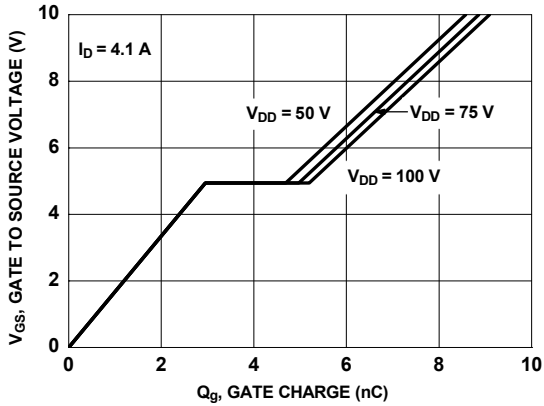
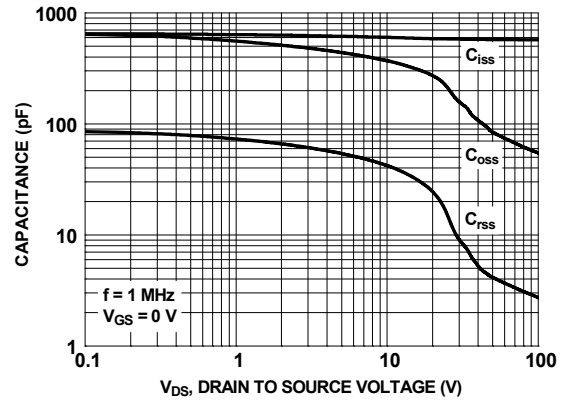


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

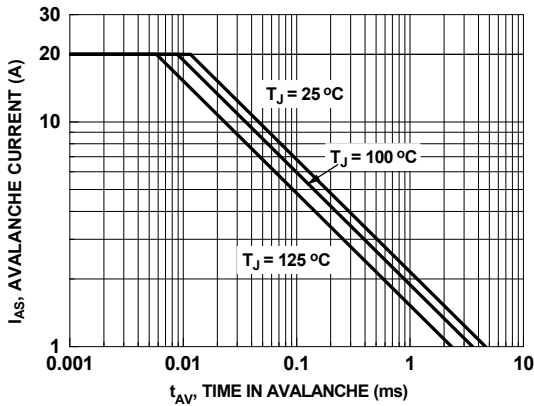
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



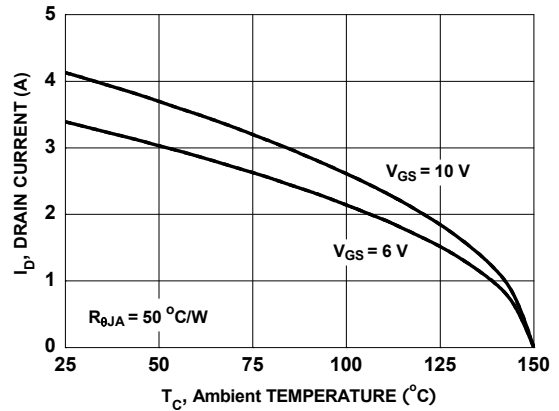
**Figure 7. Gate Charge Characteristics**



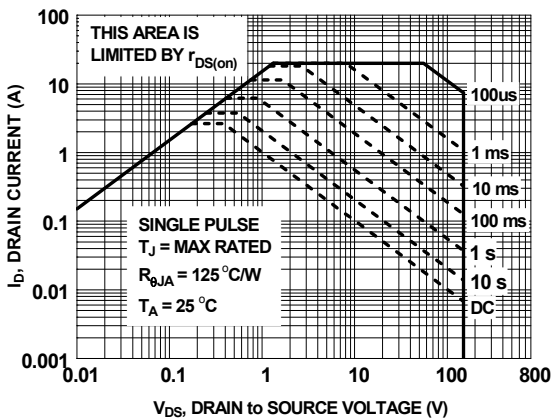
**Figure 8. Capacitance vs Drain to Source Voltage**



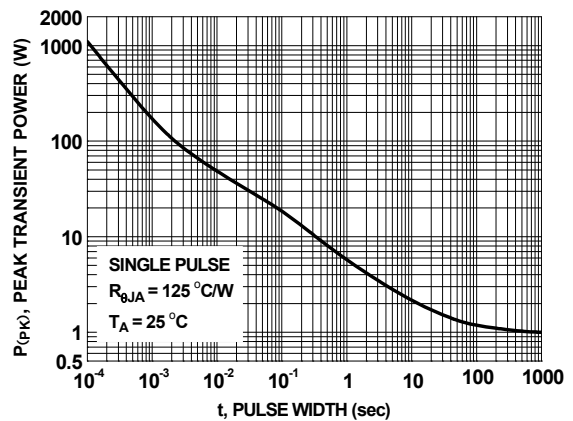
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

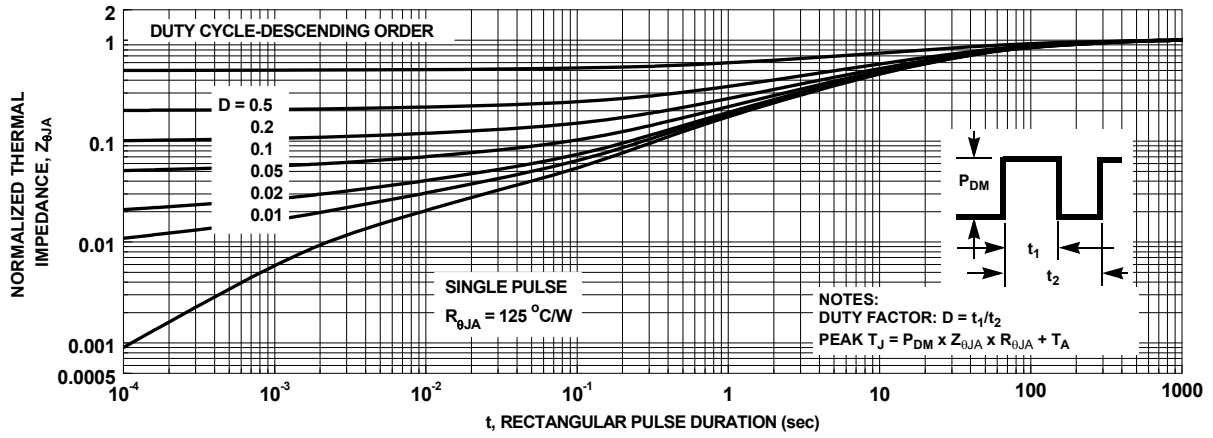


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



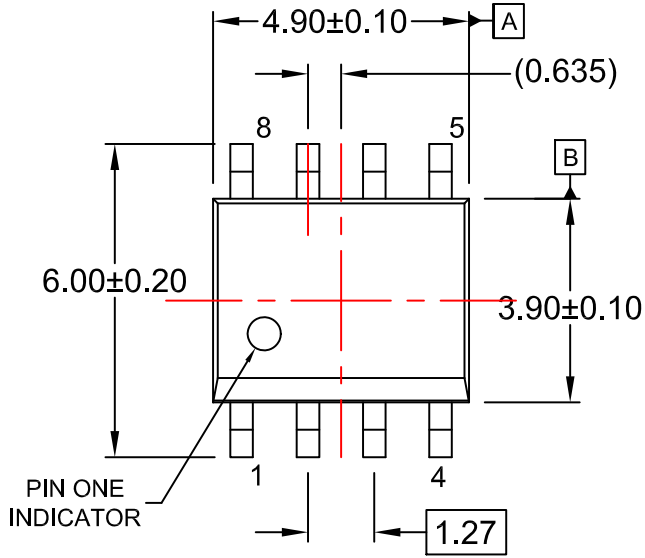
**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**

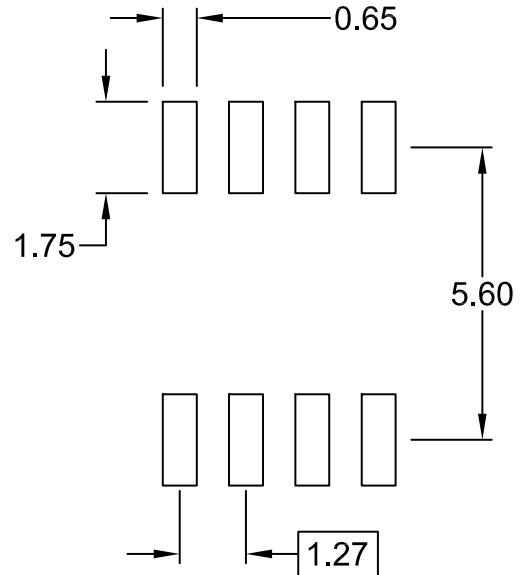
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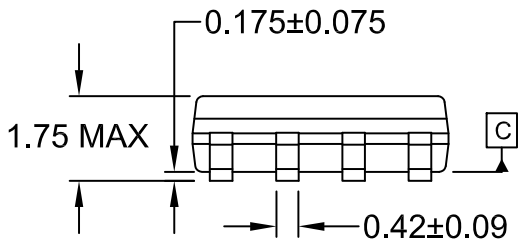
**SOIC8**  
**CASE 751EB**  
**ISSUE A**



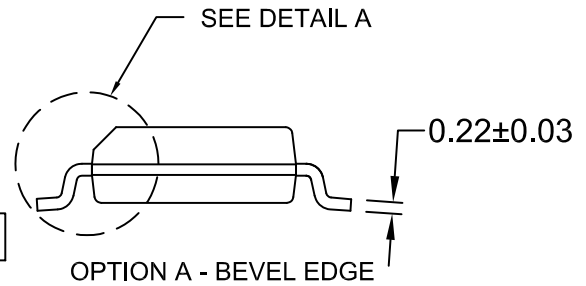
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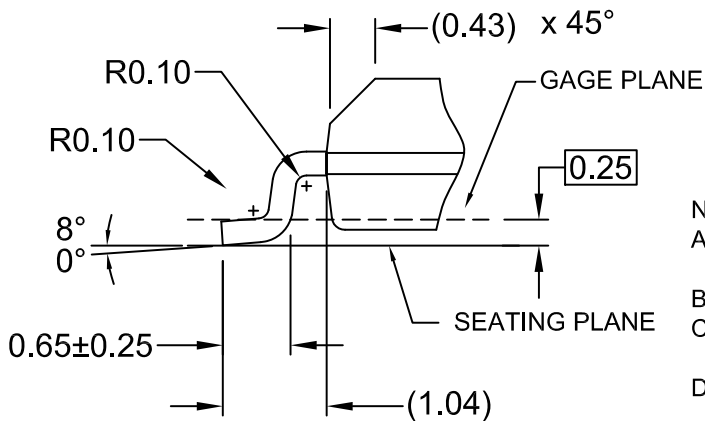
LAND PATTERN RECOMMENDATION



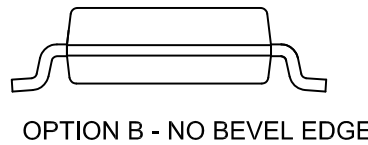
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OPTION A - BEVEL EDGE




**DETAIL A**  
 SCALE: 2:1



OPTION B - NO BEVEL EDGE

- NOTES:
- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
  - D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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