Over-Voltage and Over-Current Charger Protection IC With Integrated Charging FET and LDO Mode

Check for Samples: bq24351

FEATURES

- **Robust Protection**
  - **Input Over-Voltage Protection**
  - **Input Over-Current Protection**
  - **Accurate Battery Over-Voltage Protection**
  - **Thermal Shutdown**
  - **Output Short-Circuit Protection**
- **Integrated Charging FET**
- **10.5V Over-Voltage Protection**
- **LDO Mode Operation**
  - **6.38V Output Voltage Regulation**
- **Current Limited Power Supply for Host Controller**
- **Soft-Start to Prevent Inrush Currents**
- **Soft-Stop to Prevent Voltage Spikes**
- **30V Maximum Input Voltage**
- **Supports Up to 1A Load Current**
- **Small 2mm × 2mm 8pin SON Package**

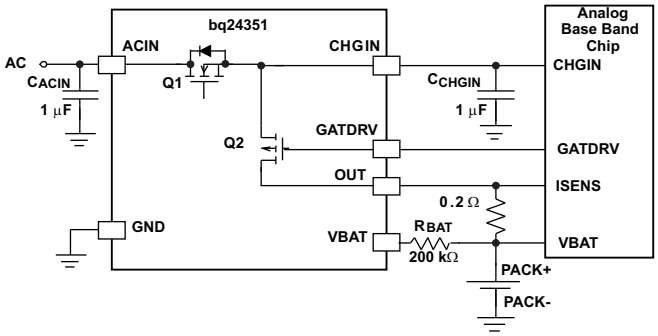
APPLICATIONS

- **Mobile Phones**
- **Low-Power Handheld Devices**

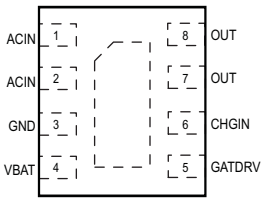
DESCRIPTION

The bq24351 is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage and the battery voltage. In case of an input over-voltage condition, the IC will turn off the internal power FET after a blanking time. If the battery voltage rises to unsafe levels during charging process, power is removed from the system. If the input current exceeds the over current threshold for a limited time, the IC will turn off the output power. The integrated charging FET can regulate the charge voltage and current according to the control from the host. The device can also provide a voltage source with over voltage and over current protection for host controller.

TYPICAL APPLICATION CIRCUIT



PIN ASSIGNMENT



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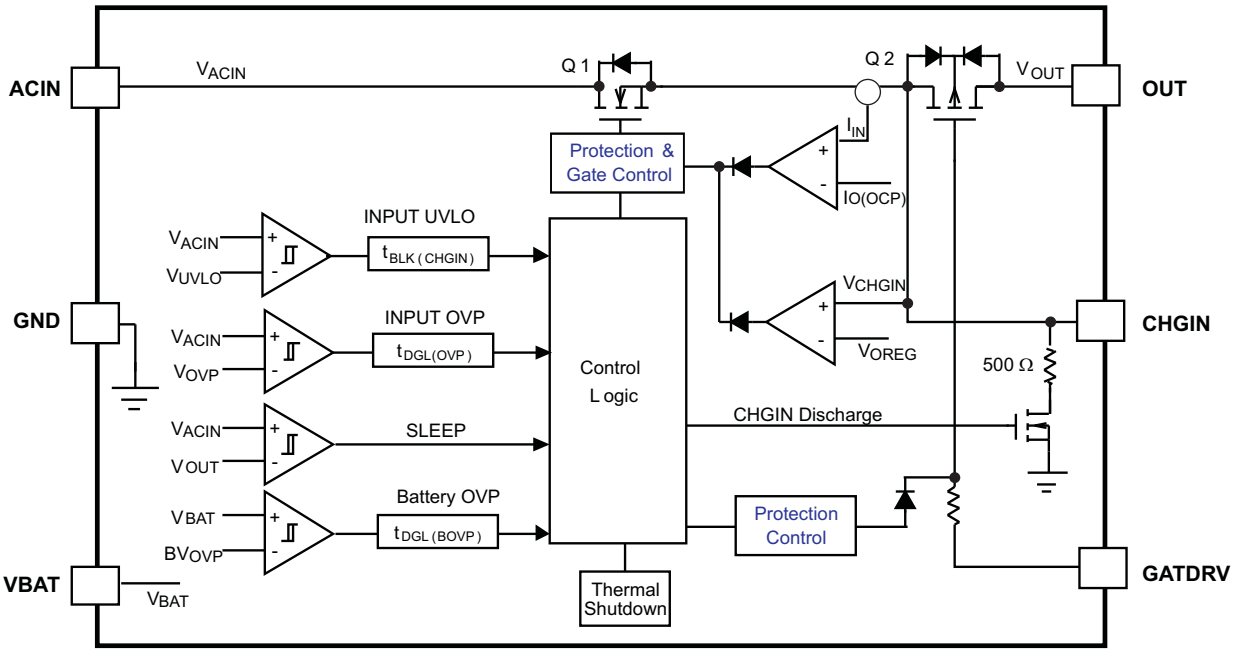
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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
ACIN	1,2	I	Power Supply Input, connect to an external DC supply. Connect an external 1-μF ceramic capacitor (minimum) to GND.
OUT	7,8	O	Output terminal to the charging system.
VBAT	4	I	Battery voltage sense input. Connected to pack positive terminal through a resistor. Connected to ground if battery OVP function is not used.
GATDRV	5	I	P-FET gate drive input , connected to gate drive pin of the host charger controller
CHGIN	6	O	Output power pin for power input of host charger controller. Connect an external ceramic bypass capacitor (1.0-μF minimum) to GND.
GND	3	–	Ground terminal
Thermal PAD			There is an internal electrical connection between the exposed thermal pad and the GND pin of the device. The thermal pad must be connected to the same potential as the GND pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. GND pin must be connected to ground at all times.

ORDERING INFORMATION(1)

PART NUMBER	MARKING	MEDIUM	QUANTITY	PACKAGE	INPUT OVP THRESHOLD
bq24351DSGR	QUO	Tape and Reel	3000	2mm × 2mm SON	10.5 V
bq24351DSGT	QUO	Tape and Reel	250	2mm × 2mm SON	10.5 V

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE / UNIT
Input voltage	ACIN (with respect to GND)	–0.3 V to 30 V
Output voltage	OUT, CHGIN (with respect to GND)	–0.3 V to 7V
Input voltage	VBAT, GATDRV (with respect to GND)	–0.3 V to 7 V
Input current	ACIN	–1.8 A(2) to 1.4 A
Junction temperature, T_J		–40°C to 150°C
Storage temperature, T_{STG}		–65°C to 150°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) Reverse current is specified for a maximum of 50 hours at T_J < 150°C.

THERMAL INFORMATION

THERMAL METRIC(1)		bq24351 SON 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	61.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	61.3	
θ_{JB}	Junction-to-board thermal resistance(4)	15.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.4	
ψ_{JB}	Junction-to-board characterization parameter(6)	15.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	8.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNITS
V_{ACIN}	ACIN voltage range	4.4	15	V
I_{ACIN}	Current, ACIN pin		1	A
T_J	Junction temperature	–40	125	°C

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ELECTRICAL CHARACTERISTICS

Refer to the typical application circuit shown in Figure 1 . These specifications apply over ACIN = 5V, T_J = -40 to 125°C, unless otherwise specified. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACIN						
V_{UVLO}	Under-voltage lock-out threshold	ACIN: 3V → 2V, ACIN falling	1.8	1.95	2.1	V
		ACIN: 2V → 3V, ACIN rising	2.5			
$t_{BLK(CHGIN)}$	Input power on blanking time	ACIN rising to CHGIN rising		10		ms
I_{DD}	Operating current	No load on OUT and CHGIN pin			500	µA
INPUT TO OUTPUT CHARACTERISTICS						
	On resistance from ACIN to OUT	I_{OUT} = 1.0A, ACIN = 5V, GATDRV = 0V		415	685	mΩ
	On resistance from ACIN to CHGIN	I_{CHGIN} = 1.0A, ACIN = 5V, I_{OUT} = 0A		250	495	mΩ
INPUT OVER-VOLTAGE PROTECTION (OVP)						
V_{OREG}	CHGIN voltage in LDO mode	ACIN = 7.1V, GATDRV = CHGIN, I_{CHGIN} = 0 to 1A	6.25	6.38	6.52	V
V_{OVP}	Input OVP threshold	ACIN rising	10.2	10.5	10.8	V
$V_{HYS-OVP}$	Input OVP recovery hysteresis	ACIN: 12V → 9V	145	160	175	mV
$t_{DGL(OVP)}$	Input OVP deglitch time	ACIN rising to CHGIN falling		256		µS
$t_{REC(OVP)}$	Input OVP recovery time	ACIN falling below V_{OVP} to CHGIN rising		8.2		ms
INPUT OVER CURRENT LIMITING AND PROTECTION (OCP)						
$I_{O(OCP)}$	OCP threshold		1.02	1.2	1.38	A
$t_{DGL(OCP)}$	OCP blanking time			176		µs
$t_{REC(OCP)}$	OCP recovery time			131		ms
BATTERY OVER-VOLTAGE PROTECTION						
BV_{OVP}	Battery OVP threshold	VBAT rising	4.3	4.35	4.4	V
$V_{HYS-BOVP}$	Battery OVP hysteresis	VBAT falling	200	250	300	mV
I_{VBAT}	VBAT pin leakage current	VBAT = 4.25V, series connection of a 200-kΩ resistor, T_J = 25°C			10	nA
$t_{DGL(BOVP)}$	Battery OVP deglitch time	VBAT rising to CHGIN falling		8.2		ms
$t_{REC(BOVP)}$	Battery OVP recovery time	VBAT falling below BVOVP to CHGIN rising		131		ms
CHGIN						
V_{SEXIT}	Sleep mode exit threshold and CHGIN turn on threshold, ACIN-OUT	ACIN rising, OUT = 4.2 V	24	90	160	mV
V_{SENTRY}	Sleep mode entry threshold and CHGIN turn off threshold, ACIN-OUT	ACIN falling, OUT = 4.2 V	10	55	105	mV
I_{DDSLP}	Sleep mode supply current	OUT = 4.2 V, GATDRV = 4.2 V, ACIN = VSS			10	µA
R_{DIS}	CHGIN discharge resistor			500		Ω
	Leakage current from OUT to CHGIN	OUT = 4.2 V, GATDRV = 4.2 V, CHGIN = 0 V, ACIN = 0 V, T_J = 85°C			1	µA
INTEGRATED P-FET PARAMETERS						
Vt	Threshold voltage, CHGIN-GATDRV	CHGIN = 5V, OUT = 3.6V, I_{OUT} = 10mA	500	680	800	mV
Ig	GATDRV pin leakage current			0.1	1	µA
Ioff	Off state leakage current at OUT pin	ACIN = 5V, GATDRV = CHGIN, OUT = 0V		1		µA
Ronp	On resistance of P-FET (from CHGIN to OUT)	I_{OUT} = 1.0A, ACIN = 5V, GATDRV = 0V		165	225	mΩ
Gm	Forward transconductance	ACIN = 5V, I_{OUT} = 5mA, GATDRV = 3.5V		27		mA/V
Cg	Input capacitance at the GATDRV pin	CHGIN = GATDRV = 5V		104		pF
THERMAL PROTECTION						
$T_{J(OFF)}$	Thermal shutdown threshold	Junction temperature rising	140	150	160	°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis	Junction temperature falling		20		°C

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TYPICAL APPLICATION CIRCUIT

ACIN = 5V, ICHARGE = 1A, VBAT = 4.2V

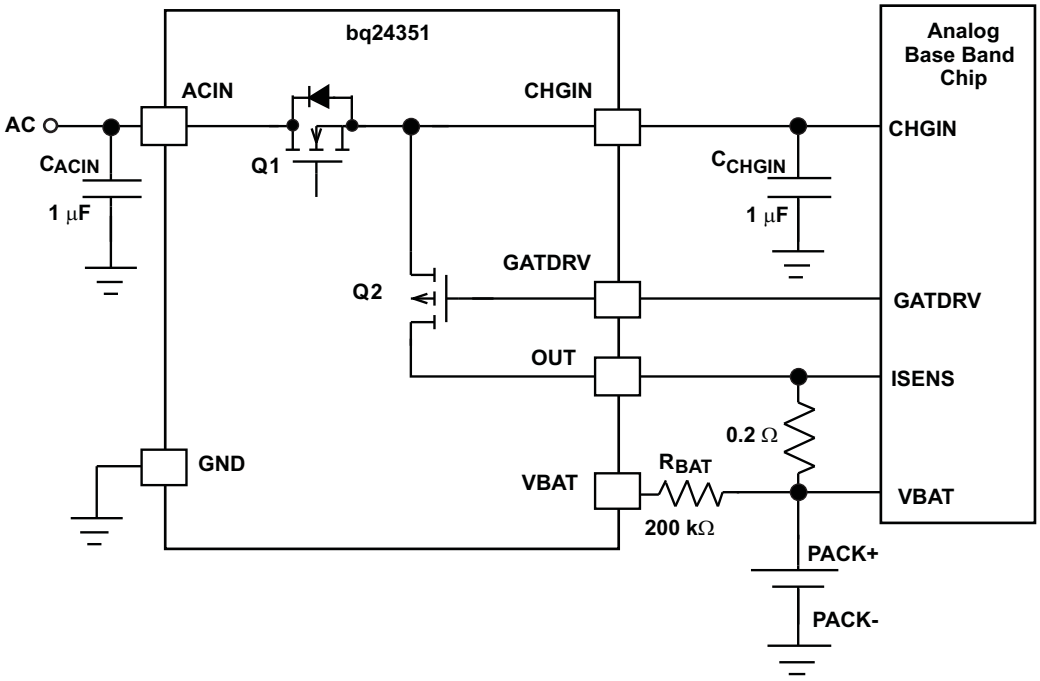


Figure 1. Host Controlled One-Cell Charger Application Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

Using circuit shown in typical application circuit Figure 1, T_A = 25°C, unless otherwise specified.

ACIN RAMP UP

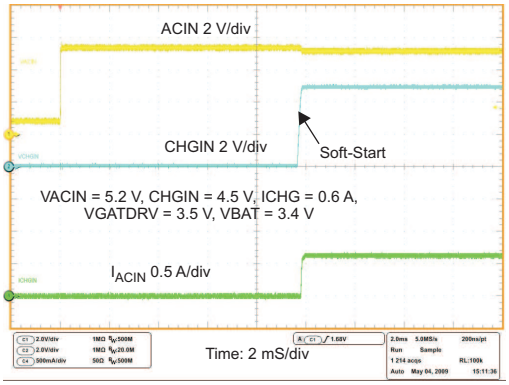


Figure 2.

ACIN RAMP DOWN

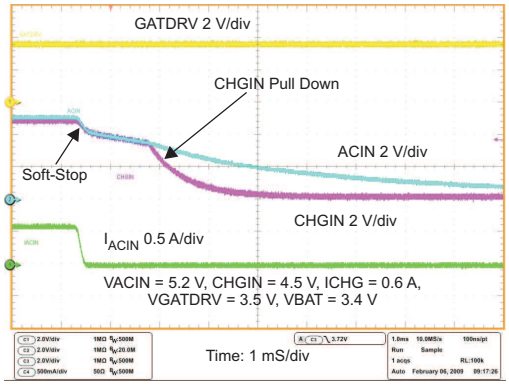


Figure 3.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

ACIN OVP (BLANKING TIME)

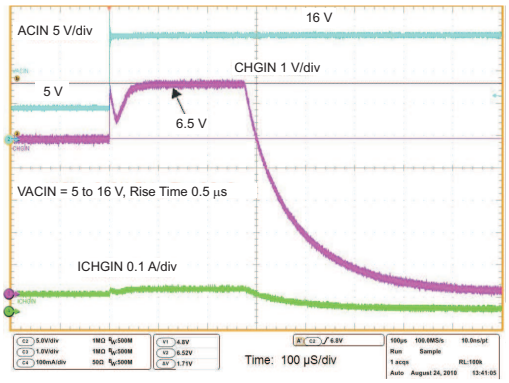


Figure 4.

ACIN OVP

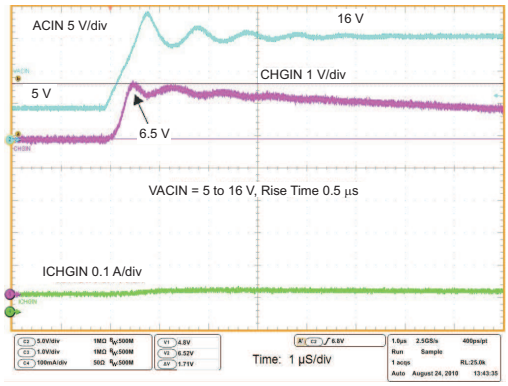


Figure 5.

ACIN OVP

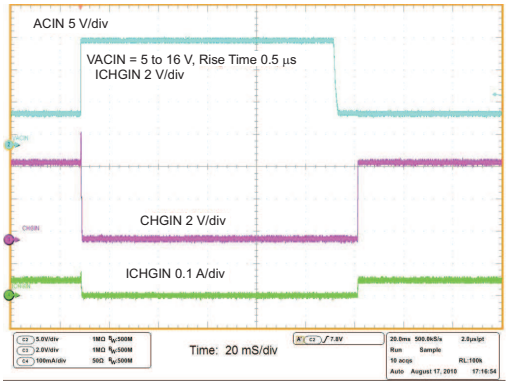


Figure 6.

CHGIN OCP

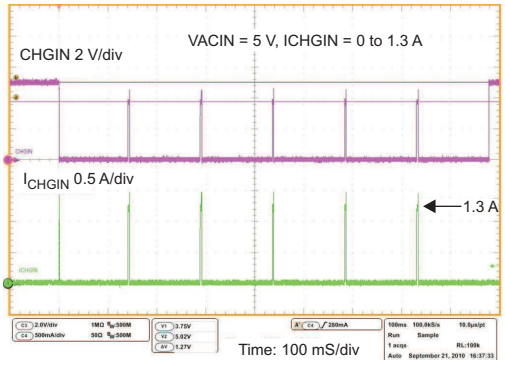


Figure 7.

CHGIN OCP

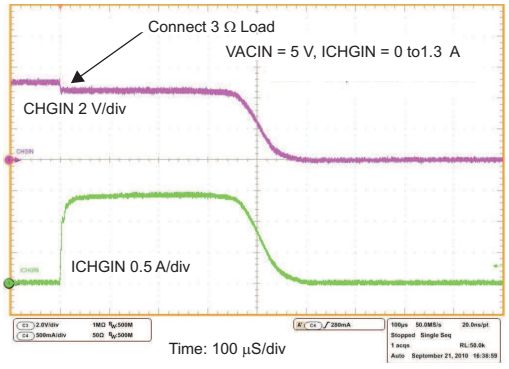


Figure 8.

BATTERY OVP

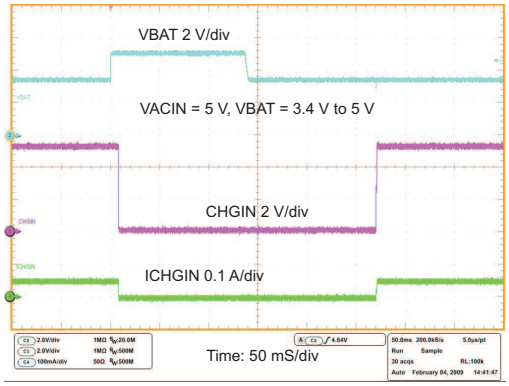


Figure 9.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

BATTERY OVP

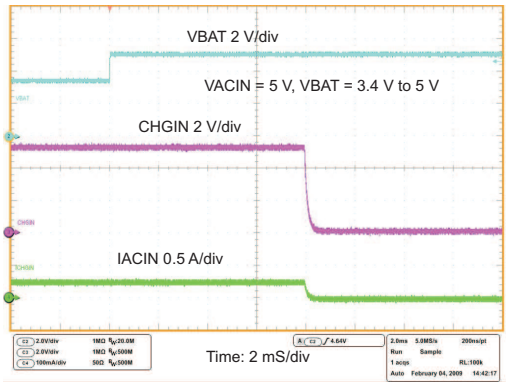


Figure 10.

Rdson vs Vgs

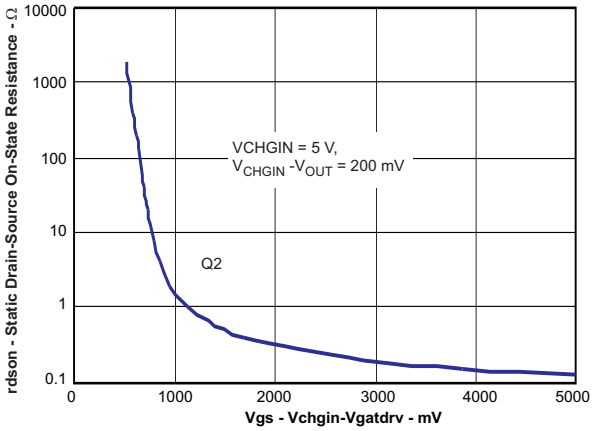


Figure 11.

FET ON RESISTANCE vs TEMPERATURE

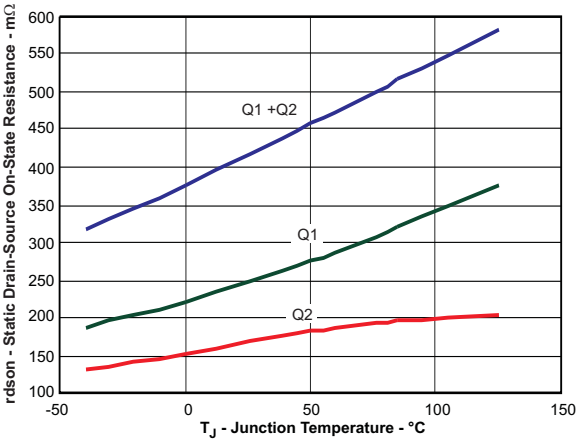


Figure 12.

BACKGROUND

During the charging process for portable devices, input voltage spikes usually happen when the AC/DC adaptor is plugged in, or charge current is cut off quickly under fault conditions, such as input OVP, OCP, or battery OVP and so on. The over voltage stress may damage the analog baseband chip which has lower voltage rating due to its increased complexity. Therefore, over voltage protection is needed for the safe operation of portable devices. Another challenge arises from the charge circuit that uses external charging FET in series with a reverse blocking diode as the charging device. The battery may not be fully charged when input voltage is low due to the additional diode voltage drop. bq24351 will provide the solution for above problems since it has input OVP, OCP, battery OVP function, together with integrated charging FET which will eliminate the reverse blocking diode in the previously mentioned charge circuit, as shown in Figure 1.

DETAILED FUNCTIONAL DESCRIPTION

The bq24351 is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage and the battery voltage. In case of an input over-voltage condition, the IC will turn off the internal power FET after a blanking time. If the battery voltage rises to unsafe levels during charging process, power is removed from the system. If the input current exceeds the over current threshold for a limited time, the IC will turn off the output power. The integrated charging FET can regulate the charge voltage and current according to the control from the host. The device can also provide a voltage source with over-voltage and over-current protection for host controller.

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POWER DOWN

The device remains in power down mode when the input voltage at the ACIN pin is below the under-voltage threshold V_{UVLO}. The FET Q1 and Q2 connected between ACIN and OUT pins are off.

POWER-ON RESET

The device resets when the input voltage at the ACIN pin exceeds the UVLO threshold. All internal counters and other circuit blocks are reset. The IC then waits for duration $t_{BLK(CHGIN)}$ for the input voltage to stabilize. If, after $t_{BLK(CHGIN)}$, the input voltage and battery voltage are in normal range, FET Q1 is turned ON. The IC has a soft-start feature to control the inrush current. The soft-start minimizes the ringing at the input, where the ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit. Once the soft-start sequence starts, the IC monitors the load current. If the load current is larger than $I_{O(OCP)}$ for more than $t_{DGL(OCP)}$, FET Q1 and Q2 are switched off. The IC then repeats the power-on sequence after $t_{REC(OCP)}$.

When a short-circuit is detected at power-on and Q1 is switched off, to prevent the input voltage from spiking up due to resonance between the inductance of the input cable and the input capacitor, Q1 is turned off slowly by reducing its gate-drive gradually, resulting in a “soft-stop”.

SLEEP MODE

When ACIN falls to below sleep mode entry threshold (V_{SENTRY}), the device operates in sleep mode and turns off Q1 and Q2 by internal circuit regardless of the gate drive signal from GARDRV pin. The device exits sleep mode when ACIN rising to above sleep mode exit threshold (V_{SEXIT}). In this way, the device behaves like a diode and no external reverse blocking diode is needed in the application circuit.

OPERATING

The device continuously monitors the input voltage, the input current and the battery voltage as described in detail below:

Input Over-Voltage Protection and LDO Mode Operation

The CHGIN output of the IC operates similar to a linear regulator. Figure 13 shows the typical input OVP performance. When the ACIN input voltage is less than $V_{O(REG)}$, and above the V_{UVLO}, the CHGIN output voltage tracks the input voltage with a voltage drop caused by RDS(on) of the protection FET Q1. When the ACIN input voltage is greater than $V_{O(REG)}$ plus the RDS(on) drop of Q1, and less than V_{OVP}, the CHGIN output voltage is regulated to $V_{O(REG)}$, and this is also referred as LDO mode operation. If the input voltage rises above V_{OVP}, the internal FET Q1 and Q2 are turned off after a blanking time of $t_{DGL(OVP)}$, removing power from the circuit. When the input voltage drops below $V_{OVP} – V_{HYS-OVP}$, and is still above V_{UVLO}, the FET Q1 and Q2 are turned on again after a deglitch time of $t_{REC(OVP)}$, which ensures that the input supply is stabilized when the IC starts up again.

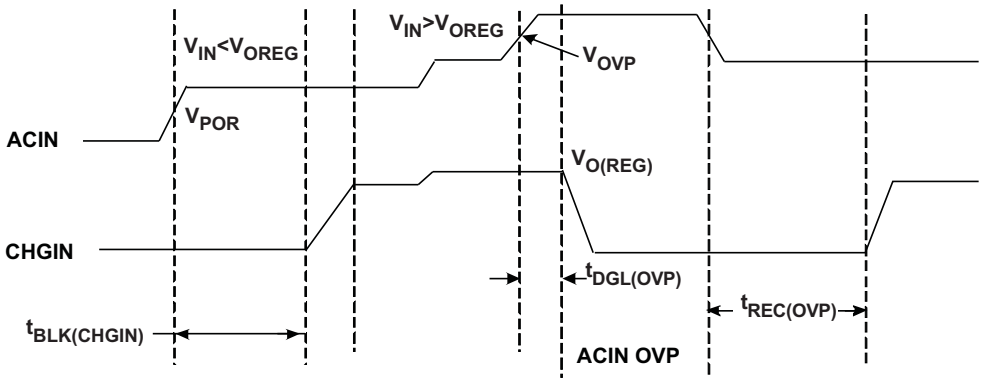


Figure 13. Input OVP Timing Diagram

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Over Current Limiting and Protection

The device includes a low drop out linear regulator. This current regulator uses Q1 as the controlling power device. Once the soft start sequence starts, the input current is limited to the Over Current Protection (OCP) threshold, IO(OCP). If the input current through the IC attempts to exceed the OCP threshold, the switch Q1 is opened only enough to maintain the current at the OCP level. Once the soft start sequence ends, the input current is no longer limited and can go beyond the OCP threshold. However, if the current remains above the OCP threshold for longer than the deglitch period, $t_{DGL(OCP)}$, both the switch Q1 and Q2 are opened completely, as shown in Figure 14. In this fault case, the switch Q1 is turned off slowly, typically taking 100 µS.

Once the OCP feature has been activated, the switch Q1 and Q2 will remain off for the OCP recovery time, $t_{REC(OCP)}$. Following this time the switch will turn on, using the soft start sequence. If the current through the IC remains below the OCP threshold, the switch will remain closed and normal operation resumes. If the current through the IC attempts to exceed the OCP threshold again, the operation described above repeats.

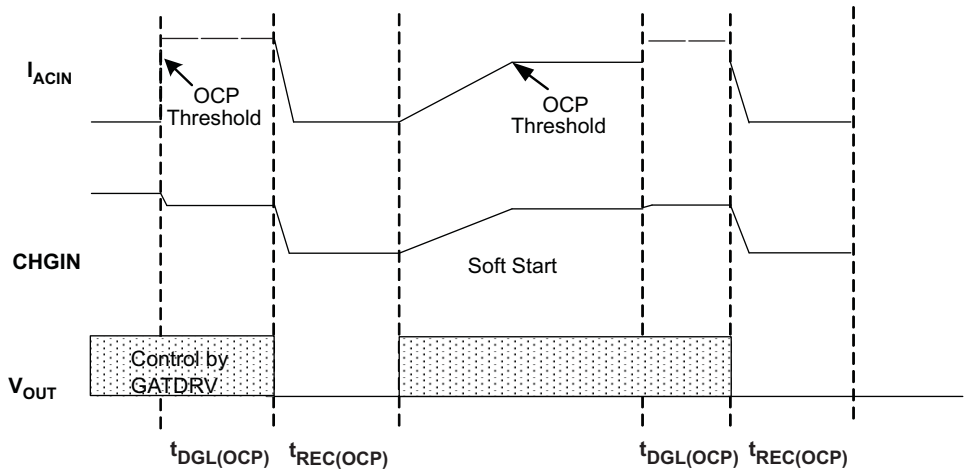


Figure 14. Charge Current OCP Timing Diagram

Battery Over-Voltage Protection

The battery over-voltage threshold, BV_{OVP}, is internally set to 4.35V. If the battery voltage exceeds the BV_{OVP} threshold, the FET Q1 and Q2 are turned off after a deglitch time of $t_{DGL(BOVP)}$. The FET is turned on once the battery voltage drops to $BV_{OVP} - V_{HYS-BOVP}$ and remains below this threshold for $t_{REC(BOVP)}$, as shown in Figure 15. In this battery over-voltage fault case, Q1 is switched OFF gradually for a smooth transient response.

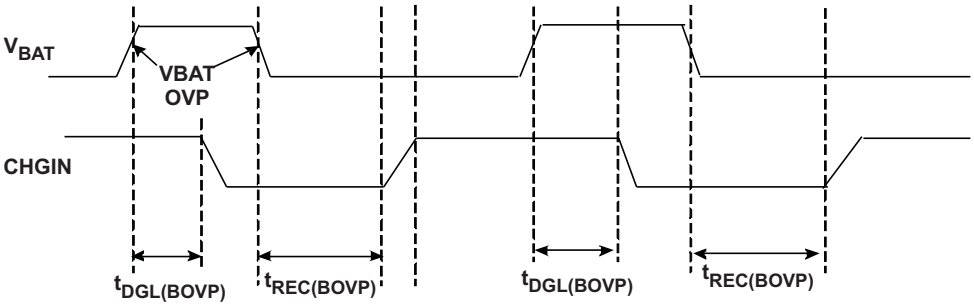


Figure 15. Battery OVP Timing Diagram

Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, the FET Q1 and Q2 are turned off. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

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APPLICATION INFORMATION

Selection of R_{BAT}

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the ACIN pin may appear on the VBAT pin. This voltage can be as high as 30V, and applying 30V to the battery in case of the failure of the device can be hazardous. Connecting the VBAT pin through R_{BAT} prevents a large current from flowing into the battery in case of failure of the IC. In the interests of safety, R_{BAT} should have a very high value. The problem with a large R_{BAT} is that the voltage drop across this resistor because of the VBAT bias current IVBAT causes an error in the BV_{OVP} threshold. This error is over and above the tolerance on the nominal 4.35V BV_{OVP} threshold.

Choosing R_{BAT} in the range 100kΩ to 470kΩ is a good compromise. In the case of IC failure, with R_{BAT} equal to 100kΩ, the maximum current flowing into the battery would be (30V – 3V) ÷ 100kΩ = 270μA, which is low enough to be absorbed by the bias currents of the system components. R_{BAT} equal to 100kΩ would result in a worst-case voltage drop of $R_{BAT} \times I_{VBAT} \neq$ 1mV. This is negligible compared to the internal tolerance of 50mV on the BV_{OVP} threshold.

If the Battery OVP function is not required, the VBAT pin should be connected to GND.

Selection of Input and Output Bypass Capacitors

The input capacitor C_{ACIN} is for decoupling, and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up. C_{ACIN} prevents the input voltage from overshooting to dangerous levels. It is strongly recommended that a ceramic capacitor of at least 1μF be used at the input of the device. It should be located in close proximity to the ACIN pin.

C_{CHGIN} should also be a ceramic capacitor of at least 1μF, located close to the CHGIN pin. C_{CHGIN} also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

PCB Layout Guidelines

1. This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this IC. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for the maximum voltages expected to be seen in the system.
2. The device uses SON packages with a PowerPAD™. For good thermal performance, the PowerPAD should be thermally coupled with the PCB ground plane. In most applications, this will require a copper pad directly under the IC. This copper pad should be connected to the ground plane with an array of thermal vias.
3. C_{ACIN} and C_{CHGIN} should be located close to the IC. Other components like R_{BAT} should also be located close to the IC.

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Changes from Original (October 2010) to Revision A **Page**

- Changed title from: Over-Voltage and Over-Current Charger Front-End Protection IC With Integrated Charging FET, to: Over-Voltage and Over-Current Charger Protection IC With Integrated Charging FET and LDO Mode 1
- Added 10.5V Over-Voltage Protection to Features 1
- Added 6.38V Output Voltage Regulation to Features 1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ24351DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QUO	Samples
BQ24351DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QUO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

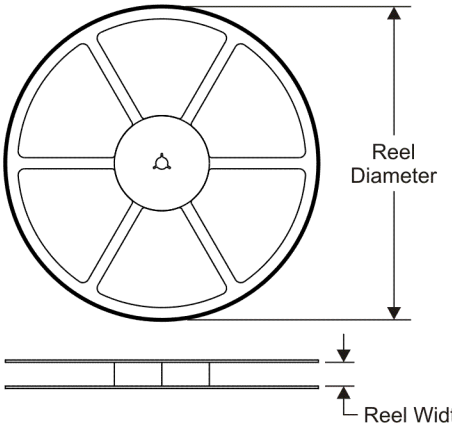
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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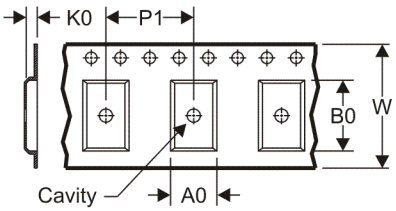
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

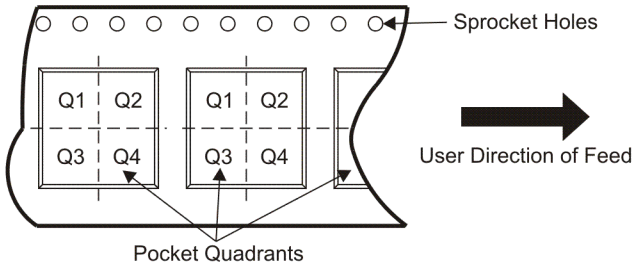


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

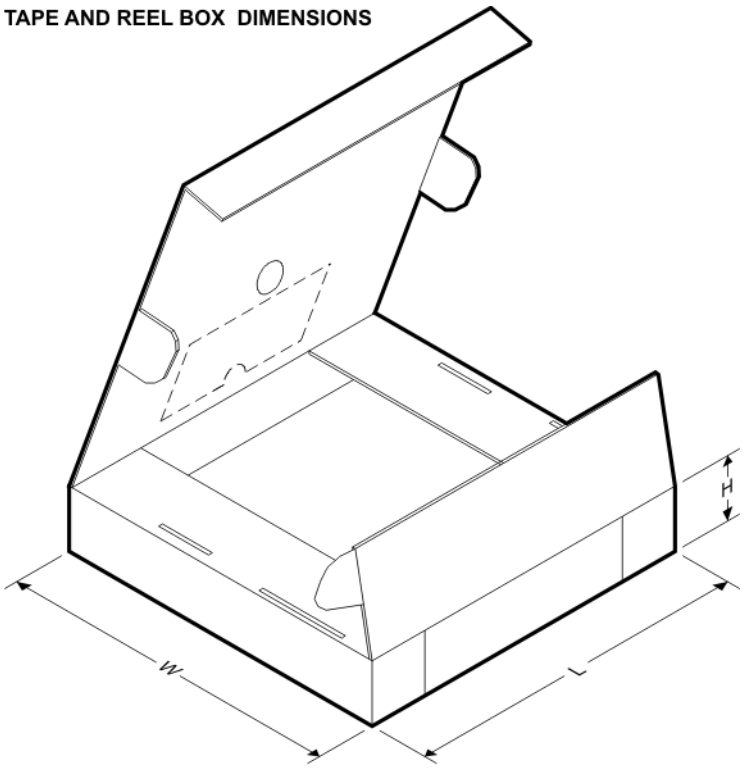
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24351DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24351DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

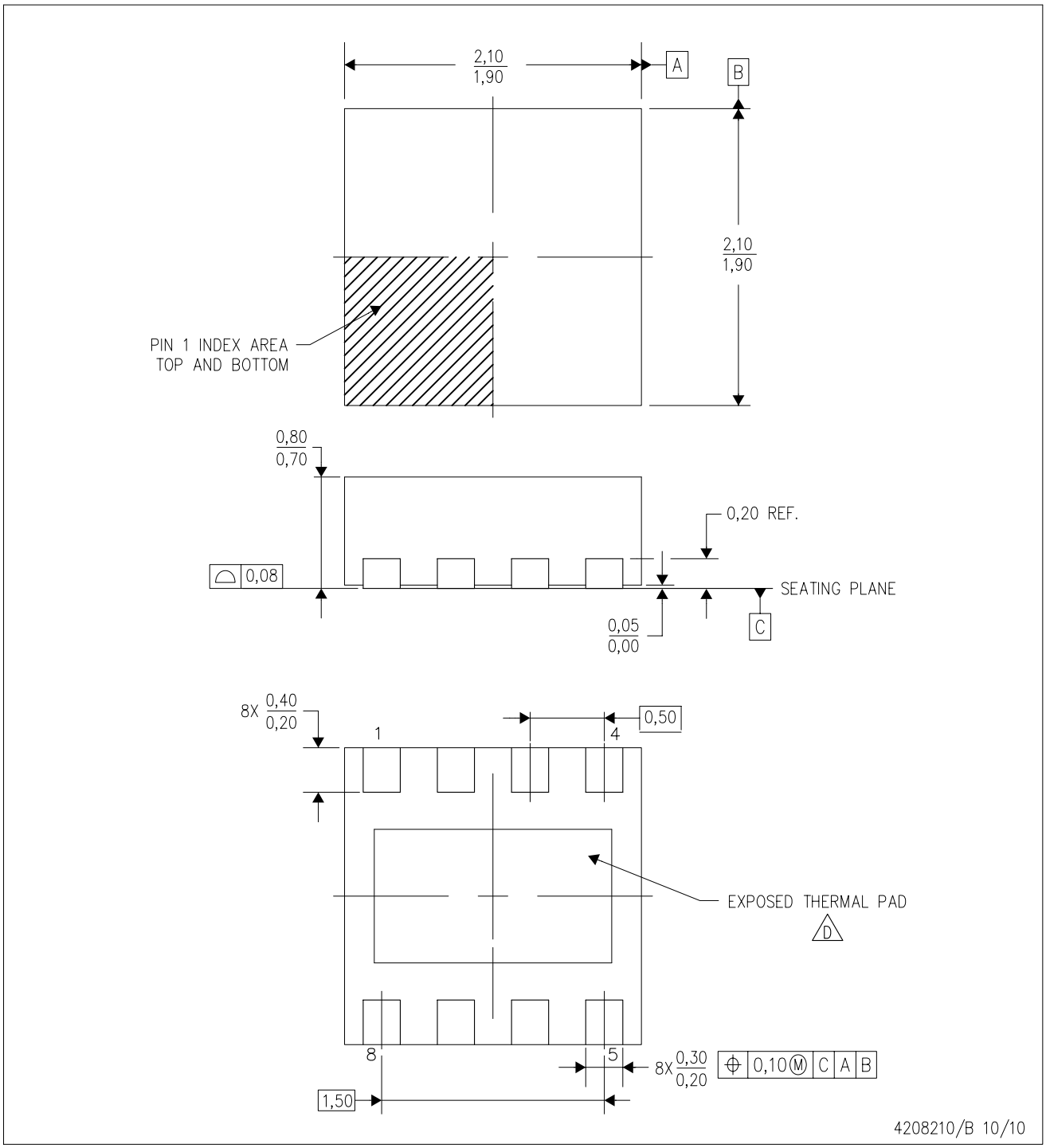
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24351DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
BQ24351DSGT	WSON	DSG	8	250	195.0	200.0	45.0

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

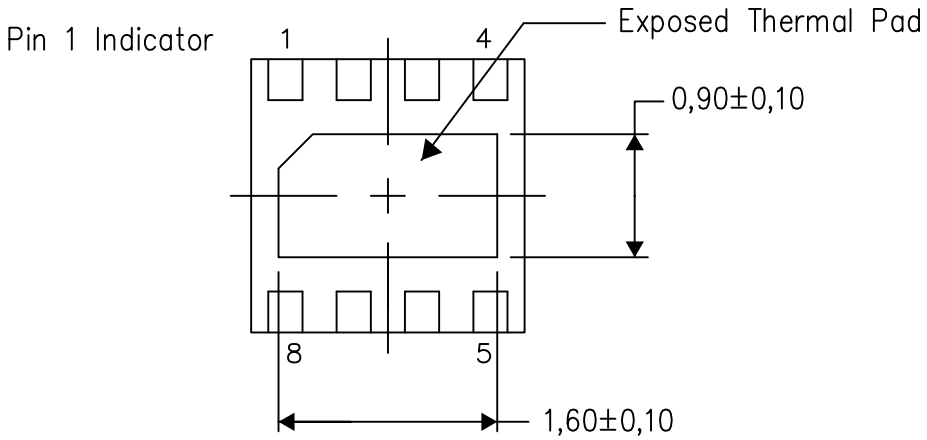
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



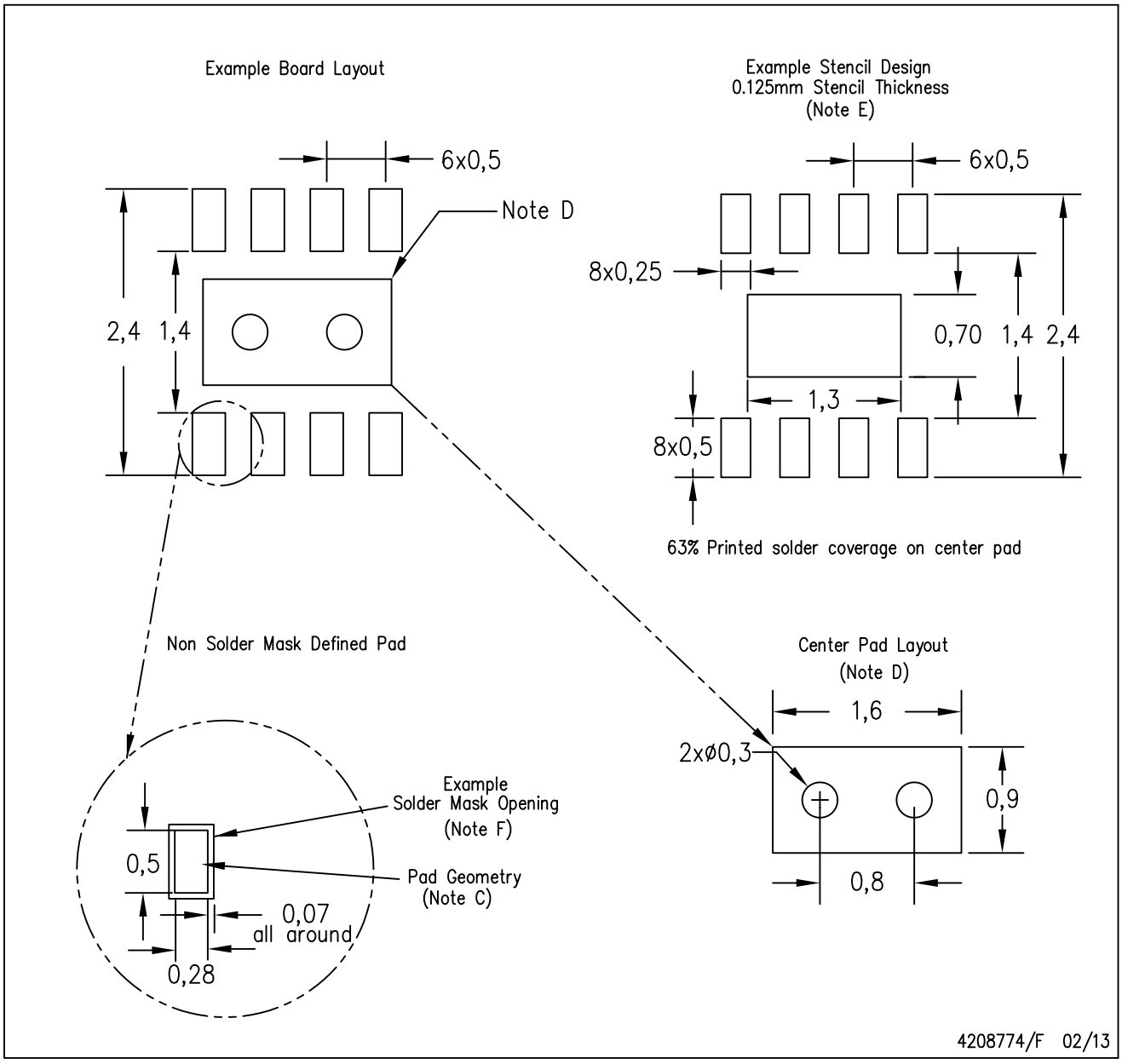
Bottom View

Exposed Thermal Pad Dimensions

4208347/G 08/13

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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