

Pb Free Plating Product

IXTP60N10T



60A,100V Heatsink Trench N-Channel Power MOSFET

General Description

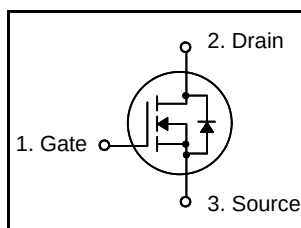
IXTP60N10T is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged EAS capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching especially for E-Bike controller applications.

Features

- $V_{DS}=100V$; $I_D=60A@V_{GS}=10V$;
 $R_{DS(ON)} < 18.3m\Omega @ V_{GS}=10V$
- Special Designed for E-Bike Controller Application
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

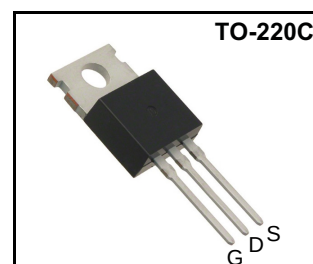
- E-Bike Controller Applications
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply
- Inverter Application
- Amplifier Application



$$BV_{DSS} = 100V$$

$$R_{DS(ON)} = 0.0183 \text{ ohm}$$

$$I_D = 60A$$

ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175^\circ\text{C}$)	I_D	60	A
		50	
Pulsed Drain Current	I_{DM}	100	
Avalanche Current	I_{AS}	45	
Single Avalanche Energy ^a	E_{AS}	101	mJ
Maximum Power Dissipation ^a	P_D	150 ^b	W
		3.75	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^c	R_{thJA}	40	$^\circ\text{C/W}$
Junction-to-Case (Drain)	R_{thJC}	1.0	

Notes:

a. Duty cycle $\leq 1\%$.

b. See SOA curve for voltage derating.

c. When Mounted on 1" square PCB (FR-4 material).

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

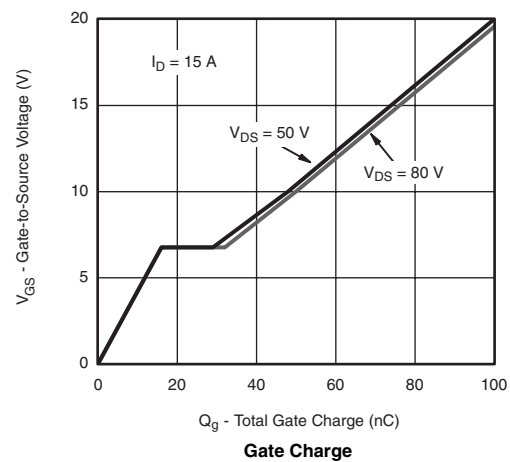
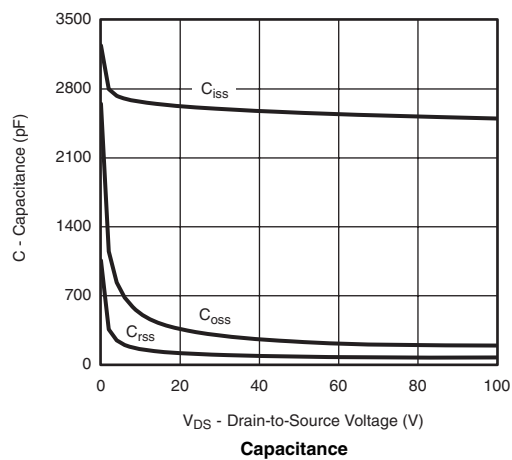
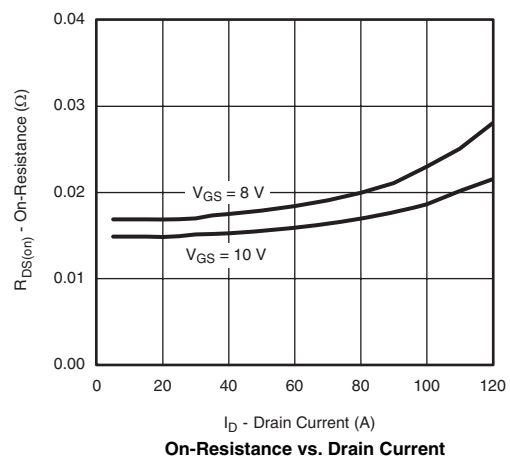
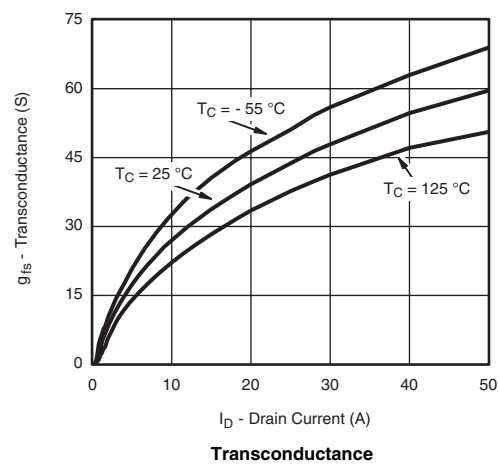
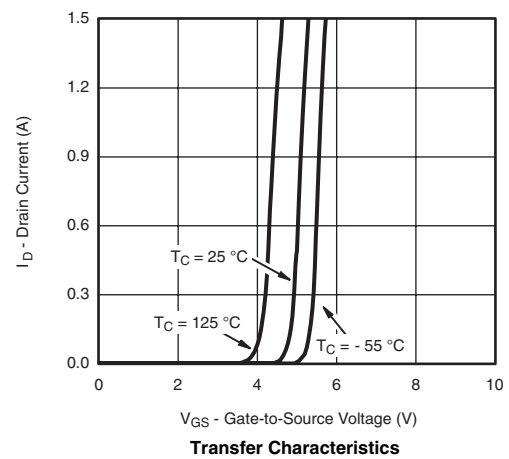
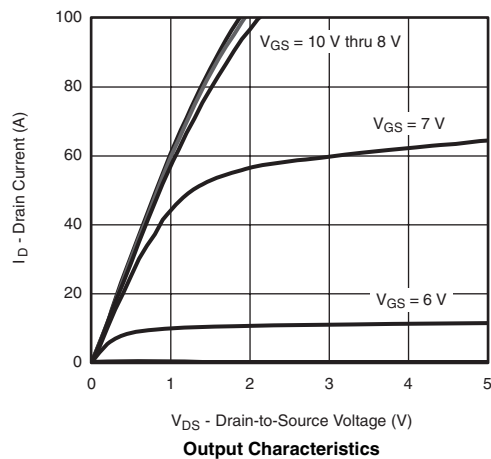
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.5		4.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^{\circ}\text{C}$			50	
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^{\circ}\text{C}$			250	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}, V_{GS} = 10\text{ V}$	50			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		0.015	0.0183	Ω
		$V_{GS} = 10\text{ V}, I_D = 15\text{ A}, T_J = 125\text{ }^{\circ}\text{C}$		0.027	0.033	
		$V_{GS} = 8.0\text{ V}, I_D = 10\text{ A}$		0.018	0.023	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		33		S
Dynamic ^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}, f = 1\text{ MHz}$		2600		pF
Output Capacitance	C_{oss}			230		
Reverse Transfer Capacitance	C_{rss}			80		
Total Gate Charge ^c	Q_g	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		48	75	nC
Gate-Source Charge ^c	Q_{gs}			16		
Gate-Drain Charge ^c	Q_{gd}			13		
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.25	1.1	2.4	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 1.0\text{ }\Omega$ $I_D \cong 50\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		12	20	ns
Rise Time ^c	t_r			10	20	
Turn-Off Delay Time ^c	$t_{d(off)}$			18	35	
Fall Time ^c	t_f			8	15	
Drain-Source Body Diode Characteristics $T_C = 25\text{ }^{\circ}\text{C}^b$						
Continuous Current	I_S				60	A
Pulsed Current	I_{SM}				100	
Forward Voltage ^a	V_{SD}	$I_F = 15\text{ A}, V_{GS} = 0\text{ V}$		0.85	1.5	V
Reverse Recovery Time	t_{rr}	$I_F = 50\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		80	120	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			4		A
Reverse Recovery Charge	Q_{rr}			160	240	nC

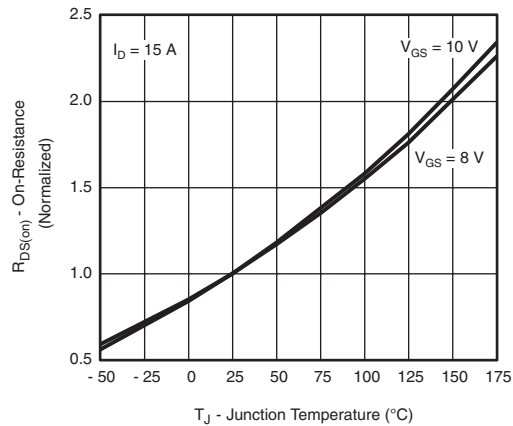
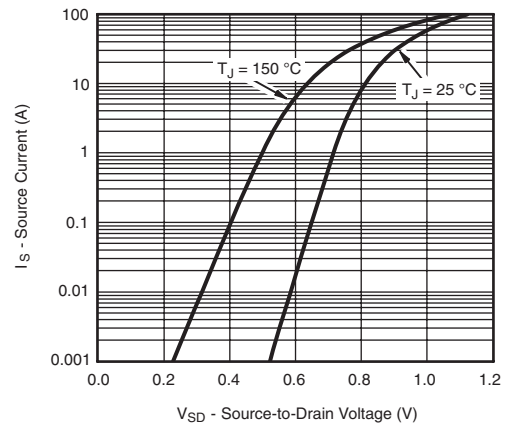
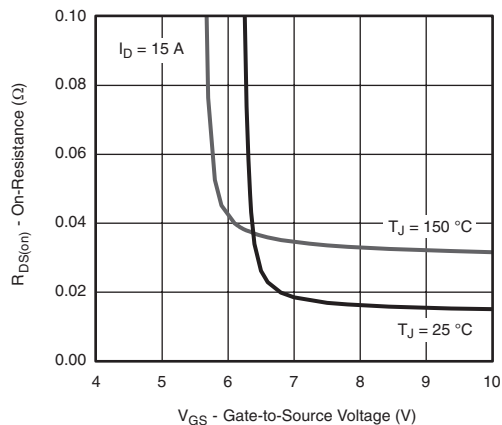
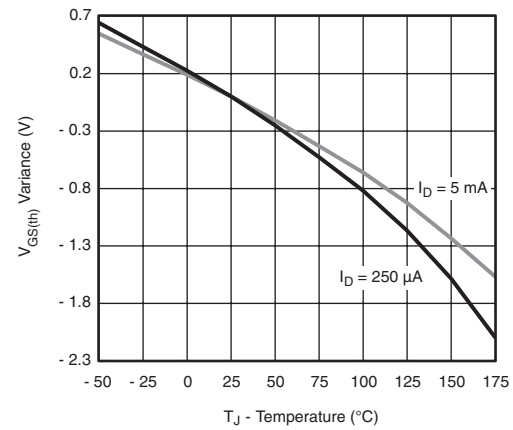
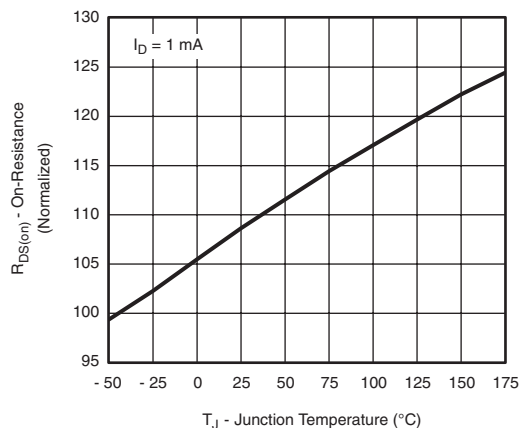
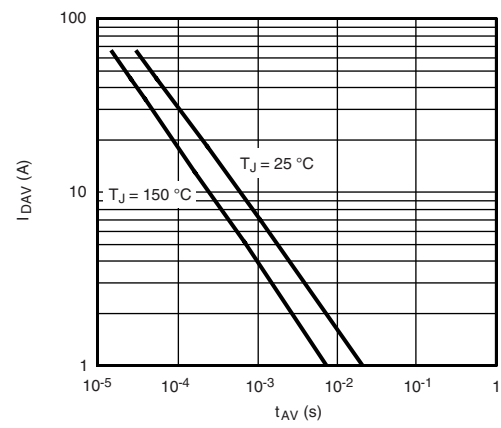
Notes:

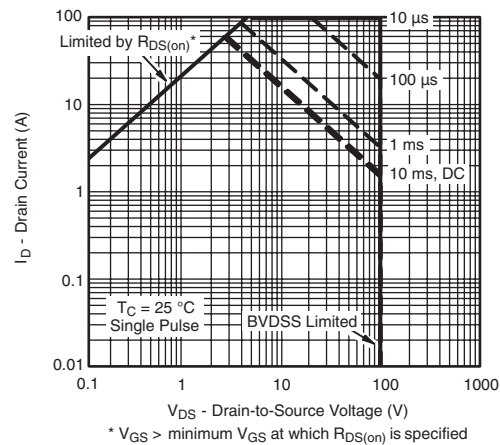
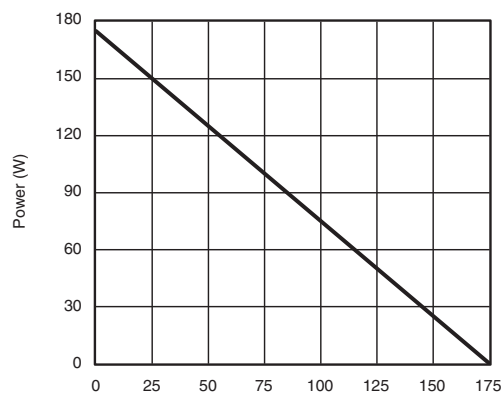
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

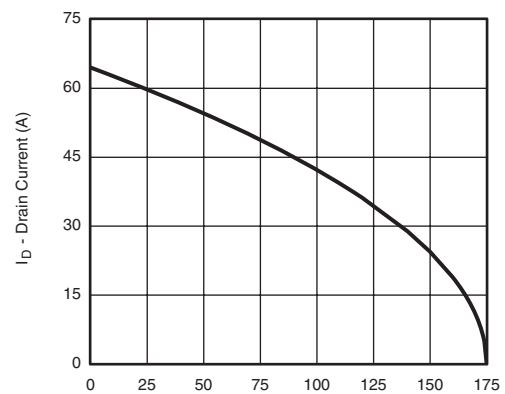
c. Independent of operating temperature.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


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On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

On-Resistance vs. Junction Temperature

Avalanche Current vs. Time

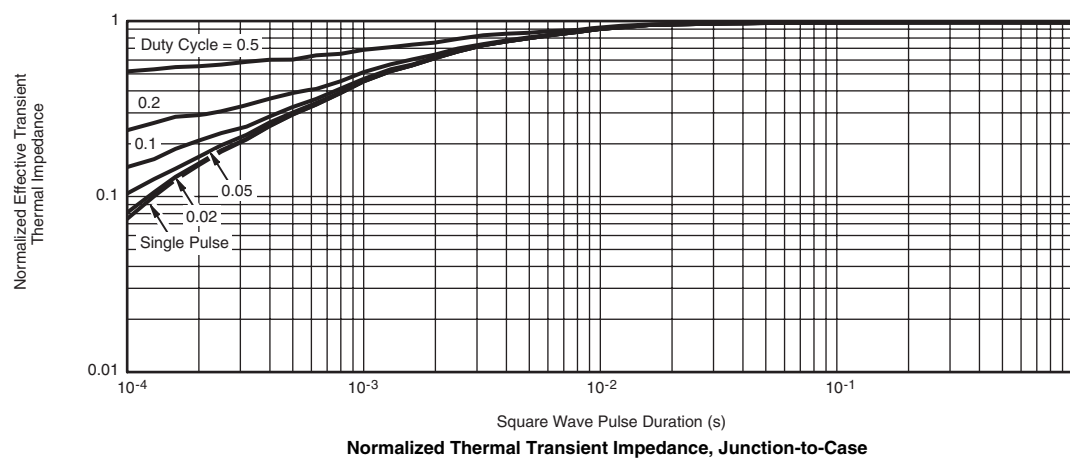
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Safe Operating Area


T_C - Case Temperature (°C)
Power Derating, Junction-to-Case

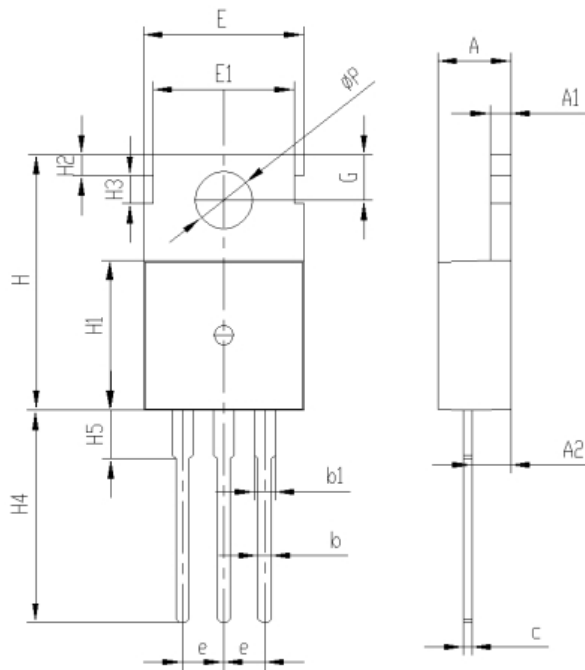


T_C - Case Temperature (°C)
Current Derating*

* The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

TO-220C PACKAGE OUTLINE



Symbol	Dimensions(millimeters)	
	Min.	Max.
A	4.30	4.70
A1	1.17	1.37
A2	2.20	2.60
b	0.60	1.00
b1	1.17	1.37
b2	1.90	2.30
c	0.30	0.70
e	2.34	2.74
E	9.70	10.1
E1	8.50	8.90
H	15.5	15.9
H1	9.00	9.40
H2	1.10	1.50
H3	1.50	1.90
H4	12.58	13.58
H5	2.80	3.20
G	2.60	3.00
ΦP	3.40	3.80