RKD700KL

Silicon Schottky Barrier Diode for Backflow prevention

REJ03G1337-0100
Rev.1.00
Jan 19, 2006

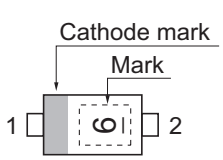
Features

- Low reverse current, Low capacitance.
- Extremely small Flat Lead Package (EFP) is suitable for surface mount design.

Ordering Information

Type No.	Laser Mark	Package Name	Package Code
RKD700KL	6	EFP	PXSF0002ZA-A

Pin Arrangement





1. Cathode
2. Anode

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Repetitive peak reverse voltage	V_{RRM}	30	V
Reverse voltage	V_R	30	V
Non-Repetitive peak forward surge current	I_{FSM} *	200	mA
Average rectified current	I_O	50	mA
Junction temperature	Tj	125	°C
Storage temperature	Tstg	–55 to +125	°C

Note: 10 ms Sinewave 1 pulse

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Forward voltage	V_{F1}	—	0.11	0.14	V	I_F = 1 µA
	V_{F2}	—	—	0.33		I_F = 1 mA
	V_{F3}	—	—	0.43		I_F = 10 mA
Reverse current	I_{R1}	—	—	45	nA	V_R = 3 V
	I_{R2}	—	—	1	µA	V_R = 30 V
Capacitance	C	—	—	2.8	pF	V_R = 1 V, f = 1 MHz

Note: For EFP package, the material of lead is exposed for cutting plane. There for, soldering nature of lead tip part is considered as unquestioned. Please kindly consider soldering nature.

Main Characteristic

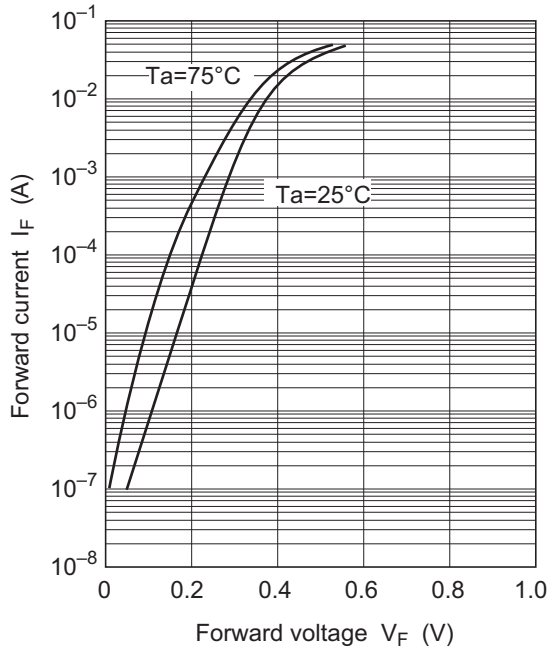


Fig.1 Forward current vs. Forward voltage

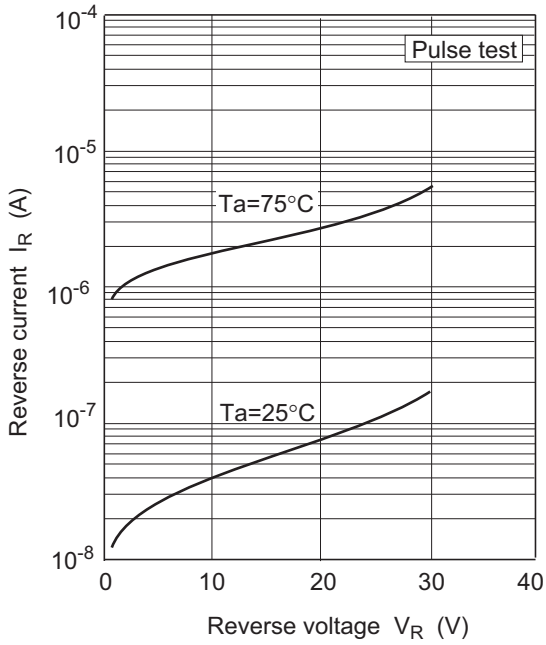


Fig.2 Reverse current vs. Reverse voltage

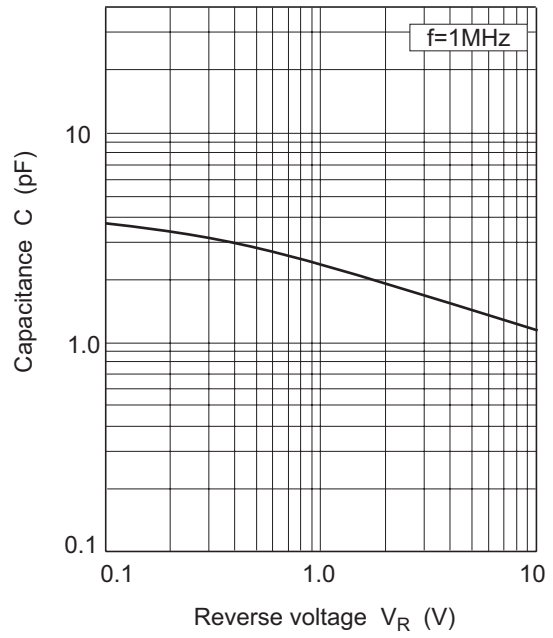
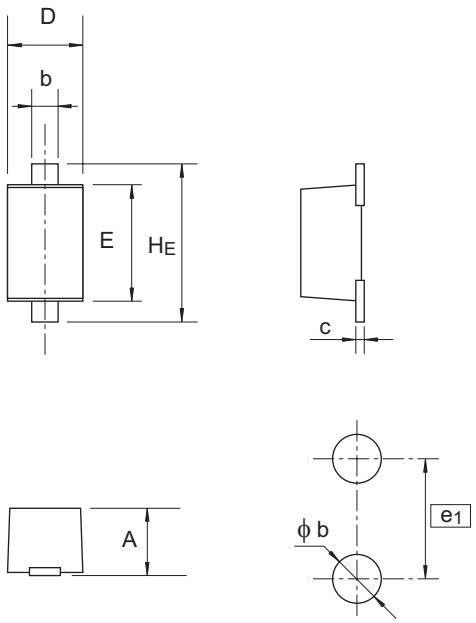


Fig.3 Capacitance vs. Reverse voltage

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
EFP	—	PXSF0002ZA-A	EFP / EFPV	0.0007g



Pattern of terminal position areas

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	0.44	0.47	0.50
b	0.25	0.30	0.35
c	0.08	0.13	0.18
D	0.55	0.60	0.65
E	0.75	0.80	0.85
H_E	0.95	1.00	1.05
ϕ b	—	0.40	—
e1	—	1.00	—

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