DATA SHEET

# GPCE2064A

## 16-bit Sound Controller with

## 32K X 16 ROM

Jun 02, 2016

Version 1.2

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# 16-BIT SOUND CONTROLLER WITH 32K X 16 ROM

## 1 GENERAL DESCRIPTION

GPCE2064A, a 16-bit architecture sound controller, features 16-bit *μ'nSP*™ microprocessor developed by Sunplus Technology. This high processing speed assures the *μ'nSP*™ is capable of handling complex digital signal processing easily and rapidly. GPCE2064A is applicable to the areas of digital sound processing and voice recognition. The operating voltage of 2.4V through 5.5V and speed of 0.16MHz through 49.152MHz yield the GPCE2064A to be easily used in varieties of applications. The memory capacity includes 32K-word ROM plus a 2K-word working SRAM. Other features include 32 programmable multi-functional I/Os, three 16-bit timers/counters, 32768Hz Real Time Clock, Low Voltage Reset/Detection, eight channels 12-bit ADC (one channel built-in MIC amplifier with auto gain controller), one 14-bit DAC with push-pull amplifier and many others.

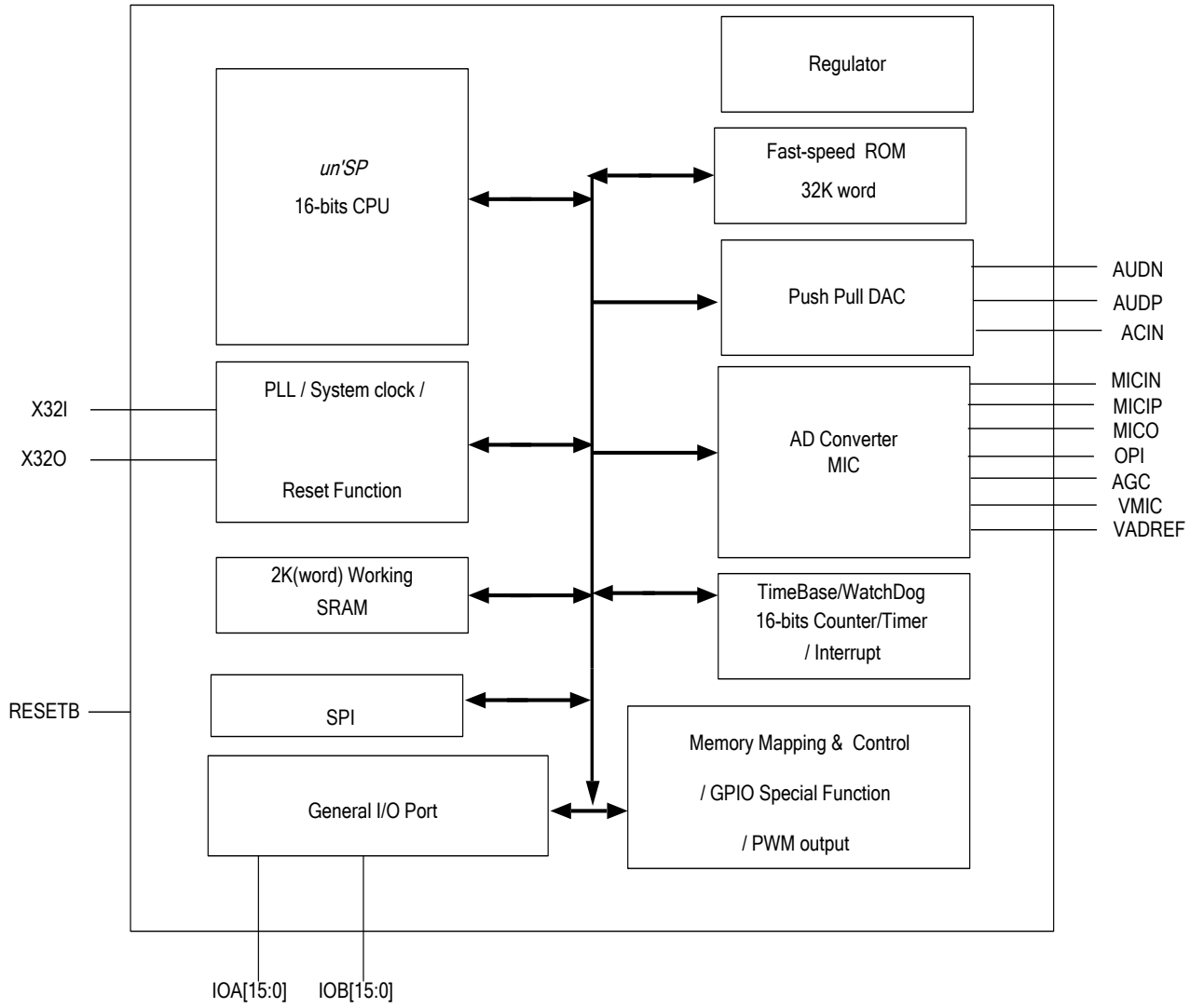
## 2 FEATURES

- 16-bit *μ'nSP*™ microprocessor
- CPU Clock: 0.16MHz - 49.152MHz
- Operating Voltage: 2.4V - 5.5V
- Power regulator built-in with input voltage: 2.4~5.5V, output voltage: 2.4~3.3V
- IO PortA & B Operating Voltage: 2.4V - 5.5V
- 32K-word fast speed ROM
- 2K-word working SRAM
- Software-based audio processing
- Two sets of 14-bit software channel with noise filter, mixer and scalar to play high quality sound
- Standby mode for power saving
- Three 16-bit timers/counters
- One 14-bit DAC with push-pull amplifier. Supports cascade mode
- 32 general I/Os (bit programmable)
- Key wakeup function (IOA0 - 15)
- PLL feature for system clock
- 32768Hz Real Time Clock (RTC), crystal or internal resistor oscillator selected.
- Eight channels of 12-bit AD converter
- ADC
- Built-in microphone amplifier and AGC or PGA function selected
- Low voltage reset and low voltage detection
- Watchdog Enable (option)
- One SPI serial interface I/O

## 3 APPLICATION FIELD

- Voice Recognition Product
- Intelligent Interactive Talking Toy
- Advanced Educational Toy
- Kids Learning Product
- Kids Storybook
- General Speech Synthesizer
- Long Duration Audio Product
- Recording / Playback Product

## 4 BLOCK DIAGRAM

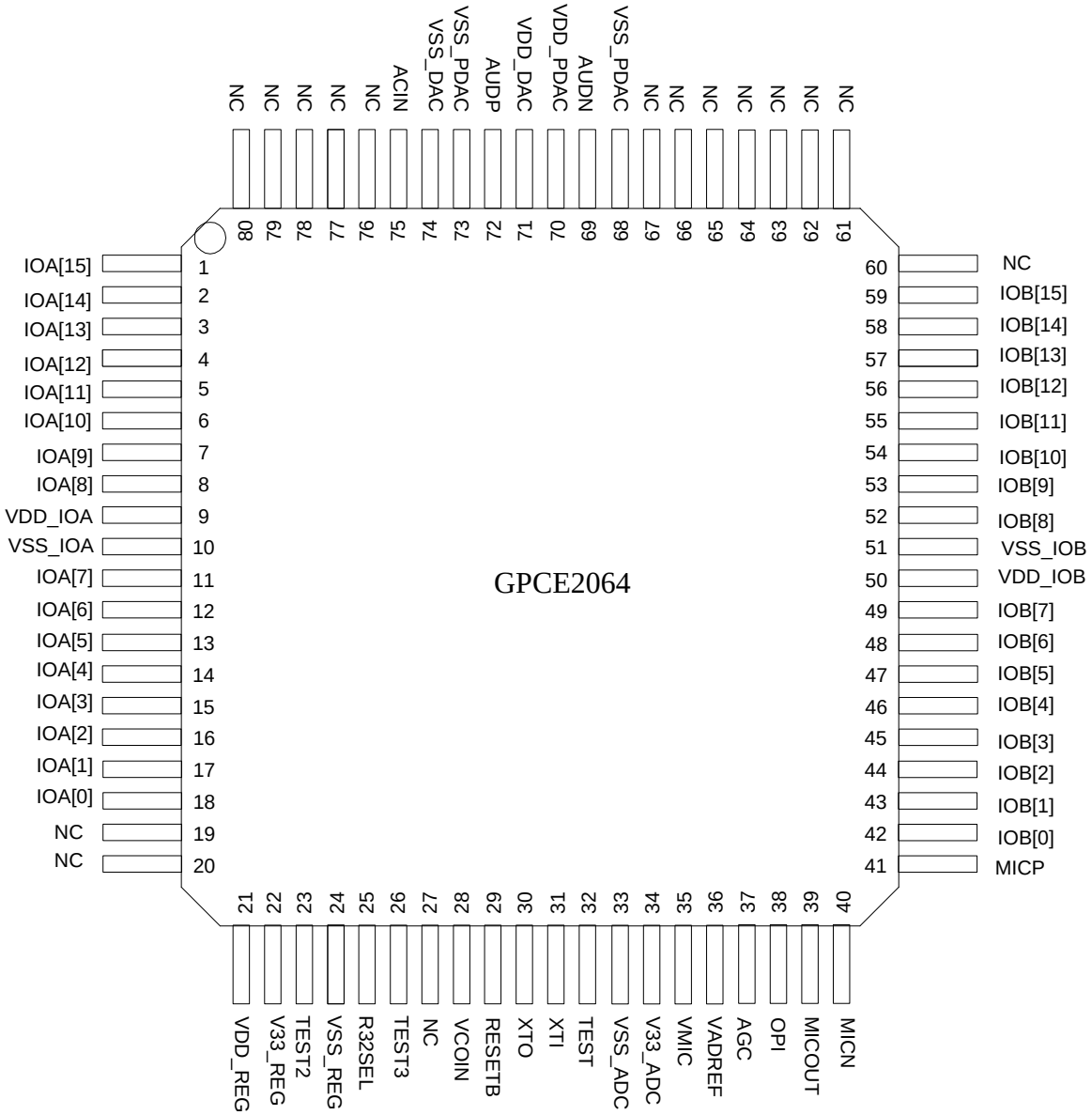


## 5 SIGNAL DESCRIPTIONS

| Mnemonic | PIN No. | Type | Description |
|---|---|---|---|
| PORT A, Port B | | | |
| IOA[15:0] | 66-69, 1-4, 7-14 | I/O | IOA[15:0]: bi-directional I/O ports<br>It can be programmed as wakeup I/O pins |
| IOB [15:0] | 52-45, 42-35 | I/O | IOB [15:0]: bi-directional I/O ports |
| Power & GND | | | |
| VDD_IOA | 5 | P | Power VDD for Port A |
| VSS_IOA | 6 | G | Power GND for Port A |
| VDD_IOB | 43 | P | Power VDD for Port B |
| VSS_IOB | 44 | G | Power GND for Port B |
| V33_ADC | 27 | P | Power VDD for AD(3.3V) |
| VSS_ADC | 26 | G | Power GND for AD |
| V33_REG | 16 | P | 3V power output from regulator |
| VDD_REG | 15 | P | Positive supply for regulator(2.4V~5.5V) |
| VSS_REG | 18 | G | Ground reference for regulator |
| VDD_DAC | 59 | P | Positive 5V supply for push-pull DAC |
| VDD_PDAC | 57, 58 | P | Positive 5V supply for push-pull DAC post driver |
| VSS_DAC | 64 | I | Ground reference for push-pull DAC |
| VSS_ PDAC | 53, 54, 62, 63 | I | Ground reference for push-pull DAC post driver |
| CLK SYSTEM/ ICE INTERFACE | | | |
| XTI | 24 | I | 32KHz Oscillator crystal input |
| XTO | 23 | O | 32K Oscillator crystal output |
| OPTION | | | |
| TEST | 25 | I | TEST Mode selection pin, do not connect the pin |
| TEST2 | 17 | I | TEST2 Mode selection pin, do not connect the pin |
| TEST3 | 20 | I | TEST3 Mode selection pin, do not connect the pin |
| R32SEL | 19 | I | R32K or Xtal32K select. Connected to VSS when Xtal32K is selected, and connected to V33_REG when R32K is selected. |
| DAC | | | |
| AUDP | 60, 61 | O | Audio output of push pull DAC |
| AUDN | 55, 56 | O | Audio output of push pull DAC |
| ACIN | 65 | U | Audio analog mixer in |
| ADC | | | |
| MICP | 34 | I | MIC amplifier input positive (Internal Floating) |
| MICN | 33 | I | MIC amplifier input negative (refer to application circuit) |
| MICOUT | 32 | O | MIC amplifier output (refer to application circuit) |
| OPI | 31 | I | Audio amplifier negative input (refer to application circuit) |
| AGC | 30 | IO | AGC by pass filter (refer to application circuit) |
| VMIC | 28 | O | Microphone power supply |
| VADREF | 29 | O | AVREF_DA reference pin |
| PLL | | | |
| VCOIN | 21 | I | PLL low pass filter input |
| Other Signal | | | |
| RESETB | 22 | I | System reset pin (active low) (internal 47Kohm pull high resistor) |

### 5.1 PIN Map

LQFP80



# 6 FUNCTION DESCRIPTIONS

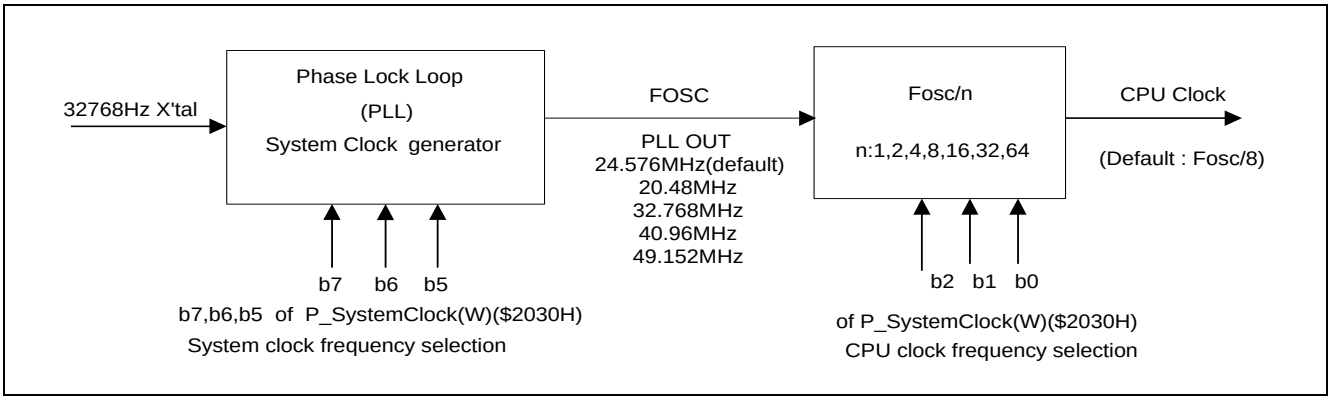
## 6.1 CPU

The GPCE2064A is equipped with a 16-bit μ'nSP™, the newest 16-bit microprocessor by Sunplus (pronounced as micro-n-SP). Eight registers are involved in μ'nSP™: R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP) and SR (Segment Register). The interrupts include three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK.

## 6.2 Memory

### 6.2.1 SRAM

The amount of SRAM is 2K-word (including Stack), ranged from $0000 through $07FF with access speed of two CPU clock cycles.




### 6.2.2 ROM

GPCE2064A features a 32K-word high-speed memory with access speed of two CPU clock cycles.

## 6.3 PLL, Clock, Power Mode

### 6.3.1 PLL (Phase Lock Loop)

The purpose of PLL is to provide a base frequency (32768Hz) and to pump the frequency from 20.48MHz to 49.152MHz for system clock ($F_{OSC}$). The default PLL frequency is 24.576MHz.

#### 6.3.1.1 System clock

Basically, the system clock is provided by PLL and programmed by the Port_SystemClock (R/W) to determine the clock frequency for system. The default system clock $F_{OSC}$ = 24.576MHz and CPU clock is $F_{OSC}$/8 if not specified. The initial CPU clock is Fosc/8 after system wakes up and adjusts to desired CPU clock via programming the Port_SystemClock (R/W). This avoids ROM reading failure when system awakes.

#### 6.3.1.2 32768Hz RTC

The Real Time Clock (RTC) is normally used in watch, clock or other time related products. A 2Hz-RTC (0.5 seconds) function is loaded in GPCE2064A. The RTC counts the time as well as to wake CPU up whenever RTC occurs. Since the RTC is generated each 0.5 seconds, time can be traced by the number of RTC occurrences. In addition, GPCE2064A supports 32768Hz crystal oscillator in normal mode and auto-power-saving mode. In normal mode, 32768Hz OSC always runs at the highest power consumption. In auto-power-saving mode, however, it runs at normal mode for the first 7.5 seconds and switches back to power-saving mode automatically to save powers.

## 6.4 Standby Mode

The GPCE2064A features a power savings mode (or called standby mode) for low power applications. To enter standby mode, the desired key wakeup port (IOA[15:0]) must be configured to input first. And read the Port_IOA_Data to latch the IOA state before entering the standby mode. Also remember to enable the corresponding interrupt source(s) for wakeup. After that, stop the CPU clock by writing $5555 into Port_System_Sleep(W) to enter standby mode. In such mode, SRAM and I/Os remain in the previous states until CPU being awakened. The wakeup sources in GPCE2064A include KEY wakeup (IOA[15:0]), RTC wakeup, FIQ and IRQ0 - IRQ7. After GPCE2064A is awakened, CPU will continue to execute the program from where it slept. Programmer can also enable or disable the 32768Hz RTC when CPU is in standby mode.

## 6.5 Low Voltage Detection and Low Voltage Reset

### 6.5.1 Low voltage detection (LVD)

The Low Voltage Detection (LVD) reports the circumstance of present voltage. There are four LVD levels to be selected: 2.6V, 2.8V, 3.0V and 3.2V. Those levels can be programmed via P_LVD_Ctrl. As an example, suppose LVD is given 2.8V. When the voltage drops below 2.8V, the b12 of P_LVD_Ctrl is read as HIGH. In such state, program can be designed to react this condition.

### 6.5.2 Low voltage reset

In addition to the LVD, the GPCE2064A has another important function, Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops below LVR level. Without LVR, the CPU becomes unstable and malfunctions when the operating voltage drops below LVR level. The LVR will reset all functions to the initial operational (stable) states when the voltage drops below LVR level.

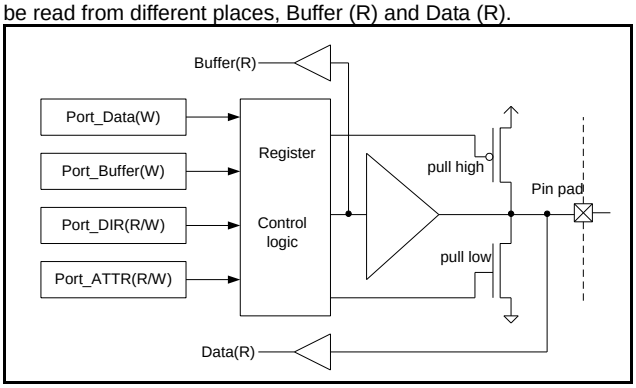
## 6.6 Interrupt

The GPCE2064A has 13 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is a high-priority interrupt while IRQ is the low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources.

| Interrupt Source | Interrupt Name / FIQ Name | IRQ Priority |
|---|---|---|
| Timer A | IRQ0_TMA/FIQ_TMA | 1(High) |
| Timer B | IRQ1_TMB/FIQ_TMB | 2 |
| Timer C | IRQ2_TMC/FIQ_TMC | 3 |
| SPI | IRQ3_SPI/FIQ_SPI | 4 |
| Key wakeup | IRQ5_KEY/FIQ_KEY | 5 |
| EXT1 | IRQ5_EXT1/FIQ_EXT1 | 6 |
| EXT2 | IRQ5_EXT2/FIQ_EXT2 | 7 |
| 4096Hz | IRQ6_4KHz/FIQ_4KHz | 8 |
| 2048Hz | IRQ6_2KHz/FIQ_2KHz | 9 |
| 512Hz | IRQ6_512Hz/FIQ_512Hz | 10 |
| 64Hz | IRQ7_64Hz/FIQ_64Hz | 11 |
| 16Hz | IRQ7_16Hz_FIQ_16Hz | 12 |
| 2Hz | IRQ7_2Hz/FIQ_2Hz | 13(Low) |

## 6.7 I/O

Two I/O ports are built in GPCE2064A - PortA and PortB, total has 32 bit-programmable I/Os. The PortA is a general purpose I/O with programmable wakeup capability, i.e. IOA [15:0] is the key wakeup port. To activate key wakeup function, latch data on Port_IOA_Data and enable the key wakeup function. Wakeup is triggered when the PortA state is different from at the time latched. Furthermore, the I/O ports can be operated at 5V level, higher than the CPU core which is a 3V level system. Suppose system operating voltage is running at 3.3V, VDDIO (power for I/O) operates from 3.3V to 5.5V. In such condition, the I/O pad is capable of operating from 0V through VDDIO. The following diagram is an I/O schematic. Although data can be written into the same register through Port_Data and Port_Buffer, they can be read from different places, Buffer (R) and Data (R).




In addition to a general purpose I/O port function, PortA/B also shares/carries some special functions. A summary of PortA/B special functions is listed as follows:

### 6.8 Special Function in Port

| Port | Special Function | Function Description | Note |
|---|---|---|---|
| IOA0 | IO_PWM | IO_PWM Output | Refer to Timer section |
| IOA1 | IROUT | IR Output | - |
| IOA2 | - | - | - |
| IOA3 | - | - | - |
| IOA4 | High driving I/O | - | - |
| IOA5 | High driving I/O | - | - |
| IOA6 | High driving I/O | - | - |
| IOA7 | High driving I/O | - | - |
| IOA8 | Feedback Input1 | - | Refer to below Example 1 |
| | EXT1 | External interrupt source 1 (negative edge triggered) | Set IOA8 as floating input mode |
| IOA9 | Feedback Output1 | Work with IOA8 by adding a RC circuit between them to get an OSC to EXT1 interrupt | Set IOA9 as inverted output |
| IOA10 | Feedback Input2 | - | Refer to below Example 1 |
| | EXT2 | External interrupt source 2 (negative edge triggered) | Set IOA10 as floating input mode |
| IOA11 | Feedback Output2 | Work with IOA10 by adding a RC circuit between them to get an OSC to EXT2 interrupts | Set IOA11 as inverted output |
| IOA12 | SPI CS | SPI chip select | Refer to SPI section |
| IOA13 | SPI CK | SPI clock | Refer to SPI section |
| IOA14 | SPI TX | SPI data output | Refer to SPI section |
| IOA15 | SPI RX | SPI data input | Refer to SPI section |
| IOB0 | AN0 | ADC Channel 0 | Refer to ADC section |
| IOB1 | AN1 | ADC Channel 1 | Refer to ADC section |
| IOB2 | AN2 | ADC Channel 2 | Refer to ADC section |
| IOB3 | AN3 | ADC Channel 3 | Refer to ADC section |
| IOB4 | AN4 | ADC Channel 4 | Refer to ADC section |
| IOB5 | AN5 | ADC Channel 5 | Refer to ADC section |
| IOB6 | AN6 | ADC Channel 6 | Refer to ADC section |
| IOB7 | AN7 | ADC Channel 7 | Refer to ADC section |
| IOA[15:0], IOB[15:0] | Io toggle | Io toggle function | Refer to IO Special Functions section |

Refer to the above table, the configuration of IOA9, IOA10, IOA11, and IOA12 involves feedback function in which an OSC frequency can be obtained from EXT1 (EXT2) by simply adding a RC circuit between IOA8 (IOA10) and IOA9 (IOA11).

### 6.9 Timer / Counter

GPCE2064A provides three 16-bit timers/counters - TimerA, TimerB and TimerC or so called universal counters. The clock source of Timer A/B/C are from clock source Input 1 and clock source Input 2 (see below table) which perform AND operation to form the varieties of combinations. When timer overflows, a timeout signal (TAOUT) is sent to CPU interrupt module to generate a timer interrupt signal. In addition, Timer A/B/C hardware interrupt events can be used to latch the DAC audio output and trigger ADC conversion.

Example to Timer A, sending a write signal into TMA_CNT, the value of TMA_DATA (value=N) will reload into TMA_CNT and set an appropriated clock source. Timer wills up-count from N, N+1, N+2… 0XFFFF. An INT signal is generated at the moment of timer rolling over from “0xFFFF” to “0x0000”, and an INT signal is processed by INT controller immediately. At the same time, N will be reloaded into TMA_CNT and start counting again.

In Timer A, the clock Input 1 is a high frequency source and clock Input 2 is a low frequency clock source. The combination of clock Input 1 and input 2 provides varieties of speeds to

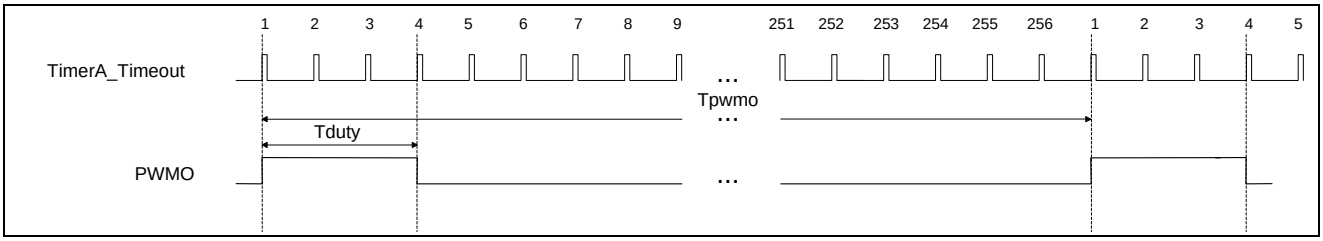
TimerA/CounterA - “1” representing pass signal (not gating), and “0” meaning timer deactivated. For instance, if Input 1=”1”, the clock is depending on Input 2. If Input 1=”0”, the TimerA is deactivated. The EXT1/ETX2 is the external clock source 1 and external clock source 2.

| TMXSEL | Input 1 | Input 2 |
|---|---|---|
| 0000 | ‘0’ | ‘0’ |
| 0001 | ‘1’ | ‘1’ |
| 0010 | $F_{RTC}$ | EXT2 |
| 0011 | $F_{PLL}$ | EXT2 |
| 0100 | EXT2 | 64Hz |
| 0101 | EXT2 | 16Hz |
| 0110 | EXT2 | 2Hz |
| 0111 | EXT2 | ‘1’ |
| 1000 | $F_{RTC}$ | 64Hz |
| 1001 | $F_{RTC}$ | 16Hz |
| 1010 | $F_{RTC}$ | 2Hz |
| 1011 | $F_{RTC}$ | ‘1’ |
| 1100 | $F_{PLL}$ | 64Hz |
| 1101 | $F_{PLL}$ | 16Hz |
| 1110 | $F_{PLL}$ | 2Hz |
| 1111 | $F_{PLL}$ | ‘1’ |

The following clock source A/B/C means clock source for Timer A/B/C respectively. Generally speaking, the clock source A and C are fast clock sources and source B comes from RTC system (32768Hz). Therefore, clock source B can be utilized as a precise counter for time counting, e.g., the 2Hz clock can be used for real time counting.

### 6.9.1 IO PWM

One IO PWMs which duty is selected from 1/256 to 254/256. Example the below figure is a 3/256-duration cycle. The PWMO waveform is made by selecting a pulse width through Port_PWM_Ctrl. As a result, each 256 cycles will generate a pulse width defined in control port. These PWM signals can be applied for controlling the speed of motor or other devices.




### 6.9.2 Timebase

Timebase, generated by 32768Hz crystal oscillator, is a combination of frequency selection. Furthermore, timebase generates 4KHz, 2KHz, 512Hz, 64Hz, 16Hz and 2Hz interrupt sources (FIQ6/IRQ6, FIQ7/IRQ7) for Real-Time-Clock

## 6.10 Sleep Mode, Wakeup, Halt Mode, and Watchdog

### 6.10.1 Sleep and wakeup modes

1) Sleep: After power-on reset, IC starts running until a sleep command is issued. When a sleep command is accepted, IC will turn the system clock (PLL) off. After all, it enters sleep mode.
2) Wakeup: CPU awaking from sleep mode requires a wakeup signal to turn the system clock (PLL) on. The FIQ/IRQ signal makes CPU to complete the wakeup process and initialization. The CPU wakeup source is given in the following table.

| Wakeup Source |
|---|
| FIQ source |
| Timer A interrupt |
| Timer B interrupt |
| Timer C interrupt |
| SPI interrupt |
| EXT1/EXT2/KEY |
| RTC |

### 6.10.2 Watchdog Reset

The GPCE2064A provides another important feature, watchdog reset. If the watchdog function is enabled, a reset signal is generated to reset system when watchdog counter is overflow.

The purpose of watchdog is to monitor whether the system operates normally. Within a certain period, watchdog register must be cleared. If it is not cleared, CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again.

### 6.11 Soft Reset Protection

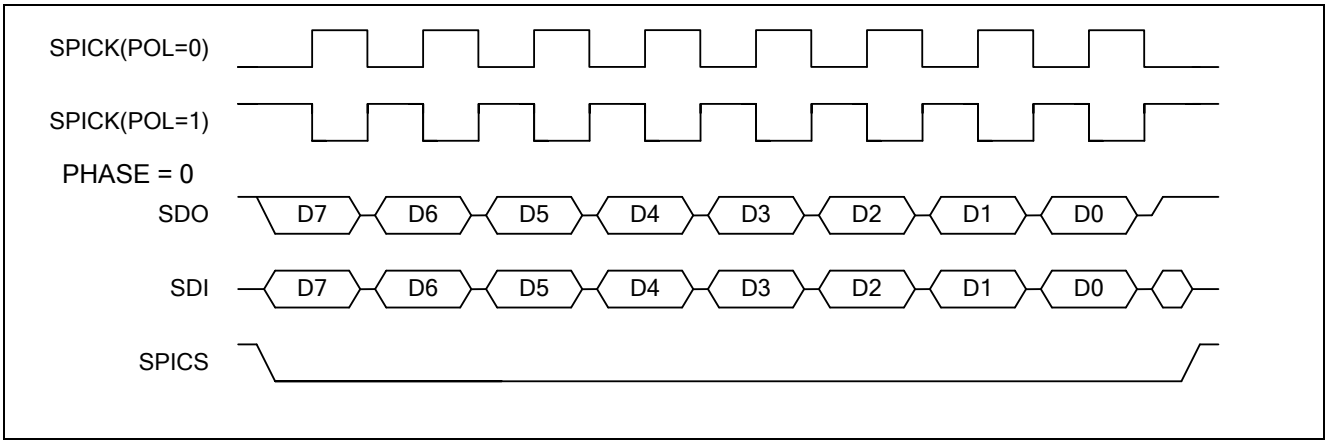
Software reset. Writes $5555 into P_System_Reset will reset the whole system like hardware reset (pull low RESETB pin), except a flag will set on in P_System_LVD_Ctrl(R/W).

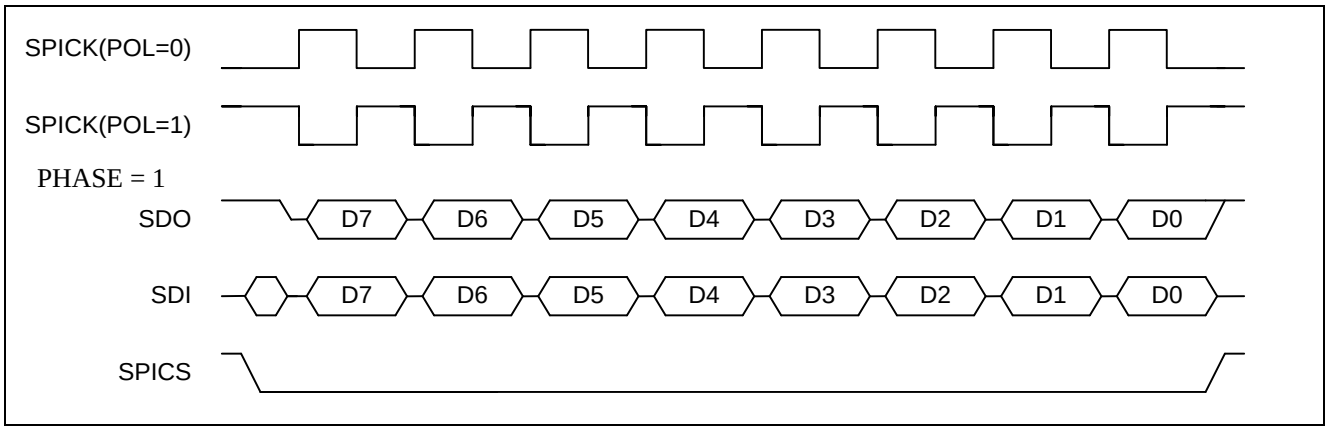
### 6.12 ADC (Analog to Digital Converter) / DAC

The GPCE2064A has eight channels 12-bit ADC (Analog to Digital Converter). The function of an ADC is to convert analog signal to digital signal, e.g. a voltage level into a digital word. The eight channels of ADC can be eight channels of line-in from IOB [7:0] or one channel microphone (MIC) input through amplifier PGA controller, and AGC controller. The MIC amplifier circuit is capable of reducing common mode noise by transmitting signals through differential MIC Inputs (MICN, MICP). Moreover, an external resistor can be applied to adjust microphone gain and time of AGC operating. The AD needs to select source of line-in before conversion. The ADC takes pad (VDD_ADC) as voltage reference.

### 6.13 SPI

A Serial Peripheral Interface (SPI) controller is built in GPCE2064A to facilitate communicating with other devices and components. There are four control signals on SPI - SPICS (IOA12), SPICK (IOA13), SDO (IOA14), and SDI (IOA15).




### 6.14 Audio Algorithm

The following speech types can be used in GPCE2064A: PCM, SACM_S200, SACM_S480, SACM_S530, SACM_A1600, SACM_A1601, SACM_A1800, SACM_A3400pro, SACM_A3600, SACM_DVR520, SACM_DVR1600, SACM_DVR1800, SACM_DVR3200, and SACM_DVR4800. For melody synthesis, the GPCE2064A supports SACM_MS01 (FM) and SACM_MS02 (wave-table) synthesizers.

# 7 ELECTRICAL SPECIFICATIONS

## 7.1 Absolute Maximum Ratings

| Characteristics | Symbol | Ratings |
|---|---|---|
| DC Supply Voltage | $V_+$ | < 4.0V |
| PortA/B Pad Supply Voltage | $V_{IO}$ | < 7.0V |
| Input Voltage Range | $V_{IN}$ | -0.5V to $V_+$ + 0.5V |
| Operating Temperature | $T_A$ | 0℃ to +60℃ |
| Storage Temperature | $T_{STO}$ | -50℃ to +150℃ |

**Note:** Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see DC Electrical Characteristics.

## 7.2 DC Characteristics (VDD = 3.3V, VDDIO = 4.5V (PortA & B), TA = 25℃)

| Characteristics | Symbol | Limit | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operating Voltage | VDD | 2.7 | 3.3 | 3.6 | V | - |
| Operating Current | $I_{OP}$ | - | 13 | - | mA | $F_{OSC}$ = 49.152MHz, AD, DAC disable, non-loading |
| Standby Current | $I_{STB}$ | - | - | 5 | μA | Disable 32KHz crystal |
| | | | | 10 | μA | Enable 32KHz,Disable PLL($F_{OSC}$) |
| Input High Level | $V_{IH}$ | 0.7$VDD_{IO}$ | - | - | V | - |
| Input Low Level | $V_{IL}$ | - | - | 0.3$VDD_{IO}$ | V | - |
| Output High Current | $I_{OH}$ | - | -20 | - | mA | $V_{OH}$ = 0.7VDD |
| Output Low Current (PA[3:0], PB[7:0]) | $I_{OL}$ | - | 20 | - | mA | $V_{OL}$ = 0.3VDD |
| Output Low Current (PA[7:4]) | $I_{OL}$ | - | 40 | - | mA | $V_{OL}$ = 0.3VDD |
| Input Pull-Low Resister (PA15:0, PB15:8) | $R_{PL}$ | - | 120 | - | KΩ | $V_{IN}$ = VDD |
| Input Pull-Low Resister (PB[7:0]) | $R_{PL}$ | - | 1200 | - | KΩ | $V_{IN}$ = VDD |
| Input Pull-High Resister (PA15:0, PB15:0) | $R_{PH}$ | - | 110 | - | KΩ | $V_{IN}$ = VSS |
| Internal ROSC frequency deviation | ⊿F/F | -3% | 32768 | +3% | HZ | V33_REG = 3.3V |

## 7.3 DC Characteristics (VDD = 3.3V, VDDIO = 3.3V (PortA & B), TA = 25℃)

| Characteristics | Symbol | Limit | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operating Voltage | VDD | 2.7 | 3.3 | 3.6 | V | - |
| Operating Current | $I_{OP}$ | - | 13 | - | mA | $F_{OSC}$ = 49.152MHz, AD, DAC disable, non-loading |
| Standby Current | $I_{STB}$ | - | - | 3 | μA | Disable 32KHz crystal |
| | | | | 6 | μA | Enable 32KHz,Disable PLL($F_{OSC}$) |
| Input High Level | $V_{IH}$ | 0.7$VDD_{IO}$ | - | - | V | - |
| Input Low Level | $V_{IL}$ | - | - | 0.3$VDD_{IO}$ | V | - |
| Output High Current | $I_{OH}$ | - | -11 | - | mA | $V_{OH}$ = 0.7VDD |

| Characteristics | Symbol | Limit | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output Low Current (PA[3:0], PB[7:0]) | $I_{OL}$ | - | 11 | - | mA | $V_{OL}$ = 0.3VDD |
| Output Low Current (PA[7:4]) | $I_{OL}$ | - | 25 | - | mA | $V_{OL}$ = 0.3VDD |
| Input Pull-Low Resister (PA15:0, PB15:8) | $R_{PL}$ | - | 120 | - | KΩ | $V_{IN}$ = VDD |
| Input Pull-Low Resister (PB[7:0]) | $R_{PL}$ | - | 1200 | - | KΩ | $V_{IN}$ = VDD |
| Input Pull-High Resister (PA15:0, PB15:0) | $R_{PH}$ | - | 110 | - | KΩ | $V_{IN}$ = VSS |
| Internal ROSC frequency deviation | ⊿F/F | -3% | 32768 | +3% | HZ | V33_REG = 3.3V |

### 7.4 ADC Characteristics (VDD = 3.3V, TA = 25℃)

| Characteristics | Symbol | Limit | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| ADC LINE_IN Input Voltage Range from IOB[7:0] | VINL (Note 1) | VSS-0.3 | - | VDD+0.3 | V |
| ADC Microphone Input Voltage Range | VINM | VSS-0.3 | - | VDD+0.3 | V |
| Resolution of ADC | RESO | - | - | 12 | bits |
| Signal-to-Noise Plus Distortion of ADC from Line in | SINAD (Note 3) | - | 55 | - | dB |
| Effective Number of Bit | ENOB (Note 4) | 8.0 | 9.0 | - | bits |
| Integral Non-Linearity of ADC | INL | - | ±8.0 | - | LSB (Note 2) |
| Differential Non-Linearity of ADC | DNL (Note 6) | - | ±3 | - | LSB |
| AD Conversion Rate | $F_{CONV}$ | - | - | $F_{CPU}$/256 | Hz |
| Microphone Amplifier Gain | $A_{MIC}$ | - | - | 42(Note 5) | dB |

**Note1:** Internal protection diodes clamp the analog input to VDD and VSS. These diodes allow the analog input to swing from (VSS-0.3V) to (VDD+0.3V) without causing damage to the devices.

**Note2:** LSB means Least Significant Bit. With VINL = 2.6V, 1LSB = 2.6V/2^12 = 0.635mV.

**Note3:** The SINAD testing condition at VINLp-p = 0.8*VDD, $F_{CONV}$ = Fcpu/512 = 49MHz/256 = 192KHz, Fin=1.0KHz Sine waves at VDD = 3.0V from the IOB [7:0] input.

**Note4:** ENOB = (SINAD-1.76)/6.02.

**Note5:** The microphone amplifier maximum gain = 15 * (60K/(1.5K+REXT) V/V. The REXT is external resistor between OPI and MICOUT. The gain is 132V/V (=42dB) when REXT is 5.1K.

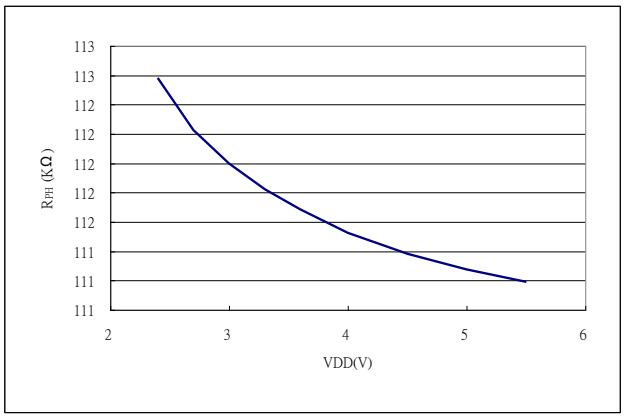
### 7.5 DAC Characteristics (V50_DAC = 5.0V, TA = 25℃)

| Characteristics | Symbol | Limit | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| DAC Resolution | RESO | - | - | 14 | bit |
| THD+n (5V @0.6W) | - | - | 1 | - | % |
| Noise at No Signal | - | - | -97 | - | dBr A |
| Dynamic Range(-60dB) | - | - | -82 | - | dBr A |

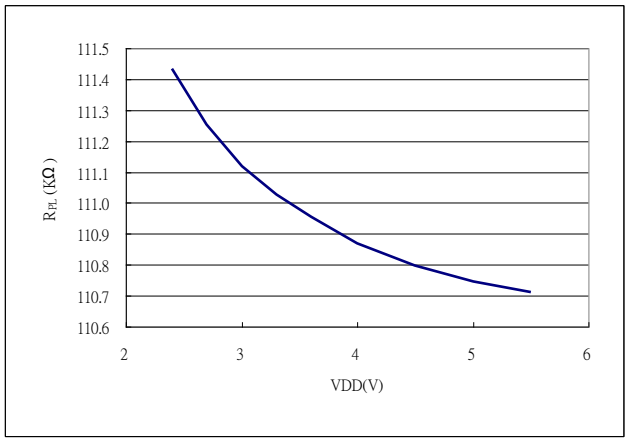
### 7.6 Regulator Characteristics ($T_A$ = 25℃)

| Characteristics | Symbol | Limit | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input Voltage | VREGI | 2.3 | 4.5 | 5.5 | V | |
| Maximum Current Output | IREGO | - | - | 60 | mA | VDD5V (Regulator in )= 4.5V, △VDD (Regulator out ) <100mV |
| Output Voltage | VREGO | 2.3 | 3.3 | 3.3 | V | |
| Standby Current | IRGES | - | 2.5 | - | uA | |

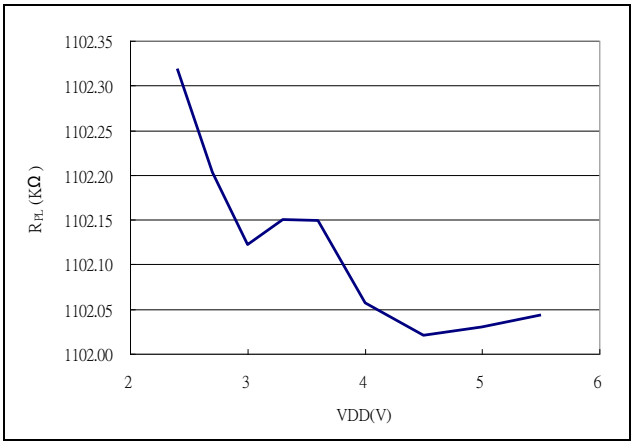
### 7.7 Pull High Resister and VDDIO




### 7.8 Pull Low Resister and VDDIO (Normal PAD)

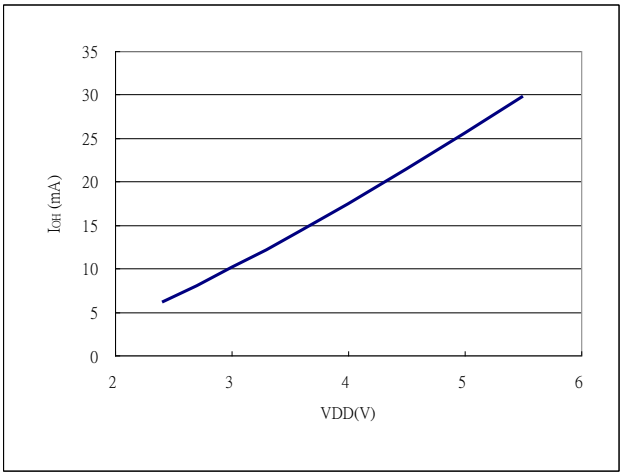



### 7.9 Pull Low Resister and VDDIO (IOB[7:0] PAD with input high)



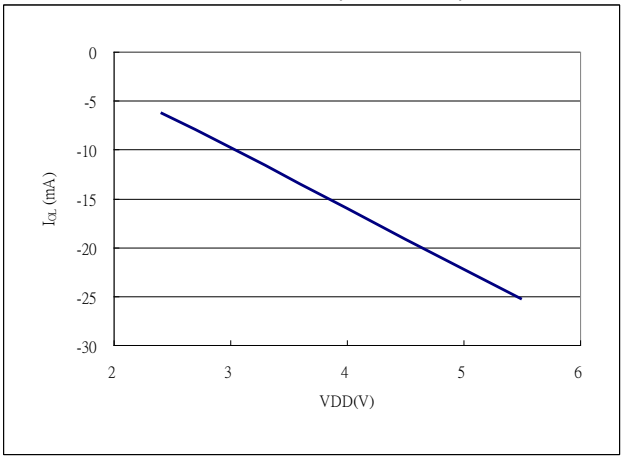

### 7.10 I/O Output High Current $I_{OH}$ and VDDIO

Test Condition: VOH = 0.7 * VDDIO



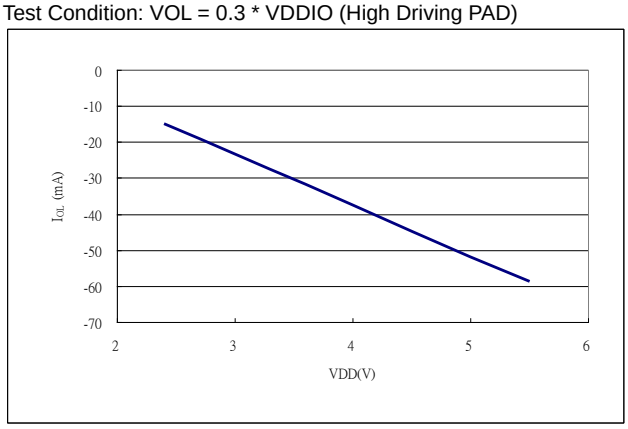
### 7.11 I/O Output Low Current $I_{OL}$ and VDDIO (Normal Pad)

Test Condition: VOL = 0.3 * VDDIO (Normal PAD)

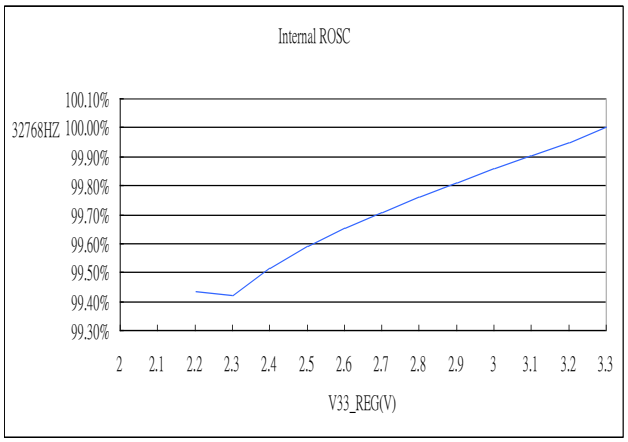



### 7.12 I/O Output Low Current $I_{OL}$ and VDDIO (High driving pad)

Test Condition: VOL = 0.3 * VDDIO (High Driving PAD)

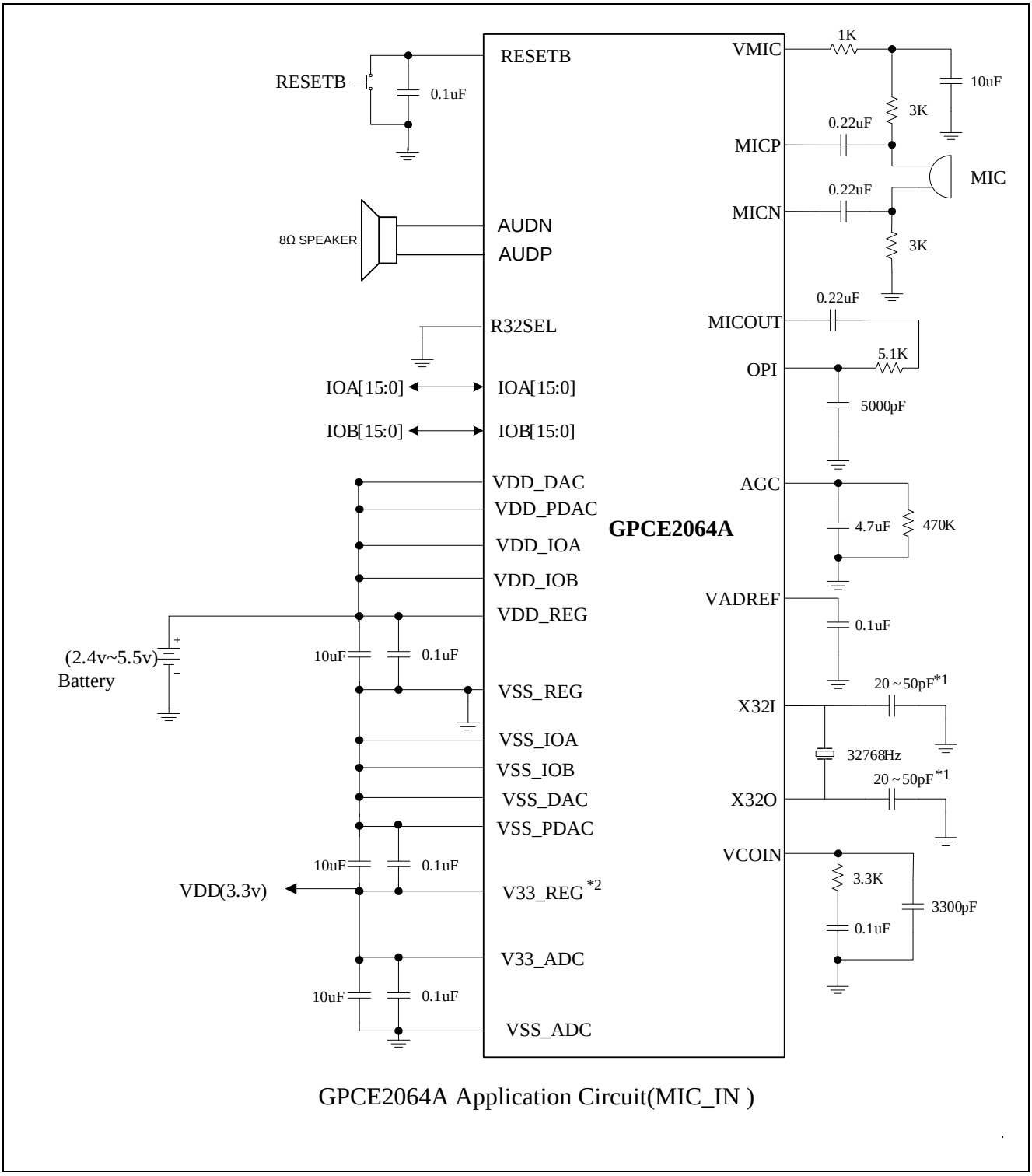



### 7.13 Internal ROSC and V33_REG



## 8 APPLICATION CIRCUITS

### 8.1 Application Circuit with Regulator, XTAL32K Selected

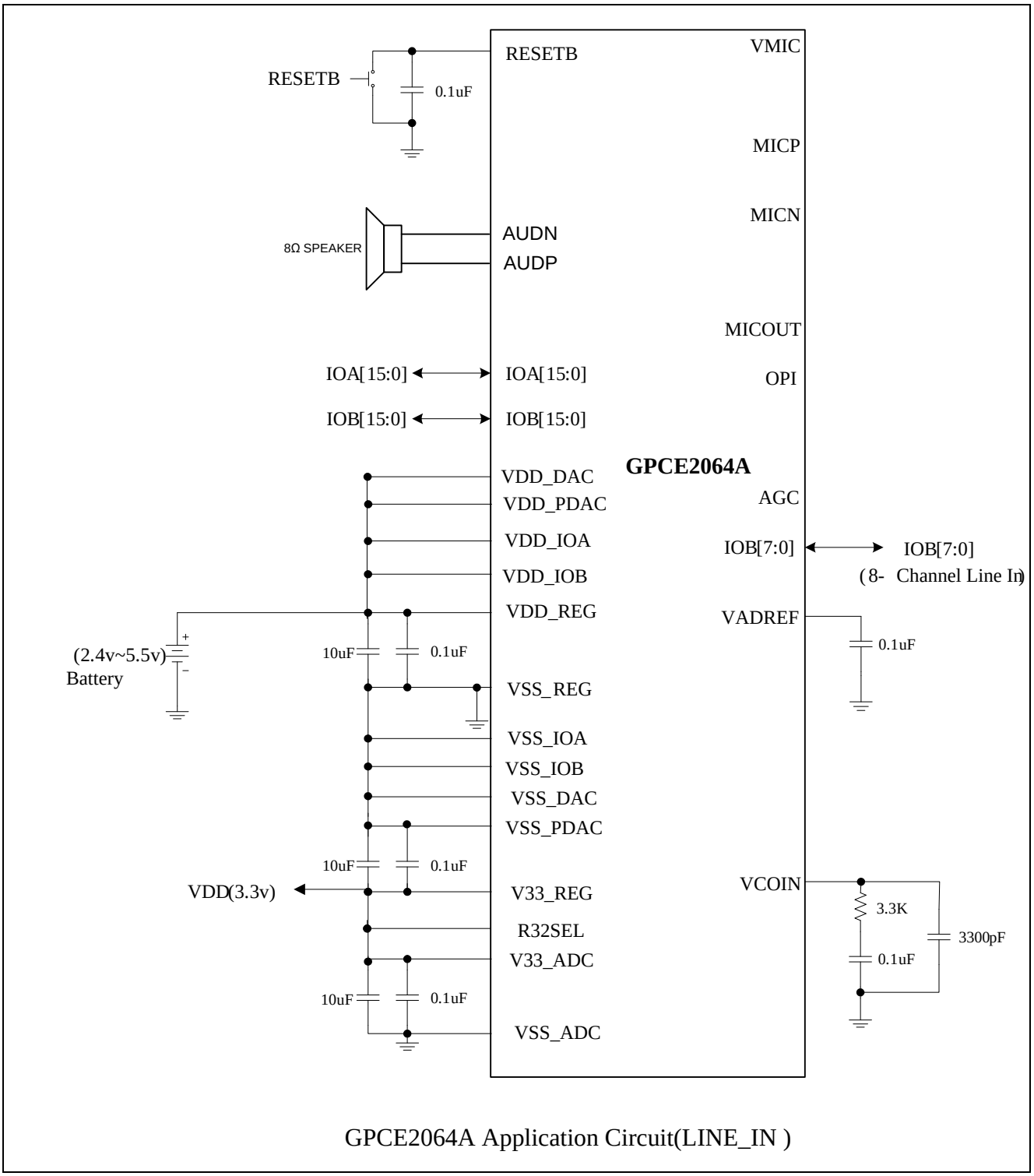



GPCE2064A Application Circuit(MIC_IN )

**Note1:** These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

**Note2:** VDD33_REG is output of built-in regulator with maximum current 60mA. It is recommended that only use it for internal power pad.

### 8.2 Application Circuit with Regulator, Internal ROSC32K Selected

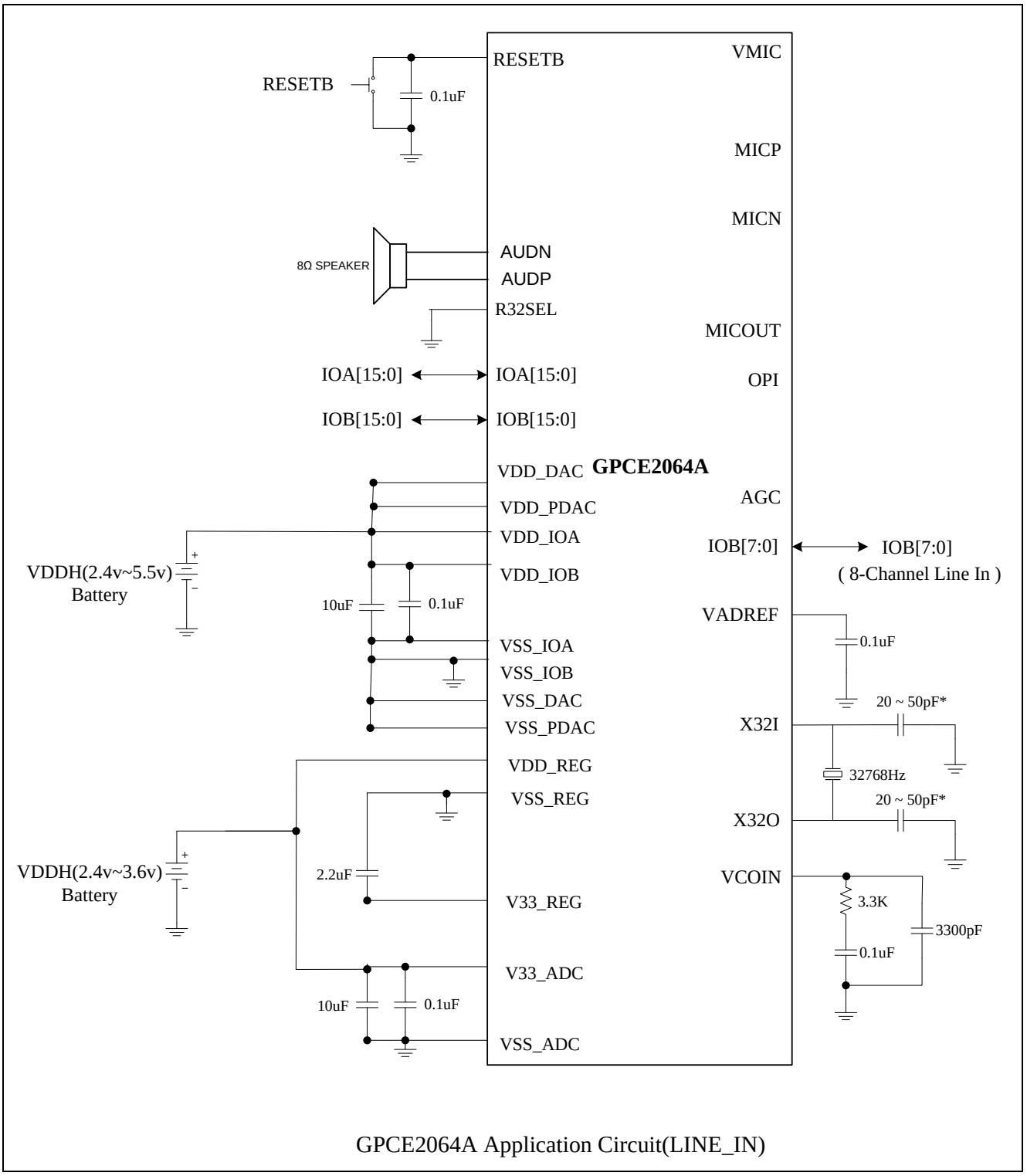



GPCE2064A Application Circuit(LINE_IN )

**Note1:** These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

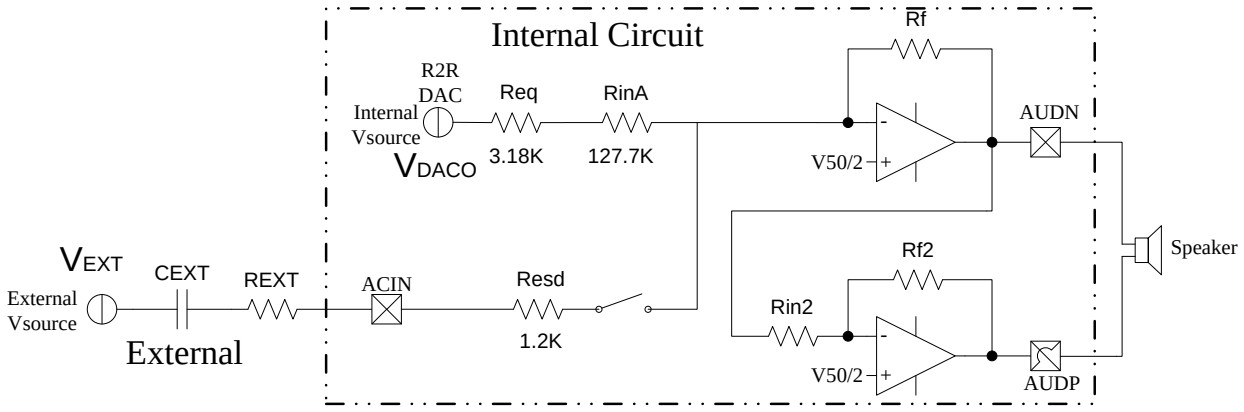
**Note2:** VDD33_REG is output of built-in regulator with maximum current 60mA. It is recommended that only use it for internal power pad.

### 8.3 Application Circuit without Regulator, XTAL32K Selected




GPCE2064A Application Circuit(LINE_IN)

### 8.4 Push Pull DAC Mixed with another DAC




$$V_{AUDN} = \frac{V_{DACO}}{R_{eq} + R_{inA}} \times R_f + \frac{V_{EXT}}{R_{EXT} + R_{ESD}} \times R_f$$

$$= \frac{V_{DACO}}{3.18K + 127.7K} \times R_f + \frac{V_{EXT}}{R_{EXT} + 1.2K} \times R_f$$

$$V_{AUDP} = -V_{AUDN}$$

# 9 PACKAGE/PAD LOCATIONS

## 9.1 Ordering Information

| Product Number | Package Type |
|---|---|
| GPCE2064A-NnnV-C | Chip form |
| GPCE2064A-NnnV-QL04x | Halogen Free Package |

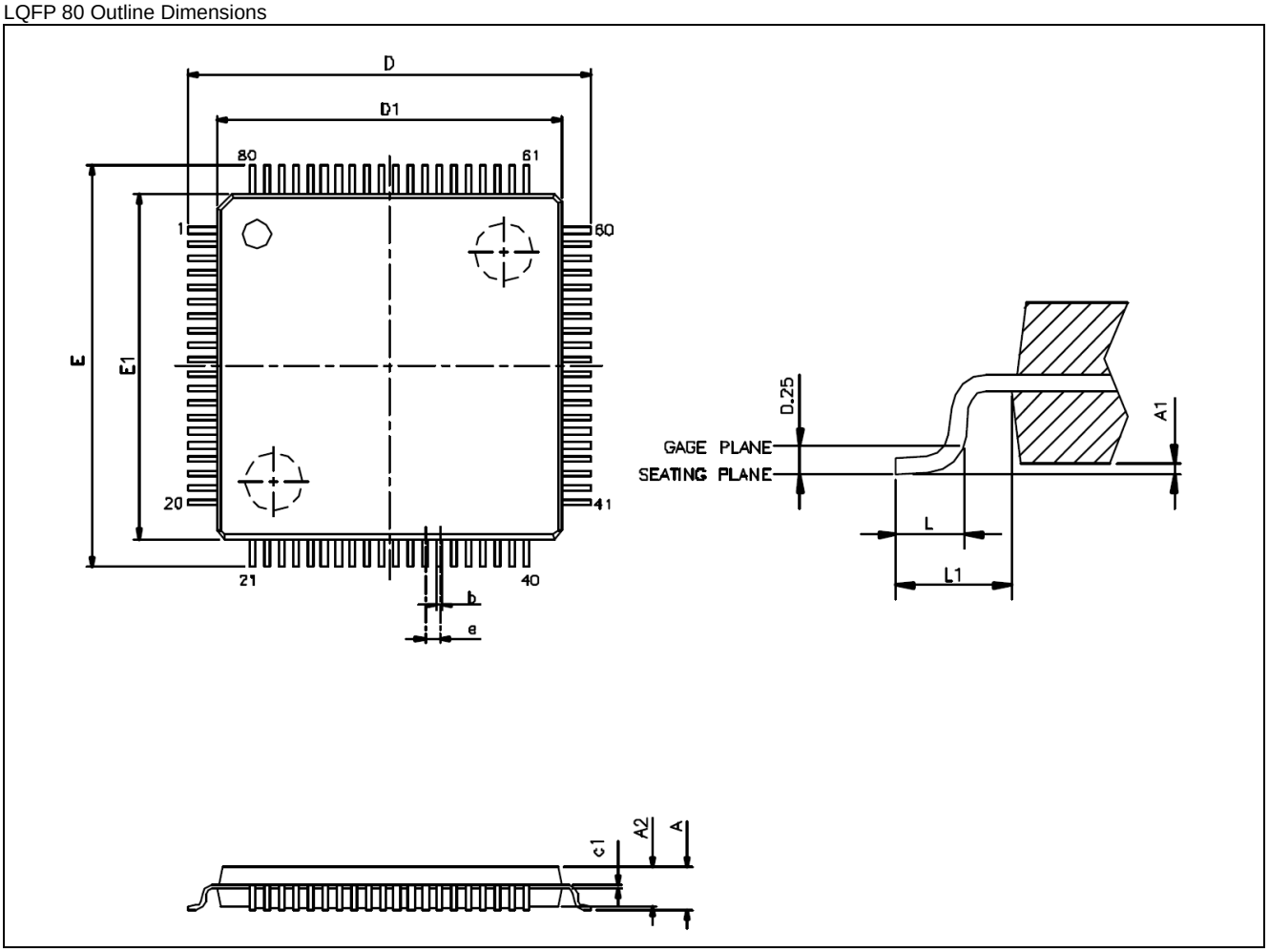
**Note1:** Code number is assigned for customer.

**Note2:** Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

**Note3:** Package form number (x = 1 - 9, serial number).

## 9.2 Package Information

LQFP 80 Outline Dimensions




| Symbol | Dimension in mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | - | 1.45 |
| b | 0.17 | - | 0.27 |
| c1 | 0.09 | - | 0.16 |
| D | 14.00 BSC | | |
| D1 | 12.00 BSC | | |

| Symbol | Dimension in mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| E | | 14.00 BSC | |
| E1 | | 12.00 BSC | |
| e | | 0.50 BSC. | |
| L | 0.45 | - | 0.75 |
| L1 | | 1 REF | |

## 10 DISCLAIMER

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## 11 REVISION HISTORY

| Date | Revision # | Description | Page |
|---|---|---|---|
| Jun 02, 2016 | 1.2 | Modify pin descriptions of chapter 5. | 6 |
| May 10, 2012 | 1.1 | 1. Add 5.2 PIN Map.<br>2. Modify 7.2 & 7.3 DC Characteristics.<br>3. Add 7.13 diagram.<br>4. Modify 8.3 diagram<br>5. Modify 9 PACKAGE/PAD LOCATIONS. | 7<br>13, 14<br>16<br>19<br>21, 22 |
| Oct. 12, 2011 | 1.0 | Original | 23 |