# Triple Buck Regulator with 1.2A and Two 600mA Outputs and Individual Programmable References

## FEATURES

- **Three Independent Current Mode Buck DC/DC Regulators (1.2A and 2 × 600mA)**
- **Single Pin Programmable $V_{FB}$ Servo Voltages from 800mV Down to 425mV (in 25mV Steps)**
- **Pull $V_{FB}$ High to Make Each 600mA Buck a Slave for Higher Current Operation**
- **Pulse-Skipping or Burst Mode® Operation**
- **Programmable Switching Frequency (1MHz to 3MHz) or Fixed 2.25MHz**
- Synchronizable (1.2MHz to 3MHz)
- $V_{IN}$ Range 2.5V to 5.5V
- All Regulators Internally Compensated
- PGOOD Output Flag
- Quiescent Current <100µA (All Regulators in Burst Mode Operation)
- Zero Shutdown Current
- Overtemperature and Short-Circuit Protection
- Tiny 3mm × 3mm, 3mm × 4mm 20-Lead QFN and Thermally Enhanced TSSOP FE-16 Packages

## APPLICATIONS

- Portable Applications with Multiple Supply Rails
- General Purpose Step-Down DC/DC
- Dynamic Voltage Scaling Applications

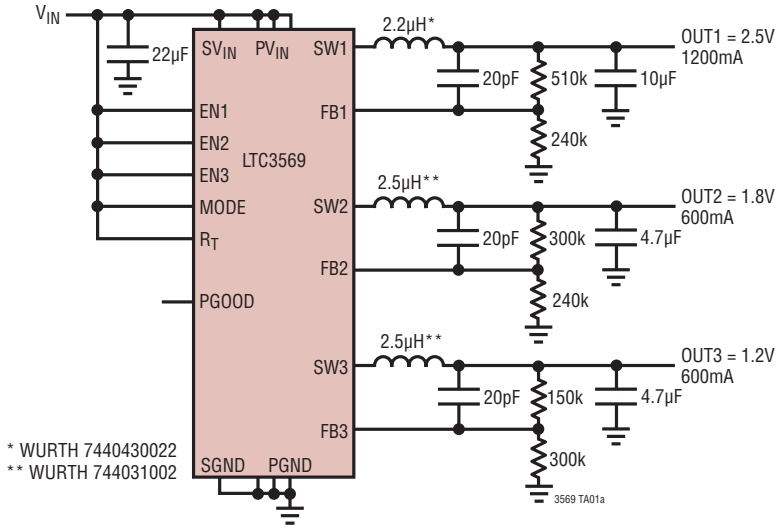
## DESCRIPTION

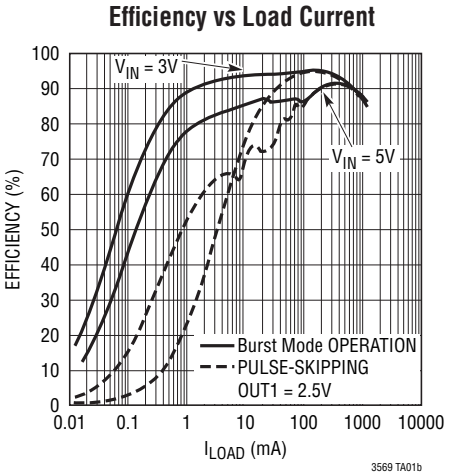
The LTC®3569 contains three monolithic, synchronous step-down DC/DC converters. Intended for medium power applications, it operates over a 2.5V to 5.5V input voltage range. The operating frequency is adjustable from 1MHz to 3MHz, allowing the use of tiny, low cost capacitors and inductors. The three output voltages are independently programmable by toggling the EN pins up to 15 times, lowering the 800mV FB references by 25mV per cycle. The first buck regulator sources load currents up to 1200mA. The other two buck regulators each provide 600mA.

The two 600mA buck regulators can also be configured to operate as slave power stages, running in parallel with another internal buck regulator to supply higher load currents. When operating as parallel, slave output stages, discrete external components are shared and available output currents sum together.

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## TYPICAL APPLICATION



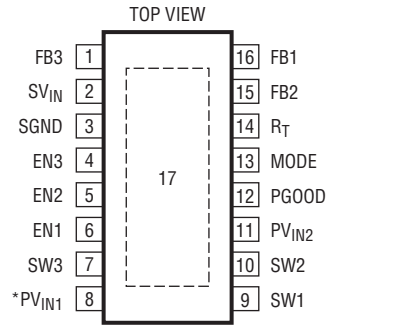



## ABSOLUTE MAXIMUM RATINGS (Notes 1, 6)

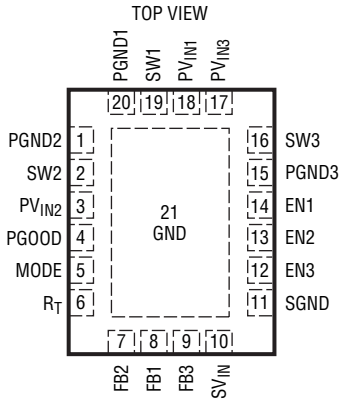
$SV_{IN}$ Voltage .....–0.3V to 6V (7V Transient)
$PV_{INX}$ Voltage.....$S_{VIN}$ – 0.3V to $S_{VIN}$ + 0.3V
ENx, MODE, PGOOD, SWx, FBx ..... –0.3V to $S_{VIN}$ + 0.3V
$R_T$ Voltage..... –0.3V to 6V
PGOOD Current..... ±1mA

Operating Junction Temperature Range
(Notes 6, 7)..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C
Peak Reflow Temperature ..... 260°C

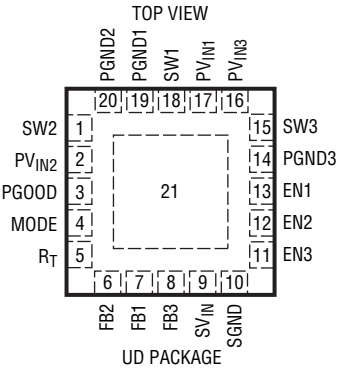
## PIN CONFIGURATION




FE PACKAGE
16-LEAD PLASTIC TSSOP
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 38°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB
*SHARES POWER WITH $PV_{IN3}$




UDC PACKAGE
20-LEAD (3mm × 4mm) PLASTIC QFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 43°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB




UD PACKAGE
20-LEAD (3mm × 3mm) PLASTIC QFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 68°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3569EUD#PBF | LTC3569EUD#TRPBF | LDQF | 20-Lead (3mm × 3mm) Plastic QFN | –40°C to 125°C |
| LTC3569IUD#PBF | LTC3569IUD#TRPBF | LDQF | 20-Lead (3mm × 3mm) Plastic QFN | –40°C to 125°C |
| LTC3569EUDC#PBF | LTC3569EUDC#TRPBF | LFYW | 20-Lead (3mm × 4mm) Plastic QFN | –40°C to 125°C |
| LTC3569IUDC#PBF | LTC3569IUDC#TRPBF | LFYW | 20-Lead (3mm × 4mm) Plastic QFN | –40°C to 125°C |
| LTC3569EFE#PBF | LTC3569EFE#TRPBF | 3569FE | 16-Lead Plastic TSSOP | –40°C to 125°C |
| LTC3569IFE#PBF | LTC3569IFE#TRPBF | 3569FE | 16-Lead Plastic TSSOP | –40°C to 125°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 3.6V unless otherwise noted (Notes 2, 7).**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $SV_{IN}$ | Input Supply Voltage | | ● | 2.5 | | 5.5 | V |
| $I_{VIN}$ | Input Current Pulse-Skipping Mode | EN1 = $SV_{IN}$, EN2, EN3 = MODE = 0V, $I_{OUT1}$, = 0A, FB1 = 0.9V (Note 3) | | | 230 | 365 | µA |
| | Input Current Burst Mode Operation | EN1 = MODE = $SV_{IN}$, EN2, EN3 = 0V, $I_{OUT1}$, = 0A, FB1 = 0.9V (Note 3) | | | 47 | 82 | µA |
| $I_{QX}$ | Additional Input Current per Buck, Pulse Skipping | MODE = 0V, $I_{OUTX}$, = 0A, FBx = 0.9V (Note 3) | | | 140 | 225 | µA |
| | Additional Input Current per Buck, Burst Mode Operation | MODE = $SV_{IN}$, $I_{OUTX}$, = 0A, FBx = 0.9V (Note 3) | | | 22 | 36 | µA |
| $I_{QSHDN}$ | Quiescent Current in Shutdown Mode | EN1, EN2, EN3 = 0V<br>$V_{SW1}$ = $V_{SW2}$ = $V_{SW3}$ = 0V | | | 0.1 | 1 | µA |
| $I_{PK1}$ | Peak Inductor Current SW1 | | | 1.8 | 2.0 | 2.5 | A |
| $I_{PK2}$, $I_{PK3}$ | Peak Inductor Current SW2, SW3 | | | 0.780 | 1.0 | 1.3 | A |
| $V_{FBX(MAX)}$ | Maximum Feedback Voltage | | ● | 0.784 | 0.8 | 0.816 | V |
| $V_{FBX(STEP)}$ | Feedback Reference Step Size | Each Toggle on ENx | | | 25 | | mV |
| $V_{FBX(MIN)}$ | Minimum Feedback Voltage | ENx Toggle 15 Times | ● | 0.405 | 0.425 | 0.44 | V |
| $V_{PROGFBX}$ | Feedback Programming Range | | | 0.425 | | 0.8 | V |
| $I_{FBX}$ | Feedback Pin Input Current | $V_{FB}$ = 0.8V | ● | | | ±0.2 | µA |
| $I_{LKSWX}$ | Switch Pin Leakage Current | $V_{SWX}$ = 1.8V, $V_{ENX}$ = $SV_{IN}$, $V_{FBX}$ = 0.9V | | | | ±1 | µA |
| $D_X$ | Maximum Duty Cycle | FBx = 0V | | 100 | | | % |
| $R_{P1}$ | $R_{DSON}$ of PSW for SW1 | $I_{SW1}$ = 100mA (Note 5) | | | 195 | | mΩ |
| $R_{N1}$ | $R_{DSON}$ of NSW for SW1 | $I_{SW1}$ = –100mA (Note 5) | | | 180 | | mΩ |
| $R_{P2}$, $R_{P3}$ | $R_{DSON}$ of PSW for SW2, SW3 | $I_{SW2}$, $I_{SW3}$ = 100mA (Note 5) | | | 265 | | mΩ |
| $R_{N2}$, $R_{N3}$ | $R_{DSON}$ of NSW for SW2, SW3 | $I_{SW2}$, $I_{SW3}$ = –100mA (Note 5) | | | 250 | | mΩ |
| RSWx_PD | SWx Pull-Down in Shutdown | ENx = 0V, $V_{SWX}$ = 1.2V, (FBx < $SV_{IN}$ ) | | | 2.3 | | kΩ |
| $\Delta V_{LINEREG}$ | Reference Voltage Line Regulation | $SV_{IN}$ = 2.5V to 5.5V | | | 0.04 | 0.2 | %/V |
| $\Delta V_{LOADREG}$ | Output Voltage Load Regulation | Pulse-Skipping Mode (Note 4) | | | 0.5 | | % |
| $t_{SS}$ | Soft-Start Reference Ramp Rate | | | | 0.75 | | V/ms |
| $t_{EN}$ | Enable Turn-On Delay | From Last ENx Rise to Begin of Soft-Start Ramp | | | 125 | 240 | µs |
| $t_{OFF}$ | Enable Turn-Off Delay | From ENx Fall to Shutdown | | | 170 | 330 | µs |
| $t_{PW}$ | Enable Pulse Width | | | 0.06 | | 55 | µs |
| $I_{ENX}$ | Enable Leakage Current | $V_{ENX}$ = 3.6V | | | 0.02 | | µA |
| $I_{MODE}$ | Mode Leakage Current | $V_{MODE}$ = 3.6V | | | 0.02 | | µA |
| $V_{IL}$ | Input Low Voltage | MODE, ENx | | | | 0.4 | V |
| $V_{IH}$ | Input High Voltage | MODE, ENx | | 1.2 | | | V |
| $T_{MODEPW}$ | Pulse Width Applied to MODE Pin for Synchronizing | | | 100 | | | ns |
| PGOOD | Power Good Threshold | $V_{FBX}$ Ramping Up<br>$V_{FBX}$ Ramping Down | | | –8<br>–12 | | %<br>% |
| $T_{PGOOD}$ | PGOOD Delay | Turn-On | | | 8 | | µs |
| | | Turn-Off | | | 2 | | µs |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 3.6V unless otherwise noted (Notes 2, 7).**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $R_{PGOOD}$ | PGOOD Pull-Down On-Resistance | $V_{FBX}$ < 0.4V | | | 380 | 525 | Ω |
| UVLO | Undervoltage Lockout | | ● | | | 2.5 | V |
| $f_{OSC}$ | Fixed Oscillator Frequency | $V_{RT} = SV_{IN}$ | ● | 1.9 | 2.25 | 2.8 | MHz |
| $f_{CLK(MAX)}$ | Maximum Programmable Oscillator Frequency | $R_T$ = 100k | ● | 3.0 | | | MHz |
| $f_{CLK(MIN)}$ | Minimum Programmable Oscillator Frequency | $R_T$ = 453k | ● | | | 1.0 | MHz |
| $f_{SYNC}$ | Sync Frequency | $V_{RT} = SV_{IN}$ | | | | 3 | MHz |
| | | $R_T$ = 453k | | 1.2 | | | MHz |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Current into a pin is positive and current out of a pin is negative. All voltages referenced to SGND.

**Note 3:** Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

**Note 4:** Specification is guaranteed by design and not 100% tested in production.

**Note 5:** Switch on-resistance verified by correlation to wafer level measurements.

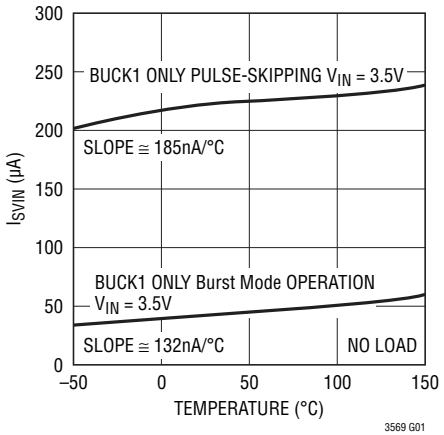
**Note 6:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature exceeds 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

**Note 7:** The LTC3569 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3569E is guaranteed to meet specified performance from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design characterization and correlation with statistical process controls. The LTC3569I is guaranteed to meet specified performance over the full –40°C to 125°C operating junction temperature range.

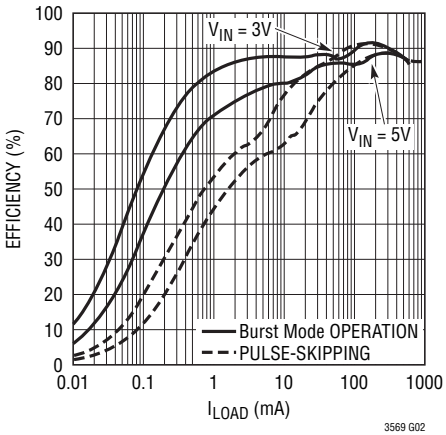
## TYPICAL PERFORMANCE CHARACTERISTICS

**$T_A$ = 25°C, unless otherwise noted.**

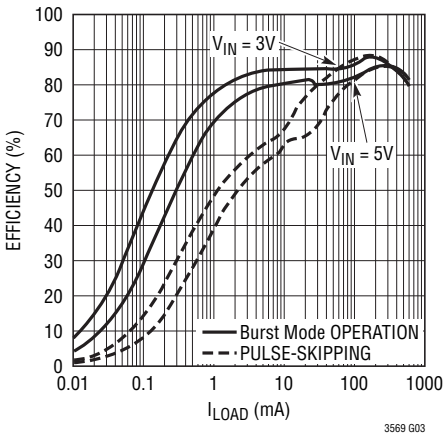
**$I_{SVIN}$ vs Temperature**




**Efficiency vs Load Current OUT2 = 1.8V**

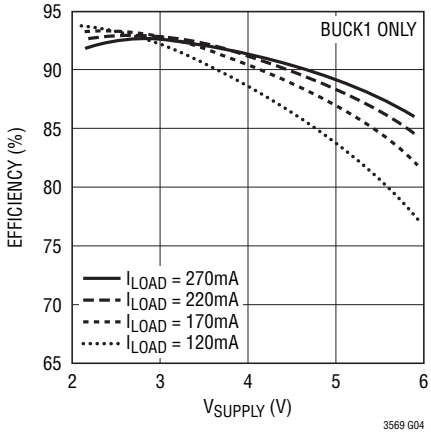



**Efficiency vs Load Current OUT3 = 1.2V**

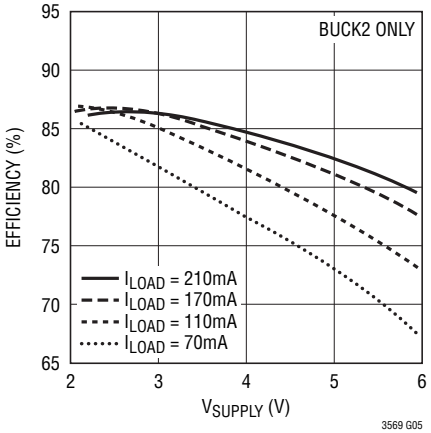


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

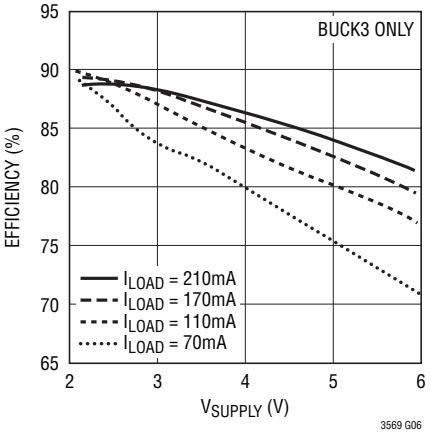
### Efficiency vs $V_{SUPPLY}$ OUT1 = 1.8V



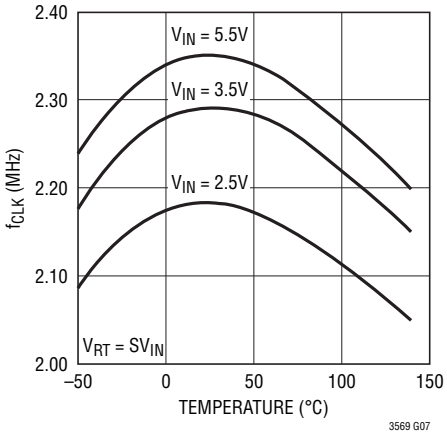

### Efficiency vs $V_{SUPPLY}$ OUT2 = 1.2V



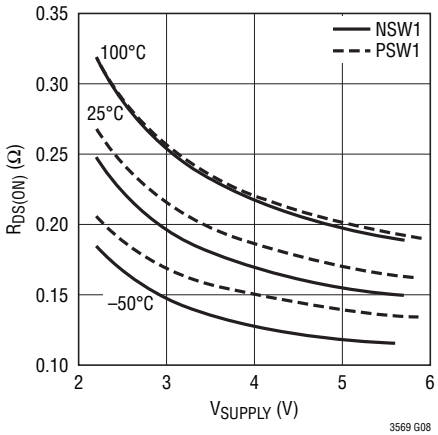

### Efficiency vs $V_{SUPPLY}$ OUT3 = 1.5V



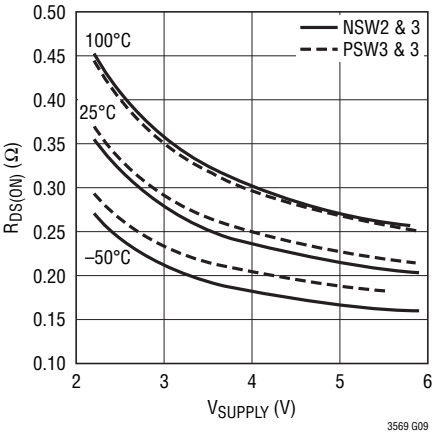

### Oscillator Frequency vs Temperature



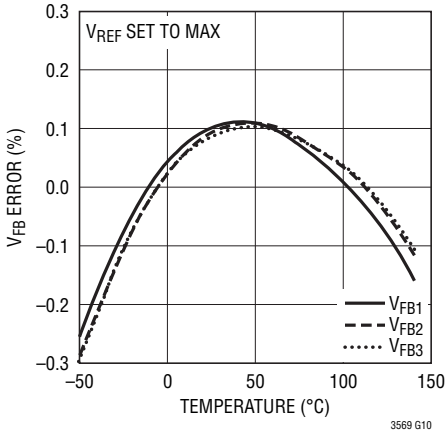

### $R_{DS(ON)}$ SW1 vs $V_{SUPPLY}$ and Temperature



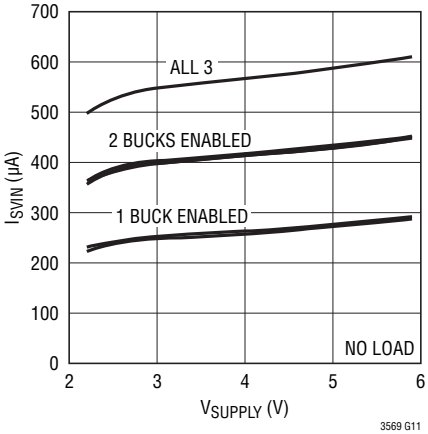

### $R_{DS(ON)}$ SW2 and SW3 vs $V_{SUPPLY}$ and Temperature



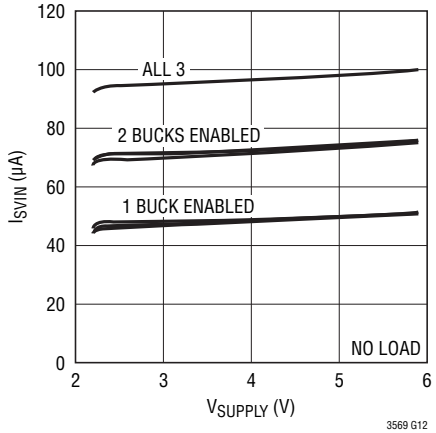

### $V_{FB}$ vs Temperature




### $I_{SVIN}$ vs $V_{SUPPLY}$ Pulse-Skipping

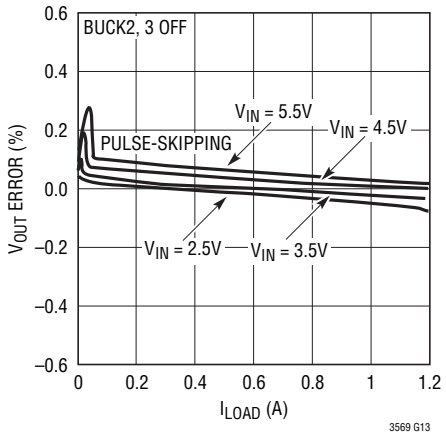



### $I_{SVIN}$ vs $V_{SUPPLY}$ Burst Mode Operation

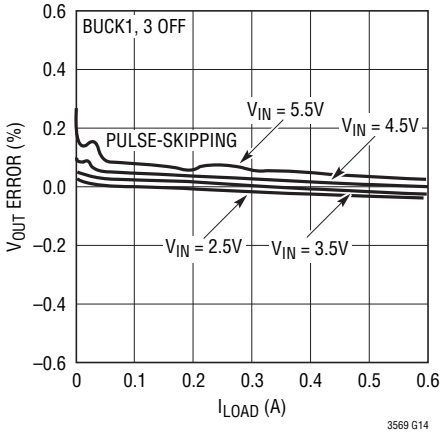


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

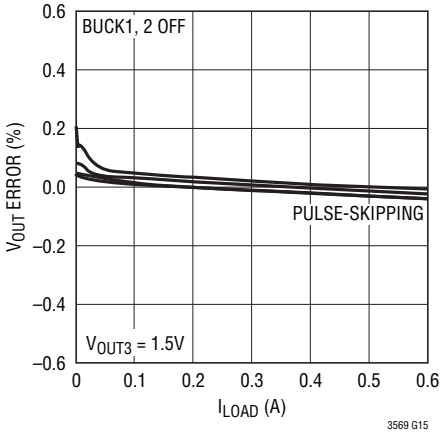
### Buck1 Load Regulation



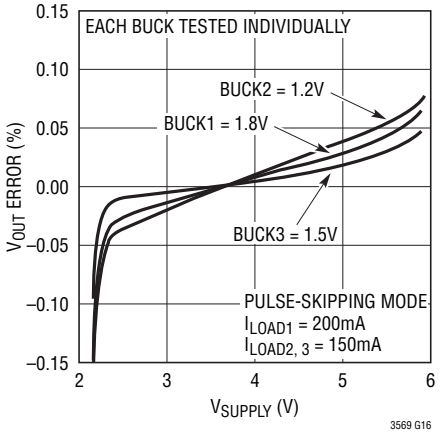

### Buck2 Load Regulation



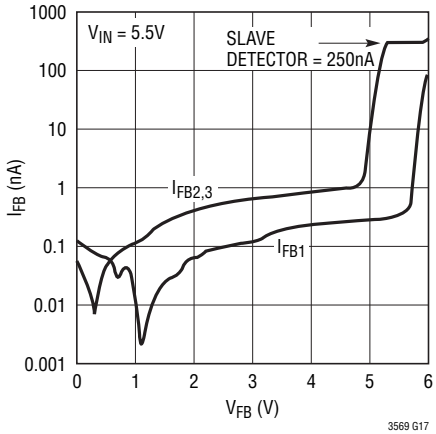

### Buck3 Load Regulation



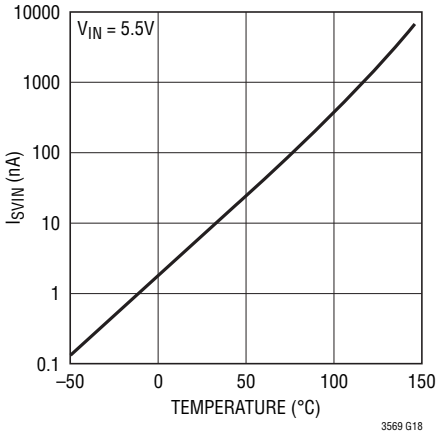

### Line Regulation




### FB Pin Leakage

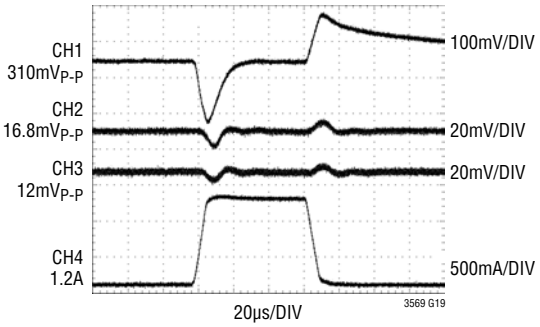



### $I_{QSD}$ vs Temperature

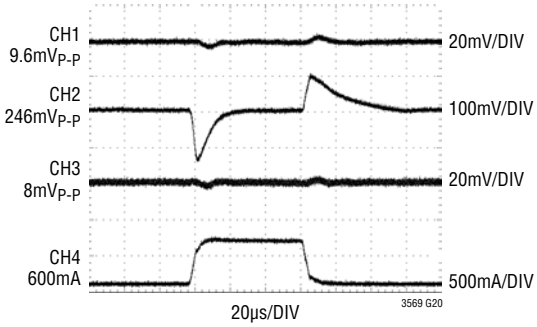


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

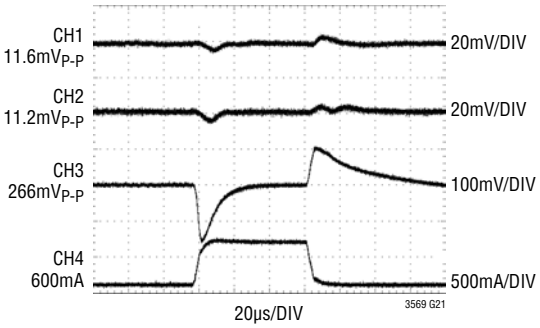
**Load Step Cross Talk, Pulse-Skipping, $V_{IN}$ = 3.6V, CH1 = $V_{OUT1}$, CH2 = $V_{OUT2}$, CH3 = $V_{OUT3}$, CH4 = $I_{LOAD1}$**



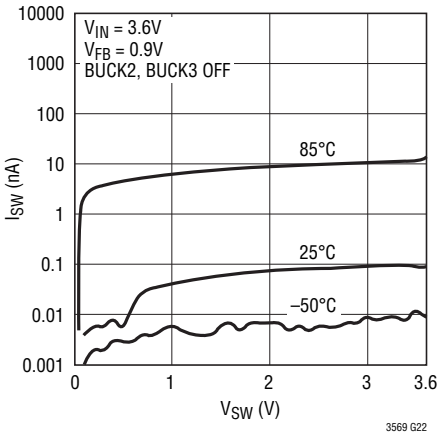

**Load Step Cross Talk, Pulse-Skipping, $V_{IN}$ = 3.6V, CH1 = $V_{OUT1}$, CH2 = $V_{OUT2}$, CH3 = $V_{OUT3}$, CH4 = $I_{LOAD2}$**



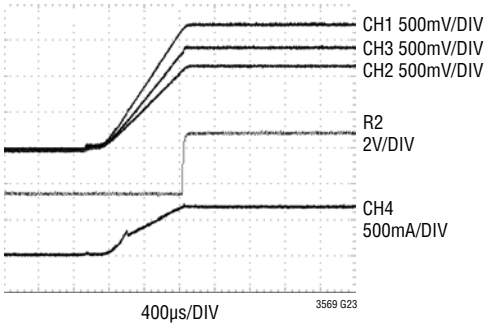

**Load Step Cross Talk, Pulse-Skipping, $V_{IN}$ = 3.6V, CH1 = $V_{OUT1}$, CH2 = $V_{OUT2}$, CH3 = $V_{OUT3}$, CH4 = $I_{LOAD3}$**



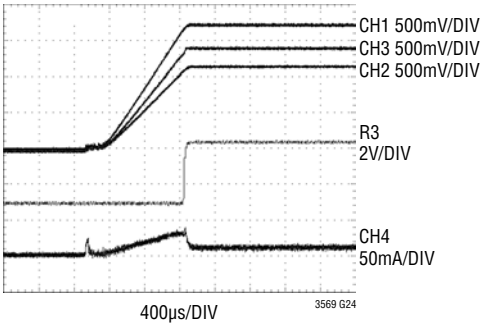

**$I_{SW}$ Leakage vs $V_{SUPPLY}$ Buck 1**




**Soft-Start Into Heavy Load, PS, $V_{IN}$ = 3.6V, CH1 = $V_{OUT1}$, CH2 = $V_{OUT2}$, CH3 = $V_{OUT3}$, CH4 = $I_{IN}$, R2 = PGOOD**




**Soft-Start Into Light Load, PS, $V_{IN}$ = 3.6V, CH1 = $V_{OUT1}$, CH2 = $V_{OUT2}$, CH3 = $V_{OUT3}$, CH4 = $I_{IN}$, R3 = PGOOD**



## PIN FUNCTIONS

**EN1:** Enable Pin for Buck 1. Toggle up to 15 times to program reference feedback level from 800mV down to 425mV.

**EN2:** Enable Pin for Buck 2. Toggle up to 15 times to program reference feedback level from 800mV down to 425mV.

**EN3:** Enable Pin for Buck 3. Toggle up to 15 times to program reference feedback level from 800mV down to 425mV.

**FB1:** Receives the feedback voltage from the external resistive divider across the output of Buck 1. Nominal voltage for this pin is programmed with the EN1 pin from 800mV down to 425mV.

**FB2:** Receives the feedback voltage from the external resistive divider across the output of Buck 2. Nominal voltage for this pin is programmed with the EN2 pin from 800mV down to 425mV. When pulled to $SV_{IN}$, Buck 2 is put into slave mode, following Buck 1.

**FB3:** Receives the feedback voltage from the external resistive divider across the output of Buck 3. Nominal voltage for this pin is programmed with the EN3 pin from 800mV down to 425mV. When pulled to $SV_{IN}$, Buck 3 is put into slave mode, following Buck 2.

**GND (Exposed Pad):** The exposed pad must be connected to PCB ground for rated thermal performance and for electrical connection in the TSSOP package.

**MODE:** Combination Mode Selection and Oscillator Synchronization Pin. This pin controls the operating mode of the device. When tied to $SV_{IN}$, Burst Mode operation is selected. When tied to SGND, pulse-skipping mode is selected. The internal clock frequency synchronizes to an external oscillator applied to this pin. When synchronizing to an external clock, drive this pin with a logic-level signal with high and low pulse widths of at least 100ns. When synchronizing to an external clock, pulse-skipping mode is automatically selected.

**PGND1:** Main Power Ground Pin for Buck 1. Connect to the (–) terminal of the output capacitor for Buck1, and (–) terminal of $C_{IN1}$. Decoupling capacitors should be summed where power supply pins are shared.

**PGND2:** Main Power Ground Pin for Buck 2. Connect to the (–) terminal of the output capacitor for Buck2, and (–) terminal of $C_{IN2}$. Decoupling capacitors should be summed where power supply pins are shared.

**PGND3:** Main Power Ground Pin for Buck 3. Connect to the (–) terminal of the output capacitor for Buck3, and (–) terminal of $C_{IN3}$. Decoupling capacitors should be summed where power supply pins are shared.

**PGOOD:** The Power Good Pin. This open-drain output is released when an enabled output has risen to within 8% of the regulation voltage. When multiple outputs are enabled, PGOOD is the logical AND of each internal PGOOD.

**$PV_{IN1}$:** Main Supply Pin for Buck 1. Decouple to PGND1 with a low ESR 4.7µF capacitor, $C_{IN1}$. Decoupling capacitors should be summed where power supply pins are shared.

**$PV_{IN2}$:** Main Supply Pin for Buck 2. Decouple to PGND2 with a low ESR 4.7µF capacitor, $C_{IN2}$. Decoupling capacitors should be summed where power supply pins are shared.

**$PV_{IN3}$:** Main Supply Pin for Buck 3. Decouple to PGND3 with a low ESR 4.7µF capacitor, $C_{IN3}$. Decoupling capacitors should be summed where power supply pins are shared. For 16-lead plastic TSSOP FE package, $PV_{IN1}$ and $PV_{IN3}$ share pin 8.

**$R_T$:** Timing Resistor Pin. The free-running oscillator frequency is programmed by connecting a resistor from this pin to ground. Tie to $SV_{IN}$ to get a fixed 2.25MHz operating frequency.

**SGND:** Main Ground Pin. Decouple to $SV_{IN}$.

**$SV_{IN}$:** Main Supply Pin. Decouple to SGND with a low ESR 1µF capacitor.

**SW1:** Buck 1 Switch. Connect to the Inductor for Buck 1. This pin swings from $PV_{IN1}$ to PGND1.

**SW2:** Buck 2 Switch. Connect to the Inductor for Buck 2. This pin swings from $PV_{IN2}$ to PGND2.

**SW3:** Buck 3 Switch. Connect to the Inductor for Buck 3. This pin swings from $PV_{IN3}$ to PGND3.

## BLOCK DIAGRAM

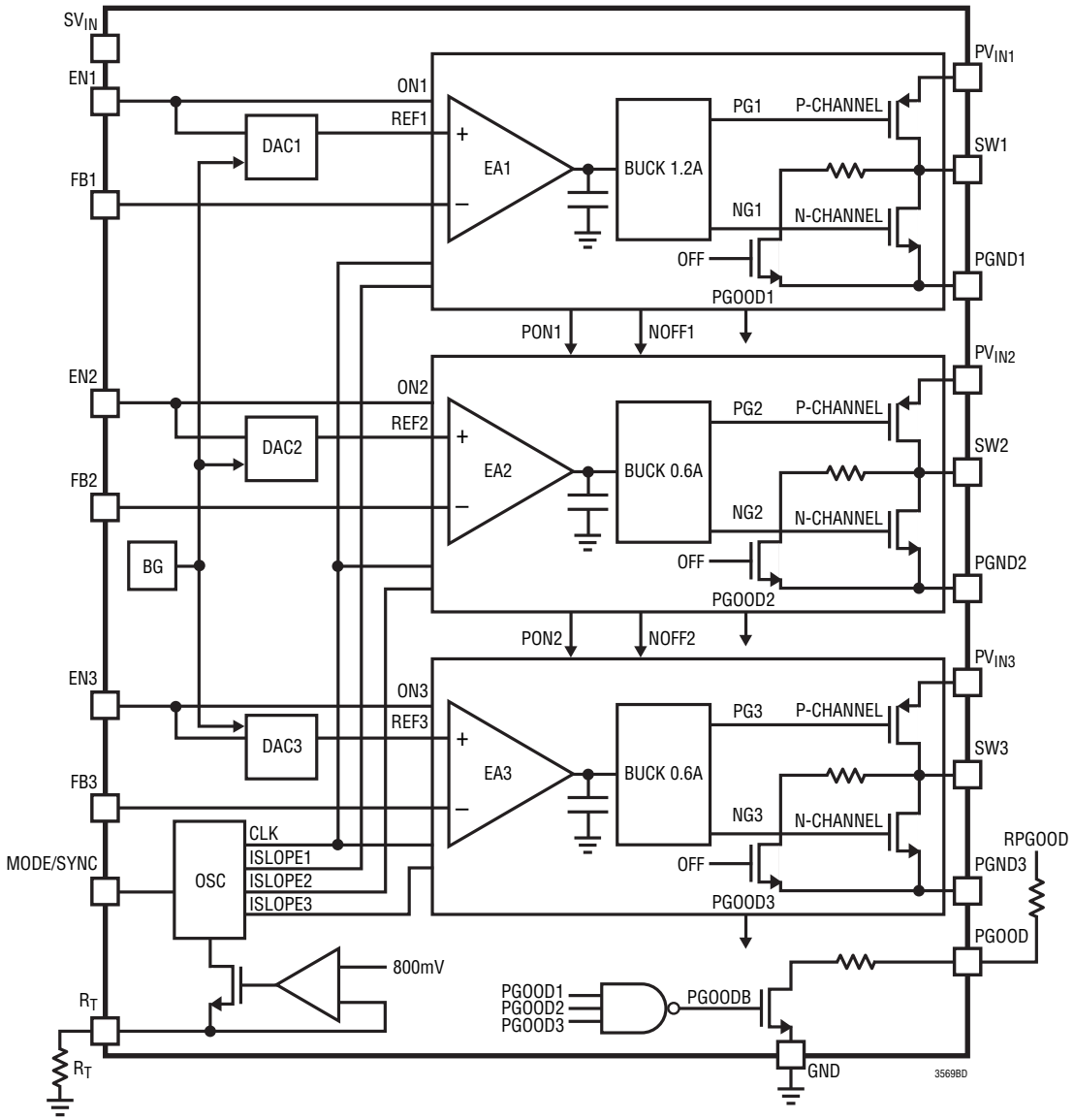



**Figure 1. Detailed Block Diagram**

# OPERATION

## Introduction

The LTC3569 contains three constant-frequency, current mode buck DC/DC regulators. Both the P-channel and synchronous rectifier (N-channel) switches are internal to each buck. The operating frequency is determined by the value of the $R_T$ resistor, or is fixed to 2.25MHz by pulling the $R_T$ pin to $SV_{IN}$, or is synchronized to an external oscillator tied to the MODE pin. Users may select pulse-skipping or Burst Mode operation to trade off output ripple for efficiency. Independent programmable reference levels allow the LTC3569 to suit a variety of applications.

The LTC3569 offers different power levels, a single 1.2A buck as well as two 600mA bucks. These three bucks may be configured in different parallel configurations, for versatile high current operation. The power stage of buck 2 can be configured as a slave to buck 1, by pulling FB2 to $SV_{IN}$. The power stage of buck 3, can be configured to be a slave to buck 2, by pulling the FB3 pin to $SV_{IN}$. To enable the slave power stage, pull the respective EN pin high. However if the master is disabled, the slave power stage is Hi-Z.

Each of the buck regulators supports 100% duty cycle operation (low dropout mode) when their input voltage drops very close to their output voltage. The switching regulators also include soft-start to limit inrush current when powering on, and short-circuit current protection.

## Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle. The P-channel current ramps up as the inductor charges. The peak inductor current is controlled by the internally compensated error amplifier output, $I_{TH}$. The current comparator (PCOMP) turns off the P-channel and turns on the N-channel synchronous rectifier when the inductor current reaches the $I_{TH}$ level minus the offset of the slope compensation ramp. The energy stored in the inductor continues to flow through the bottom switch (N-channel) and into the load until either the inductor current approaches zero, or the next clock cycle begins. If the inductor current approaches zero the N comparator

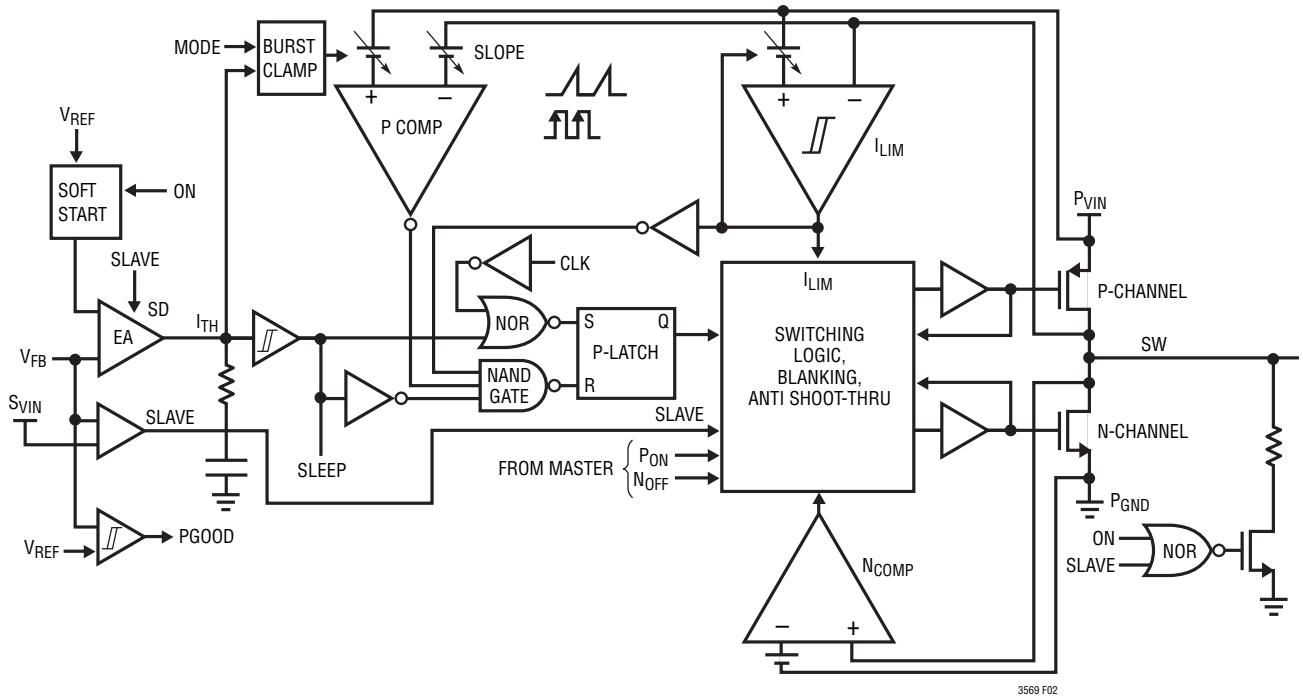



**Figure 2. Buck Block Diagram**

## OPERATION

(NCOMP) signals to turn-off the N-channel switch, so that is does not discharge the output capacitor. When a rising clock edge occurs, the P-channel switch turns on repeating the cycle.

The peak inductor current is controlled by the error amplifier (EA) and is influenced by the slope compensation. The error amplifier compares the FB pin voltage to the programmed internal reference (REF). When the load current increases, the FB voltage decreases. When the FB voltage falls below the reference voltage, the error amplifier output rises to increase the peak inductor current until the average inductor current matches the new load current. With the inductor current equal to the load current, the duty cycle will stabilize to a value equal to $V_{OUT}/V_{IN}$.

### Low Current Operation

At light loads, the FB voltage may rise above the reference voltage. If this occurs the error amplifier signals the control loop to go to sleep, and the P-channel turns off immediately. The inductor current then discharges through the N-channel switch until the inductor current approaches zero; whereupon the SW goes Hi-Z, and the output capacitor supplies power to the load. When the load discharges the output capacitor the feedback voltage falls and the error amp wakes up the buck, restarting the main control loop as if a clock cycle has just begun. This sleep cycle helps minimize the switching losses which are dominated by the gate charge losses of the power devices. Two operating modes are available to control the operation of the LTC3569 at low currents, Burst Mode operation and pulse-skipping mode.

Select Burst Mode operation to optimize efficiency at low output currents. In Burst Mode operation the inductor current reaches a fixed current before the P-channel switch compares inductor current against the value determined by $I_{TH}$. This burst clamp causes the output voltage to rise above the regulation voltage and forces a longer sleep cycle. This greatly reduces switching losses and average quiescent current at light loads, at the cost of higher ripple voltage.

Pulse-skipping mode is intended for lower output voltage ripple at light load currents. Here, the peak P-channel current is compared with the value determined by the error amplifier output. Then, the P-channel is turned off and the N-channel switch is turned on until either the next cycle begins or the N-channel comparator (NCOMP) turns off the N-channel switch. If the NCOMP trips, the SW node goes Hi-Z and the buck operates discontinuously. In pulse-skipping mode the LTC3569 continues to switch at a constant frequency down to very low currents; where it eventually begins skipping pulses. Because the LTC3569 remains active at lighter load currents in pulse-skipping mode, the efficiency performance is traded off against output voltage ripple and electromagnetic interference (EMI).

### Dropout Operation

When the input supply voltage decreases towards the output voltage the duty cycle automatically increases to 100%; which is the dropout condition. In dropout, the P-channel switch is turned on continuously with the output voltage being equal to the input voltage minus the voltage drop across the internal P-channel switch and the inductor.

### Low Supply Operation

The LTC3569 incorporates an undervoltage lockout circuit which shuts down the part when the input voltage drops below 2.5V to prevent unstable operation. The UVLO function does not reset the reference voltage DAC. (See Programming the Reference.)

### Slave Power Stage

When the FB pin of one of the two 600mA regulators is tied to $SV_{IN}$ that regulator's control circuits are disabled and the regulator's switch pin is configured to follow a master regulator; either the first 600mA regulator (regulator 2) or the 1.2A regulator (regulator 1). In this way, two regulator power stages are ganged together (e.g., switch pins shorted together to a single inductor) to support higher current levels. This permits three permutations of power levels: three independent regulators at 1.2A, 600mA and

## OPERATION

600mA; two independent regulators at 1.2A each, where regulator 3 is placed in slave mode to regulator 2 and regulator 1 operates independently; or one 1.8A regulator and a second 600mA regulator, where regulator 2 is placed in slave mode to regulator 1, and regulator 3 is independent.

When regulator 2 is operating as a slave, pull pins EN2 and FB2 up to $SV_{IN}$ to enable the slave power stage. Likewise when regulator 3 is operated as a slave, pull pins EN3 and FB3 up to $SV_{IN}$ to enable the slave power stage. If the EN pin of the slave device is pulled low, then the slave power stage is disabled and that SW pin is Hi-Z.

### Shutdown and Soft-Start

The main control loop is shut down after pulling the ENx pin to ground and waiting for the $t_{OFF}$ delay period to expire. When in shutdown, but not in slave mode, a 2k resistor to PGND discharges the output capacitor. When all three regulators are turned off the LTC3569 enters low power shutdown where all functions are disabled, and quiescent current drops to below 1µA.

A soft-start is enabled when any buck is initially turned on, or following a thermal shutdown. Soft-start ramps the programmed internal reference at a rate of about 0.75V/ms. The output voltage follows the internal reference voltage ramp throughout the soft-start period. While in soft-start, the LTC3569 is forced into pulse-skipping mode until the PGOOD flag indicates that the output voltage is nearing the programmed regulation voltage. Once the PGOOD flag has tripped, if the MODE pin is high the regulator then operates in Burst Mode, otherwise the LTC3569 continues to operate in pulse-skipping mode.

### Thermal Protection

If the die junction temperature exceeds 150°C, a thermal shutdown circuit disables all functions in the LTC3569, and the SW nodes will be pulled low with 2k pull-downs. After the die temperature drops below 125°C the LTC3569 restarts without changing the programmed reference voltage DAC; but a soft-start is initiated upon exiting thermal shutdown.

### PGOOD Pin

The PGOOD pin is an open-drain output that indicates when all of the enabled regulator's output voltages have risen to within 92% of their programmed levels. The three bucks each have separate PGOOD comparators with hysteresis. The PGOOD flag drops if one of the enabled regulator's output voltages drops below 88% of the programmed level. Output voltage transient drops of duration less than 2µs are blanked and not reported at the PGOOD pin. The PGOOD pin open-drain driver is disabled if PGOOD is pulled up to a voltage above $SV_{IN}$.

### Programming the Reference

The full-scale reference voltage for each regulator is 0.8V. The reference can be programmed in –25mV steps by toggling the respective EN pin up to 15 times for a range from 800mV down to 425mV. This is illustrated in Figure 3. The EN pins require a minimum pulse width of 60ns, but no more than 55µs, as the toggle counter times out after the EN pin remains high for around 125µs ($t_{EN}$). After the $t_{EN}$ timeout, the counter state is latched and sent on to the reference voltage DAC, and the counter is reset to full scale. If the EN pin begins to toggle again, the counter decrements on each falling edge. If the EN pin is toggled more than 15 times, the counter remains fixed at the lowest DAC reference level. To reprogram the DAC to full scale, hold the EN pin low for 170µs ($t_{OFF}$), turning off the buck, and then pull EN high once. The buck then initiates a soft-start as $V_{REF}$ ramps up to the full-scale value.

If the DAC is reprogrammed without forcing a shutdown, the soft-start ramp is not engaged and the reference steps to the new value. Avoid using the full-scale 0.8V reference in programmable output voltage applications if the application cannot tolerate the transition through shutdown and soft-start when switching between different reference levels.

## OPERATION

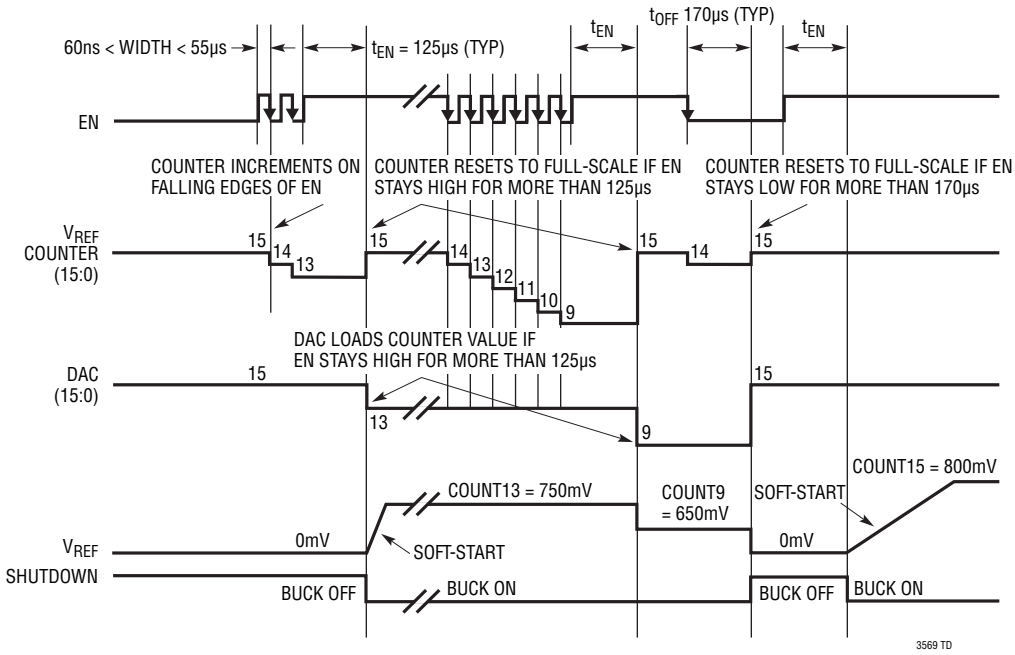



**Figure 3. $V_{REF}$ and ENx Timing Diagram**

## APPLICATIONS INFORMATION

### Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows for smaller inductor and capacitor values. Operation at lower frequencies improves the efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency, $f_{CLK}$, of the LTC3569 is determined by an external resistor that is connected between the $R_T$ pin and ground. The value of the resistor sets the ramp current that charges and discharges an internal timing capacitor within the oscillator. The relationship between oscillator frequency and $R_T$ is calculated by the following equation:

$$R_T = (5.1855 \bullet 10\hat{}11) \bullet (f_{CLK})^{-1.027}$$

Or may be selected following the graph in Figure 4.

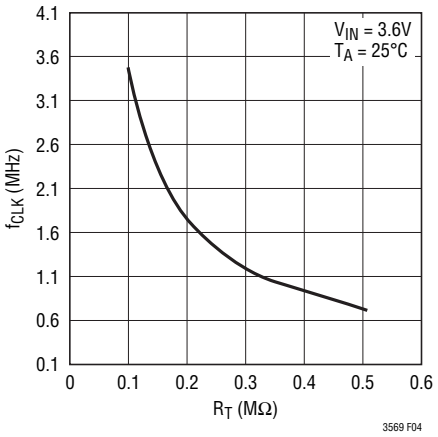



**Figure 4. $f_{CLK}$ vs $R_T$**

The minimum frequency is limited by leakage and noise coupling due to the large resistance of $R_T$.

If the $R_T$ pin is tied to $SV_{IN}$ the oscillation frequency is fixed at 2.25MHz.

Keep excess capacitance and noise (e.g., from the SW pins) away from the $R_T$ pin. It is recommended to remove the GND plane beneath the $R_T$ pin trace, and to route the $R_T$ pin PCB trace away from the SW pins.

### Minimum On-Time And Duty-Cycle

The maximum usable operating frequency is limited by the minimum on-time and the required duty cycle. In buck regulators, the duty cycle (DC) is the ratio of output to input voltage: $DC = V_{OUT}/V_{IN} = t_{ON}/(t_{OFF} + t_{ON})$. At low duty cycles, the SW node is high for a small fraction of the total clock period. As this time period approaches the speed of the gate drive circuits and the comparators internal to the LTC3569, the dynamic loop response suffers. To avoid minimum on-time issues it is recommended to adjust the operating frequency down so as to keep the minimum duty cycle pulse width above 80ns. Thus, the maximum operating frequency should be selected such that the duty cycle does not demand SW pulse widths below the minimum on-time. The maximum clock frequency, $f_{CLKMAX}$, is selected from either the internal fixed frequency clock, or a timing resistor at the $R_T$ pin, or synchronizing clock applied to the MODE pin. The minimum on-time requirement is met by adhering to the following formula:

$$f_{CLKMAX} = (V_{OUT}/V_{IN(MAX)})/t_{MIN-ON}$$

For example, if $V_{OUT}$ is 0.8V and $V_{IN}$ ranges up to 5.5V, the maximum clock frequency is limited to no more than 1.8MHz.

### Mode Selection And Frequency Synchronization

The MODE pin is a multi-purpose pin which provides mode selection and frequency synchronization. Connecting this pin to $SV_{IN}$ enables Burst Mode operation, which provides the best low current efficiency at the cost of a higher output voltage ripple. When this pin is connected to ground, pulse-skipping operation is selected which provides the lowest output voltage and current ripple at the cost of low current efficiency.

Synchronize the LTC3569 to an external clock signal by tying a clock source to the MODE pin. Select the $R_T$ pin resistance so that the internal oscillator frequency is set to 20% lower than the applied external clock frequency to ensure adequate slope compensation, since slope compensation is derived from the internal oscillator. During synchronization, the mode is set to pulse skipping.

The external clock source applied to the MODE pin requires minimum low and high pulse widths of about 100ns.

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### Setting the Output Voltages

The LTC3569 develops independent internal reference voltages for each of the feedback pins. These reference voltages are programmed from 0.8V down to 0.425V in –25mV increments by toggling the appropriate EN pin. The output voltage is set by a resistive divider according to the following formula (refer to Figure 9 for resistor designations):

$V_{OUT1} = V_{REF1}(1 + R1/R2)$,

where $V_{REF1}$ is programmed by toggling the EN1 pin.

$V_{OUT2} = V_{REF2}(1 + R3/R4)$,

where $V_{REF2}$ is programmed by toggling the EN2 pin.

$V_{OUT3} = V_{REF3}(1 + R5/R6)$,

where $V_{REF3}$ is programmed by toggling the EN3 pin.

Keeping the current small (<5µA) in these resistors maximizes efficiency, but making the current too small may allow stray capacitance to cause noise problems and reduce the phase margin of the error amp loop.

To improve the frequency response, use a feedforward capacitor, $C_F$, on the order of 20pF across the leading feedback resistor (R1, R3, and R5). Take care to route each FB line away from noise sources, such as the inductor or the SW line. Remove the ground plane from below the FB PCB routes to limit stray capacitance to GND on these pins.

### Inductor Selection

Although the inductor does not influence the operating frequency, the inductor value has a direct effect on ripple current. The inductor ripple current $\Delta I_L$ decreases with higher inductance and increases with higher $V_{IN}$ or $V_{OUT}$:

$\Delta I_L = V_{OUT}/(f_{CLK} \bullet L) \bullet (1 - V_{OUT}/V_{IN})$

Accepting larger values of $\Delta I_L$ allows the use of low inductances, but results in higher output voltage ripple, greater core losses, and lower output current capability.

A reasonable starting point for setting ripple current is $\Delta I_L = 0.3 \bullet I_{OUT(MAX)}$, where $I_{OUT(MAX)}$ is the maximum load current. The largest ripple current $\Delta I_L$ occurs at the maximum input voltage. To guarantee that the ripple current stays below a specified maximum, choose the inductor value according to the following equation:

$L = V_{OUT}/(f_{CLK} \bullet \Delta I_L) \bullet (1 - V_{OUT}/V_{IN(MAX)})$

The inductor value also has an effect on Burst Mode operation. The transition to low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values increase the burst frequency and reduces efficiency.

Choose an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure that the inductor core does not saturate during normal operation. If an output short-circuit is a possible condition, select an inductor that is rated to handle the maximum peak current specified for the regulators. To maximize efficiency, choose an inductor with a low DC resistance; as power loss in the inductor is due to $I^2R$ losses. Where $I^2$ is the square of the average output current and R is the ESR of the inductor.

**Table 1. Low Profile Inductors**

| VENDOR/ PART NUMBER | VALUE (µH) | IDC (APPROX.) | RDC (Ω) | HEIGHT (mm) |
|---|---|---|---|---|
| Wurth | | | | |
| 7440430022 | 2.2 | 2.50 | 0.023 | 2.80 |
| 744031002 | 2.5 | 1.45 | 0.050 | 1.65 |
| MuRata | | | | |
| LQH55PN1R2 | 1.2 | 2.60 | 0.021 | 1.85 |
| LQH55PN2R2 | 2.2 | 2.10 | 0.031 | 1.85 |
| Toko, DEV518C | | | | |
| 1124BS-1R8N | 1.8 | 2.70 | 0.047 | 1.80 |
| 1124BS-2R4M | 2.4 | 2.30 | 0.054 | 1.80 |
| EPCOS | | | | |
| B824691152M000 | 1.5 | 1.70 | 0.046 | 1.20 |
| B824691221M000 | 2.2 | 1.55 | 0.065 | 1.20 |

## APPLICATIONS INFORMATION

### Input/Output Capacitor Selection

Use low equivalent series resistance (ESR) ceramic capacitors at the switching regulator outputs as well as at the input supply pins. It is recommended to use only X5R or X7R ceramic capacitors because they retain their capacitance over wider voltage and temperature ranges than other ceramic types.

For good transient response and stability the input and output capacitors should retain at least 50% of rated capacitance value over temperature and bias voltage. Check with capacitor data sheets to ensure that bias voltage and temperature derating is taken into account when selecting capacitors.

In continuous mode, the input supply current is a square wave of duty cycle $V_{OUT}/V_{IN}$. The maximum input capacitor ripple current is approximated by:

$$C_{IN} \text{ required } I_{RMS} \approx I_{OUT(MAX)}(V_{OUT}(V_{IN}–V_{OUT}))^{1/2}/V_{IN}$$

This formula's maximum is approximately $I_{RMS} = I_{OUT(MAX)}/2$.

In an output short-circuit situation, the input capacitor ripple current is approximately:

$$C_{IN} \text{ required } I_{RMS} \approx I_{PK}/\sqrt{3}$$

Thus, the ripple current in an output short-circuit is about 2.5 times larger than for nominal operation. Take care in selecting the input capacitor so as not to exceed the capacitor manufacturer's specification for self heating due to the ripple current.

Two factors influence the selection of the output capacitor. The first is load voltage droop, $V_{DROOP}$, the second is the output capacitor ESR effect on ripple voltage.

Load voltage droops on a load current step, $\Delta I_{OUT}$, where the output capacitor supports the output voltage for typically 2 to 3 clock cycles until the inductor current charges up to the load step current level. A good estimate of output capacitor value required to maintain a droop of less than $V_{DROOP}$ is given by:

$$C_{OUT} \approx 2.5 \bullet \Delta I_{OUT}/(f_{CLK} \bullet V_{DROOP})$$

The second factor that influences the selection of the output capacitor is the effect of output capacitor ESR on the output voltage ripple as a result of the inductor ripple current. The amplitude of voltage ripple, $\Delta V_{OUT}$, is determined by:

$$\Delta V_{OUT} \approx \Delta I_L(ESR + 1/(8 \bullet f_{CLK} \bullet C_{OUT}))$$

Where $\Delta I_L$ is the ripple current in the inductor, and ESR is the equivalent series resistance of the output capacitor. Using ceramic capacitors, this voltage ripple is usually negligible.

**Table 2. Capacitors**

| VENDOR/PART NUMBER | VALUE (µF) |
|---|---|
| Murata: GRM21BR71A106KE51 | 10 |
| Murata: 06036D475KAT | 4.7 |
| TDK: C1608X5R0J106M<br>C1608X7R1C105K | 10<br>1 |

### Printed Circuit Board Layout Considerations

There are three main considerations to take into account while designing a PCB layout for the LTC3569. The first consideration is regarding switching noise coupling onto the FB pin traces and the $R_T$ pin trace, or causing radiated electromagnetic induction (EMI). The noise is mitigated by placing the inductors and input decoupling capacitors as close as possible to the LTC3569. Furthermore, careful placement of a contiguous ground plane directly under the high frequency switching node traces of the LTC3569 mitigates EMI; since high frequency eddy currents follow the ground plane in loops. The larger the area of the current return loops the larger EMI that is radiated. Placing input decoupling capacitors close to the corresponding $PV_{IN}$/PGND pins directly reduces the area (and therefore the inductance) of ground returns. Also, place a group of vias directly under the grounded backside of the package leading to an internal ground plane. Place the ground plane on the second layer of the PCB to minimize parasitic inductance.

## APPLICATIONS INFORMATION

The second consideration is stray capacitance on the FB pin traces and the $R_T$ pin trace to GND. This is taken into account by cutting the ground plane beneath these traces. However, wherever the ground plane is cut, add additional decoupling capacitors across the break to provide a path for high-frequency ground return currents to flow.

Finally, the third consideration is stray impedance between the SW node and the inductor when operating with a slave power stage. It is important to keep the stray inductance of the slave power device to a minimum, by keeping the trace from slave SW to the main SW as short as possible. This requirement is necessary to ensure that the slave power device's share of the inductor current does not exceed that of the master as well as to keep the current density in the slave device under control. The inductor should be placed close to the master SW pin to minimize stray impedance and allow the master to control the inductor current.

### Thermal Considerations

In the majority of applications, the LTC3569 does not dissipate much heat due to its high efficiency. However, in applications where the LTC3569 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, the LTC3569 will be turned off and 2k resistive pull-downs are tied to all the SW nodes.

To prevent the LTC3569 from exceeding maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. Temperature rise is:

$$t_{RISE} = P_D \bullet \theta_{JA}$$

Where $P_D$ is the power dissipated by the regulator and $\theta_{JA}$ is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, $T_J$, is given by:

$$T_J = t_{RISE} + T_A.$$

Where $T_A$ is the ambient temperature.

As an example, consider the case when the LTC3569 is in dropout at an input voltage of 2.7V with load currents of 1000mA, 500mA and 500mA for bucks 1, 2 and 3 respectively, at an ambient temperature of 85°C. From the Typical Performance Characteristics, the $R_{DS(ON)}$ of buck1 is 0.190Ω, and for buck2 and buck3 it is 0.265Ω. Therefore, power dissipated by the LTC3569 is:

$$P_D = I_1^2 R_{DS(ON)1} + I_2^2 R_{DS(ON)2} + I_3^2 R_{DS(ON)3}$$
$$= 190mV + 66.25mW + 66.25mV$$
$$= 322.5mW$$

At 85°C ambient the junction temperature is:

$$T_J = 322.5mW \bullet 68°C/W + 85°C = 106.9°C.$$

This junction temperature is below the absolute maximum junction temperature of 125°C.

### Design Example 1: 2.5V, 1.8V and 1.2V From a Li-Ion Battery

As a design example, consider using the LTC3569 in a portable application with a Li-Ion battery source. The battery provides an $SV_{IN}$ from 2.9V to 4.2V. The loads require 2.5V, 1.8V and 1.2V with current requirements of up to 800mA, 400mA and 400mA respectively when active. The first load, with the 2.5V rail has no standby requirements, however loads 2 and 3 each require a current of 1mA in standby. Since two of the loads require low current operation, Burst Mode operation is selected. With $V_{IN(MAX)}$ at 4.2V and $V_{OUT(MIN)}$ = 1.2V, the maximum clock frequency is 3.57MHz based on minimum on-time requirements. To simplify the board layout, the fixed 2.25MHz internal frequency is selected.

## APPLICATIONS INFORMATION

### Selecting The Inductors

Calculating the inductor values for 30% ripple current at maximum $SV_{IN}$:

L1 = 2.5V/(2.25MHz•240mA)•(1–2.5V/4.2V)= 1.9µH

L2 = 1.8V/(2.25MHz•120mA)•(1–1.8V/4.2V)= 3.8µH

L3 = 1.2V/(2.25MHz•120mA)•(1–1.2V/4.2V)= 3.1µH

Choosing a vendor's closest values gives L1 = 2.2µH, L2 = L3 = 3.3µH. These values result in the maximum ripple currents of:

$\Delta I_{L1}$ = 2.5V/(2.25MHz•2.2µH)•(1–2.5V/4.2V) = 204mA

$\Delta I_{L2}$ = 1.8V/(2.25MHz•3.3µH)•(1–1.8V/4.2V) = 139mA

$\Delta I_{L3}$ = 1.2V/(2.25MHz•3.3µH)•(1–1.2V/4.2V) = 115mA

### Selecting The Output Capacitors

The value of the output capacitors are calculated based on a 5% load droop for maximum load current step. The output droop is usually about 2.5 times the linear drop of the first cycle and is estimated based on the following formula:

$C_{OUT} = 2.5 \bullet I_{OUT(MAX)}/(f_{CLK} \bullet V_{DROOP})$

The output capacitor values are calculated as:

$C_{OUT1}$ = 2.5•800mA/(2.25MHz•125mV) = 7.1µF

$C_{OUT2}$ = 2.5•400mA/(2.25MHz•90mV) = 4.9µF

$C_{OUT3}$ = 2.5•400mA/(2.25MHz•60mV) = 7.4µF

Choosing the closest standard values gives, $C_{OUT1}$ = 10µF, $C_{OUT2}$ = 4.7µF and $C_{OUT3}$ = 10µF.

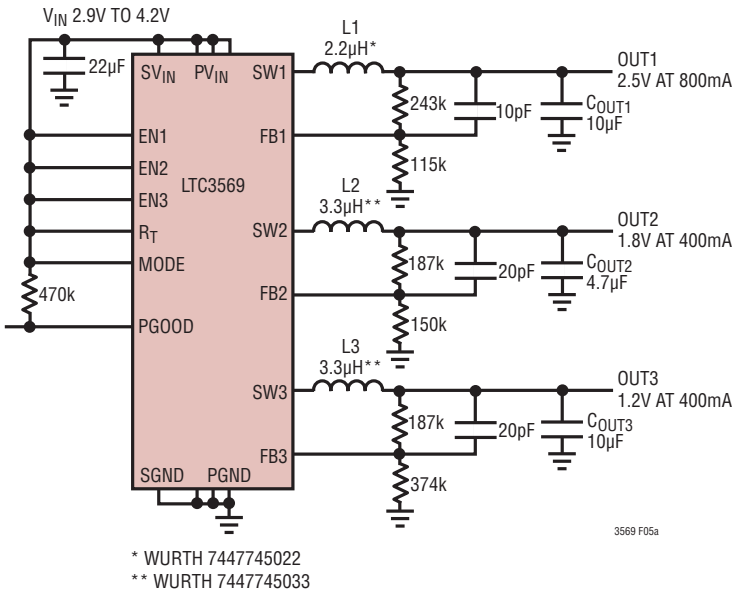
A 22µF input capacitor is selected since the Li-Ion battery has sufficiently low output impedance.

### Setting The Output Voltages

Without toggling the EN pins the LTC3569 develops a 0.8V reference voltage for each of the feedback pins. The output voltages are set by a resistive divider as follows:

$V_{OUT} = 0.8 \bullet (1 + R1/R2)$

The resistors in Figure 5 are selected as the nearest 1% standard resistor values. To improve frequency response feedforward capacitors of 10pF and 20pF are used.




**Design Example 1: Burst Mode Operation**

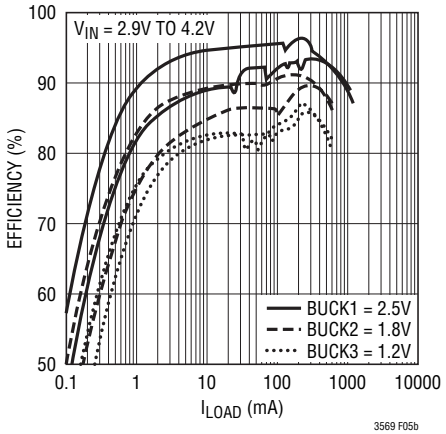



**Figure 5. Triple Buck DC/DC Regulators: 800mA, 400mA, 400mA**

## APPLICATIONS INFORMATION

### Design Example 2: Dual Bucks, 1.8V at 1.8A and 1.5V at 600mA

For this example, the LTC3569 is configured to deliver two fixed voltages of 1.8V and 1.5V from a generic supply over the full operating range, 2.5V to 5.5V. The load requirements range from <1mA in standby mode up to 1.8A for the 1.8V supply and 600mA for the 1.5V supply.

The fixed internal clock frequency of 2.25MHz meets the minimum on-time requirements. Burst Mode operation is selected for high efficiency at the low standby current level. Calculating the inductor values for 30% ripple current at max $SV_{IN}$:

$L1 = 1.8V/(2.25MHz \bullet 540mA) \bullet (1–1.8V/5.5V) = 1.0\mu H$

$L2 = 1.5V/(2.25MHz \bullet 180mA) \bullet (1–1.5V/5.5V) = 2.2\mu H$

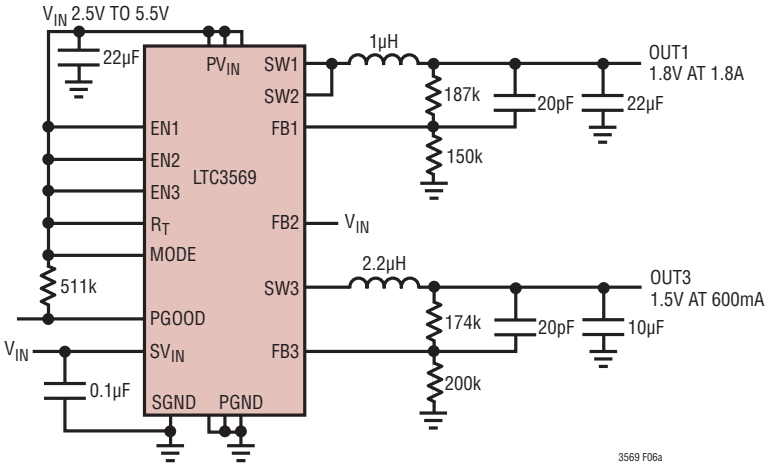
Calculating the value of the output capacitors:

$C_{OUT1} = 2.5 \bullet 1800mA/(2.25MHz \bullet 90mV) = 22\mu F$

$C_{OUT2} = 2.5 \bullet 600mA/(2.25MHz \bullet 75mV) = 8.9\mu F$

An input capacitor of 22µF is selected to support the maximum ripple current of 1.2A. An additional 0.1µF low ESR capacitor is placed between $SV_{IN}$ and SGND.

The resistor values shown in Figure 6 are selected as the closest standard 1% resistors to obtain the correct output voltages with the full-scale reference voltages of 0.8V. And 20pF feedforward capacitors are placed across the leading feedback resistors.




**Design Example 2: 1.8A Load Step on Buck1 with Buck2 Slave, Burst Mode Operation**

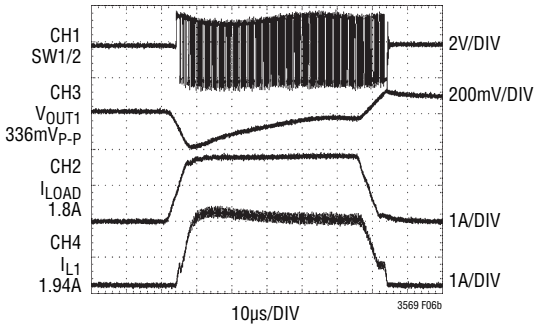



**Figure 6. Dual Buck DC/DC Regulators: 1.8V at 1800mA, and 1.5V at 600mA**

## APPLICATIONS INFORMATION

### Design Example 3: Dual Programmable Bucks

In this example consider two buck regulators operating from a 2.5V to 5.5V unregulated supply that are required to generate two independently programmable supplies that must step from 1.2V in standby up to 1.8V when active, with a maximum load current of 1.2A when active and 1mA in standby. Additionally, this application anticipates possible output short circuits, and is required to operate without damage in such a situation.

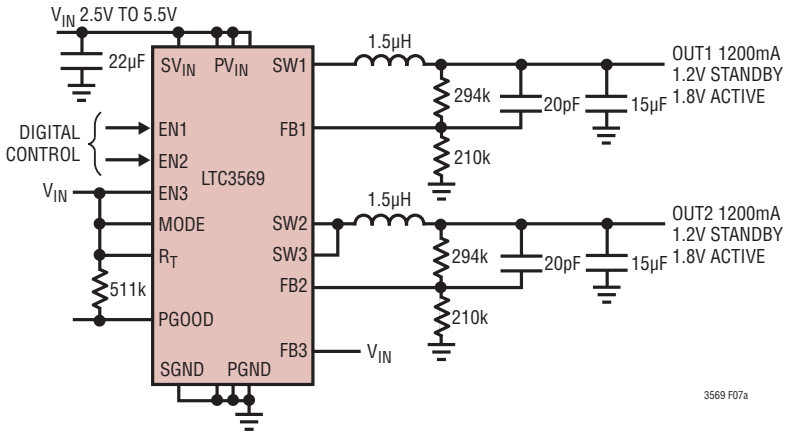
Buck 1 is selected for the first regulator, and buck 3 is configured as a slave power stage in parallel with buck 2 by pulling FB3 up to $V_{IN}$ to obtain the required current level for the second regulator. Burst Mode operation is selected to achieve high efficiency during standby operation. The internal 2.25MHz clock frequency is selected, as it satisfies the minimum on-time requirement. Next, two reference voltages are selected to match the ratio of the active to standby voltages: 1.8V/1.2V = 1.5. The 0.75V and 0.5V reference levels mach this ratio. The resistors shown in Figure 7 are selected to obtain the correct feedback ratio from standard 1% resistors. Calculating the inductor values for 30% ripple current at maximum $SV_{IN}$:

$$L = 1.8V/(2.25MHz \bullet 360mA) \bullet (1–1.8V/5.5V) = 1.5\mu H.$$

The output capacitor values are selected as the nearest standard value to obtain 5% voltage droop at maximum load current step.

$$C_{OUT} = 2.5 \bullet 1200mA/(2.25MHz \bullet 90mV) \approx 15\mu F.$$

Select an output capacitor with an ESR of less than 50mΩ to obtain an output voltage ripple of less than 30mV. Finally select an input capacitor rated for the worst-case short-circuit ripple current of $2\ I_{PK}/\sqrt{3} \approx 2.5A$, when both outputs are shorted to GND.




**Design Example 3: Soft-Start to Standby (1.2V)**

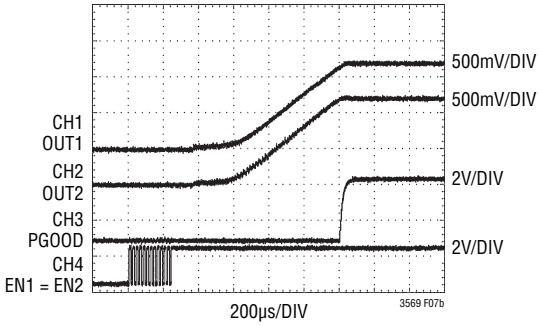



**Figure 7. Dual Programmable Buck DC/DC Regulators: 1200mA, 1200mA**

## APPLICATIONS INFORMATION

### Design Example 4: Dual Programmable Bucks

In this example consider two buck regulators operating from a 2.5V to 5.5V unregulated supply that are required to generate two independently programmable supplies that must step from 1.2V in standby up to 1.6V when active, with a maximum load current of 0.8A when active and 1mA in standby. Furthermore, when switching between active and standby, the load voltage should not droop.

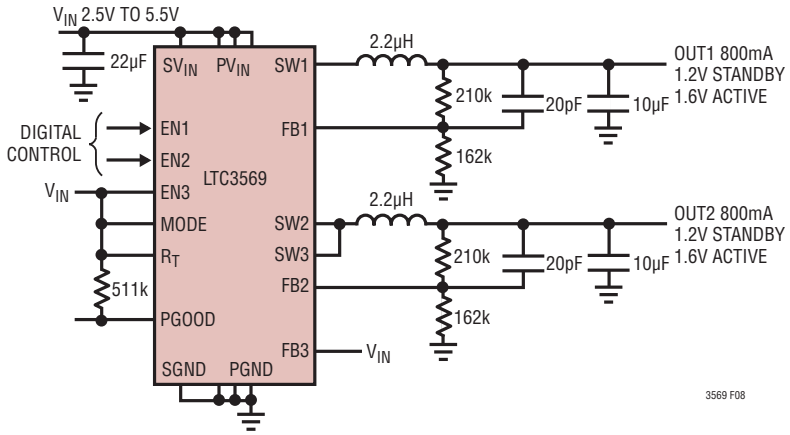
Buck 1 is selected for the first regulator, and buck 3 is configured as a slave power stage in parallel with buck 2 by pulling FB3 up to $V_{IN}$ to obtain the required current level for the second regulator. Burst Mode operation is selected to achieve high efficiency during standby operation. The internal 2.25MHz clock frequency is selected, as it satisfies the minimum on-time requirement. Next, two reference voltages are selected to match the ratio of the active to standby voltages: 1.6V/1.2V = 1.3333. There are three reference value ratios that match this ratio: 0.8V and 0.6V, 0.7V and 0.525V, and 0.6V and 0.45V. As the load cannot tolerate a voltage droop when switching from standby to active, the 0.7V and 0.525V references are selected to match the ratio of output voltages. With this ratio, the buck does not need to be shutdown as it would if the full-scale 0.8V reference level was chosen. The resistors shown in Figure 8 are selected to obtain the nearest feedback ratio from standard 1% resistors. Calculating the inductor values for 30% ripple current at maximum $SV_{IN}$:

$$L = 1.6V/(2.25MHz \bullet 240mA) \bullet (1–1.6V/5.5V) \approx 2.2\mu H.$$

The output capacitor values are selected as the nearest standard value to obtain 5% voltage droop at maximum load current step.

$$C_{OUT} = 2.5 \bullet 800mA/(2.25MHz \bullet 90mV) \approx 10\mu F.$$

Select an output capacitor with an ESR of less than 50mΩ to obtain an output voltage ripple of less than 30mV. Finally select an input capacitor rated for the worst-case short-circuit ripple current of $2\ I_{PK}/\sqrt{3} \approx 2.5A$, when both outputs are shorted to GND.



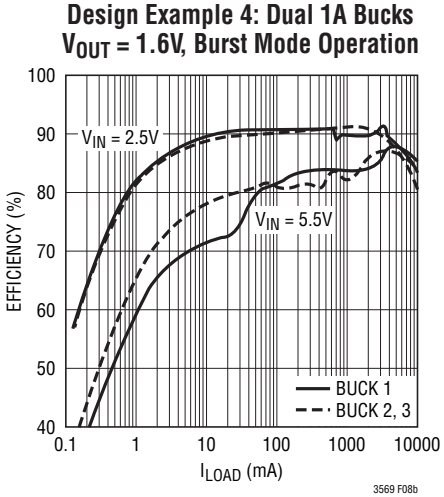
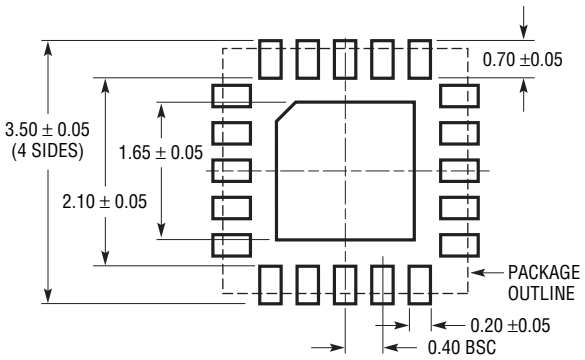




**Figure 8. Dual Programmable Buck DC/DC Regulators**

# PACKAGE DESCRIPTION

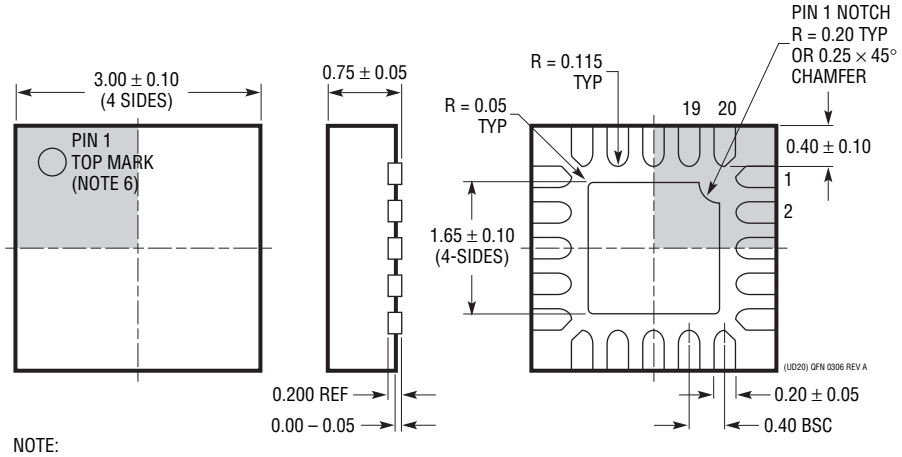
**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**UD Package**
**20-Lead Plastic QFN (3mm × 3mm)**
(Reference LTC DWG # 05-08-1720 Rev A)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

BOTTOM VIEW—EXPOSED PAD

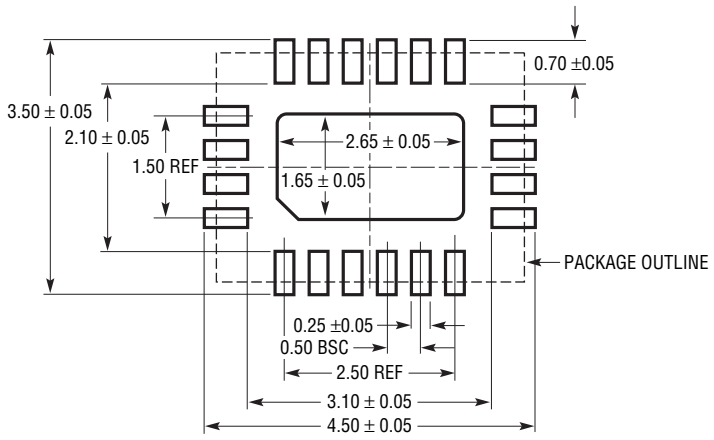



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

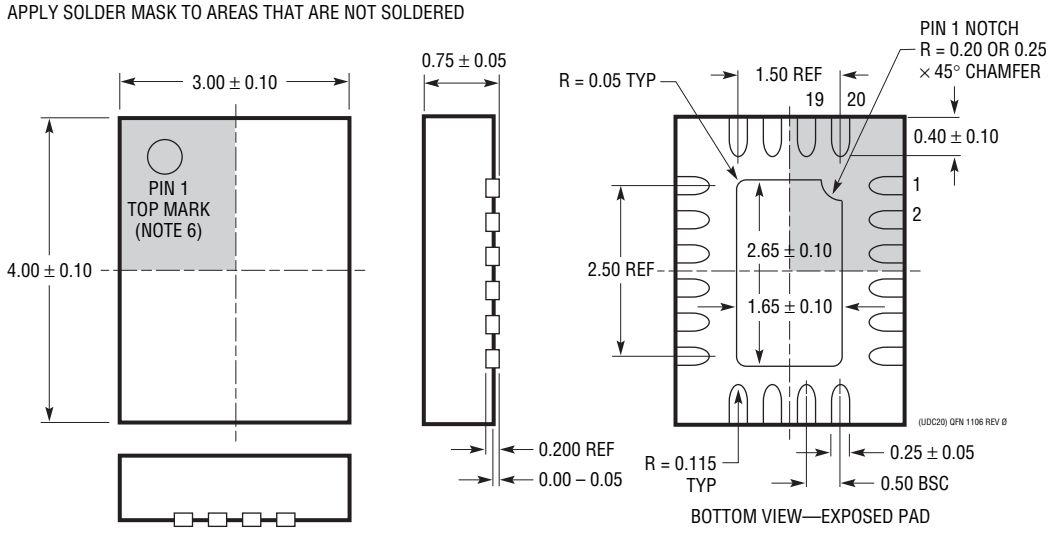
# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**UDC Package**
**20-Lead Plastic QFN (3mm × 4mm)**
(Reference LTC DWG # 05-08-1742 Rev Ø)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



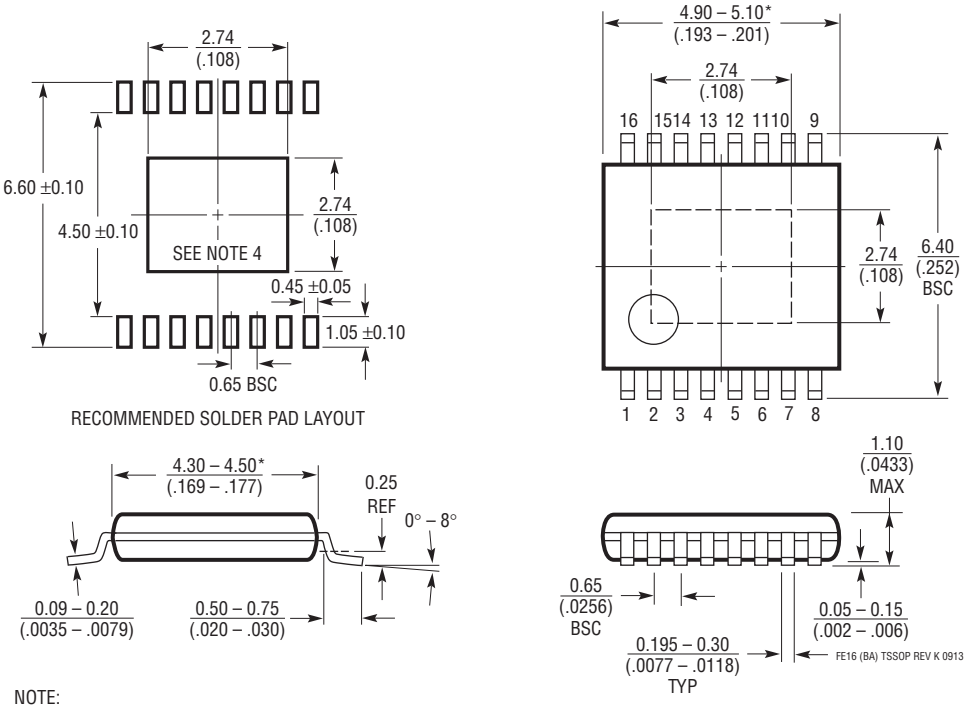

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**FE Package**
**16-Lead Plastic TSSOP (4.4mm)**
(Reference LTC DWG # 05-08-1663 Rev K)
**Exposed Pad Variation BA**




NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

## REVISION HISTORY (Revision history begins at Rev D)

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| D | 01/11 | Added UDC package. Reflected throughout the data sheet | 1 to 26 |
| E | 04/14 | Added spec for PGOOD Current to Absolute Maximum Ratings | 2 |
| | | Clarified Pin Configuration for FE package | 2 |
| | | Clarified Pin Description for $PV_{IN3}$ for FE package | 8 |



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## TYPICAL APPLICATION

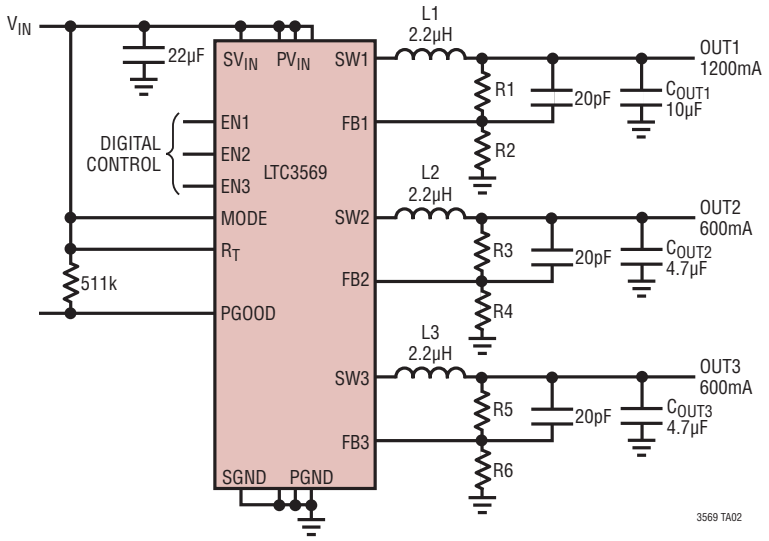



**Figure 9. Triple Programmable Buck DC/DC Regulators**

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC3406A/ LTC3406AB | 600mA, 1.5MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 20µA, $I_{SD}$ <1µA, ThinSOT™ Package |
| LTC3407A/ LTC3407A-2 | Dual 600mA/600mA 1.5MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 40µA, $I_{SD}$ <1µA, MS10E, 3mm × 3mm DFN-10 Package |
| LTC3411A | 1.25A, 4MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 60µA, $I_{SD}$ <1µA, MS10, 3mm × 3mm DFN-10 Package |
| LTC3412A | 2.5A, 4MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 60µA, $I_{SD}$ <1µA, 4mm × 4mm QFN-16, TSSOP-16E Package |
| LTC3417A-2 | Dual 1.5A/1A, 4MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.3V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 125µA, $I_{SD}$ <1µA, TSSOP-16E, 3mm × 5mm DFN-16 Package |
| LTC3419/LTC3419-1 | Dual 600mA/600mA 2.25MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 35µA, $I_{SD}$ <1µA, MS10, 3mm × 3mm DFN-10 Package |
| LTC3544/LTC3544B | Quad 100mA/200mA/200mA/300mA, 2.25MHz Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.3V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 70µA, $I_{SD}$ <1µA, 3mm × 3mm QFN-16 Package |
| LTC3545/LTC3545-1 | Triple, 800mA × 3, 2.25MHz Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.3V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 58µA, $I_{SD}$ <1µA, 3mm × 3mm QFN-16 Package |
| LTC3547/LTC3547B | Dual 300mA, 2.25MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 40µA, $I_{SD}$ <1µA, DFN-8 Package |
| LTC3548/LTC3548-1/ LTC3548-2 | Dual 400mA and 800mA $I_{OUT}$, 2.25MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 40µA, $I_{SD}$ <1µA, MS10E, 3mm × 3mm DFN-10 Package |
| LTC3561 | 1.25A, 4MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 240µA, $I_{SD}$ <1µA, 3mm × 3mm DFN-8 Package |
| LTC3562 | Quad, $I^2C$ Interface, 600mA/600mA/400mA/400mA, 2.25MHz Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.9V to 5.5V, $V_{OUT(MIN)}$ = 0.425V, $I_Q$ = 100µA, $I_{SD}$ <1µA, 3mm × 3mm QFN-20 Package |


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