OPA1637 High-Performance, High-Voltage, Low-Noise Burr-Brown™ Audio Fully-Differential Amplifier

Texas Instruments
Burr-Brown Audio

ADVANCE INFORMATION

1 Features

- Low input voltage noise: 3.7 nV/√Hz at 1 kHz
- Low THD + N: –120 dB at 10 kHz
- Low supply current: 950 µA at ±18 V
- Input offset voltage: ±200 µV (maximum)
- Input bias current: 2 nA (maximum)
- Gain-bandwidth product: 9.2 MHz
- Differential output slew rate: 15 V/µs
- Wide input and output common-mode range
- Wide single-supply operating range: 3 V to 36 V
- Low supply current power-down feature: < 20 µA
- Amplifier overload power limit
- Current limit
- Package: 8-pin VSSOP
- Temperature range: –40°C to +125°C

2 Applications

- Professional audio mixer or control surface
- Professional microphones and wireless systems
- Professional speaker systems
- Soundbar
- Turntable

3 Description

The OPA1637 is a low-noise, low total harmonic distortion (THD), Burr-Brown™ fully differential amplifier that easily filters and drives fully differential, audio signal chains. The OPA1637 is also used to convert single-ended sources to differential outputs required by high-fidelity analog-to-digital converters (ADCs). Designed for exceptional low noise and THD, the bipolar super-beta inputs yield a very low noise figure at very-low quiescent current and input bias current. This device is designed for audio circuits where low power consumption is required along with excellent signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR).

The OPA1637 features high-voltage supply capability, allowing for supply voltages up to ±18 V. This capability allows high-voltage differential signal chains to benefit from the improved headroom and dynamic range without adding separate amplifiers for each polarity of the differential signal. Very-low voltage and current noise enables the OPA1637 for use in high-gain configurations with minimal impact to the audio signal noise.

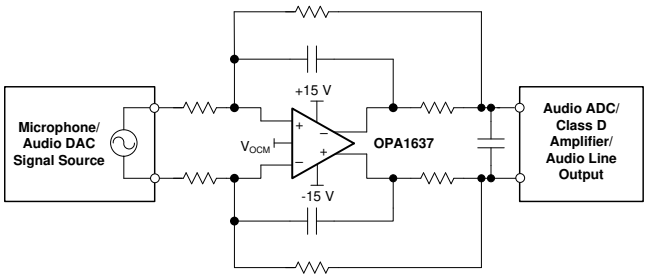
The OPA1637 is characterized for operation over the wide temperature range of –40°C to +125°C, and is available in an 8-pin VSSOP package.

Device Information[1]

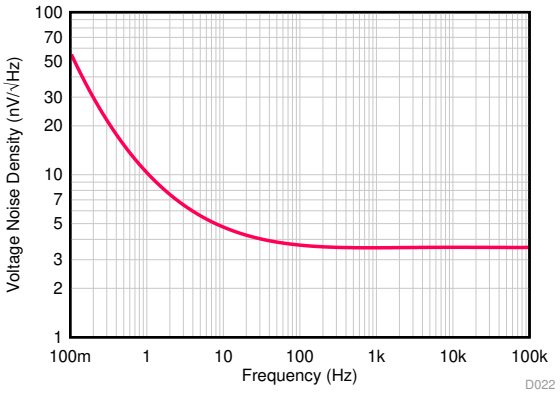
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA1637	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Low-Noise, Low-Power, Fully-Differential Amplifier Gain Block and Interface



Low Input Voltage Noise



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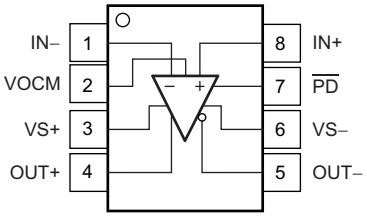
4 Revision History

DATE	REVISION	NOTES
December 2019	*	Initial release

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5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN–	1	I	Inverting (negative) amplifier input
IN+	8	I	Noninverting (positive) amplifier input
OUT–	5	O	Inverting (negative) amplifier output
OUT+	4	O	Noninverting (positive) amplifier output
$\overline{PD}$	7	I	Power down. $\overline{PD}$ = logic low = power off mode. $\overline{PD}$ = logic high = normal operation. The logic threshold is referenced to VS+. If power down is not needed, leave $\overline{PD}$ floating.
VOCM	2	I	Ouput common-mode voltage control input
VS–	6	I	Negative power-supply input
VS+	3	I	Positive power-supply input

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply		40	V
		Dual supply		±20	V
	IN+, IN–, Differential voltage(2)			±0.5	V
	IN+, IN–, VOCM, $\overline{PD}$, OUT+, OUT− voltage(3)		V_{VS-} – 0.5	V_{VS+} + 0.5	V
	IN+, IN− current		–10	10	mA
	OUT+, OUT− current		–50	50	mA
	Output short-circuit(4)			Continuous	
T_A	Operating Temperature		–40	150	°C
T_J	Junction Temperature		–40	175	°C
T_{stg}	Storage Temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins IN+ and IN– are connected with anti-parallel diodes in between the two terminals. Differential input signals that are greater than 0.5 V or less than –0.5 V must be current-limited to 10 mA or less.
(3) Input terminals are diode-clamped to the supply rails (VS+, VS–). Input signals that swing more than 0.5 V greater or less the supply rails must be current-limited to 10 mA or less.
(4) Short-circuit to V_S / 2.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply	3		36	V
		Dual-supply	±1.5		±18	
T_A	Specified temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA1637 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	181.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	101.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

at T_A = 25°C, V_S (dual supply) = ±1.5 V to ±18 V, V_{VOCM} = 0 V, input common mode voltage (V_{ICM}) = 0 V, R_F = 2 kΩ, $V_{\overline{PD}}$ = V_{VS+}, R_L = 10 kΩ(1) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_O(2) = 100 mV_{PP}, G = –1 V/V		7		MHz
GBP	Gain-bandwidth product	V_O = 100 mV_{PP}, G = –10 V/V		9.2		MHz
FBP	Full-power bandwidth	V_O = –1 V_{PP}, G = –1 V/V		2.5		MHz
SR	Slew rate	G = –1, 10-V step		15		V/µs
	Settling time	0.1% of final value, G = –1 V/V, V_O = 10-V step		1		µs
		0.01% of final value, G = –1 V/V, V_O= 10-V step		2		
THD+N	Total harmonic distortion and noise	Differential input, f = 10 kHz, V_O = 10 V_{PP}		–120		dB
		Single-ended input, f = 10 kHz, V_O = 10 V_{PP}		–115		
HD2	Second-order harmonic distortion	Differential input, f = 10 kHz, V_O = 10 V_{PP}		–120		dB
		Single-ended input, f = 10 kHz, V_O = 10 V_{PP}		–120		
HD3	Third-order harmonic distortion	Differential input, f = 10 kHz, V_O = 10 V_{PP}		–120		dB
		Single-ended input, f = 10 kHz, V_O = 10 V_{PP}		–120		
e_n	Input differential voltage noise	f = 1 kHz		3.7		nV/√Hz
		f = 10 Hz		4		
		f = 0.1 Hz to 10 Hz		0.1		μV_{PP}
e_i	Input current noise, each input	f = 1 kHz		300		fA/√Hz
		f = 10 Hz		400		
		f = 0.1 Hz to 10 Hz		13.4		pA_{PP}
	Overdrive recovery time	G = 5 V/V, 2x output overdrive, dc-coupled		3.3		µs
Z_O	Open-loop output impedance	f = 100 kHz (differential)		14		Ω
C_{LOAD}	Capacitive load drive	Differential capacitive load, no output Isolation resistors, phase margin = 30°		50		pF
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_S = ±2.5 V, $V_{VS–}$ + 0.2 V < V_O < V_{VS+} – 0.2 V	115	120		dB
		V_S = ±2.5 V, $V_{VS–}$ + 0.3 V < V_O < V_{VS+} – 0.3 V, T_A = –40°C to +125°C	115	120		
		V_S = ±18 V, $V_{VS–}$ + 0.4 V < V_O < V_{VS+} – 0.4 V	115	120		
		V_S = ±18 V, $V_{VS–}$ + 0.6 V < V_O < V_{VS+} – 0.6 V, T_A = –40°C to +125°C	110	120		
V_{IO}	Input-referred offset voltage			10	±200	µV
		T_A = –40°C to +125°C			±250	
	Input offset voltage drift	T_A = –40°C to +125°C		0.1	±1	µV/°C
I_B	Input bias current			±0.2	±2	nA
		T_A = –40°C to +125°C			±4	
	Input bias current drift	T_A = –40°C to +125°C		±2	±15	pA/°C
I_{OS}	Input offset current			±0.2	±1	nA
		T_A = –40°C to +125°C			±3	
	Input offset current drift	T_A = –40°C to +125°C		±1	±10	pA/°C
PSRR	Power-supply rejection ratio			0.025	0.5	µV/V
		T_A = –40°C to +125°C			1	

(1) R_L is connected differentially, from OUT+ to OUT–.
(2) V_O refers to the differential output voltage, V_{OUT+} – $V_{OUT–}$.

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Electrical Characteristics (continued)

at T_A = 25°C, V_S (dual supply) = ±1.5 V to ±18 V, V_{VOCM} = 0 V, input common mode voltage (V_{ICM}) = 0 V, R_F = 2 kΩ, $V_{\overline{PD}}$ = V_{VS+}, R_L = 10 kΩ(1) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
	Common-mode voltage	T_A = –40°C to +125°C	$V_{VS–}$ + 1		V_{VS+} – 1	V
CMRR	Common-mode rejection ratio	$V_{VS–}$ + 1 V ≤ V_{ICM} ≤ V_{VS+} – 1 V	126	140		dB
		$V_{VS–}$ + 1 V ≤ V_{ICM} ≤ V_{VS+} – 1 V, T_A = –40°C to +125°C	120			
	Input impedance differential mode	V_{ICM} = 0 V		1 || 1		GΩ || pF
OUTPUT						
	Output voltage difference from supply voltage	V_S = ±2.5 V		±100		mV
		V_S = ±2.5 V, T_A = –40°C to +125°C		±100		
		V_S = ±18 V		±230		
		V_S = ±18 V, T_A = –40°C to +125°C		±270		
I_{SC}	Short-circuit current			±31		mA
OUTPUT COMMON-MODE VOLTAGE (V_{OCM}) CONTROL						
	Input voltage		$V_{VS–}$ + 1		V_{VS+} – 1	
	Small-signal bandwidth from VOCM pin	V_{VOCM}= 100 mV_{PP}		2		MHz
	Large-signal bandwidth from VOCM pin	V_{VOCM} = 0.6 V_{PP}		5.7		
	Slew rate from VOCM pin	V_{VOCM} = 0.5-V step, rising		3.5		V/µs
		V_{VOCM} = 0.5-V step, falling		5.5		
	DC output balance	V_{VOCM} fixed midsupply (V_O = ±1 V)		78		dB
	Output balance SSBW	V_{VOCM} fixed midsupply, V_O / V_{VOCM} (–3 dB from dc)		TBD		kHz
	Output balance LSBW	V_{VOCM} fixed midsupply, V_O / V_{VOCM} with V_O = 5 V_{PP} (–3 dB from dc)		TBD		kHz
	VOCM input impedance			2.5 || 1		MΩ || pF
	VOCM offset from mid-supply	VOCM pin floating		±1		mV
	VOCM common-mode offset voltage	V_{VOCM} = V_{ICM}, V_O = 0 V		±1	±6	mV
		V_{VOCM} = V_{ICM}, V_O = 0 V, T_A = –40°C to +125°C			±10	
	VOCM common-mode offset voltage drift	V_{VOCM} = V_{ICM}, V_O = 0 V, T_A = –40°C to +125°C		±20	±60	µV/°C
POWER SUPPLY						
I_Q	Quiescent operating current			0.95	1.2	mA
		T_A = –40°C to +125°C			1.5	
POWER DOWN						
$V_{\overline{PD}(HI)}$	Power-down enable voltage	T_A = –40°C to +125°C	V_{VS+} – 0.5			V
$V_{\overline{PD}(LOW)}$	Power-down disable voltage	T_A = –40°C to +125°C			V_{VS+} – 2.0	V
	$\overline{PD}$ bias current	$V_{\overline{PD}}$ = V_{VS+} – 2 V		1	2	µA
	Powerdown quiescent current			10	20	µA
	Turn-on time delay	Time to V_O = 90% of final value		10		µs
	Turn-off time delay	Time to V_O = 10% of original value		15		µs

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6.6 Typical Characteristics

at T_A = 25°C, V_{VOCM} = 0 V, R_F = 2 kΩ, R_L = 10 kΩ, V_{OUT} = 2 V_{PP} G = 1 V/V, and $\overline{VPD}$ = VS+ (unless otherwise noted)

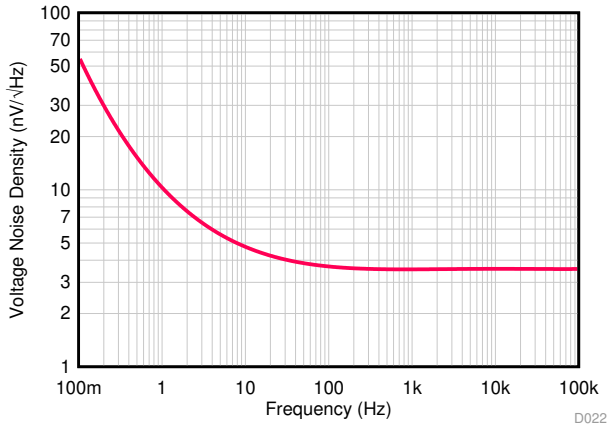


Figure 1. Input-Referred Voltage Noise vs Frequency

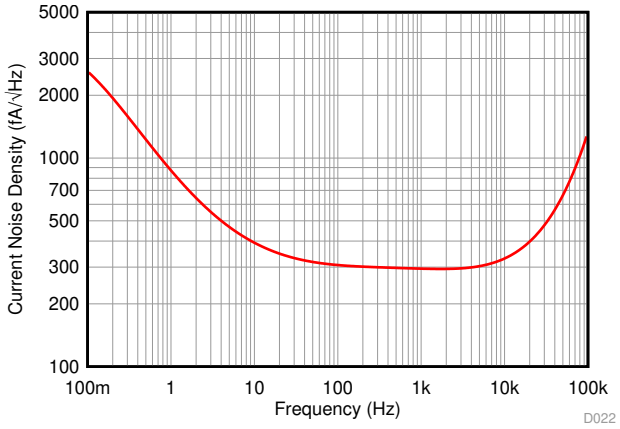


Figure 2. Current Noise vs Frequency

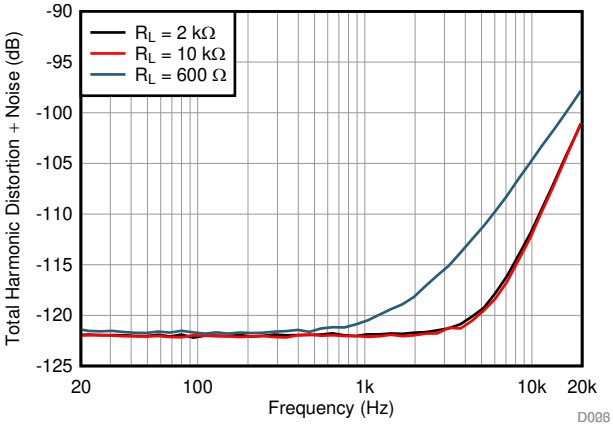


Figure 3. Total Harmonic Distortion + Noise vs Frequency

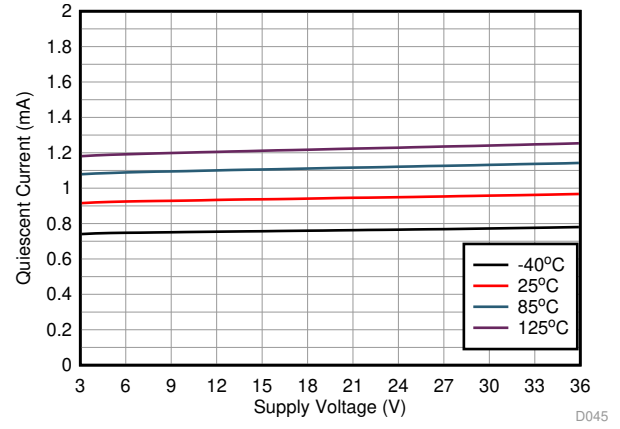


Figure 4. Quiescent Current vs Supply Voltage

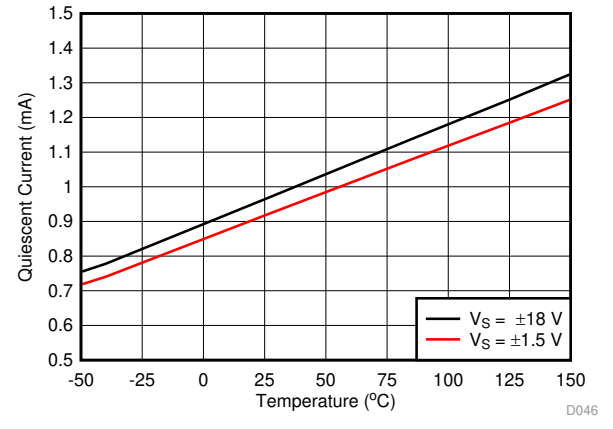


Figure 5. Quiescent Current vs Temperature

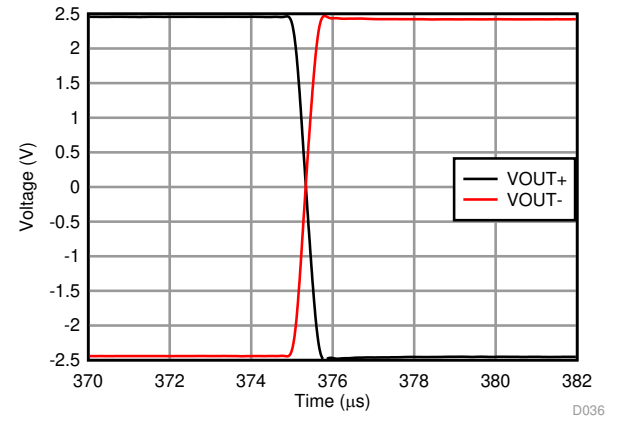


Figure 6. Large-Signal Step Response

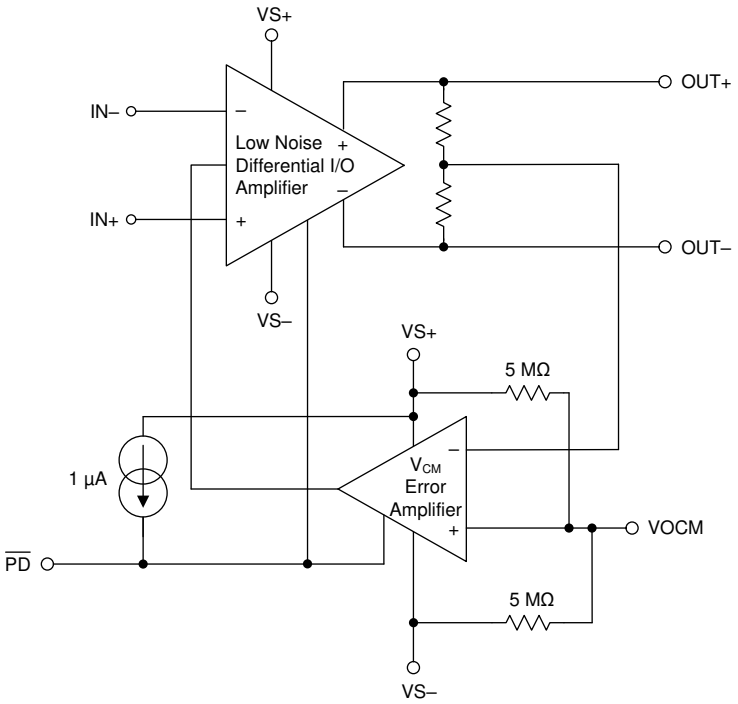
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7 Detailed Description

7.1 Overview

The OPA1637 is a low-noise, low-distortion fully-differential amplifier (FDA) that features Texas Instrument's super-beta bipolar input devices. Super-beta input devices feature very low input bias current as compared to standard bipolar technology. The low input bias current and current noise makes the OPA1637 an excellent choice for audio applications that require low-noise differential signal processing without significant current consumption. This device is also designed for analog-to-digital audio input circuits that require low noise in a single fully-differential amplifier because of lower current consumption at lower noise levels than what is achievable with two low-noise amplifiers. The OPA1637 also features high-voltage capability, which allows the device to be used in ±15-V supply circuits without any additional voltage clamping or regulators. This feature enables a direct, single solution for a 24-dBm differential output drive (commonly found on mixers and digital audio interfaces), without any additional amplification.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Super-Beta Input Bipolar Transistors

The OPA1637 is designed on a modern bipolar process that features TI's super-beta input transistors. Traditional bipolar transistors feature excellent voltage noise and offset drift, but suffer a tradeoff in high input bias current (I_B) and input bias current noise. Super-beta transistors offer the benefits of low voltage noise and offset drift with an order of magnitude reduction in input bias current and reduction in input bias current noise. For audio circuits, input bias current noise can dominate in circuits where higher resistance input resistors are used. The OPA1637 enables a fully-differential, low-noise amplifier design without restrictions of low input resistance at a power level unmatched by traditional single-ended amplifiers.

7.3.2 Power Down

The OPA1637 features a power-down circuit to disable the amplifier when a low-power mode is required by the system. In the power-down state, the amplifier outputs are high-impedance, and the amplifier total quiescent current is reduced to less than 20 µA.

7.3.3 Flexible Gain Setting

The OPA1637 offers considerable flexibility in the configuration and selection of resistor values. Low input bias current and bias current noise allows for larger gain resistor values with minimal impact to noise or offset. The design starts with the selection of the feedback resistor value. The 2-kΩ feedback resistor value used for the characterization curves is a good compromise between power, noise, and phase margin considerations. With the feedback resistor values selected (and set equal on each side), the input resistors are set to obtain the desired gain, with input impedance also set with these input resistors. Differential I/O designs provide an input impedance that is the sum of the two input resistors. Single-ended input to differential output designs present a more complicated input impedance. Most characteristic curves implement the single-ended to differential design as the more challenging requirement over differential-to-differential I/O.

7.3.4 Amplifier Overload Power Limit

In many bipolar-based amplifiers, the output stage of the amplifier can draw significant (several milliamperes) of quiescent current if the output voltage becomes clipped (meaning the output voltage becomes limited by the negative or positive supply voltage). This condition can cause the system to enter a high-power consumption state, and potentially cause oscillations between the power supply and signal chain. The OPA1637 has an advanced output stage design that eliminates this problem. When the output voltage reaches the V_{VS+} or $V_{VS–}$ voltage, there is virtually no additional current consumption from the nominal quiescent current. This feature helps eliminate any potential system problems when the signal chain is disrupted by a large external transient voltage.

7.4 Device Functional Modes

The OPA1637 requires external resistors for correct signal-path operation. When setting the gain with these external resistors, the amplifier can be either on with the $\overline{PD}$ pin left floating, asserted to a voltage greater than V_{VS+} – 0.5 V, or turned off by forcing $\overline{PD}$ to a voltage lower than V_{VS+} – 2 V. Disabling the amplifier shuts off the quiescent current and stops correct amplifier operation. The signal path is still present for the source signal through the external resistors, which provides poor signal isolation from the input to output in power-down mode.

Internal protection diodes remain present across the input pins in both operating and shutdown mode. Large input signals during disable can turn on the input differential protection diodes, thus producing a load current in the supply, even in shutdown.

The VOCM control pin sets the output average voltage. Left open, VOCM defaults to an internal midsupply value. Driving this high-impedance input with a voltage reference within the valid range sets a target for the internal V_{CM} error amplifier. If floated to obtain a default midsupply reference for VOCM, an external decoupling capacitor must be added on the VOCM pin to reduce the otherwise high output noise for the internal high-impedance bias.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Most applications for the OPA1637 strive to deliver the best dynamic range in a design that delivers the desired signal processing along with adequate phase margin for the amplifier itself. The following sections detail some of the design issues with analysis and guidelines for improved performance.

8.1.1 Driving Capacitive Loads

The capacitive load of an ADC or some other next-stage device is commonly required to be driven. Directly connecting a capacitive load to the output pins of a closed-loop amplifier such as the OPA1637 can lead to an unstable response. One typical remedy to this instability is to add two small series resistors (R_O) at the outputs of the OPA1637 before the capacitive load. Good practice is to leave a place for the R_O elements in a board layout (a 0-Ω value initially) for later adjustment, in case the response appears unacceptable.

8.1.2 Operating the Power-Down Feature

The power-down feature on the OPA1637 allows the device to be put into a low power-consumption state, in which quiescent current is minimized. To force the device into the low-power state, drive the $\overline{PD}$ pin to less than 2 V less than the positive supply voltage (V_{VS+} – 2 V). Driving the $\overline{PD}$ pin to less than 2 V forces the internal logic to disable both the differential and common-mode amplifiers. The $\overline{PD}$ pin has an internal pullup current that allows for the pin to be used in an open-drain MOSFET configuration without an additional pullup resistor, as seen in Figure 7. In this configuration, the logic level can be referenced to the MOSFET, and the voltage at the $\overline{PD}$ pin is level-shifted to account for use with high supply voltages. Be sure to select an N-type MOSFET with a maximum B_{VDSS} greater than the total supply voltage.

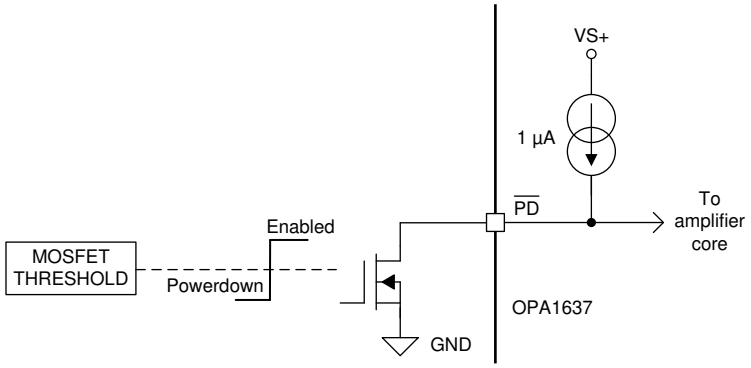


Figure 7. Power-Down ($\overline{PD}$) Pin Interface With Low-Voltage Logic Level Signals

For applications that do not use the power-down feature, tie the $\overline{PD}$ pin to the positive supply voltage.

When $\overline{PD}$ is low (device is in power down) the output pins will be in a high-impedance state.

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Application Information (continued)

8.1.3 Noise Performance

The first step in the output noise analysis is to reduce the application circuit to the simplest form with equal feedback and gain setting elements to ground. Figure 8 shows the simplest analysis circuit with the FDA and resistor noise terms to be considered.

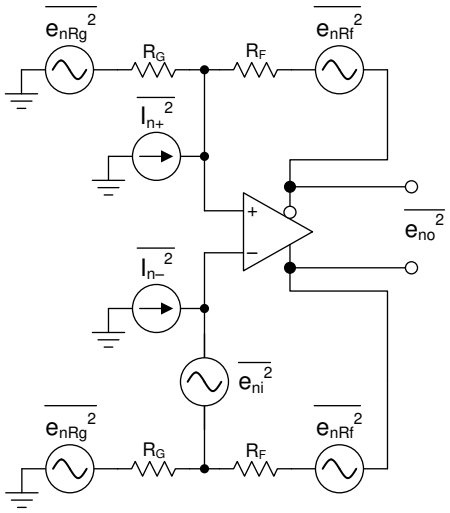


Figure 8. FDA Noise Analysis Circuit

The noise powers are shown in Figure 8 for each term. When the R_F and R_G (or R_I) terms are matched on each side, the total differential output noise is the root sum squared (RSS) of these separate terms. Using NG ≡ 1 + R_F / R_G, the total output noise is given by Equation 1. Each resistor noise term is a 4kT × R power (4kT = 1.6E-20J at 290K).

$$e_o = \sqrt{(e_{ni}NG)^2 + 2(i_N R_F)^2 + 2(4kTR_F NG)} \quad (1)$$

The first term is simply the differential input spot noise times the noise gain, the second term is the input current noise terms times the feedback resistor (and because there are two uncorrelated current noise terms, the power is two times one of them), and the last term is the output noise resulting from both the R_F and R_G resistors, at again twice the value for the output noise power of each side added together. Running a wide sweep of gains when holding R_F to 2 kΩ gives the standard values and resulting noise listed in Table 1.

When the gain increases, the input-referred noise approaches only the gain of the FDA input voltage noise term at 3.7 nV/√Hz.

Table 1. Swept Gain of the Output- and Input-Referred Spot Noise Calculations

GAIN (V/V)	R_F	R_{G1}	A_V	E_O (nV/√Hz)	E_I (nV/√Hz)
0.1	2000	20000	0.1	9.4	93.9
1	2000	2000	1	13.6	13.6
2	2000	1000	2	17.8	8.9
5	2000	402	4.98	29.5	5.9
10	2000	200	10	48.6	4.9

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8.2 Typical Applications

8.2.1 An MFB Filter Driving an ADC Application

A common application use case for fully-differential amplifiers is to easily convert a single-ended signal into a differential signal to drive a differential input source, such as an ADC or class D amplifier. Figure 9 shows an example of OPA1637 used to convert a single-ended low voltage signal audio source, such as a small electret microphone, and deliver a low-noise differential signal that is common-mode shifted to the center of the ADC input range. A multiple-feedback (MFB) configuration is used to provide a Butterworth filter response, giving a 40 dB/decade rolloff with a –3-dB frequency of 30 kHz.

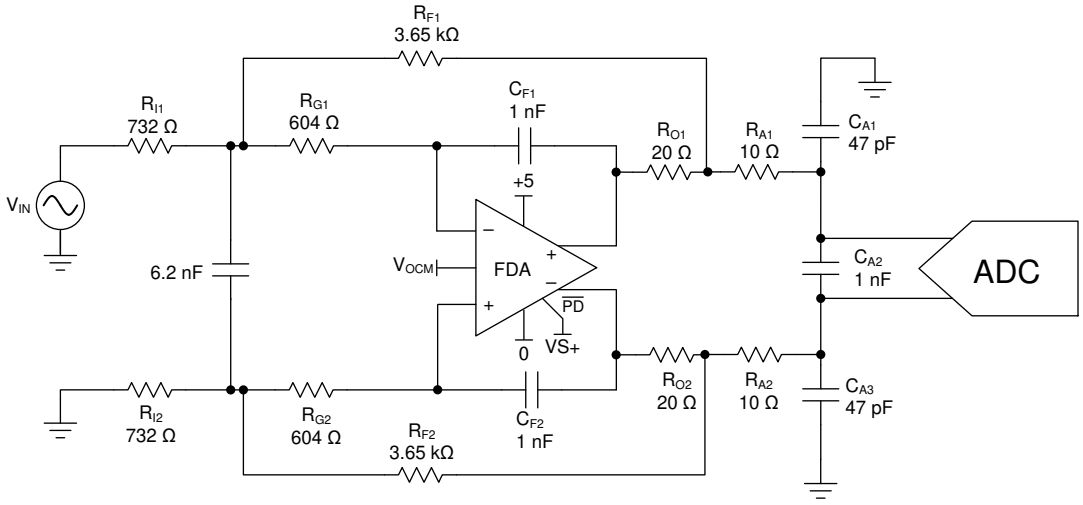


Figure 9. Example 100-kHz Butterworth Filter

8.2.1.1 Design Requirements

The requirements for this application are:

- Single-ended to differential conversion
- 5-V/V gain
- Active filter set to a Butterworth, 30-kHz response shape
- Output RC elements set by SAR input requirements (not part of the filter design)
- Filter element resistors and capacitors are set to limit added noise over the OPA1637 and noise peaking

8.2.1.2 Detailed Design Procedure

The design proceeds using the techniques and tools suggested in the *Design Methodology for MFB Filters in ADC Interface Applications* application note. The process includes:

- Scale the resistor values to not meaningfully contribute to the output noise produced by the OPA1637.
- Select the RC ratios to hit the filter targets when reducing the noise gain peaking within the filter design.
- Set the output resistor to 10 Ω into a 1-nF differential capacitor.
- Add 47-pF common-mode capacitors to the load capacitor to improve common noise filtering.
- Inside the loop, add 20-Ω output resistors after the filter feedback capacitor to increase the isolation to the load capacitor.

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Typical Applications (continued)

8.2.1.3 Application Curve

The gain and phase plots are shown in Figure 10. The MFB filter features a Butterworth responses feature very flat passband gain, with a 2-pole roll-off at 30 kHz to eliminate any higher-frequency noise from contaminating the signal chain and potentially alias back into the audio band.

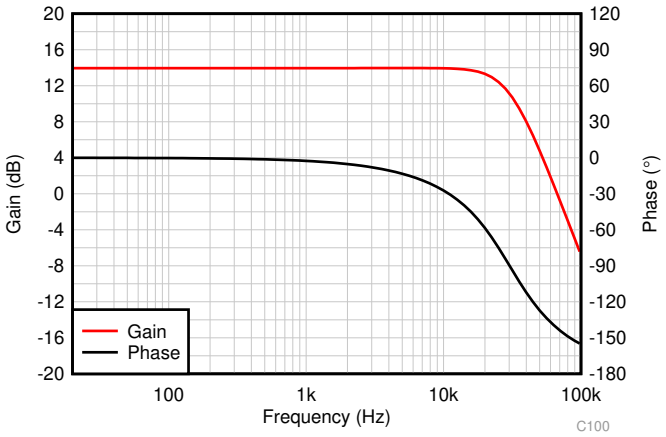


Figure 10. Gain and Phase Plot for a 30-kHz Butterworth Filter

ADVANCE INFORMATION

Typical Applications (continued)

8.2.2 Differential Microphone Input to Line Level

Professional dynamic microphone typically feature low output impedance to minimize noise coupling on the microphone cable. Interfacing the microphone with high-impedance circuitry typically requires the use of an impedance conversion stage, which can be done with a transformer or discrete amplifiers. The flexibility of OPA1637 allows the device to be configured with a low differential input impedance and 20 dB of gain, simplifying the impedance conversion and gain stage into a single device. Figure 11 shows an example of a differential, low input impedance, microphone level voltage (10 mV to 100 mV) amplifier to a line-level amplitude signal that also has adjustable dc common-mode shift capability, making the OPA1637 a great choice for driving an ADC Class D amplifier.

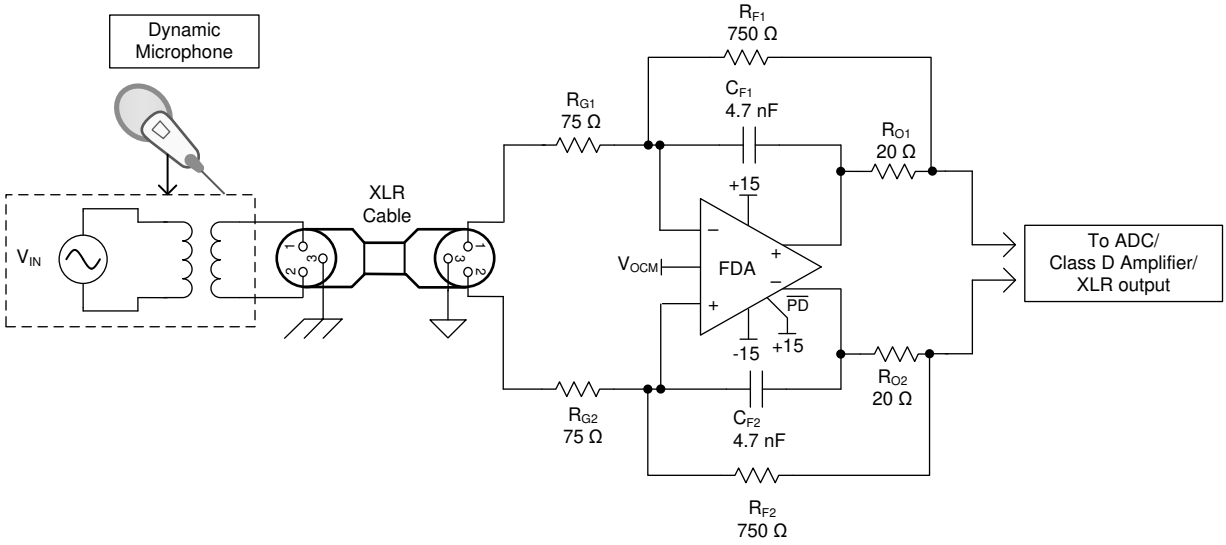
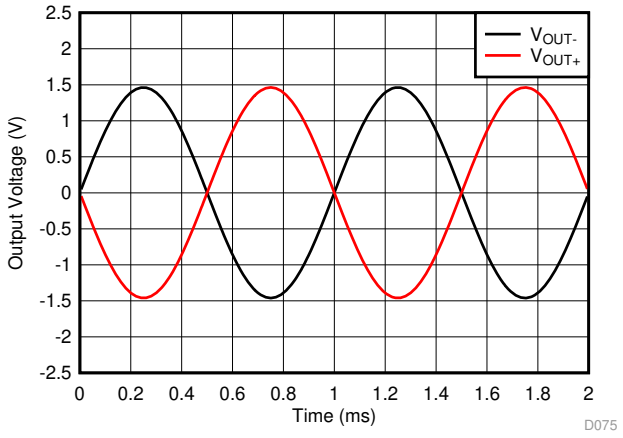


Figure 11. Fully Differential, Low-Noise, 20-dB Microphone Gain Block With DC Shift

8.2.2.1 Application Curve



V_{OCM} = 0 V

Figure 12. Output Waveform of the Microphone Amplifier

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9 Power Supply Recommendations

The OPA1637 operates from supply voltages of 3.0 V to 36 V (±1.5 V to ±18 V, dual supply). Connect ceramic bypass capacitors from both VS+ and VS– to GND.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations

- Keep differential signals routed together to minimize parasitic impedance mismatch.
- Connect a 0.1-µF capacitor to the supply nodes through a via.
- Connect a 0.1-µF capacitor to the VOCM pin if no external voltage is used.
- Keep any high-frequency nodes that can couple through parasitic paths away from the VOCM node.
- Clean the PCB board after assembly to minimize any leakage paths from excess flux into the VOCM node.

10.2 Layout Example

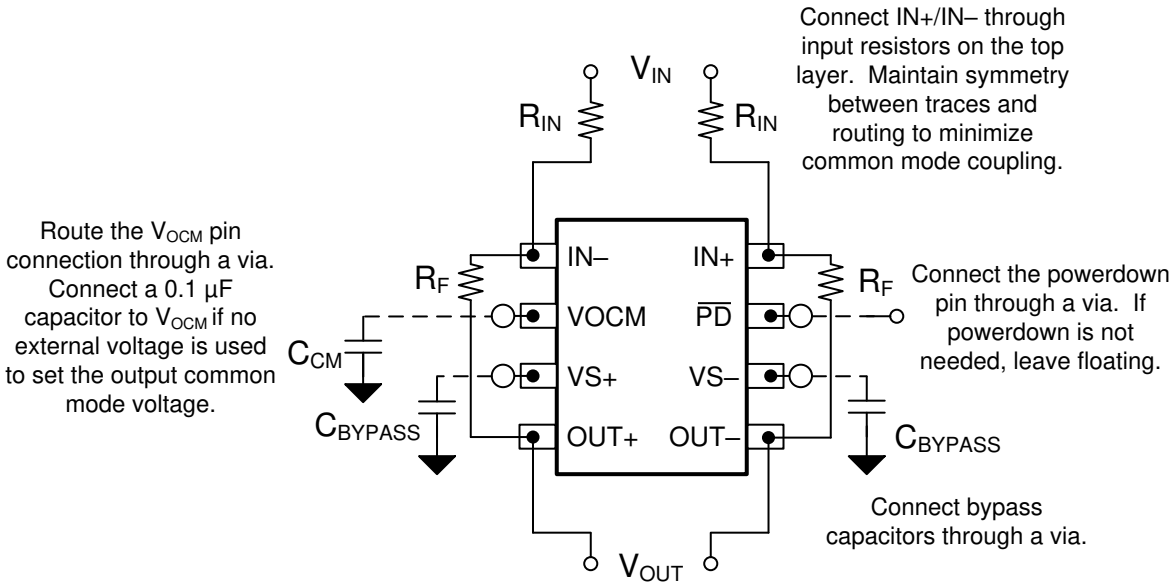


Figure 13. Example Layout

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

- OPA1637 TINA-TI™ model
- *TINA-TI Gain of 0.2 100kHz Butterworth MFB Filter*
- *TINA-TI 100kHz MFB filter LG test*
- *TINA-TI Differential Transimpedance LG Sim*

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *INA188 Precision, Zero-Drift, Rail-to-Rail Out, High-Voltage Instrumentation Amplifier* data sheet
- Texas Instruments, *OPAx192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim™* data sheet
- Texas Instruments, *OPA161x SoundPlus™ High-Performance, Bipolar-Input Audio Operational Amplifiers* data sheet
- Texas Instruments, *Design Methodology for MFB Filters in ADC Interface Applications* application report
- Texas Instruments, *Design for Wideband Differential Transimpedance DAC Output* application report

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XOPA1637DGKR	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

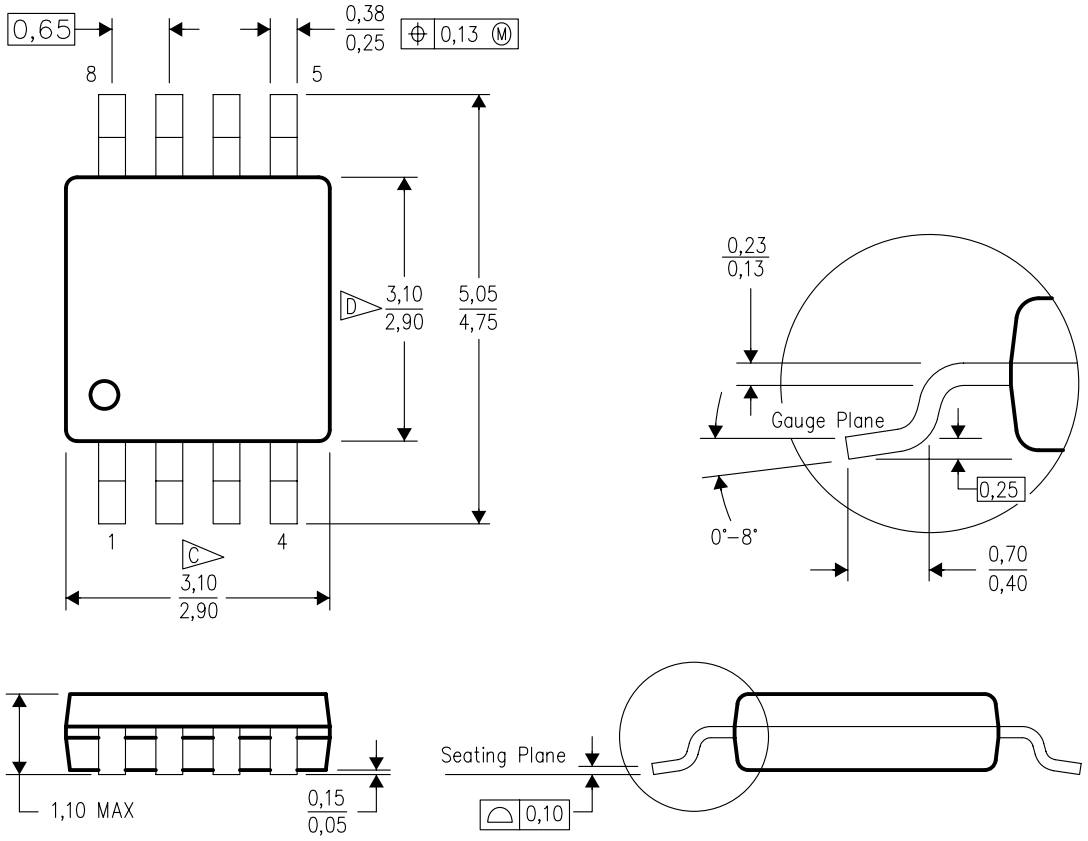
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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