

NUD3105

Integrated Relay, Inductive Load Driver

This device is used to switch inductive loads such as relays, solenoids incandescent lamps, and small DC motors without the need of a free-wheeling diode. The device integrates all necessary items such as the MOSFET switch, ESD protection, and Zener clamps. It accepts logic level inputs thus allowing it to be driven by a large variety of devices including logic gates, inverters, and microcontrollers.

Features

- Provides a Robust Driver Interface Between DC Relay Coil and Sensitive Logic Circuits
- Optimized to Switch Relays from 3.0 V to 5.0 V Rail
- Capable of Driving Relay Coils Rated up to 2.5 W at 5.0 V
- Internal Zener Eliminates the Need of Free-Wheeling Diode
- Internal Zener Clamp Routes Induced Current to Ground for Quieter Systems Operation
- Low $V_{DS(on)}$ Reduces System Current Drain
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices

Typical Applications

- Telecom: Line Cards, Modems, Answering Machines, FAX
- Computers and Office: Photocopiers, Printers, Desktop Computers
- Consumer: TVs and VCRs, Stereo Receivers, CD Players, Cassette Recorders
- Industrial: Small Appliances, Security Systems, Automated Test Equipment, Garage Door Openers
- Automotive: 5.0 V Driven Relays, Motor Controls, Power Latches, Lamp Drivers

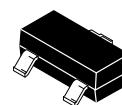


ON Semiconductor®

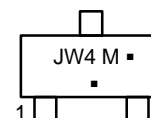
<http://onsemi.com>

RELAY/INDUCTIVE LOAD DRIVER 0.5 AMPERE, 8.0 VOLT CLAMP

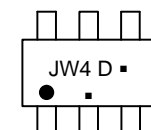
MARKING DIAGRAMS



SOT-23
(TO-236)
CASE 318



SC-74
CASE 318F
STYLE 7



JW4 = Device Code
M = Date Code*
D = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)
*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NUD3105LT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
NUD3105DMT1G	SOT-74 (Pb-Free)	3000 / Tape & Reel
SZNUD3105DMT1G	SOT-74 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NUD3105

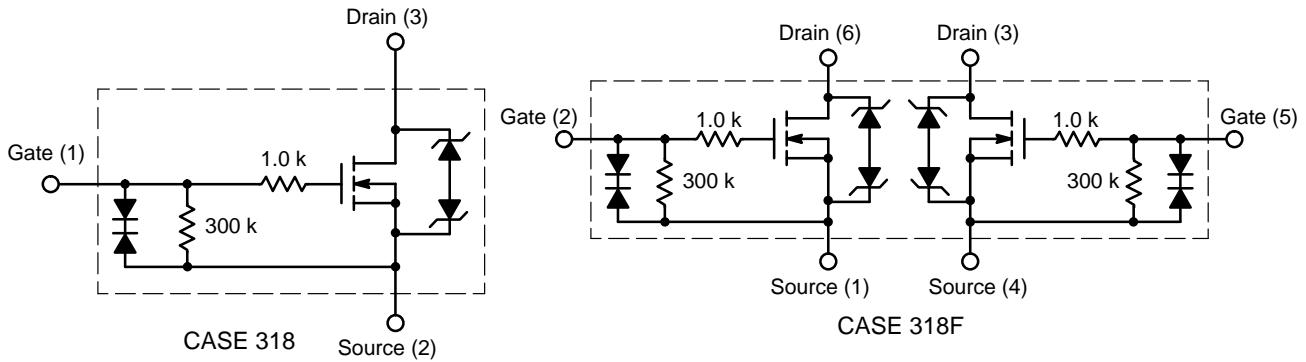


Figure 1. Internal Circuit Diagrams

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Rating	Value	Unit
V_{DS}	Drain to Source Voltage – Continuous	6.0	V_{dc}
V_{GS}	Gate to Source Voltage – Continuous	6.0	V_{dc}
I_D	Drain Current – Continuous	500	mA
E_z	Single Pulse Drain-to-Source Avalanche Energy ($T_{Jinitial} = 25^\circ\text{C}$) (Note 2)	50	mJ
E_{zpk}	Repetitive Pulse Zener Energy Limit ($DC \leq 0.01\%$) ($f = 100\text{ Hz}$, $DC = 0.5$)	4.5	mJ
T_J	Junction Temperature	150	$^\circ\text{C}$
T_A	Operating Ambient Temperature	-40 to 85	$^\circ\text{C}$
T_{stg}	Storage Temperature Range	-65 to +150	$^\circ\text{C}$
P_D	Total Power Dissipation (Note 1) Derating Above 25°C	SOT-23 225 1.8	mW mW/ $^\circ\text{C}$
	Total Power Dissipation (Note 1) Derating Above 25°C	SC-74 380 1.5	mW mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	SOT-23 556	$^\circ\text{C}/\text{W}$
		SC-74 329	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- This device contains ESD protection and exceeds the following tests:
Human Body Model 2000 V per MIL_STD-883, Method 3015.
Machine Model Method 200 V.
- Refer to the section covering Avalanche and Energy.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
V_{BRDSS}	Drain to Source Sustaining Voltage (Internally Clamped), ($I_D = 10\text{ mA}$)	6.0	8.0	9.0	V
B_{VGS0}	$I_g = 1.0\text{ mA}$	-	-	8.0	V
I_{DSS}	Drain to Source Leakage Current ($V_{DS} = 5.5\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 25^\circ\text{C}$) ($V_{DS} = 5.5\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 85^\circ\text{C}$)	-	-	15	μA
		-	-	15	
I_{GSS}	Gate Body Leakage Current (318) ($V_{GS} = 3.0\text{ V}$, $V_{DS} = 0\text{ V}$) ($V_{GS} = 5.0\text{ V}$, $V_{DS} = 0\text{ V}$)	5.0	-	19	μA
		-	-	50	
I_{GSS}	Gate Body Leakage Current (318F) ($V_{GS} = 3.0\text{ V}$, $V_{DS} = 0\text{ V}$) ($V_{GS} = 5.0\text{ V}$, $V_{DS} = 0\text{ V}$)	5.0	-	35	μA
		-	-	65	

NUD3105

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
ON CHARACTERISTICS					
V _{GS(th)}	Gate Threshold Voltage (V _{GS} = V _{DS} , I _D = 1.0 mA) (V _{GS} = V _{DS} , I _D = 1.0 mA, T _J = 85°C)	0.8 0.8	1.2 –	1.4 1.4	V
R _{DS(on)}	Drain to Source On-Resistance (I _D = 250 mA, V _{GS} = 3.0 V) (I _D = 500 mA, V _{GS} = 3.0 V) (I _D = 500 mA, V _{GS} = 5.0 V) (I _D = 500 mA, V _{GS} = 3.0 V, T _J = 85°C) (I _D = 500 mA, V _{GS} = 5.0 V, T _J = 85°C)	– – – – –	– – – – –	1.2 1.3 0.9 1.3 0.9	Ω
I _{DS(on)}	Output Continuous Current (V _{DS} = 0.25 V, V _{GS} = 3.0 V) (V _{DS} = 0.25 V, V _{GS} = 3.0 V, T _J = 85°C)	300 200	400 –	– –	mA
g _{FS}	Forward Transconductance (V _{OUT} = 5.0 V, I _{OUT} = 0.25 A)	350	570	–	mmhos

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance (V _{DS} = 5.0 V, V _{GS} = 0 V, f = 10 kHz)	–	25	–	pF
C _{oss}	Output Capacitance (V _{DS} = 5.0 V, V _{GS} = 0 V, f = 10 kHz)	–	37	–	pF
C _{rss}	Transfer Capacitance (V _{DS} = 5.0 V, V _{GS} = 0 V, f = 10 kHz)	–	8.0	–	pF

SWITCHING CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units
t _{PHL} t _{PLH}	Propagation Delay Times: High to Low Propagation Delay; Figure 1 (5.0 V) Low to High Propagation Delay; Figure 1 (5.0 V)	– –	25 80	– –	nS
t _{PHL} t _{PLH}	High to Low Propagation Delay; Figure 1 (3.0 V) Low to High Propagation Delay; Figure 1 (3.0 V)	– –	44 44	– –	
t _f t _r	Transition Times: Fall Time; Figure 1 (5.0 V) Rise Time; Figure 1 (5.0 V)	– –	23 32	– –	nS
t _f t _r	Fall Time; Figure 1 (3.0 V) Rise Time; Figure 1 (3.0 V)	– –	53 30	– –	

NUD3105

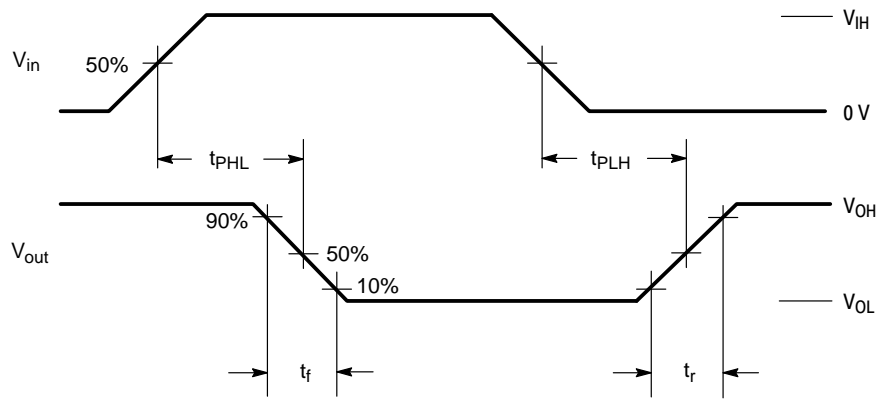


Figure 1. Switching Waveforms

TYPICAL CHARACTERISTICS

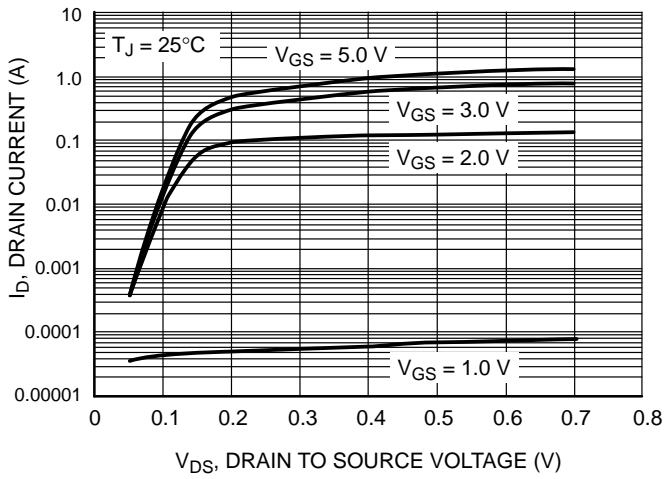


Figure 2. Output Characteristics

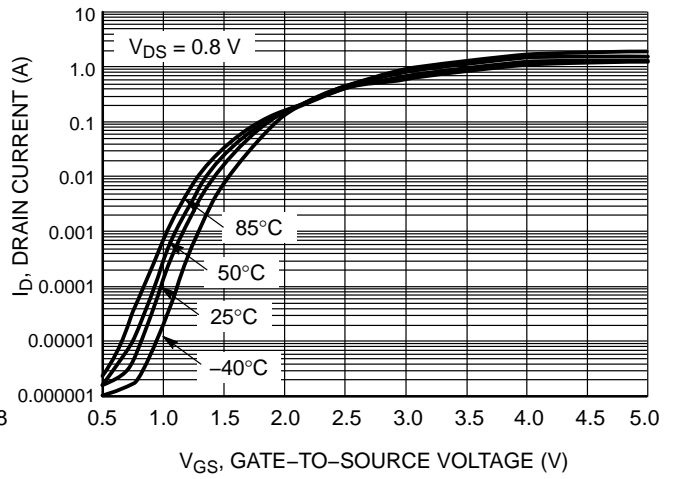


Figure 3. Transfer Function

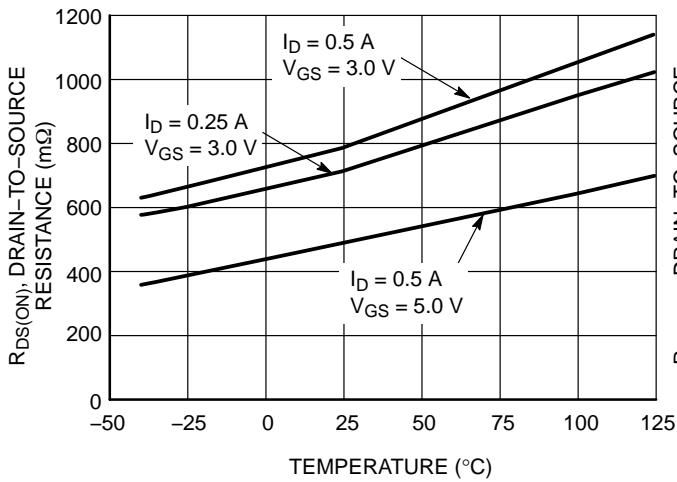


Figure 4. On Resistance Variation vs. Temperature

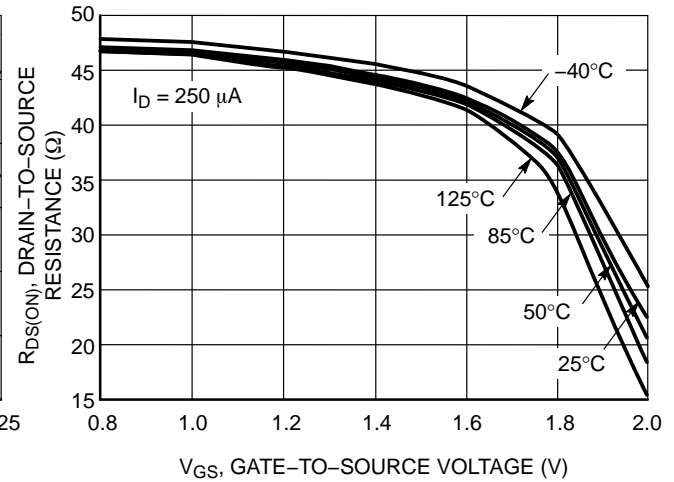


Figure 5. $R_{DS(ON)}$ Variation with Gate to Source Voltage

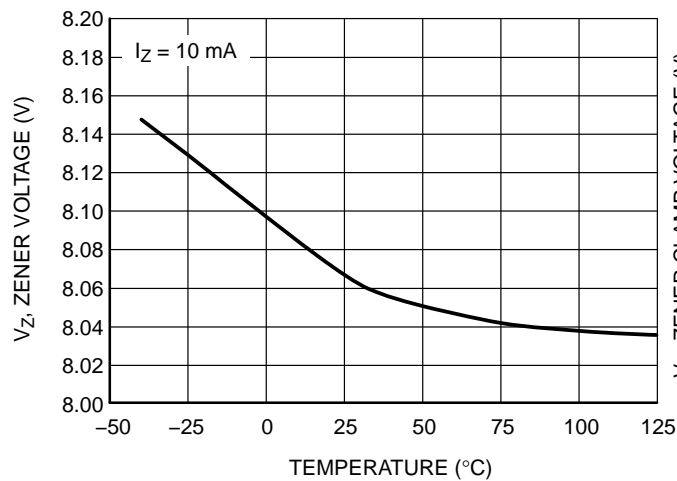


Figure 6. Zener Voltage vs. Temperature

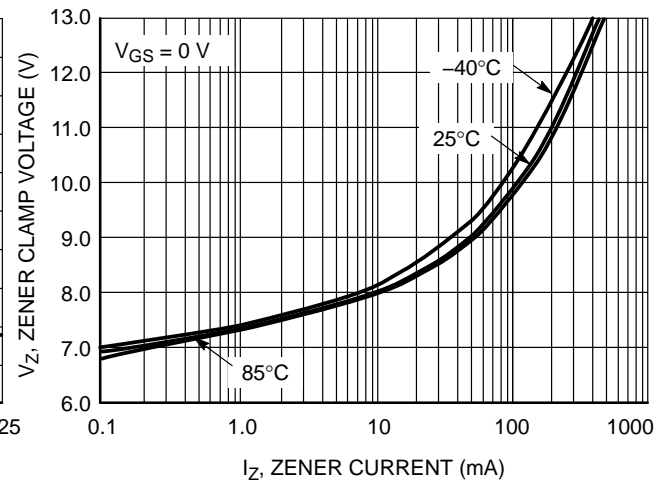


Figure 7. Zener Clamp Voltage vs. Zener Current

NUD3105

TYPICAL CHARACTERISTICS

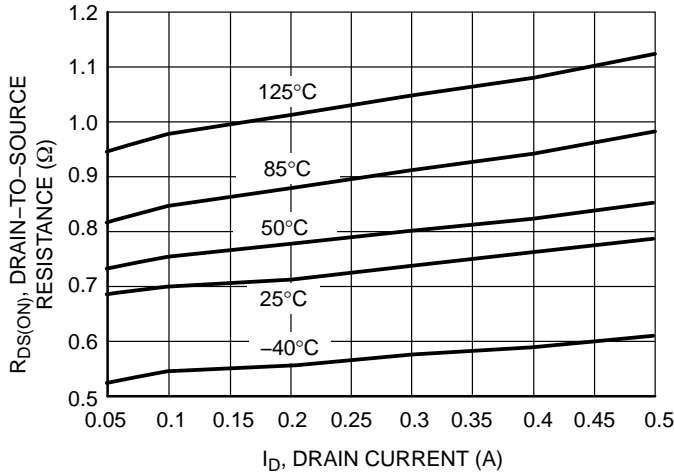


Figure 8. On-Resistance vs. Drain Current and Temperature

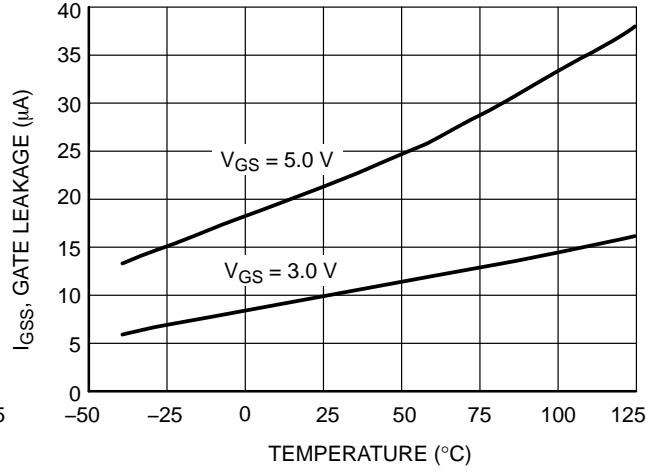


Figure 9. Gate Leakage vs. Temperature

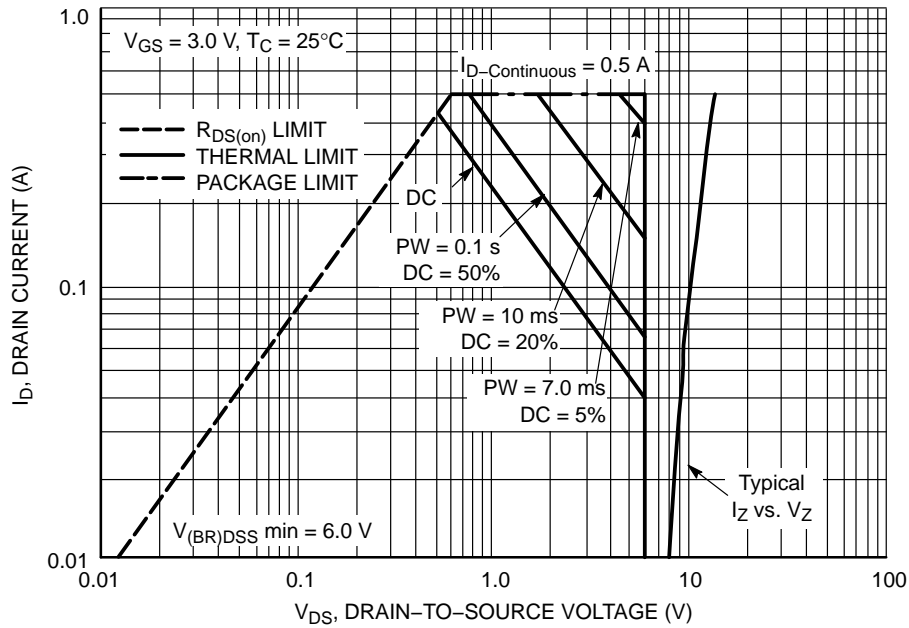


Figure 10. Safe Operating Area

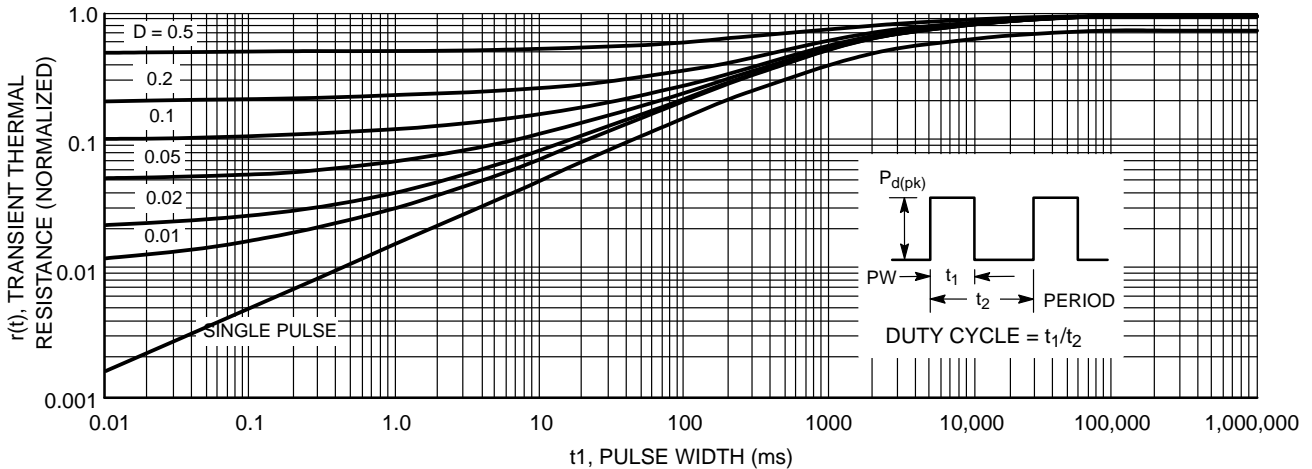


Figure 11. Transient Thermal Response

NUD3105

Designing with this Data Sheet

1. Determine the maximum inductive load current (at max V_{CC} , min coil resistance & usually minimum temperature) that the NUD3105 will have to drive and make sure it is less than the max rated current.
2. For pulsed operation, use the Transient Thermal Response of Figure 11 and the instructions with it to determine the maximum limit on transistor power dissipation for the desired duty cycle and temperature range.
3. Use Figures 10 and 11 with the SOA notes to insure that instantaneous operation does not push the device beyond the limits of the SOA plot.
4. Verify that the circuit driving the gate will meet the $V_{GS(th)}$ from the Electrical Characteristics table.
5. Using the max output current calculated in step 1, check Figure 7 to insure that the range of Zener clamp voltage over temperature will satisfy all system & EMI requirements.
6. Use I_{GSS} and I_{DSS} from the Electrical Characteristics table to ensure that "OFF" state leakage over temperature and voltage extremes does not violate any system requirements.
7. Review circuit operation and insure none of the device max ratings are being exceeded.

APPLICATIONS DIAGRAMS

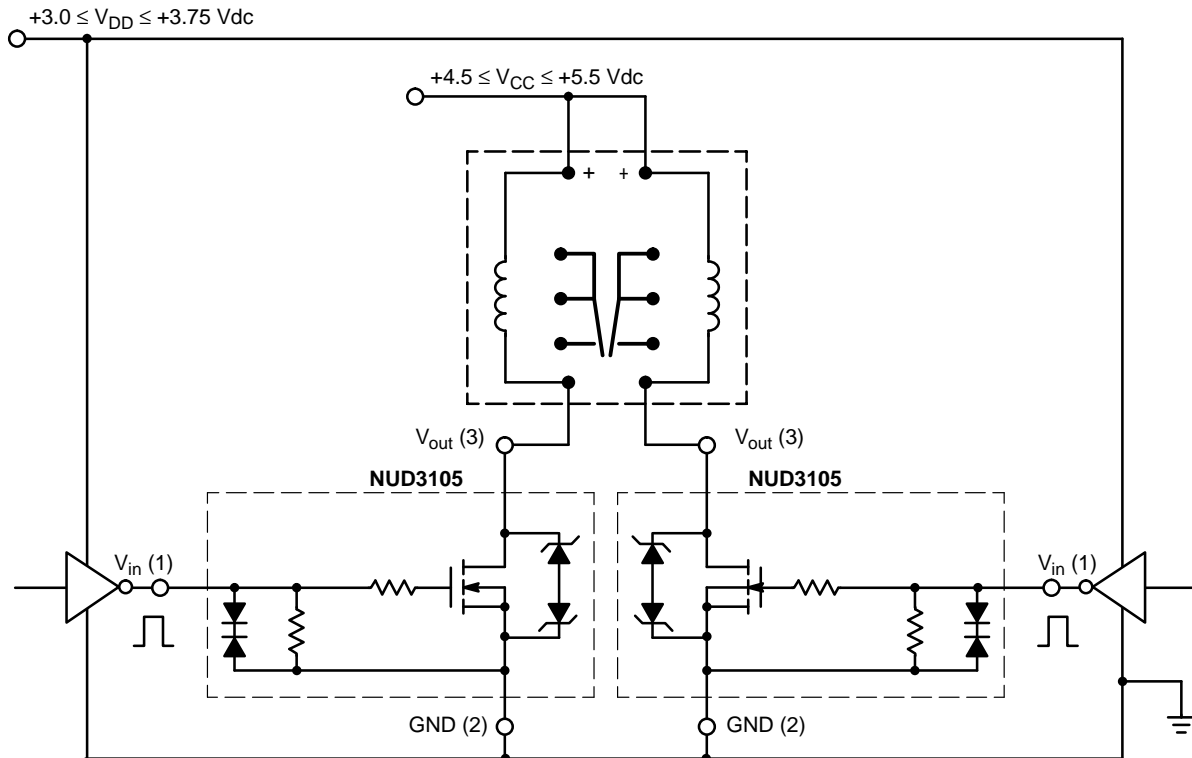


Figure 12. A 200 mW, 5.0 V Dual Coil Latching Relay Application with 3.0 V Level Translating Interface

NUD3105

Max Continuous Current Calculation

for TX2-5V Relay, $R_1 = 178 \Omega$ Nominal @ $R_A = 25^\circ\text{C}$

Assuming $\pm 10\%$ Make Tolerance,

$R_1 = 178 \Omega * 0.9 = 160 \Omega$ Min @ $T_A = 25^\circ\text{C}$

T_C for Annealed Copper Wire is $0.4\%/^\circ\text{C}$

$R_1 = 160 \Omega * [1 + (0.004) * (-40^\circ - 25^\circ)] = 118 \Omega$ Min @ -40°C

$I_O \text{ Max} = (5.5 \text{ V Max} - 0.25\text{V}) / 118 \Omega = 45 \text{ mA}$

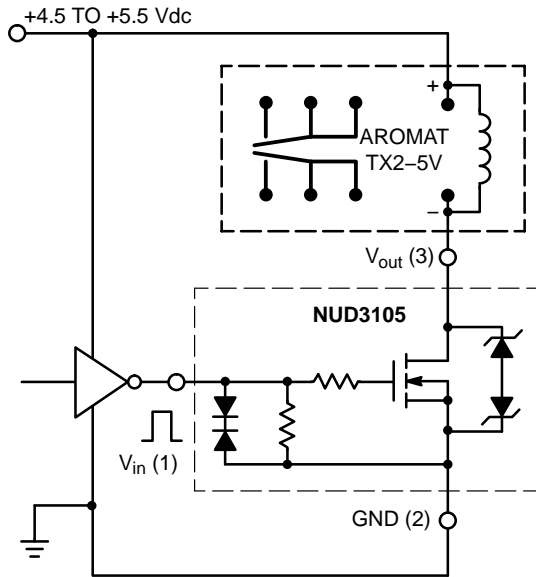


Figure 13. A 140 mW, 5.0 V Relay with TTL Interface

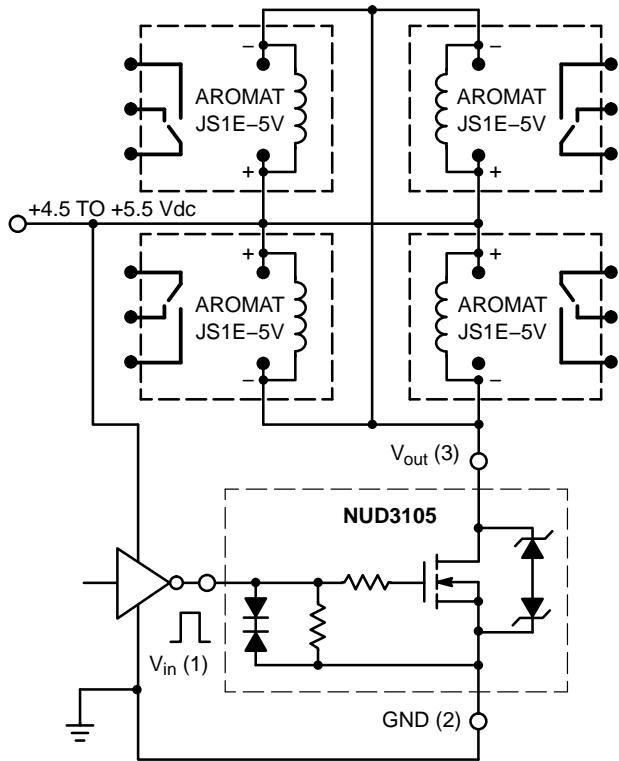
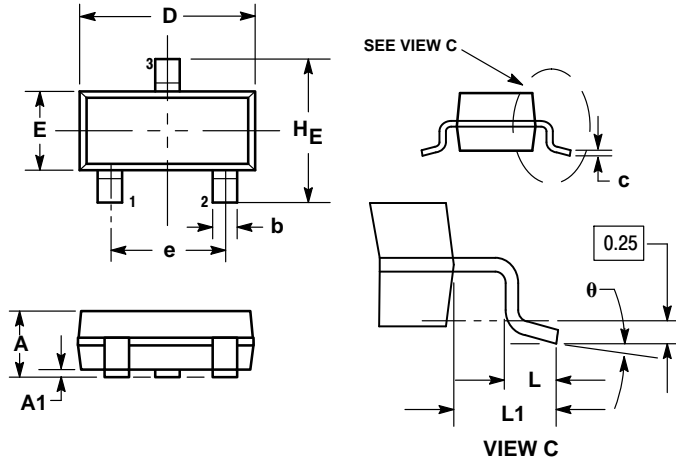


Figure 14. A Quad 5.0 V, 360 mW Coil Relay Bank

NUD3105

PACKAGE DIMENSIONS

SOT-23 (TO-236)
CASE 318-08
ISSUE AP

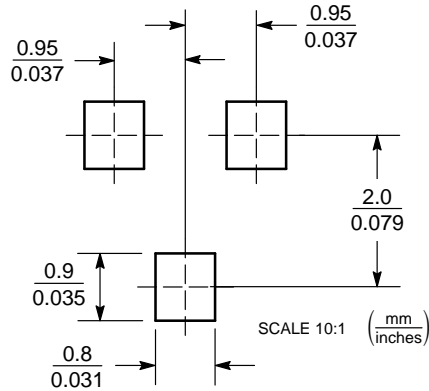


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

SOLDERING FOOTPRINT*

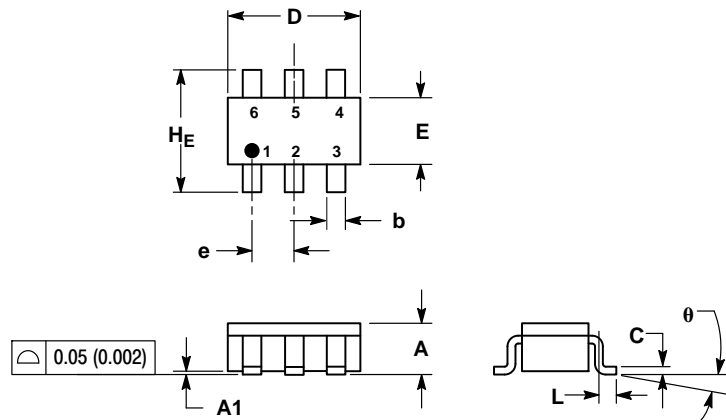


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NUD3105

PACKAGE DIMENSIONS

SC-74 CASE 318F-05 ISSUE N



NOTES:

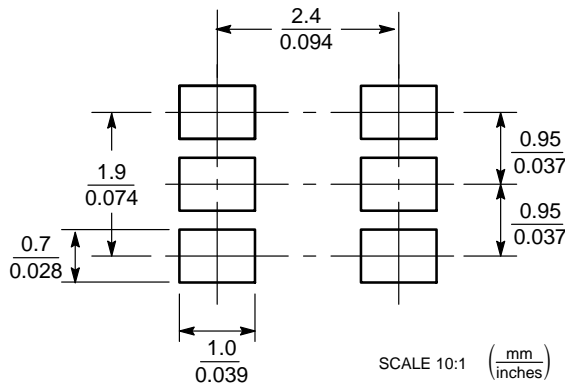
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F-01, -02, -03, -04 OBSOLETE. NEW STANDARD 318F-05.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°

STYLE 7:

- PIN 1. SOURCE 1
- GATE 1
- DRAIN 2
- SOURCE 2
- GATE 2
- DRAIN 1

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative