Ordering number : EN*5221

CMOS LSI

LC65E1104

On-Chip UVEPROM 4-Bit Single-Chip Microcontroller

Preliminaly

Overview

The LC65E1104 is an on-chip UVEPROM version of Sanyo's LC651104N/F/L and LC651102N/F/L CMOS 4-bit single-chip microcontrollers. The LC65E1104 has the same functions and pin assignment as the LC651104N/F/L and LC651102N/F/L mask ROM products, although the A/D characteristics and certain other characteristics differ somewhat. It includes a 4-KB on-chip EPROM.

The LC65E1104 is provided in DIC30S and MFC30S window packages and is ideal for program development and evaluation since program data can be rewritten multiple times.

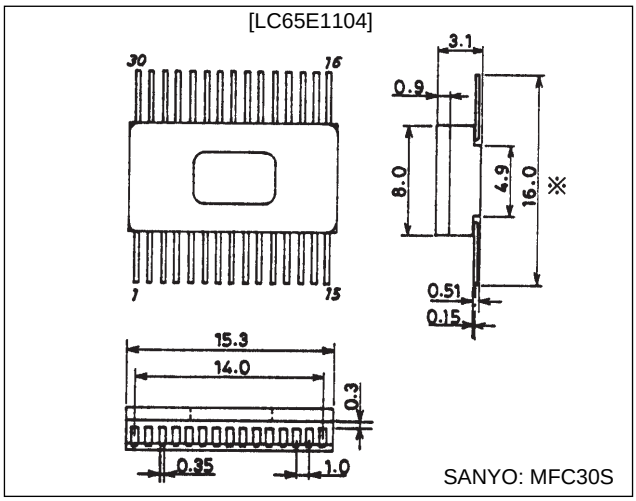
Features

- EPROM data option switching
  The following four LC65E1104 functions can be specified by EPROM data:
  — Port C and D output levels at reset
  — Clock oscillator option
  — Clock predivider option
  — Watchdog reset option
  However, note that the port output circuit type cannot be changed. These circuits are always open-drain outputs.
- Internal UVEPROM capacity: 4096 bytes
- The LC65E1104 on-chip UVEPROM can be programmed and verified using a general-purpose EPROM programmer.
  Sanyo provides special-purpose 30-to-28-pin adapters (the W65EP1104D for the DIC package and the W65EP1104M for the MFC package) to allow commercial EPROM programmers to be used with the LC65E1104.
- Data security function
- Pin compatible with the LC651104/1102 mask ROM devices
- Instruction cycle time: 0.92 µs to 20 µs (A/D converter cycle time: 0.98 µs to 12 µs)
- Factory shipment: DIC-30S (with window), MFC-30S (with window)

Package Dimensions

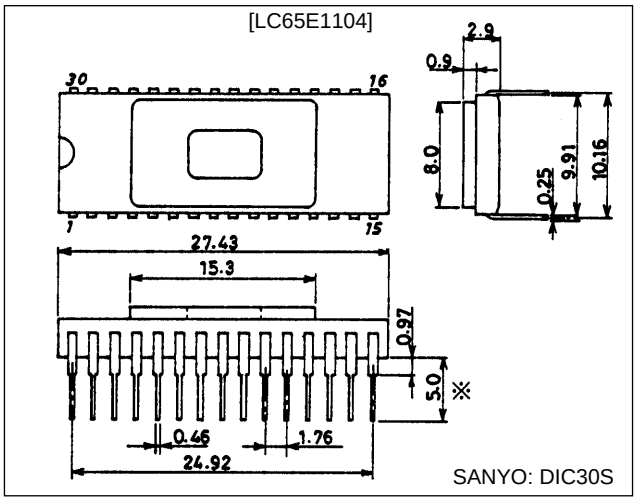
unit: mm

3212-MFC30S



unit: mm

3215-DIC30S



Note: These figures are provided for reference purposes and do not include tolerance specifications. Official drawings are available on request from your Sanyo representative.

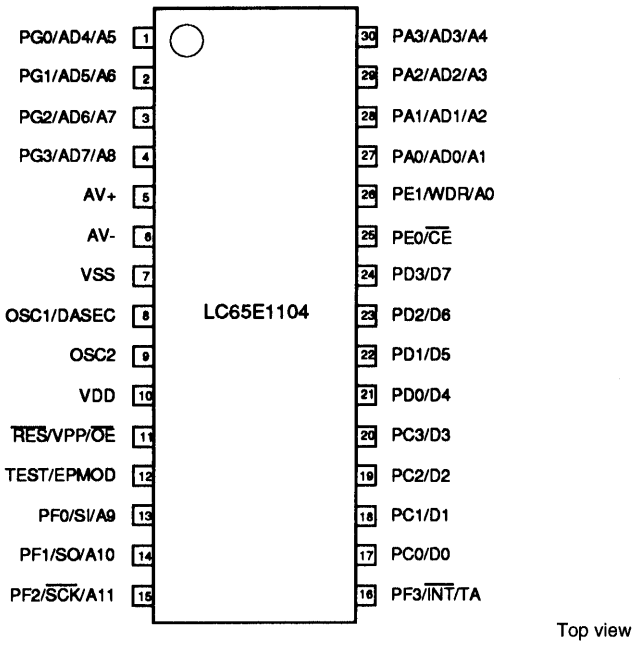
SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

LC651104/1102 series organization

Model name	Pins	ROM capacity	RAM capacity	Package
LC651104N/F/L, LC651102N/F/L	30	4 k/2 k	256 W	DIP30S, DIP30S-D, MFP30S
LC65E1104	30	4 k	256 W	DIC30S, MFC30S
LC65P1104	30	4 k	256 W	DIP30S-D, MFP30S

Pin Assignment

Common to DIC/MFC



Top view

Usage Notes

The LC65E1104 was designed for developing and evaluating programs for the LC651104/1102 series microcontrollers. Keep the following points in mind when using the LC65E1104.

1. Protecting EPROM data from UV exposure
   Keep the LC65E1104's package window covered with an opaque seal when using the device.
2. The LC65E1104 differs from the LC651104N/F/L and LC651102N/F/L as listed in the table below.

Item		LC65E1104	LC651104F/1102F	LC651104N/1102N	LC651104L/1102L
I/O circuit configuration		Open drain (N channel)	Open drain or pull-up resistor-provided output selectable bit by bit (user mask option)		
Port C and D output levels at reset		High or low selected in 4-bit units (by EPROM data)	High or low selected in 4-bit units (user mask option)		
Oscillator	Resonator	RC/ceramic (by EPROM data)	RC/ceramic (user mask option)		
	Predivider option	1/1, 1/3, 1/4 (by EPROM data)	1/1 only (user mask option)	1/1, 1/3, 1/4 (user mask option)	
Watchdog reset		Available/not available (by EPROM data)	Available/not available (user mask option)		
Operating supply voltage range (V_{DD})		3.0 to 6.0 V*	4.0 t 6.0 V	3.0 to 6.0 V	2.5 to 6.0 V
Normal mode current drain		Mask version + about 3 mA (typical)	2 mA (typical)	1.5 mA (typical)	1.5 mA (typical)
Low-level input current ($\overline{RES}$ terminal)		–50 µA (typical)	–10 µA (typical)		
Operating temperature range		+10 to +40°C	–40 to +85°C		
Package		DIC30S (with window) MFC30S (with window)	DIP30S, DIP30S-D MFP30S		

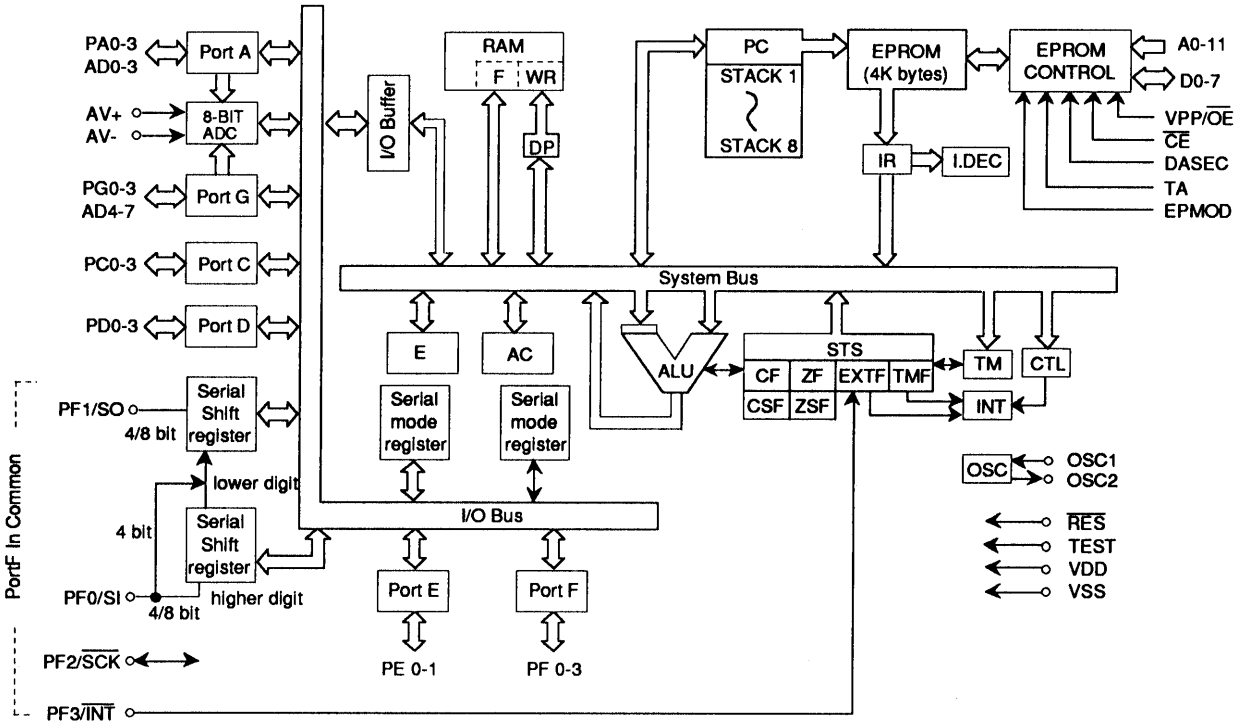
Note: A/D converter operating supply voltage range: 4.7 to 5.3 V

Pin Names

OSC1, OSC2	RC or ceramic oscillator	TEST	Test
$\overline{RES}$	Reset	$\overline{INT}$	Interrupt request pin
PA0 to PA3	Shared-function I/O ports A0 to A3	SI	Serial input pin
PC0 to PC3	Shared-function I/O ports C0 to C3	SO	Serial output pin
PD0 to PD3	Shared-function I/O ports D0 to D3	$\overline{SCK}$	Serial clock input/output pin
PE0 to PE1	Shared-function I/O ports E0 to E1	AD0 to AD7	AD converter input pin
PF0 to PF3	Shared-function I/O ports F0 to F3	AV+, AV–	AD converter reference voltage input
PG0 to PG3	Shared-function I/O ports G0 to G3	WDR	Watchdog reset pin

Note: The SI, SO, $\overline{SCK}$, and $\overline{INT}$ pins are shared function pins that are also used as the PF0 to PF3 pins, respectively.

System Block Diagram



RAM	Data memory	ROM	Program memory
F	Flag	PC	Program counter
WR	Working register	INT	Interrupt control
AC	Accumulator	IR	Instruction register
ALU	Arithmetic and logic unit	I.DEC	Instruction decoder
DP	Data pointer	CF, ZSF	Carry flag, Carry save flag
E	E register	ZF, ZSC	Zero flag, zero save flag
CTL	Control register	EXTF	External interrupt request flag
OSC	Oscillator	TMF	Internal interrupt request flag
TM	Timer	STS	Status register

Pin Description

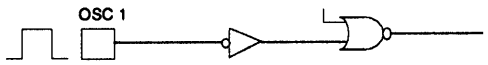
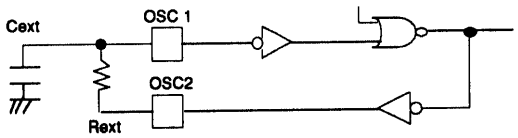
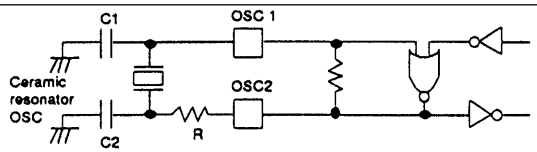
Symbol	Pins	I/O	Function	Option	At reset	PROM mode
V_{DD} V_{SS}	1 1	— —	Power supply	—	—	—
OSC1/DASEC	1	I	• Connections for the external RC or ceramic oscillator circuit used as the system clock oscillator. • If external clock input is used, leave the OSC2 pin open.	1. Pin 2: RC oscillator external clock 2. Pin 2: Ceramic oscillator 3. Predivider option • No predivider • 1/3 predivider • 1/4 predivider	—	EPROM control signal DASEC
OSC2	1	O				
PA0/AD0/A1 PA1/AD1/A2 PA2/AD2/A3 PA3/AD3/A4	4	I/O	• I/O port: A0 to A3 Input in 4-bit units (IP instruction) Output in 4-bit units (OP instruction) Testing in single-bit units (BP and BNP instructions) Setting or clearing in single-bit units (SPB and RPB instructions) • Standby is controlled by PA3 • The PA3 pin must be free from chattering during the halt instruction execution cycle. Each of these four pins has two functions as listed below. PA0/AD0: AD converter input pin AD0 PA1/AD1: AD converter input pin AD1 PA2/AD2: AD converter input pin AD2 PA3/AD3: AD converter input pin AD3	Open drain type output	High-level output (Output Nch transistor: Off)	Address inputs A1 to A4
PC0/D0 PC1/D1 PC2/D2 PC3/D3	4	I/O	• I/O port: C0 to C3 Identical to PA0 to PA3* • Option permits output at reset to be high or low. Note: * No standby control function is provided.	1. Open drain type output 2. Output at reset: high 3. Output at reset: low 2., 3.: Specified in a group of 4 bits	• High-level output • Low-level output (Option-selectable)	Data lines D0 to D3
PD0/D4 PD1/D5 PD2/D6 PD3/D7	4	I/O	I/O port: D0 to D3 Identical to PC0 to PC3	Identical to PC0 to PC3	Identical to PC0 to PC3	Data lines D4 to D7
PE0/$\overline{CE}$ PE1/WDR/A0	2	I/O	• I/O port: E0 and E1 Input in 4-bit units (IP instruction) Output in 4-bit units (OP instruction) Setting or clearing in single-bit units (SPB, RPB instructions) Testing in single-bit units (BP and BNP instructions) • PE0 provides a continuous burst (64·Tcyc) function.	1. Open drain type output	High-level output (Output Nch transistor: Off)	• EPROM control signal CE • Address input A0
PF0/SI/A9 PF1/SO/A10 PF2/SCK/A11 PF3/$\overline{INT}$/TA	4	I/O	• I/O ports F0 tp F3 Identical to PE0 to PE1* • Shared with the serial interface and $\overline{INT}$ input. Program-selectable SI Serial input port SO Serial output port SCK Serial clock input/output $\overline{INT}$ Interrupt request input The serial I/O function can be switched between 4-bit and 8-bit operation under program control. Note: * No burst pulse output function is provided.	Identical to PE0 to PE1	Identical to PE0 to PE1 Serial port: Disabled Interrupt source: $\overline{INT}$	• Address inputs A9 to A11 • EPROM control signal TA

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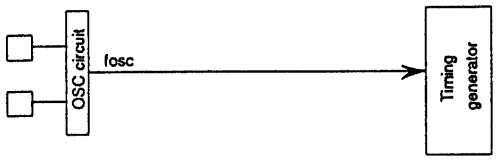
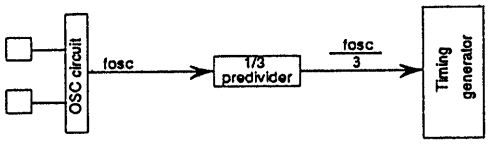
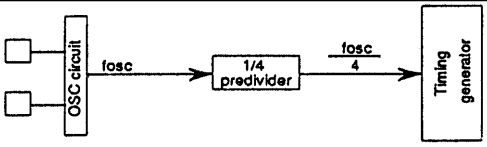
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Symbol	Pins	I/O	Function	Option	At reset	PROM mode
PG0/AD4/A5 PG1/AD5/A6 PG2/AD6/A7 PG3/AD7/A8	4	I/O	• I/O ports G0 to G3 Identical to PE0 to PE1* Note: * No burst pulse output function is provided. • Each of these four pins has two functions as listed below. PG0/AD4: AD converter input pin AD4 PG1/AD5: AD converter input pin AD5 PG2/AD6: AD converter input pin AD6 PG3/AD7: AD converter input pin AD7	Identical to PE0 to PE1	Identical to PE0 to PE1	Address inputs A5 to A8
AV+	1	—	Reference voltage input pin for A/D conversion.	—	—	—
AV–	1	—				
$\overline{RES}$/VPP/$\overline{OE}$	1		• System reset input • Connect an external capacitor for power on reset. • Apply a low level for at least 4 clock cycles for the power-on reset.	—	—	EPROM control signal VPP/$\overline{OE}$
TEST/EPMOD	1		LSI test pin Normally connected to V_{SS}	—	—	EPROM control signal EPMOD

Oscillator circuit option

Option	Circuit	Conditions and notes
1. External clock		Leave the OSC2 pin open.
2. 2-pin RC OSC		
3. Ceramic oscillator		

Predivider option

Option	Circuit	Conditions and notes
1. No predivider (1/1)		• Applicable to all 3 oscillator options. • The oscillator or external clock frequency must not exceed 1444 kHz. (LC651104N, LC651102N) • The oscillator or external clock frequency must not exceed 4330 kHz. (LC651104F, LC651102F) • The oscillator or external clock frequency must not exceed 1040 kHz. (LC651104L, LC651102L)
2. 1/3 predivider		• Applicable to the external clock and ceramic oscillator options. • The oscillator or external clock frequency must not exceed 4330 kHz.
3. 1/4 predivider		• Applicable to the external clock and ceramic oscillator options. • The oscillator or external clock frequency must not exceed 4330 kHz.

Note: The oscillator and predivider options are summarized in the LC651104/1102 semiconductor news.

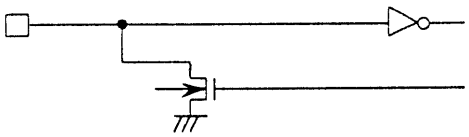
Port C and D reset output level options

Either of the following two options may be selected for the C and D I/O ports. Note that these options are specified in 4-bit units.

Option name	Conditions
1. Output at reset: high	All 4 bits of the selected port(s) (C or D or both)
1. Output at reset: low	All 4 bits of the selected port(s) (C or D or both)

Port output configuration option

All shared-function I/O ports have an open-drain output circuit in the LC65E1104.

Option	Circuit	Conditions and notes
1. Open drain output		Ports A, C, D, E and F

Watchdog reset option

This option specifies the use of the PE1/WDR pin. This pin can be specified to function either as the normal port PE1 or as the WDR watchdog reset pin.

Usage Notes

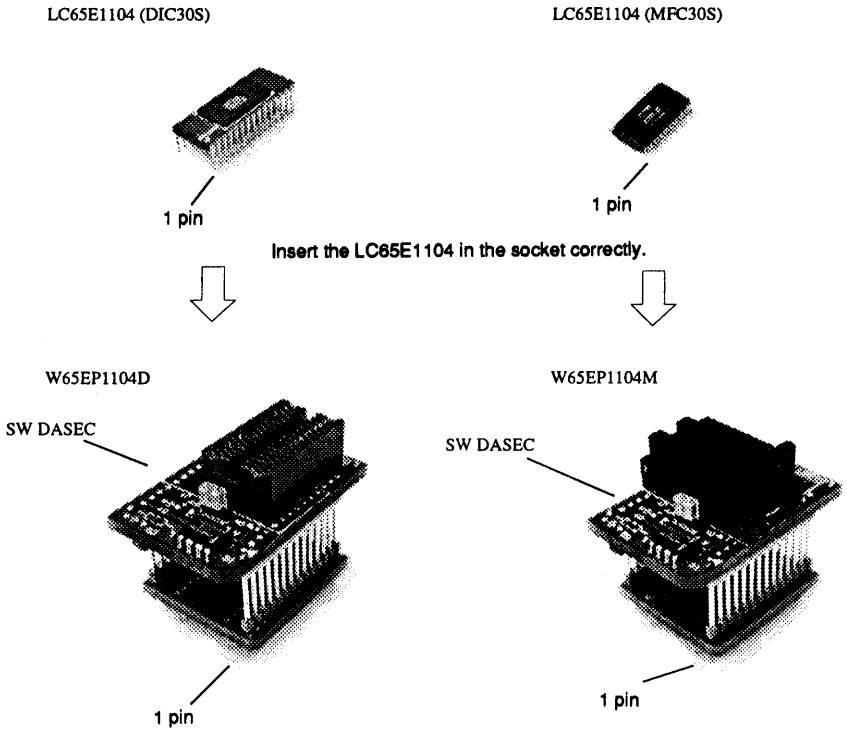
1. Option specification
   The SU60K.EXE program is used for option specification. The option code for the option specification area (addresses 1000 to 100A (hexadecimal)) is created by assembling the output of the SU60K.EXE program using the Sanyo M60K.EXE macro assembler and then linking the macro assembler output with the Sanyo L60K.EXE linker. It is also possible to load data directly into the option specification area. Specify options according to the option code creation table on page 8.
2. PROM programming
   LC65E1104 can be programmed with a general-purpose EPROM programmer using either the W65EP1104D or W65EP1104M adapter.
   - Recommended EPROM programmers

Manufacturer	EPROM programmer
Advantest	R4945, R4944, R4943 or equivalent programmer
Ando	AF-9704
AVAL	—
Minato electronics	—

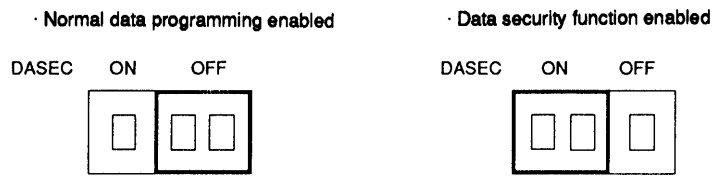
   - The Intel 27512 (VPP: 12.5 V) high-speed programming method must be used to program this device. The address range must be set to 0 to 100A (hexadecimal) and the DASEC jumper must be set to the off position.

3. Using the data security function
   The data security function prevents data already written to the microcontroller's PROM from being overwritten.
   LC651104 data security function procedure
   - Move the DASEC jumper on the EPROM programming pin adapter to the on position. This enables the data security function.
   - Attempt to reprogram the EPROM.
     Since the data security function is enabled, the EPROM programmer will display an error. Note that this error is not due to an error in either the programmer or the LSI.

Note: 1. At step 2, the data security function will not operate if all the data at the addresses to be programmed have the value FF (hexadecimal).
2. At step 2, the data security function will not apply to (i.e., will not prevent) programming using the sequence BLANK Æ PROGRAM Æ VERIFY.
3. Return the jumper to the off position after executing the data security function.



DASEC jumper setting



Option specification area

ROM area	Bit	Option specified		Option/data relationship
1000H	7	Unused		0 (fixed)
	6	Watchdog reset		0: Disabled, 1: Enabled
	5	PD	Output level at reset	0: Low level, 1: High level
	4	PC		
	3	OSC predivider (XX = bits 3, bit 2)		00: 1/1, 01: 1/3, 10: 1/4,. 11: unused
	2			
	1	OSC resonator (XX = bits 1, bit 0)		00: unused, 01: unused, 10: (2RC, EXT), 11: Ceramic
	0			
1001H	7	PC3	Output configuration	0: OD, 1: PU*
	6	PC2		
	5	PC1		
	4	PC0		
	3	PA3	Output configuration	0: OD, 1: PU*
	2	PA2		
	1	PA1		
	0	PA0		
1002H	7 6	Unused		0 (fixed)
	5	PE1	Output configuration	0: OD, 1: PU*
	4	PE0		
	3	PD3	Output configuration	0: OD, 1: PU*
	2	PD2		
	1	PD1		
	0	PD0		
1003H	7	PG3	Output configuration	0: OD, 1: PU*
	6	PG2		
	5	PG1		
	4	PG0		
	3	PF3	Output configuration	0: OD, 1: PU*
	2	PF2		
	1	PF1		
	0	PF0		
1004H to 100AH	7 6 5 4 3 2 1 0	Unused		0 (fixed)

Note: Since all LC65E1104 ports are open-drain output circuits, the pull-up resistor options are ignored. However, the port options must be selected when using the LC651104/1102 mask ROM products.
PU: Built-in pull-up resistor output circuit, OD: Open-drain output circuit

Specifications

For LC651104N, 651102N

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
Output voltage	V_O	OSC2	Allowable up to the generated voltage	V
Input voltage	V_I1	OSC1*1	–0.3 to V_{DD} + 0.3	V
	V_I2	TEST, $\overline{RES}$, AV+, AV–	–0.3 to V_{DD} + 0.3	V
Input/output voltage	V_{IO}1	PC0 to PC3, PD0 to PD3, PE0, PE1, PF0 to PF3	–0.3 to +15	V
	V_{IO}2	PA0 to PA3, PG0 to PG3	–0.3 to V_{DD} + 0.3	V
Peak output current	I_{OP}	I/O port	–2 to +20	mA
Average output current	I_{OA}	I/O port: Per pin over a 100 ms period	–2 to +20	mA
	ΣI_{OA}1	PC0 to PC3, PD0 to PD3, PE0, PE1:Total current for PC0 to PC3, PD0 to PD3, and PE0, PE1*2	–15 to +100	mA
	ΣI_{OA}2	PF0 to PF3, PG0 to PG3, PA0 to PA3: Total current for PF0 to PF3, PG0 to PG3, and PA0 to PA3*2	–15 to +100	mA
Allowable power dissipation	Pd max1	Ta = +10 to +40°C (DIC package)	250	mW
	Pd max2	Ta = +10 to +40°C (MFC package)	150	mW
Operating temperature	Topr		+10 to +40	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Conditions at Ta = +10 to +40°C, V_{SS} = 0 V, V_{DD} = 3.0 to 6.0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage	V_{DD}	V_{DD}	3.0		6.0	V
Standby supply voltage	V_{ST}	V_{DD}: RAM, register hold*3	1.8		6.0	V
High level input voltage	V_{IH}1	Port C, D, E, F: Output Nch Tr. off	0.7 V_{DD}		+13.5	V
	V_{IH}2	Port A, G: Output Nch Tr. off	0.7 V_{DD}		V_{DD}	V
	V_{IH}3	$\overline{INT}$, $\overline{SCK}$, SI: Output Nch Tr. off	0.8 V_{DD}		+13.5	V
	V_{IH}4	$\overline{RES}$: V_{DD} = 1.8 to 6 V	0.8 V_{DD}		V_{DD}	V
	V_{IH}5	OSC1: External clock mode	0.8 V_{DD}		V_{DD}	V
Low level input voltage	V_{IL}1	Port: Output Nch Tr. off, V_{DD} = 4 to 6 V	V_{SS}		0.3 V_{DD}	V
	V_{IL}2	Port: Output Nch Tr. off, V_{DD} = 3 to 6 V	V_{SS}		0.25 V_{DD}	V
	V_{IL}3	$\overline{INT}$, $\overline{SCK}$, SI: Output Nch Tr. off, V_{DD} = 4 to 6 V	V_{SS}		0.25 V_{DD}	V
	V_{IL}4	$\overline{INT}$, $\overline{SCK}$, SI: Output Nch Tr. off, V_{DD} = 3 to 6 V	V_{SS}		0.2 V_{DD}	V
	V_{IL}5	OSC1: External clock mode, V_{DD} = 4 to 6 V	V_{SS}		0.25 V_{DD}	V
	V_{IL}6	OSC1: External clock mode, V_{DD} = 3 to 6 V	V_{SS}		0.2 V_{DD}	V
	V_{IL}7	TEST: V_{DD} = 4 to 6 V	V_{SS}		0.3 V_{DD}	V
	V_{IL}8	TEST: V_{DD} = 3 to 6 V	V_{SS}		0.25 V_{DD}	V
	V_{IL}9	$\overline{RES}$: V_{DD} = 4 to 6 V	V_{SS}		0.25 V_{DD}	V
	V_{IL}10	$\overline{RES}$: V_{DD} = 3 to 6 V	V_{SS}		0.2 V_{DD}	V
Operating frequency (cycle time)	fop (Tcyc)	When the 1/3 or 1/4 predivider option is selected, clock must not exceed 4.33 MHz. V_{DD} = 3 to 6 V	200 (20)		1444 (2.77)	kHz (µs)
[External clock conditions]						
Frequency	text	OSC1: Fig 1, when clock exceeds 1.444 MHz, the 1/3 or 1/4 predivider option must be selected. V_{DD} = 3 to 6 V	200		4330	kHz
Pulse width	textH, textL		69			ns
Rise/fall time	textR, textF				50	ns
[Oscillator guaranteed constants]						
2-pin RC oscillator	Cext	OSC1, OSC2: Fig 2, V_{DD} = 3 to 6 V		270 ± 5%		pF
	Cext	OSC1, OSC2: Fig 2, V_{DD} = 4 to 6 V		270 ± 5%		pF
	Rext	OSC1, OSC2: Fig 2, V_{DD} = 3 to 6 V		12 ± 1%		kΩ
	Rext	OSC1, OSC2: Fig 2, V_{DD} = 4 to 6 V		4.7 ± 1%		kΩ
Ceramic		Fig 3		Table 1		

Electrical Characteristics at Ta = +10 to +40°C, V_{SS} = 0 V, V_{DD} = 3.0 to 6.0 V

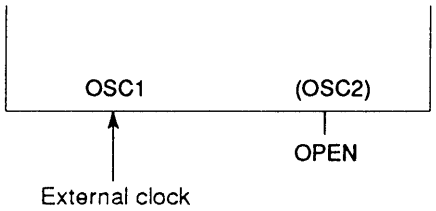
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level input current	$I_{IH}1$	Port C, D, E, F: Output Nch Tr. off (including off leak current of Nch Tr.), V_{IN} = +13.5			+5.0	µA
	$I_{IH}2$	Port A, G: Output Nch Tr. off (including off leak current of Nch Tr.), V_{IN} = V_{DD}			+5.0	µA
	$I_{IH}3$	OSC1: External clock mode, V_{IN} = V_{DD}			+1.0	µA
Low-level input current	$I_{IL}1$	Port: Output Nch Tr. off, V_{IN} = V_{SS}	–1.0			µA
	$I_{IL}2$	$\overline{RES}$: V_{IN} = V_{SS}	–150	–50		µA
	$I_{IL}3$	OSC1: External clock mode, V_{IN} = V_{SS}	–1.0			µA
Low-level output current	$V_{OL}1$	Port: I_{OL} = 10 mA, V_{DD} = 4.0 to 6.0 V			1.5	V
	$V_{OL}2$	Port: I_{OL} = 1 mA, I_{OL} of each port; 1 mA or less V_{DD} = 3.0 to 6.0 V			0.5	V
[Schmitt characteristics]						
Hysteresis voltage	VHIS			0.1 V_{DD}		V
High-level threshold voltage	VtH	$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, SI, OSC1 of Schmitt type*4	0.4 V_{DD}		0.8 V_{DD}	V
Low-level threshold voltage	VtL		0.2 V_{DD}		0.6 V_{DD}	V
[Current dissipation]						
2-pin RC oscillator	IDDOP1	V_{DD}: Output Nch Tr. off at operating, port = V_{DD}, Fig. 2, fosc = 900 kHz (typ)		4.5	6	mA
Ceramic oscillator	IDDOP2	V_{DD}: Fig 3, 4 MHz, 1/3 predivider		4.5	7	mA
	IDDOP3	V_{DD}: Fig 3, 4 MHz, 1/4 predivider		4.5	6	mA
	IDDOP4	V_{DD}: Fig 3, 400 kHz		4.0	4.5	mA
	IDDOP5	V_{DD}: Fig 3, 800 kHz		4.5	6	mA
External clock	IDDOP6	V_{DD}: 200 kHz to 1444 kHz, 1/1 predivider; 600 kHz to 4330 kHz, 1/3 predivider; 800 kHz to 4330 kHz, 1/4 predivider		4.5	7	mA
Standby mode	IDDst	V_{DD}: Output Nch Tr. off, V_{DD} = 6 V		0.05	10	µA
		V_{DD}: Port = V_{DD}, V_{DD} = 3 V		0.025	5	µA
[Oscillator characteristics]						
Ceramic OSC frequency	fCFOSC*5	OSC1, OSC2: Fig 3, fo = 400 kHz	384	400	416	kHz
		OSC1, OSC2: Fig 3, fo = 800 kHz	768	800	832	kHz
		OSC1, OSC2: Fig 3, fo = 1 MHz	960	1000	1040	kHz
		OSC1, OSC2: Fig 3, fo = 4 MHz, 1/3 predivider, 1/4 predivider	3840	4000	4160	kHz
Stabilization		Fig 4, fo = 400 kHz			10	ms
	tCFS	Fig 4, fo = 800 kHz, 1 MHz, 4 MHz, 1/3 predivider, 1/4 predivider			10	ms
2-pin RC oscillator frequency	fMOSC	OSC1, OSC2: Fig. 2, Cext = 270 pF ± 5%, Fig. 2, Rext = 4.7 kΩ ± 1%, V_{DD} = 4 to 6 V	666	900	1334	kHz
		OSC1, OSC2: Fig. 2, Cext = 270 pF ± 5%, Fig. 2, Rext = 12 kΩ ± 1%, V_{DD} = 3 to 6 V	283	400	717	kHz
[Pull-up resistance]						
I/O port $\overline{RES}$:	RU	$\overline{RES}$: V_{IN} = V_{SS}, V_{DD} = 5 V	50	100	250	kΩ
[External reset characteristics]						
Reset time	tRST			See Fig. 5		
Pin capacitance	C_P	f = 1 MHz. V_{IN} = V_{SS} for all pins other than those being tested.		10		pF
[Serial clock]						
Input clock cycle time	tCKCY1	$\overline{SCK}$: Fig. 6	3.0			µs
Output clock cycle time	tCKCY2	$\overline{SCK}$: Fig. 6		64 × tCYC*6		µs
Input clock low-level pulse width	tCKL1	$\overline{SCK}$: Fig. 6	1.0			µs
Output clock low-level pulse width	tCKL2	$\overline{SCK}$: Fig. 6		32 × tCYC		µs
Input clock high-level pulse width	tCKH1	$\overline{SCK}$: Fig. 6	1.0			µs
Output clock high-level pulse width	tCKH2	$\overline{SCK}$: Fig. 6		32 × tCYC		µs
[Serial input]						
Data setup time	tICK	SI: Specified from the rising edge of $\overline{SCK}$. Fig. 6	0.4			µs
Data hold time	tCKI		0.4			µs

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Serial output]						
Output delay time	tCKO	SO: Specified from the falling edge of $\overline{SCK}$. Nch OD only, external 1kΩ, external 50 pF, Fig. 6			0.6	μs
[Pulse output]						
Period	tPCY	PE0: Fig. 7, tCYC = 4 × system clock period, Nch OD only, external 1 kΩ, external 50 pF		64 ×tCYC		μs
High-level pulse width	tPH			32 × tCYC ± 10%		μs
Low-level pulse width	tPL			32 × tCYC ± 10%		μs
[AD conversion characteristics]						
Resolution		V_{DD} = 4.7 to 5.3 V		8		bits
Absolute accuracy		AV+ = V_{DD}, AV– = V_{SS}, V_{DD} = 4.7 to 5.3 V		±1	±2	LSB
Conversion time	TCAD	AD speed 1/1, at 26 × tCYC, V_{DD} = 4.7 to 5.3 V	72 (tCYC = 2.77 μs)		312 (tCYC = 12 μs)	μs
		AD speed 1/2, at 51 × tCYC, V_{DD} = 4.7 to 5.3 V	141 (tCYC = 2.77 μs)		612 (tCYC = 12 μs)	
Reference input voltage	AV+	AV+: V_{DD} = 4.7 to 5.3 V	AV–		V_{DD}	V
	AV–	AV–: V_{DD} = 4.7 to 5.3 V	V_{SS}		AV+	
Reference input current range	IRIF	AV+, AV–: AV+ = V_{DD}, V_{DD} = 4.7 to 5.3 V, AV– = V_{SS}	75	150	300	μA
Analog input voltage range	VAIN	AD0 to AD7: V_{DD} = 4.7 to 5.3 V	AV–		AV+	V
Analog port input current	IAIN	Port pins AD0 to AD7 Including output OFF leakage current. VAIN = V_{DD}, V_{DD}= 4.7 to 5.3 V			1	μA
		Port pins AD0 to AD7 VAIN = V_{SS}, V_{DD}= 4.7 to 5.3 V	–1			
[Watchdog timer]						
Guaranteed constant*7	Cw	WDR: V_{DD} = 3 to 6 V		0.1 ± 5%		μF
	Rw	WDR: V_{DD} = 3 to 6 V		680 ± 1%		kΩ
	RI	WDR: V_{DD} = 3 to 6 V		100 ± 1%		Ω
Clear time (discharge)	tWCT	WDR: Fig. 8, V_{DD} = 3 to 6 V	100			μs
Clear time (charge)	tWCCY	WDR: Fig. 8, V_{DD} = 3 to 6 V	36			ms
Guaranteed constant*7	Cw	WDR: V_{DD} = 4 to 6 V		0.047 ± 5%		μF
	Rw	WDR: V_{DD} = 4 to 6 V		680 ± 1%		kΩ
	RI	WDR: V_{DD} = 4 to 6 V		100 ± 1%		Ω
Clear time (discharge)	tWCT	WDR: Fig. 8, V_{DD} = 4 to 6 V	40			μs
Clear time (charge)	tWCCY	WDR: Fig. 8, V_{DD} = 4 to 6 V	18			ms

Note: 1. The LC65E1104 will accept input voltages up to the generated oscillator amplitude if the oscillator circuit in figure 4 with circuit constants in the guaranteed constants ranges is driven from within the IC.
2. Average over a 100 ms period
3. The operating supply voltage V_{DD} must be held until standby mode is enterd after the execution of a HALT instruction. The PA3 pin must be free from chattering during the HALT instruction cycle.
4. The OSC1 pin input circuit has Schmitt trigger characteristics when the 2-terminal RC oscillator option or the external clock oscillator option is selected.
5. fCFOSC: oscillator frequency. The center frequency of a ceramic oscillator has a tolerance range of about 1% around the nominal value specified by the manufacturer of the oscillator element. For details, refer to the specifications of the ceramic resonator.
6. TCYC = 4 × system clock period
7. If the LC65E1104 is used in an environment subject to condensation, leakage between PE1 and adjacent pins and leakage associated with external RCA circuits require special attention.



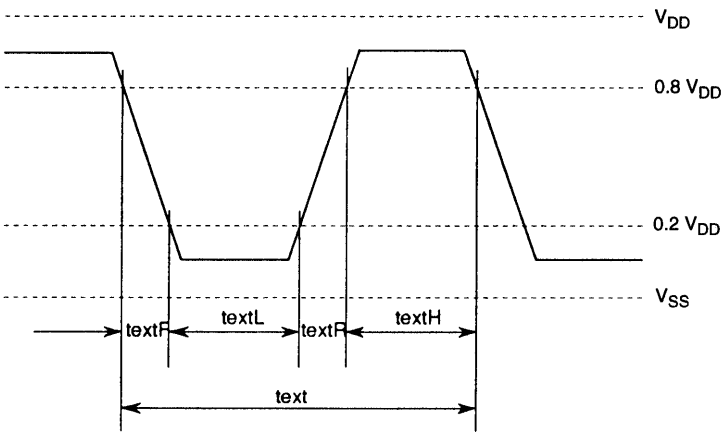


Fig. 1 External Clock Input Waveform

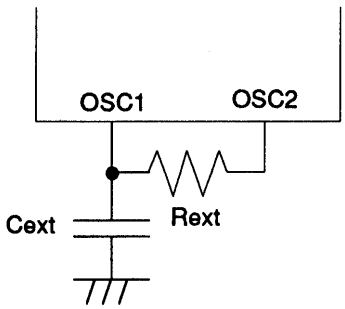


Fig. 2 2-pin RC Oscillator Circuit

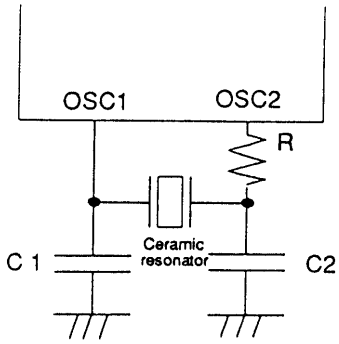


Fig. 3 Ceramic Oscillator

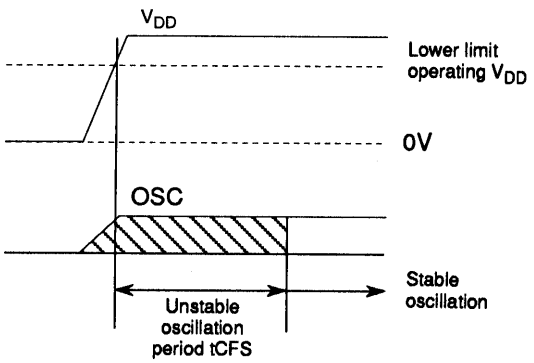


Fig. 4 Oscillator Stabilization Period

Table 1 Constants Guaranteed for Ceramic Resonator Oscillator

4 MHz (Murata) CSA4.00MG CST4.00MGW (built-in C)	C1	33 pF ± 10%
	C2	33 pF ± 10%
	R	0 Ω
4 MHz (Kyocera) KBR4.0 MSA KBR4.0MKS (built-in C)	C1	33 pF ± 10%
	C2	33 pF ± 10%
	R	0 Ω
1 MHz (Murata) CSB1000J	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	2.2 kΩ
1 MHz (Kyocera) KBR1000F	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	0 kΩ
800 kHz (Murata) CSB800J	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	2.2 kΩ
800 kHz (Kyocera) KBR800F	C1	220 pF ± 10%
	C2	220 pF ± 10%
	R	0 kΩ
400 kHz (Murata) CSB400P	C1	220 pF ± 10%
	C2	220 pF ± 10%
	R	2.2 kΩ
400 kHz (Kyocera) KBR400BK	C1	330 pF ± 10%
	C2	330 pF ± 10%
	R	0 kΩ

Note: The constants above are preliminarlly. Final ratings will be fixed after evaluation.

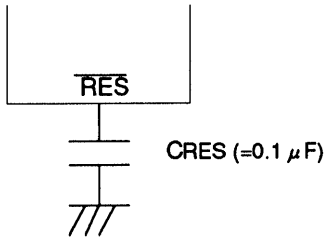


Fig. 5 Reset Circuit

Note: When the rise time of the power supply is close to 0, the reset time will be between 10 and 100 ms for a CRES of 0.5 μF. If the rise time of the power supply is significantly longer, the value of CRES must be increased so that the reset time will be 10 ms or longer.

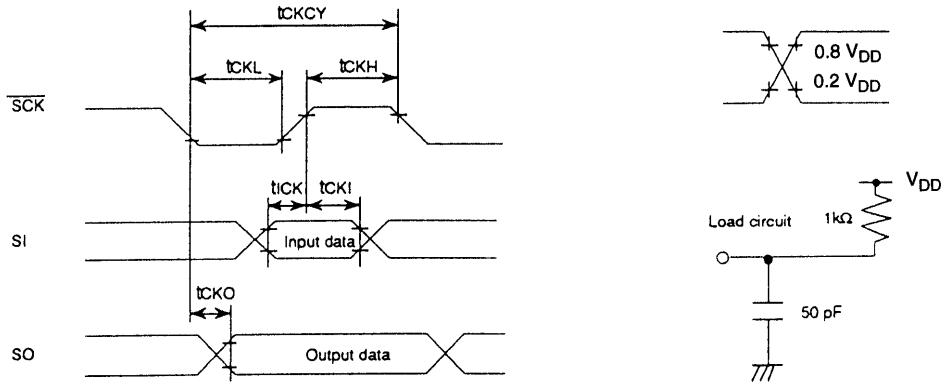
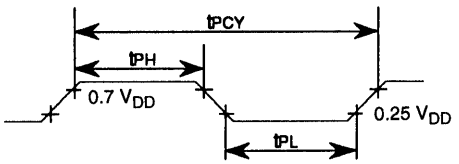
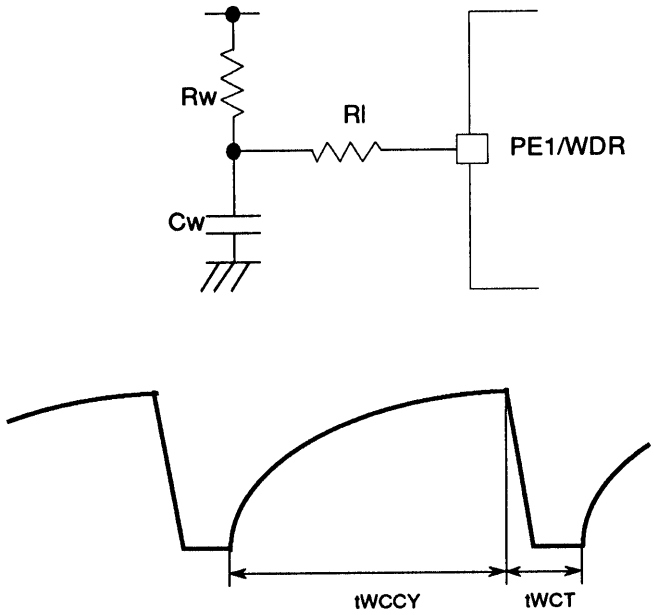


Fig. 6 Serial Input /Output Timing



The load conditions are the same as in Fig. 6.

Fig. 7 Pulse Output Timing at Port PE0



Note: 1. tWCCT: The charge time due to the time constant of the external Cw, Rw, and R1 components
2. tWCT: The discharge time due to program operation

Fig. 8 Watchdog Timer Waveform

For LC651104F, 651102F

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
Output voltage	V_O	OSC2	Allowable up to the generated voltage	V
Input voltage	V_I1	OSC1*1	–0.3 to V_{DD} + 0.3	V
	V_I2	TEST, $\overline{RES}$, AV+, AV–	–0.3 to V_{DD} + 0.3	V
Input/output voltage	V_{IO}1	PC0 to PC3, PD0 to PD3, PE0, PE1, PF0 to PF3	–0.3 to +15	V
	V_{IO}2	PA0 to PA3, PG0 to PG3	–0.3 to V_{DD} + 0.3	V
Peak output current	I_{OP}	I/O port	–2 to +20	mA
Average output current	I_{OA}	I/O port: Per pin over a 100 ms period	–2 to +20	mA
	ΣI_{OA}1	PC0 to PC3, PD0 to PD3, PE0, PE1:Total current for PC0 to PC3, PD0 to PD3, and PE0, PE1*2	–15 to +100	mA
	ΣI_{OA}2	PF0 to PF3, PG0 to PG3, PA0 to PA3: Total current for PF0 to PF3, PG0 to PG3, and PA0, PA3*2	–15 to +100	mA
Allowable power dissipation	Pd max1	Ta = +10 to +40°C (DIC package)	250	mW
	Pd max2	Ta = +10 to +40°C (MFC package)	150	mW
Operating temperature	Topr		+10 to +40	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Conditions at Ta = +10 to +40°C, V_{SS} = 0 V, V_{DD} = 4.0 to 6.0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage	V_{DD}	V_{DD}	4.0		6.0	V
Standby supply voltage	VST	V_{DD}: RAM, register hold*3	1.8		6.0	V
High-level input voltage	V_{IH}1	Port C, D, E, F: Output Nch Tr. OFF	0.7 V_{DD}		+13.5	V
	V_{IH}2	Port A, G: Output Nch Tr. OFF	0.7 V_{DD}		V_{DD}	V
	V_{IH}3	$\overline{INT}$, $\overline{SCK}$, SI: Output Nch Tr. OFF	0.8 V_{DD}		+13.5	V
	V_{IH}4	$\overline{RES}$: V_{DD} = 1.8 to 6.0 V	0.8 V_{DD}		V_{DD}	V
	V_{IH}5	OSC1: External clock mode	0.8 V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL}1	Port: Output Nch Tr. OFF	V_{SS}		0.3 V_{DD}	V
	V_{IL}2	$\overline{INT}$, $\overline{SCK}$, SI: Output Nch Tr. OFF	V_{SS}		0.25 V_{DD}	V
	V_{IL}3	OSC1: External clock	V_{SS}		0.25 V_{DD}	V
	V_{IL}4	TEST	V_{SS}		0.3 V_{DD}	V
	V_{IL}5	$\overline{RES}$	V_{SS}		0.25 V_{DD}	V
Operating frequency (cycle time)	fOP (Tcyc)		200 (20)		4330 (0.92)	kHz (µs)
[External clock conditions]						
Frequency	text		200		4330	kHz
Pulse width	textH, textL	OSC1: Fig. 1	69			ns
Rise/fall time	textR, textF	OSC1: Fig. 1			50	ns
Oscillation guaranteed constants ceramic resonator oscillator		Fig. 2	See Table 1			

Electrical Characteristics at Ta = +10 to +40°C, V_{SS} = 0 V, V_{DD} = 4.0 to 6.0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level input current	$I_{IH}1$	Port C, D, E, F: Output Nch Tr. OFF, (Including the Nch. transistor off state leakage current.), V_{IN} = +13.5			+5.0	µA
	$I_{IH}2$	Port A, G: Output Nch Tr. OFF, (Including the Nch. transistor off state leakage current.), $V_{IN} = V_{DD}$			+5.0	µA
	$I_{IH}3$	OSC1: External clock mode, $V_{IN} = V_{DD}$			+1.0	µA
Low-level input current	$I_{IL}1$	Port of OD type: Output Nch Tr. OFF, $V_{IN} = V_{SS}$	–1.0			µA
	$I_{IL}2$	$\overline{RES}$: $V_{IN} = V_{SS}$	–150	–50		µA
	$I_{IL}3$	OSC1: External clock mode, $V_{IN} = V_{SS}$	–1.0			µA
Low-level output voltage	$V_{OL}1$	Port: I_{OL} = 10 mA			1.5	V
	$V_{OL}2$	Port: I_{OL} = 1 mA, I_{OL} of each port; 1 mA or less			0.5	V
[Schmitt characteristics]						
Hysteresis voltage	VHIS			0.1 V_{DD}		V
High-level threshold voltage	VtH	$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, SI, OSC1 of Schmitt type*4	0.4 V_{DD}		0.8 V_{DD}	V
Low-level threshold voltage	VtL		0.25 V_{DD}		0.6 V_{DD}	V
[Current drain]						
Ceramic resonator oscillator	IDDOP1	V_{DD}: Fig. 2, 4 MHz, 200 kHz to 4330 kHz* Note: * Output Nch Tr. OFF at operating mode, port = V_{DD}		5	8	mA
External clock	IDDOP2			5	8	mA
Standby mode	IDDst	V_{DD}: Output Nch Tr. OFF, V_{DD} = 6 V		0.05	10	µA
		V_{DD}: Port = V_{DD}, V_{DD} = 3 V		0.025	5	µA
[Oscillator characteristics]						
Ceramic resonator oscillator	fCFOSC	OSC1, OSC2: Fig.2, fo = 4 MHz*5	3840	4000	4160	kHz
Frequency stabilization time	tCFS	Fig. 3, fo = 4 MHz			10	ms
[Pull-up resistance]						
I/O port $\overline{RES}$	RU	$\overline{RES}$: $V_{IN} = V_{SS}$, V_{DD} = 5 V	50	100	250	kΩ
[External reset characteristics]						
Reset time	tRST			See Fig. 4		
Pin capacitance	C_P	f = 1 MHz. $V_{IN} = V_{SS}$ for all pins other than those being tested.		10		pF
[Serial clock]						
Input clock cycle time	tCKCY1	$\overline{SCK}$: Fig. 5	2.0			µs
Output clock cycle time	tCKCY2	$\overline{SCK}$: Fig. 5		64 × tCYC*6		µs
Input clock low-level pulse width	tCKL1	$\overline{SCK}$: Fig. 5	0.6			µs
Output clock low-level pulse width	tCKL2	$\overline{SCK}$: Fig. 5		32 × tCYC		µs
Input clock high-level pulse width	tCKH1	$\overline{SCK}$: Fig. 5	0.6			µs
Output clock high-level pulse width	tCKH2	$\overline{SCK}$: Fig. 5		32 × tCYC		µs
[Serial input]						
Data setup time	tICK	SI: Specified from the rising edge of SCK. Fig. 5	0.2			µs
Data hold time	tCKI		0.2			µs
[Serial output]						
Output delay time	tCKO	SO: Specified from the falling edge of $\overline{SCK}$. Nch OD only, external 1 kΩ, external 50 pF, Fig.5			0.4	µs
[Pulse output]						
Period	tPCY	PE0: Fig. 6, tCYC = 4 × system clock period, Nch OD only, external 1 kΩ, external 50 pF		64 × tCYC		µs
High-level pulse width	tPH			32 × tCYC ± 10%		µs
Low-level pulse width	tPL			32 × tCYC ± 10%		µs

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[AD conversion characteristics]						
Resolution		V_{DD} = 4.7 to 5.3 V		8		bits
Absolute accuracy		AV+ = V_{DD}, AV– = V_{SS}, V_{DD} = 4.7 to 5.3 V		±1	±2	LSB
Conversion time	tCAD	AD speed 1/1, at 26 × tCYC, V_{DD} = 4.7 to 5.3 V	25 (tCYC = 0.98 µs)		312 (tCYC = 12 µs)	µs
		AD speed 1/2, at 51 × tCYC, V_{DD} = 4.7 to 5.3 V	50 (tCYC = 0.98 µs)		612 (tCYC = 12 µs)	µs
Reference input voltage	AV+	AV+: V_{DD} = 4.7 to 5.3 V	AV–		V_{DD}	V
	AV–	AV–: V_{DD} = 4.7 to 5.3 V	V_{SS}		AV+	
Reference input current range	IRIF	AV+, AV–: AV+ = V_{DD}, V_{DD} = 4.7 to 5.3 V, AV– = V_{SS}	75	150	300	µA
Analog input voltage range	VAIN	AD0 to AD7: V_{DD} = 4.7 to 5.3 V	AV–		AV+	V
Analog port input current	IAIN	Port pins AD0 to AD7 Including output OFF leakage current. VAIN = V_{DD}, V_{DD}= 4.7 to 5.3 V			1	µA
		Port pins AD0 to AD7 VAIN = V_{SS}, V_{DD}= 4.7 to 5.3 V	–1			
[Watchdog timer]						
Guaranteed constants	Cw	WDR		0.01 ± 5%		µF
	Rw	WDR		680 ± 1%		kΩ
	RI	WDR		100 ± 1%		Ω
Clear time (discharge)	tWCT	WDR: Fig. 7	10			µs
Clear time (charge)	tWCCY	WDR: Fig. 7	42			ms

Note: 1. The LC65E1104 will accept input voltages up to the generated oscillator amplitude if the oscillator circuit in figure 2 with circuit constants in the guaranteed constants ranges is driven internally.
2. Average over a period of 100 ms.
3. The operating supply voltage V_{DD} must be held until standby mode is entered after the execution of a HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.
4. The OSC1 pin input circuit has Schmitt trigger characteristics when the external clock oscillator option is selected.
5. fCFOSC: Oscillator frequency
6. TCYC = 4 × system clock period
7. If the LC65E1104 is used in an environment subject to condensation, leakage between PE1 and adjacent pins and leakage associated with external RCA circuits require special attention.

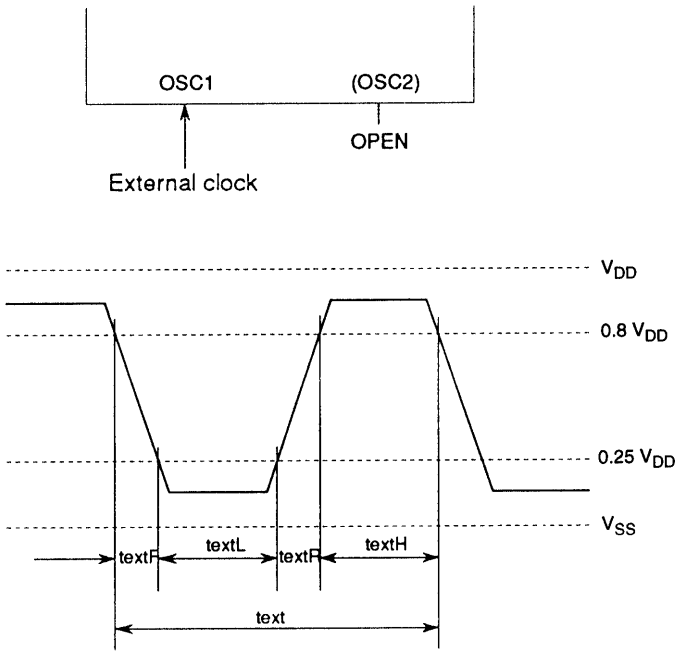


Fig. 1 External Clock Input Waveform

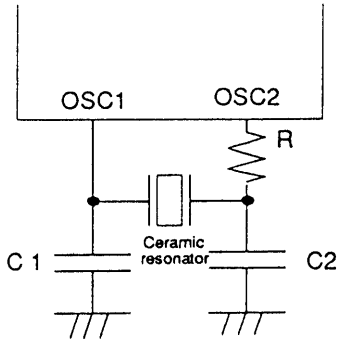


Fig. 2 Ceramic Oscillator Circuit

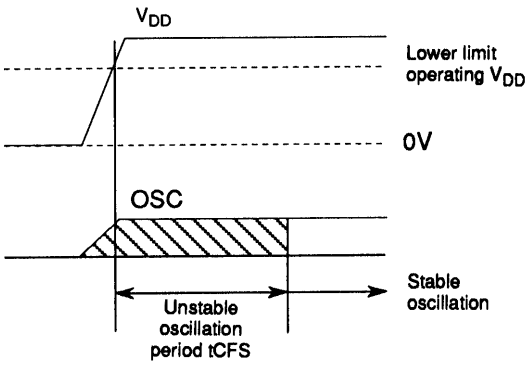


Fig. 3 Oscillator Stabilization Period

Table 1 Constants Guaranteed for Ceramic Resonator Oscillator

4 MHz (Murata) CSA4.00MG CST4.00MGW (built-in C)	C1	33 pF ± 10%
	C2	33 pF ± 10%
	R	0 Ω
4 MHz (Kyocera) KBR4.0 MSA KBR4.0MKS (built-in C)	C1	33 pF ± 10%
	C2	33 pF ± 10%
	R	0 Ω

Note: The constants above are preliminarlly. Final ratings will be fixed after evaluation.

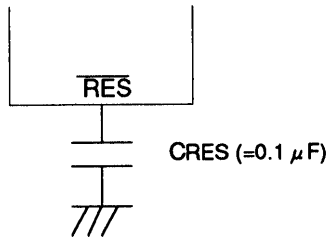


Fig. 4 Reset Circuit

Note: When the rise time of the power supply is close to 0, the reset time will be between 10 and 100 ms for a CRES of 0.5 μF. If the rise time of the power supply is significantly longer, the value of CRES must be increased so that the reset time will be 10 ms or longer.

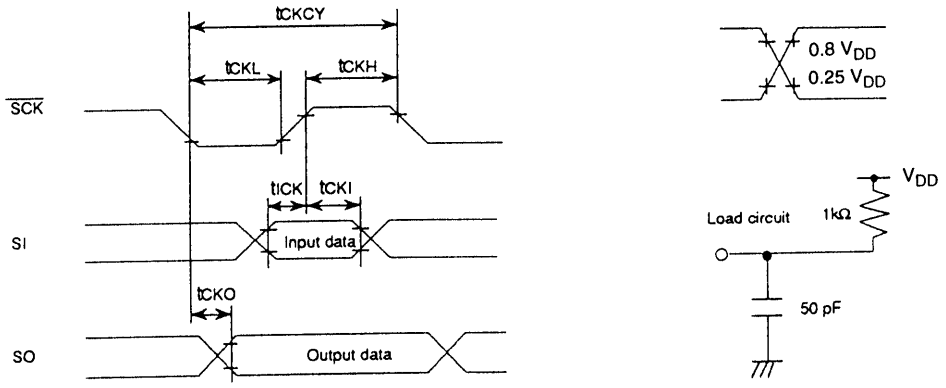
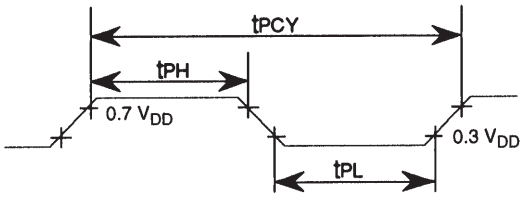
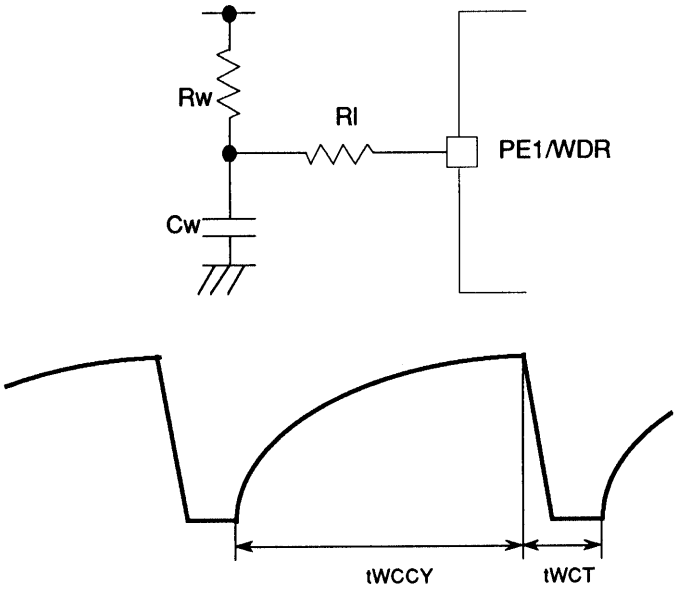


Fig. 5 Serial Input /Output Timing



The load conditions are the same as in Figure 5.

Fig. 6 Pulse Output Timing at Port PE0



Note: 1. tWCCY: The charge time due to the time constant of the external Cw, Rw, and R1 components
2. tWCT: The discharge time due to program operation

Fig. 7 Watchdog Timer Waveform

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