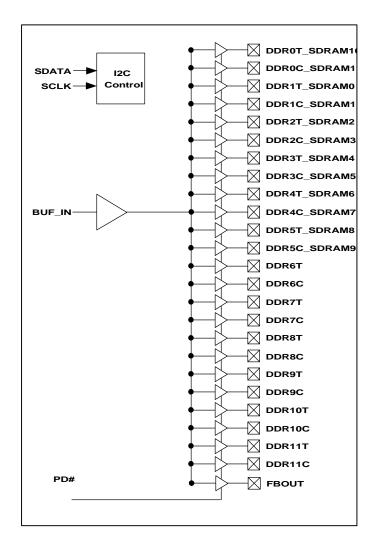


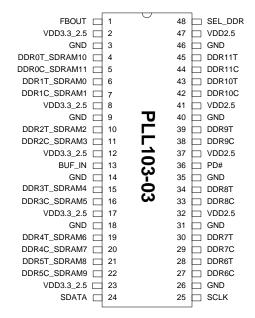
FEATURES

- Generates 24-output buffers from one input.
- Supports up to 4 DDR DIMMS or 3 SDR DIMMS and 2 DDR DIMMS.
- Supports 266MHz DDR SDRAM.
- One additional output for feedback.
- Less than 5ns delay.
- Skew between any outputs is less than 100 ps.
- 2.5V or 3.3V Supply range.
- Enhanced DDR and SDRAM Output Drive selected by I2C.
- Available in 48 pin SSOP.

BLOCK DIAGRAM



PIN CONFIGURATION



Note: #: Active Low

DESCRIPTIONS

The PLL103-03 is designed as a 3.3V/2.5V buffer to distribute high-speed clocks in PC applications. The device has 24 outputs. These outputs can be configured to support four unbuffered DDR (Double Data Rate) DIMMS or to support 2 unbuffered standard SDR (Single Data Rate) DIMMS and 2 DDR DIMMS. The PLL103-03 can be used in conjunction with the PLL202-04 or similar clock synthesizer for the VIA Pro 266 chipset.

The PLL103-03 also has an I2C interface, which can enable or disable each output clock. When power up, all output clocks are enabled (has internal pull up).



PIN DESCRIPTIONS

Name	Number	Туре	Description
FBOUT	1	0	Feedback clock for chipset. Output voltage depends on VDD3.3_2.5V.
BUF_IN	13	I	Reference input from chipset. 3.3V input for STANDARD SDRAM mode; 2.5V input for DDR-ONLY mode.
PD	36	I	Power Down Control input. When low, it will tri-state all outputs.
SEL_DDR	48	I	Input configure for DDR-ONLY mode or STANDARD SDR mode. 1 = DDR-ONLY mode (when VDD3.3_2.5 select 2.5V); 0 = SDR mode (when VDD3.3_2.5 select 3.3V). In DDR-ONLY mode, all outputs will be configured as DDR outputs. In STANDARD SDR mode, pin 4, 5, 6, 7, 10, 11, 15, 16, 19, 20, 21 and 22 will be configured as STANDARD SDR outputs, and pin 27, 28, 29, 30, 33, 34, 38, 39, 42, 43, 44 and 45 will be configured as DDR outputs.
DDR[6:11]T	28,30,34, 39,43,45	0	These outputs provide True copies of BUF_IN.
DDR[6:11]C	27,29,33, 38,42,44	0	These outputs provide complementary copies of BUF_IN.
DDR[0,1:5]T_SDRA M [10,0,2,4,6,8]	4,6,10,15,19 , 21	0	When SEL_DDR=1, these outputs provide DDR mode outputs; when SEL_DDR=0, these outputs provide standard SDRAM mode outputs. Voltage swing depends on VDD3.3_2.5.
DDR[0,1:5]C_SDRA M [11,1,3,5,7,9]	5,7,11,16,20 , 22	0	When SEL_DDR=1, these outputs provide complementary copies of BUF_IN; when SEL_DDR=0, these outputs provide standard SDRAM mode outputs. Voltage swing depends on VDD3.3_2.5.
VDD3.3_2.5	2,8,12,17,23	Р	When VDD=2.5V, SEL_DDR=1. DDR-ONLY mode is selected; when VDD=3.3V, SEL_DDR=0. STANDARD SDRAM mode is selected.
VDD2.5	32,37,41,47	Р	2.5V power supply.
GND	3,9,14,18,26	Р	Ground.



12C BUS CONFIGURATION SETTING

Address Assignment	A6	A5	A4	А3	A2	A1	Α0	R/W	
Address Assignment	1	1	0	1	0	0	1	_	
Slave Receiver/Transmitter	Provid	les both s	ave write	and readb	ack functi	onality			
Data Transfer Rate	Stand	ard mode	at 100kbi	:s/s					
Data Protocol	bytes must t termin	must be a be followe ate the tra	ccessed i d by 1 ack ansfer. Th	n sequenti knowledge e write or	al order fro bit. A byte	om lowest e transferre s both begi	to highest ed without ins with the	I from the con byte. Each by acknowledged master send	yte transferred d bit will
Following the acknowledge of this address byte, in Write Mode: the Command Byte are Count Byte must be sent by the master but ignored by the slave, in Read Mode: the Count Byte will be read by the master then all other Data Byte. Byte Count Byte defendance of the power-up is = (0x09).						de: the Byte			

12C CONTROL REGISTERS

1. BYTE 6: Outputs Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description		
Bit 7	48	1	SEL_DDR (I2C is ready only, value is set through pin48)		
Bit 6	-	0	Enhanced SDRAM Drive. 1 = Enhanced 25%		
Bit 5	-	0	Enhanced DDR Drive. 1 = Enhanced 25%		
Bit 4	-	0	Reserved		
Bit 3	45, 44	1	DDR11T, DDR11C		
Bit 2	43, 42	1	DDR10T, DDR10C		
Bit 1	39, 38	1	DDR9T, DDR9C		
Bit 0	34, 33	1	DDR8T, DDR8C		



2. BYTE 7: Outputs Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	30, 29	1	DDR7T, DDR7C
Bit 6	28, 27	1	DDR6T, DDR6C
Bit 5	21, 22	1	DDR5T_SDRAM8, DDR5C_SDRAM9
Bit 4	19, 20	1	DDR4T_SDRAM6, DDR4C_SDRAM7
Bit 3	15, 16	1	DDR3T_SDRAM4, DDR3C_SDRAM5
Bit 2	10, 11	1	DDR2T_SDRAM2, DDR2C_SDRAM3
Bit 1	6, 7	1	DDR1T_SDRAM0, DDR1C_SDRAM1
Bit 0	4, 5	1	DDR0T_SDRAM10, DDR0C_SDRAM11



ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V _{DD}	V _{SS} -0.5	7.0	V
Input Voltage, dc	Vı	Vss-0.5	V _{DD} +0.5	V
Output Voltage, dc	Vo	Vss-0.5	V _{DD} +0.5	V
Storage Temperature	T _S	-65	150	°C
Ambient Operating Temperature	TA	0	70	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. Operating Conditions

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V _{DD3.3}	3.135	3.465	V
Supply Voltage	V _{DD2.5}	2.375	2.625	V
Input Capacitance	Cin		5	pF
Output Capacitance	Соит		6	pF

3. Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	ViH	All Inputs except I2C	2.0		V _{DD} +0.3	V
Input Low Voltage	V _{IL}	All inputs except I2C	Vss-0.3		0.8	V
Input High Current	Іін	V _{IN} = V _{DD}			TBM	uA
Input Low Current	IJ	V _{IN} = 0			TBM	uA
Output High Voltage	Voh	IOL = -12mA, VDD = 2.375V	1.7			V
Output Low Voltage	VoL	IOL = 12mA, VDD = 2.375V			0.6	V
Output High Current	Іон	VDD = 2.375V, VOUT=1V	-18	-32		mA
Output Low Current	loL	VDD = 2.375V, VOUT=1.2V	26	35		mA

Note: TBM: To be measured



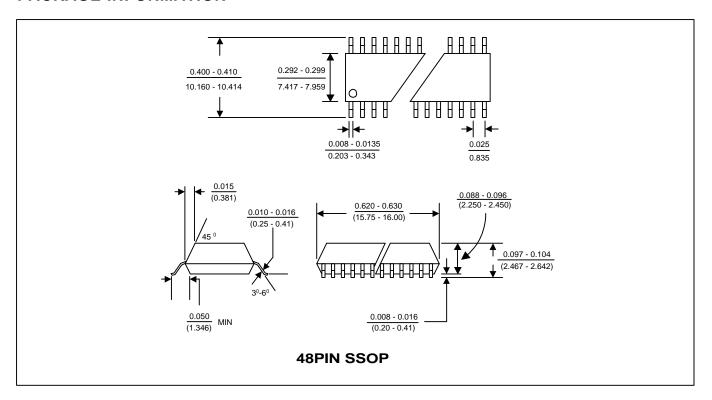
3. Electrical Specifications (Continued)

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (DDR-only mode)	I _{DD}	Unloaded outputs, 133MHz			ТВМ	mA
Supply Current (SDRAM mode)	I _{DD}	Unloaded outputs, 133MHz			ТВМ	mA
Supply Current	I _{DDS}	PD = 0			TBM	mA
Output Crossing Voltage	Voc		(VDD/2) -0.1	VDD/2	(VDD/2)+ 0.1	V
Output Voltage Swing	Vouт		1.1		VDD-0.4	V
Duty Cycle	D _T	Measured @ 1.5V	45	50	55	%
Max. Operating Frequency			66		170	MHz
Rising Edge Rate	Tor	Measured @ 0.4V ~ 2.4V	1.0	1.5	2.0	V/ns
Falling Edge Rate	T _{OF}	Measured @ 2.4V ~ 0.4V	1.0	1.5	2.0	V/ns
Clock Skew (pin to pin)	Tskew	All outputs equally loaded			100	ps
Stabilization Time	T _{ST}				0.1	ms

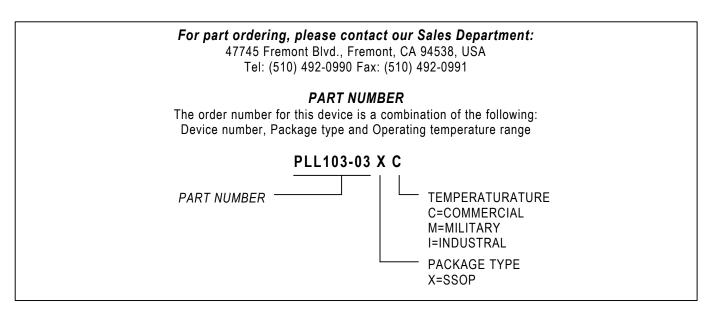
Note: TBM: To be measured



PACKAGE INFORMATION



ORDERING INFORMATION



PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by PhaseLink is believed to be accurate and reliable. However, PhaseLink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

LIFE SUPPORT POLICY: PhaseLink s products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of PhaseLink Corporation.