

# 2M x 8 SRAM MODULE

### SYS82000RKXC - 70/85/10/12

Issue 1.3: April 2001

### Description

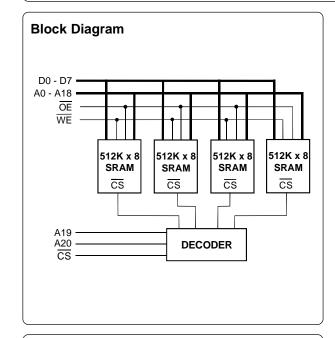
The SYS82000RKXC is a plastic 16Mbit Static RAM Module housed in a standard 38 pin Single In-Line package organised as 2M x 8 with access times of 85,100, or 120 ns.

The module is constructed using four 512Kx8 SRAMs in TSOPII packages mounted onto an FR4 epoxy substrate. This offers an extremely high PCB packing density.

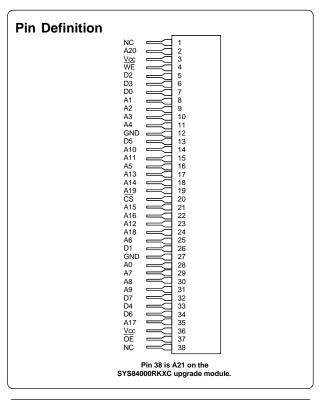
The device is offered in standard and low power versions, with the -L module having a low voltage data retention mode for battery backed applications.

#### **Features**

- Access Times of 85/100/120 ns.
- Low Power Disapation:
  Operating 600 mW (Max.)
  Standby-L Version 1.1 mW (Max.)
- 5 Volt Supply ± 10%.
- · Completely Static Operation.
- Low Voltage V<sub>CC</sub> Data Retention.
- On-board Decoding & Decoupling Capacitors.
- 38 Pin Single-In-Line package (SIP).
- Upgrade path to SYS84000RKXC (32Mbits).



#### **Pin Functions** Address Inputs A0 ~ A20 D0 ~ D7 Data Input/Output Chip Select CS WE Write Enable OE Output Enable NC No Connect Power (+5V) V<sub>cc</sub> Ground **GND**



## **Package Details**

Plastic 38 pin Single-In-Line (SIP)

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## **DC OPERATING CONDITIONS**

Absolute Maximum Ratings (1)					
Parameter	Symbol	min	typ	max	unit
Voltage on any pin relative to V <sub>ss</sub>	V <sub>T</sub>	-0.3	-	+7	V
Power Dissipation	$P_{_T}$	-	-	4.0	W
Storage Temperature	$T_{STG}$	-55	-	+125	°C

### Notes:

(1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions							
Parameter	Symbol	min	typ	max	unit		
Supply Voltage	V <sub>cc</sub>	4.5	5.0	5.5	V		
Input High Voltage	V <sub>IH</sub>	2.2	-	Vcc+0.3	V		
Input Low Voltage	V <sub>IL</sub>	-0.3	-	0.8	V		
Operating Temperature	$T_{A}$	0	-	70	°C		
	$T_Al$	-40	-	85	°C (I)		

DC Electrical Characteristics (V <sub>CC</sub> =5V±10%) TA 0 to 70°C										
Parameter	Symbol	Test Condition	min	typ	max	Unit				
I/P Leakage Current	l <sub>u</sub>	$V_{IN} = GND$ to $V_{CC}$	-4	-	4	μΑ				
Output Leakage Current	I <sub>LO</sub>	$\overline{CS} = V_{IH}, V_{I/O} = GND \text{ to } V_{CC}$	-4	-	4	μΑ				
Operating Supply Current	I <sub>cc</sub>	$\overline{\text{CS}} = V_{IL}$ , min cycle, Duty = 100%	-	-	109	mΑ				
Standby Supply Current TTL levels	I <sub>SB1</sub>	$\overline{\text{CS}} = V_{\text{IH}}$	-	-	12	mΑ				
-L Version		$\overline{\text{CS}} = \text{V}_{\text{CC}} - 0.2 \text{V}, 0.2 > \text{V}_{\text{IN}} > \text{V}_{\text{CC}} - 0.2 \text{V}$	-	-	200	μΑ				
Output Low Voltage	$V_{OL}$	$I_{OL} = 2.1 \text{mA}$	-	-	0.4	V				
Output High Voltage	V <sub>OH</sub>	$I_{OH} = -1.0 \text{mA}$	2.4	-	-	V				

Capacitance (V <sub>CC</sub> =5V±10%,T <sub>A</sub> =25	Note: Capacitan	asured.			
Parameter	Symbol	Test Condition	typ	max	Unit
Input Capacitance (CS,A19,A20)	C <sub>IN1</sub>	V <sub>IN</sub> = 0V	-	8	pF
Input Capacitance (A0-18, OE, WE)	$C_{IN2}$	$V_{IN} = 0V$	-	32	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	-	10	pF

# **Operation Truth Table**

<u>cs</u>	ŌĒ	WE	DATA PINS	SUPPLY CURRENT	MODE
Н	Х	Х	High Impedance	I <sub>SB1</sub> , I <sub>SB2</sub>	Standby
L	L	Н	Data Out	I <sub>cc</sub>	Read
L	Х	L	Data In	I <sub>cc</sub>	Write
L	Н	Н	High Impedance	I <sub>CC</sub>	Output Disabled

Notes :  $H = V_{IH}$  :  $L = V_{IL}$  :  $X = V_{IH}$  or  $V_{IL}$ 

# **AC Test Conditions**

# **Output Load**

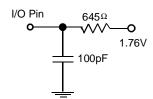
\* Input pulse levels: 0 V to 3.0V

\* Input rise and fall times: 5ns

\* Input and Output timing reference levels: 1.5V

\* Output load: see diagram

\*  $V_{CC} = 5V \pm 10\%$ 



# Low $V_{cc}$ Data Retention Characteristics - L Version Only ( $T_{OP} = 0$ °C to 70°C)

				-L Pai	rt		
Parameter	Symbol	Test Condition	min	typ	max	Unit	
V <sub>cc</sub> for Data Retention	$V_{DR}$	CS <sub>≥</sub> V <sub>cc</sub> -0.2V	2.0	-	-	V	
		$0.2V \ge V_{in} \ge V_{cc} - 0.2$					
Data Retention Current	I <sub>CCDR</sub>	$V_{cc} = 3.0V, \overline{CS} = V_{cc} - 0.2V, 0.2V \ge V_{in} \ge V_{cc} - 0.2V$	-	-	500	μΑ	
Chip Deselect to Data Ret. Tin	ne t <sub>CDR</sub>	See Retention Waveform	0	-	-	ns	
Operation Recovery Time	t <sub>p</sub>	See Retention Waveform	5	-	-	ms	

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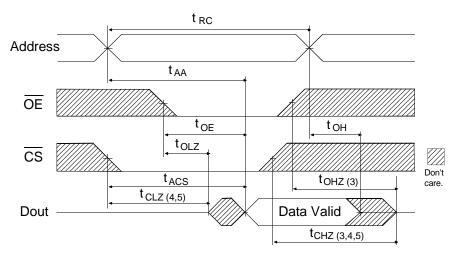
# **AC OPERATING CONDITIONS**

Read Cycle								
		-8	5	-1	10	-12	2	
Parameter	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	t <sub>RC</sub>	85	-	100	-	120	-	ns
Address Access Time	$t_{AA}$	-	85	-	100	-	120	ns
Chip Select Access Time	t <sub>ACS</sub>	-	85	-	100	-	120	ns
Output Enable to Output Valid	$t_{OE}$	-	45	-	50	-	55	ns
Output Hold from Address Change	$t_OH$	10	-	10	-	10	-	ns
Chip Selection to Output in Low Z	$t_{\scriptscriptstyle{CLZ}}$	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t <sub>oLZ</sub>	5	-	5	-	5	-	ns
Chip Deselection to O/P in High Z	t <sub>CHZ</sub>	0	30	0	35	0	40	ns
Output Disable to Output in High Z	$\mathbf{t}_{OHZ}$	0	30	0	35	0	40	ns

Write Cycle								
		-85		-10		-12		
Parameter	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	t <sub>wc</sub>	85	-	100	-	120	-	ns
Chip Selection to End of Write	t <sub>cw</sub>	75	-	80	-	100	-	ns
Address Setup Time	t <sub>AS</sub>	0	-	0	-	0	-	ns
Address Valid to End of Write	t <sub>AW</sub>	75	-	80	-	100	-	ns
Write Pulse Width	$t_{WP}$	65	-	70	-	80	-	ns
Write Recovery Time	$\mathbf{t}_{WR}$	5	-	5	-	5	-	ns
Write to Output in High Z	$\mathbf{t}_{WHZ}$	0	30	0	35	0	40	ns
Data to Write Time Overlap	$t_{DW}$	35	-	40	-	45	-	ns
Data Hold from Write Time	$t_{_{DH}}$	0	-	0	-	0	-	ns
Output active from end of write	t <sub>ow</sub>	5	-	5	-	5	-	ns

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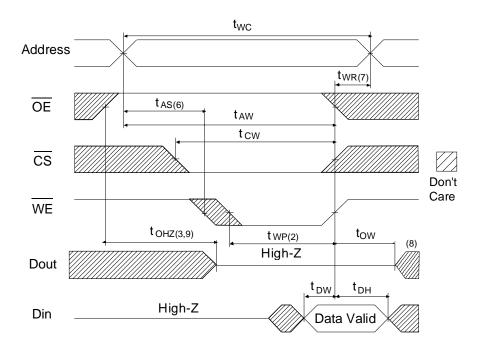
# Read Cycle Timing Waveform (1,2)



### **AC Read Characteristics Notes**

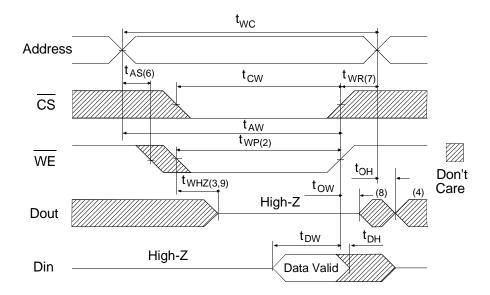
- (1) WE is High for Read Cycle.
- (2) All read cycle timing is referenced from the last valid address to the first transition address.
- (3) t<sub>CHZ</sub> and t<sub>OHZ</sub> are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.
- (4) At any given temperature and voltage condition,  $t_{CHZ}$  (max) is less than  $t_{CLZ}$  (min) both for a given module and from module to module.
- (5) These parameters are sampled and not 100% tested.

### Write Cycle No.1 Timing Waveform(1,4)



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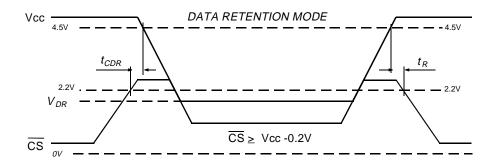
## Write Cycle No.2 Timing Waveform (1,5)



### **AC Write Characteristics Notes**

- (1) All write cycle timing is referenced from the last valid address to the first transition address.
- (2) All writes occur during the overlap of  $\overline{CS}$  and  $\overline{WE}$  low.
- (3) If  $\overline{OE}$ ,  $\overline{CS}$ , and  $\overline{WE}$  are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.
- (4) Dout is the Read data of the new address.
- (5)  $\overline{OE}$  is continuously low.
- (6) Address is valid prior to or coincident with  $\overline{CS}$  and  $\overline{WE}$  low, too avoid inadvertant writes.
- (7)  $\overline{\text{CS}}$  or  $\overline{\text{WE}}$  must be high during address transitions.
- (8) When  $\overline{CS}$  is low: I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.
- (9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

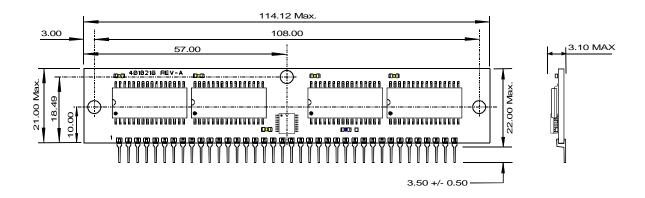
### **Data Retention Waveform**



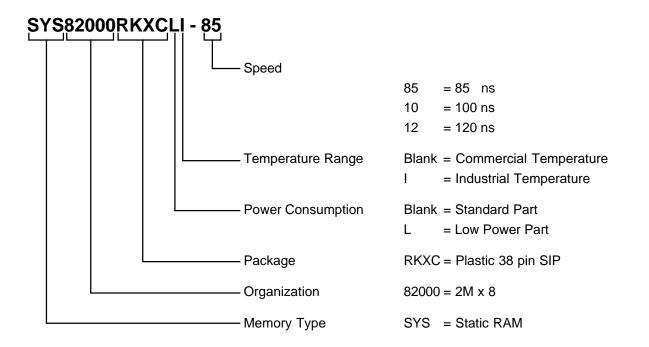
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Package Information Dimensions in mm

## Plastic 38 Pin Single-In-Line (SIP)



## **Ordering Information**



#### Note:

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Our products are subject to a constant process of development. Data may be changed at any time without notice. Products are not authorised for use as critical components in life support devices without the express written approval of a company director.