- **Drive Capability and Output Counts**
  - **80 mA (Current Sink) x 16 Bits**
- **Constant Current Output Range**
  - **5 to 80 mA (Current Value Setting for All Output Terminals Using External Resistor and Internal Brightness Control Register)**
- **Constant Current Accuracy**
  - **±4 % (Maximum Error Between Bits)**
- **Voltage Applied to Constant Current Output Terminals**
  - **Minimum 0.4 V (Output Current 5 mA to 40 mA)**
  - **Minimum 0.7 V (Output Current 40 mA to 80 mA)**
- **1024 Gray Scale Display**
  - **Pulse Width Control 1024 Steps**
- **Brightness Adjustment†**
  - **All Output Current Adjustment for 64 Steps (Adjustment for Brightness Deviation Between LED Modules)**
  - **Output Current Adjustment by Output (OUT0 to OUT15) for 128 Steps (Adjustment for Brightness Deviation Between Dots)**
  - **Brightness Control by 16 Steps Frequency Division Gray Scale Control Clock (Brightness Adjustment for Panel)**
- **Gray Scale Clock Generation**
  - **Gray Scale Control Clock Generation by Internal PLL or External Input Selectable**
- **Clock Invert/Noninvert Selectable at Cascade Operation**
  - **Clock Invert Selectable to Reduce Changes in Duty Ratio**
- **Protection**
  - **Watchdog Timer (WDT) Function (Turn Output Off When Scan Signal Stopped)**
  - **Thermal Shutdown (TSD) Function (Turn Output Off When Junction Temperature Exceeds Limit)**
- **LOD**
  - **LED Open Detection (Detection for LED Disconnection)**
- **Data Input/Output‡**
  - **Port A (for Data Display)**
  - **Clock Synchronized 10 Bit Parallel Input (Schmitt-Triggered Input)**
  - **Clock Synchronized 10 Bit Parallel Output (3-State Output)**
  - **Port B (for Dot Correction Data)**
  - **Clock Synchronized 7 Bit Parallel Input (Schmitt-Triggered Input)**
  - **Clock Synchronized 7 Bit Parallel Output**
- **Input/Output Signal Level**
  - **CMOS Level**
- **Power Supply Voltage**
  - **4.5 V to 5.5 V (Logic, Analog and Constant Current)**
  - **3 V to 5.5 V (Interface)**
- **Maximum Output Voltage . . . 15 V**
- **Data Transfer Rate . . . 20 MHz (Max)**
- **Gray Scale Clock Frequency**
  - **16 MHz (Max) Using Internal PLL**
  - **8 MHz (Max) Using External Clock**
- **Operating Free-Temperature Range −20°C to 85°C**
- **100-Pin Package HTQFP ($P_D$ = 4.7 W, $T_A$ = 25°C)**

† Adjustable for these functions independently.
‡ Allows to write all the data at port A by setting.



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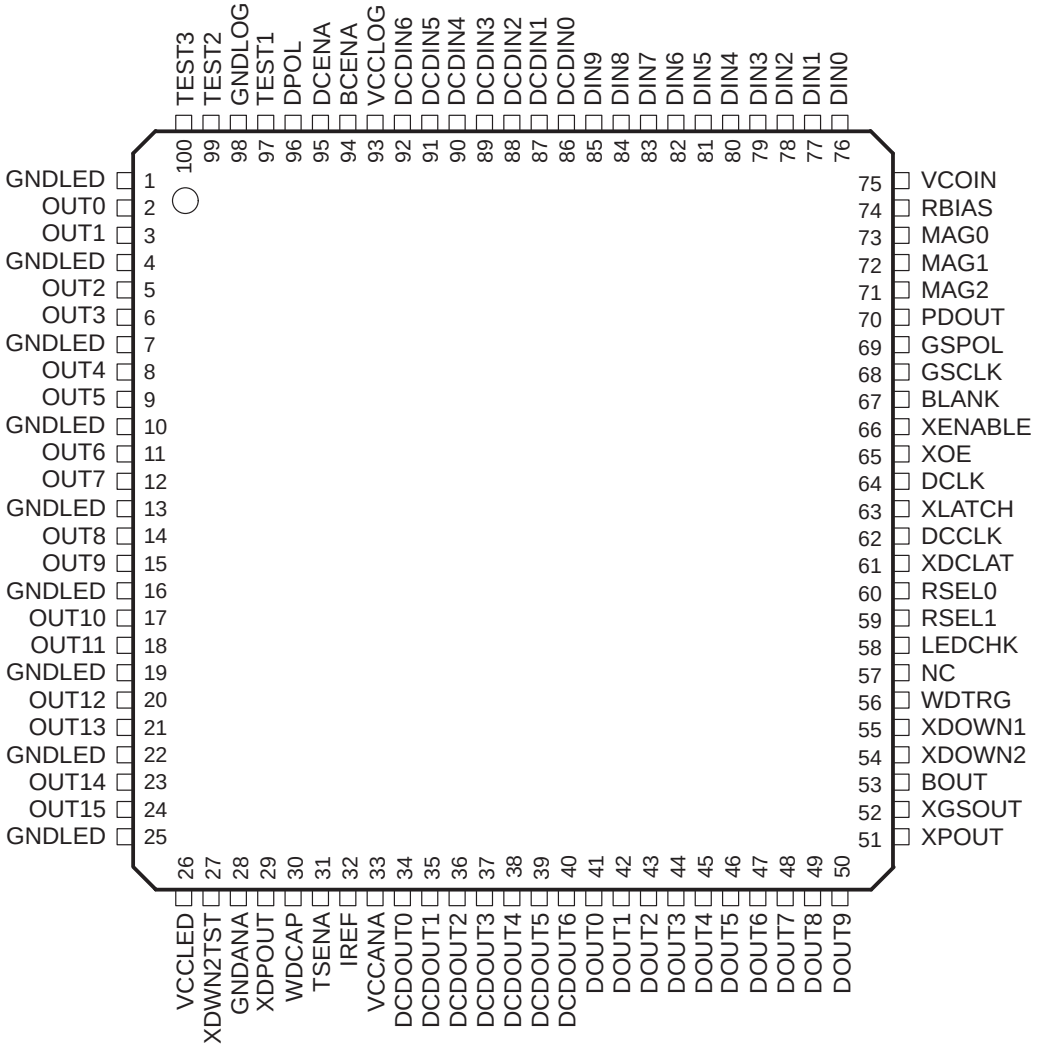
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## description

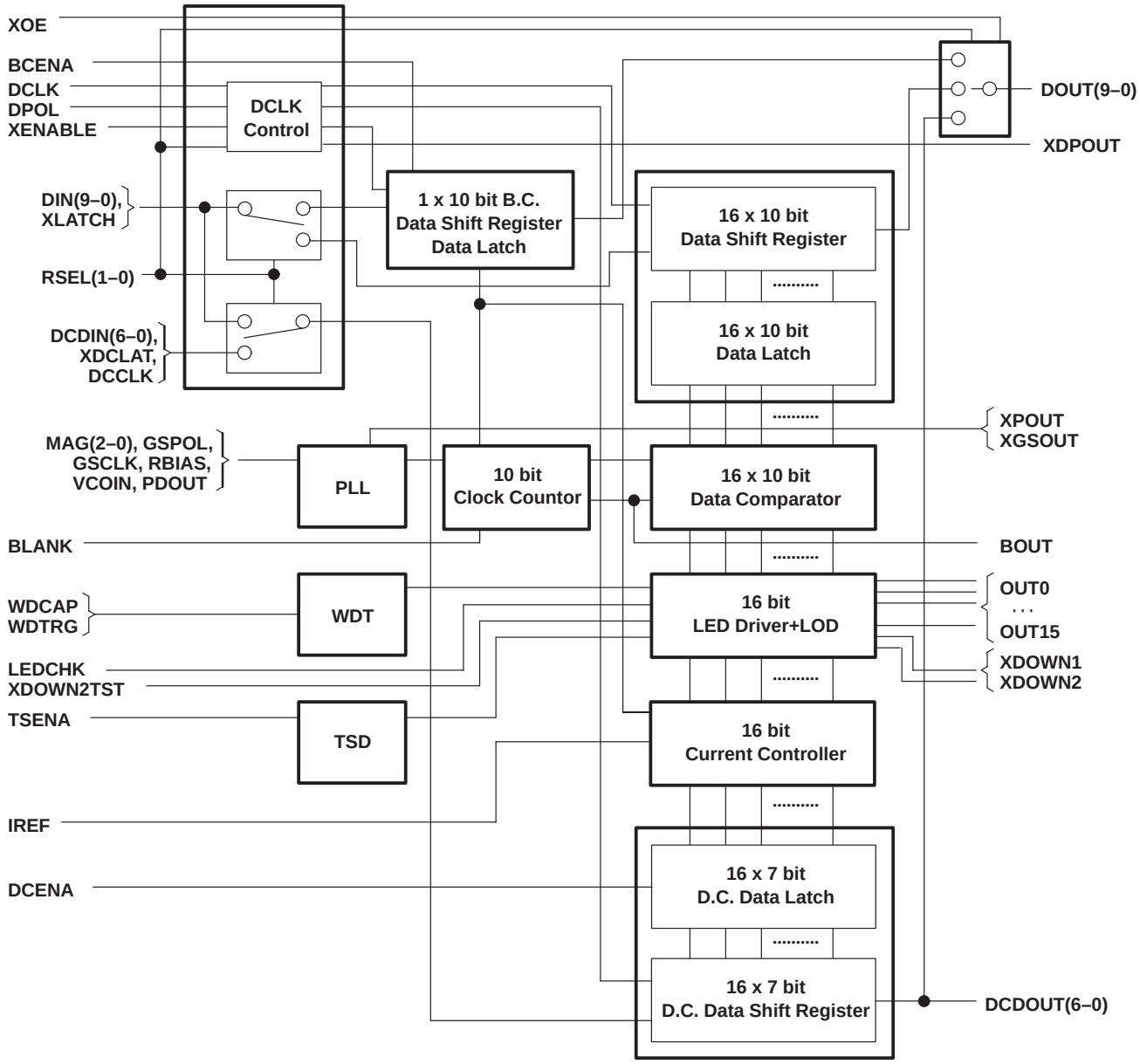
The TLC5911 is a constant current driver incorporating shift register, data latch, and constant current circuitry with a current value adjustable, PLL circuitry for gray scale control clock generation, and 1024 gray scale display using pulse width control. The output current is maximum 80 mA with 16 bits, and the current value of constant current output can be set by one external resistor. The device has two channel I/O ports. The brightness deviation between LED modules (ICs) can be adjusted by external data input from the display data port, and the brightness control for the panel can be accomplished by the brightness adjustment circuitry. Independent of these functions, the device incorporates the shift register and data latch to correct the deviation between LEDs by adjusting the output current using data from the dot correction data port. Moreover, the device incorporates WDT circuitry, which turns constant current output off when the scan signal stops during the dynamic scanning operation, and TSD circuitry, which turns constant current output off when the junction temperature exceeds the limit. Also the LED open detection (LOD) circuitry is used to make error signal output at the LED disconnection.

## pin assignments

**PZP PACKAGE**
**(TOP VIEW)**



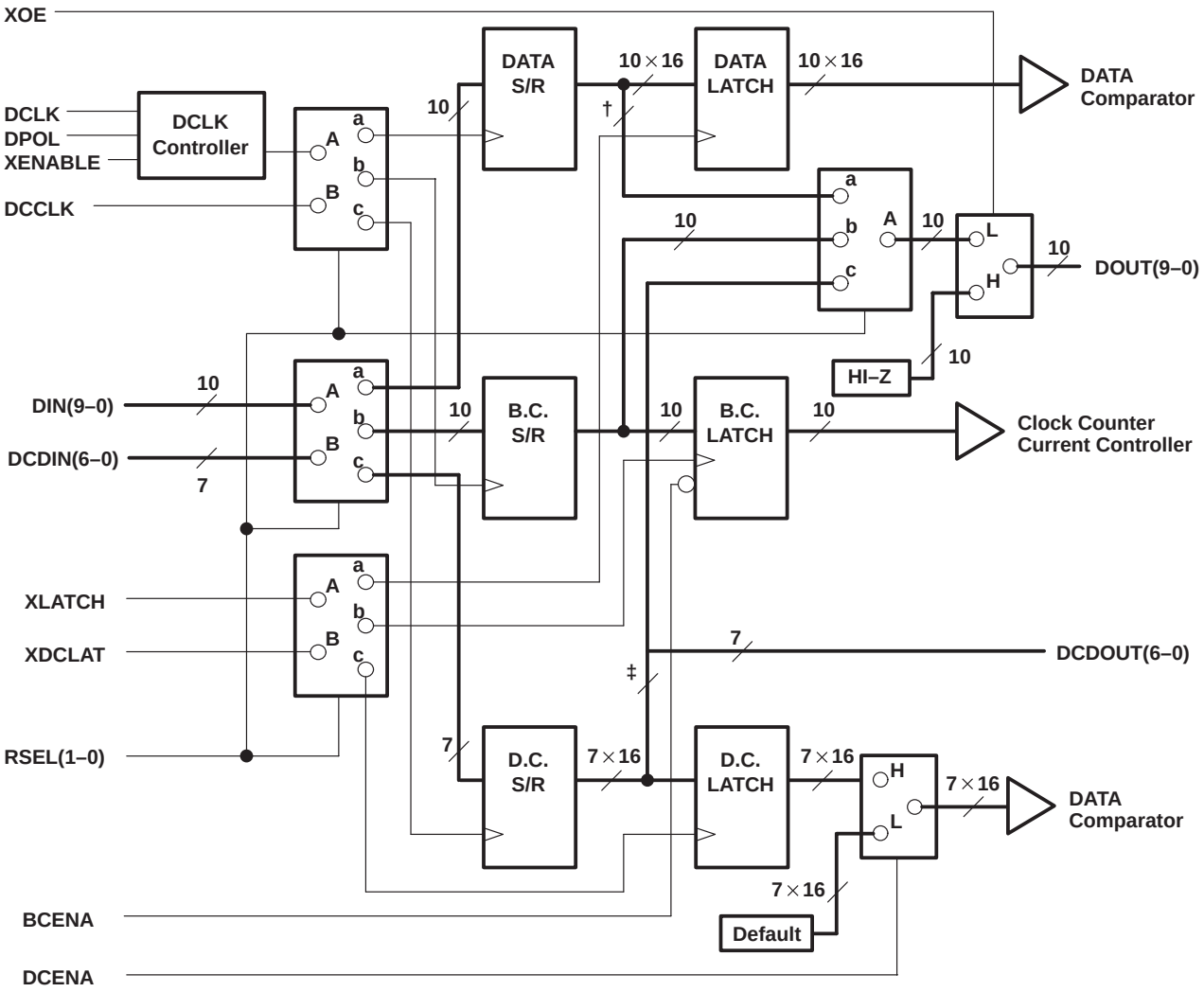
## functional block diagram




Legend:
B.C. (Brightness Control): Adjustment for brightness deviation between LED modules, and between panels.
D.C. (Dot Control): Adjustment for brightness deviation between dots.

NOTE: All the input terminals are with Schmitt triggered inverter except RBIAS, VCOIN, PDOUT, IREF and WDCAP.

## functional block diagram for shift register and data latch



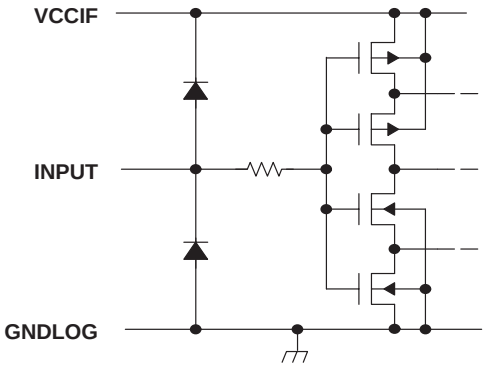

† Connecting to 16th 10-bit Bus
‡ Connecting to 16th 7-bit Bus

Legend:
B.C. (Brightness Control): Adjustment for brightness deviation between LED modules, and between panels.
D.C. (Dot Control): Adjustment for brightness deviation between dots.

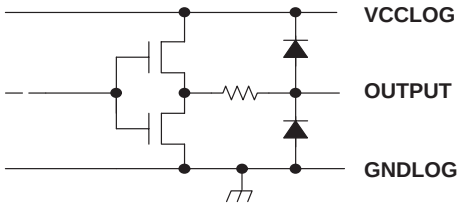
| RSEL | | CONNECTION |
|---|---|---|
| RSEL1 | RSEL0 | |
| L | L | A – a, B – c |
| L | H | A – b, B – c |
| H | L | A – c |
| H | H | INHIBIT |

## equivalent input and output schematic diagrams

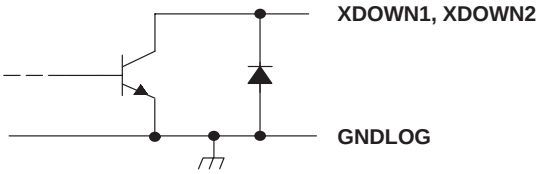
**Input**



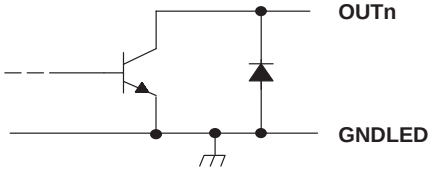

**DOUT0–9, DCDOUT0–6, XGSOUT, XPOUT, BOUT**




**XDOWN1, XDOWN2**




**OUTn**




## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| BCENA | 94 | I | Brightness control enable. When BCENA is low, the brightness control latch is set to the default value. The output current value in this status is 100% of the value set by an external resistor. The frequency division ratio of GSCLK is1/1. When BCENA is high, writing to brightness control latch is enabled. |
| BLANK | 67 | I | Blank (Light off). When BLANK is high, all output of the constant current driver are turned off. When GSPOL is high, all the output is turned on (LED on) synchronizing to the falling edge of GCLK after next rising edge of GSCLK when BLANK goes from high to low. When GSPOL is low, all the output is turned on (LED on) synchronizing to the rising edge of GCLK after next falling edge of GSCLK when BLANK goes from high to low. |
| BOUT | 53 | O | BLANK buffered output |
| DCCLK | 62 | I | Clock input for data transfer. The input data is from DCDIN (port B) . The output data at DCDOUT. All data on the shift register for dot correction data from DCDIN is shifted by 1 bit and is synchronized to the rising edge of DCCLK. |
| DCDIN0 – DCDIN6 | 86,87,88, 89,90,91,92 | I | Input for 7 bit parallel data (port B). These terminals are used as shift register input for dot correction data. |
| DCDOUT0 – DCDOUT6 | 34,35,36, 37,38,39,40 | O | Output for 7 bit parallel data (port B). These terminals are used as shift register output for dot correction data. |
| DCENA | 95 | I | Latch enable for dot correction data. When DCENA is low, the latch is set to the default value. At this time, the output current value is 100% of the value set by an external resistor. |
| DCLK | 64 | I | Clock input for data transfer. The input data is from DIN (port A) , all the data on the shift register selected by RSEL0, 1 and the output data at DOUT are shifted by 1 bit and synchronized to DCLK. Note that whether synchronizing to the rising or falling edge of DCLK is dependent on the value of DPOL. |

## Terminal Functions (Continued)

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| DIN0 – DIN9 | 76,77,78,79,80, 81,82,83,84,85 | I | Input for 10 bit parallel data (port A). These terminals are inputs for shift register for gray scale data, brightness control, and dot correction data. The register selected is determined by RSEL0, 1. |
| DOUT0 – DOUT9 | 41,42,43,44,45, 46,47,48,49,50 | O | Output for 10 bit parallel data (port A). These terminals are outputs for shift register for gray scale data, brightness control, and dot correction data. The register selected is determined by RSEL0, 1. |
| DPOL | 96 | I | Selects the valid edge of DCLK. When DPOL is high, the rising edge of DCLK is valid. When DPOL is low, the falling edge of DCLK is valid. |
| GNDANA | 28 | | Analog ground (Internally connected to GNDLOG and GNDLED) |
| GNDLOG | 98 | | Logic ground (Internally connected to GNDANA and GNDLED) |
| GNDLED | 1,4,7,10,13, 16,19,22,25 | | LED driver ground (Internally connected to GNDANA and GNDLED) |
| GSCLK | 68 | I | Clock input for gray scale. When MAG0 through MAG2 are all low, GSCLK is used for pulse width control. When MAG0 through MAG2 are not low, GSCLK is used for PLL timing control. The gray scale display is accomplished by lighting the LED until the number of GSCLK or PLL clocks counted is equal to the data latched. |
| GSPOL | 69 | I | Select the valid edge of GSCLK. When GSPOL is high, the rising edge of GSCLK is valid. When GSPOL is low, the falling edge of GSCLK is valid. |
| IREF | 32 | I/O | Constant current value setting. LED current is set to the desired value by connecting an external resistor between IREF and GND. The 38 times current is compared to current across the external resistor sink on the output terminal. |
| LEDCHK | 58 | I | LED disconnection detection enable. When LEDCHK is high, the LED disconnection detection is enabled and XDOWN2 is valid. When LEDCHK is low, the LED disconnection detection is disabled. |
| MAG0 – MAG2 | 73,72,71 | I | PLL multiple ratio setting. The clock frequency generated by PLL referenced to GSCLK is set . |
| NC | 57 | | No internal connection |
| OUT0 – DOUT15 | 2,3,5,6,8,9,11, 12,14,15,17,18, 20,21,23,24 | O | Constant current output |
| PDOUT | 70 | I/O | Resistor connection for PLL feedback adjustment |
| RBIAS | 74 | I/O | Resistor connection for PLL oscillation frequency setting |
| RSEL0<br>RSEL1 | 60<br>59 | I | Input/output port selection and shift register data latch switching.<br>When RSEL1 is low and RSEL0 is low, the gray scale data shift register latch is selected to port A, and the dot correction register latch is selected to port B.<br>When RSEL1 is low and RSEL0 is high, the brightness control register latch is selected to port A, and the dot correction register latch is selected to port B.<br>When RSEL1 is high and RSEL0 is low, the dot correction register latch is selected to port A and no register latch is selected to port B. |
| TEST1 – TEST3 | 97,99,100 | I | TEST. Factory test terminal. These terminals should be connected to GND. |
| THERMAL PAD | Package bottom | | Heat sink pad. This pad is connected to the lowest potential IC or thermal layer. |
| TSENA | 31 | I | TSD enable. When TSENA is high, TSD is enabled. When TSENA is low, TSD is disabled. |
| VCCANA | 33 | | Analog power supply voltage |
| VCCLOG | 93 | | Logic power supply voltage |
| VCCLED | 26 | | LED driver power supply voltage |
| VCOIN | 75 | I/O | Capacitance connection for PLL feedback adjustment |
| WDCAP | 30 | I/O | WDT detection time adjustment. WDT detection time is adjusted by connecting a capacitor between WDCAP and GND. When WDCAP is directly connected to GND, the WDT function is disabled. In this case, WDTRG should be tied to high or low level. |

## Terminal Functions (Continued)

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| WDTRG | 56 | I | WDT trigger input. By applying a scan signal to this terminal, the scan signal can be monitored by turning the constant current output off and protecting the LED from the damage of burning when the scan signal stops during the constant period designed. |
| XDCLAT | 61 | I | Data latch for dot correction. When XDCLAT is high, data on the shift register for dot correction data from DCDIN (port B) goes through latch. When XDCLAT is low, the data is latched. Accordingly, if data on the shift register is changed during XDCLAT high, the new value is latched (level latch). |
| XDOWN1 | 55 | O | Shutdown. XDOWN1 is configured as open collector. It goes low when the constant current output is shut down by the WDT or TSD function. |
| XDOWN2 | 54 | O | LED disconnection detection output. XDOWN2 is configured as open collector. XDOWN2 goes low when a LED disconnection is detected. |
| XDPOUT | 29 | O | DPOL output inverted |
| XDWN2TST | 27 | I | Test for XDOWN2. When XDWN2TST is low, XDOWN2 goes low. (This terminal is internally pulled up with 50 kΩ) |
| XENABLE | 66 | I | DCLK enable. When XENABLE is low, data transfer is enabled. Data transfer starts on the valid edge of DCLK after XENABLE goes low. During XENABLE high, no data is transferred. |
| XGSOUT | 52 | O | Clock output for gray scale. When MAG0 through MAG2 are all low, a clock with GSCLK inverted appears on this terminal. When MAG0 through MAG2 are not low., PLLCLK appears on this terminal. |
| XLATCH | 63 | I | Latch. When XLATCH is high, data on shift register from DIN (port A) goes through latch. When XLATCH is low, data is latched. Accordingly, if the data on the shift register is changed during XLATCH high, this new value is latched (level latch). |
| XOE | 65 | I | Data output enable. When XOE is low, the DOUT0–9 terminals are driven. When XOE is high, the DOUT0–9 terminals go to a high-impedance state. |
| XPOUT | 51 | O | GSPOL output inverted |

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Logic supply voltage, $V_{CC(LOG)}$ . . . . . – 0.3 V to 7 V
Supply voltage for constant current circuit, $V_{CC(LED)}$ . . . . . – 0.3 V to 7 V
Analog supply voltage, $V_{CC(ANA)}$ . . . . . – 0.3 V to 7 V
Output current (DC), $I_{OL(C)}$ . . . . . 85 mA
Input voltage range, $V_I$ . . . . . – 0.3 V to VCCLOG + 0.3 V
Output voltage range, $V_{(DOUT)}$, $V_{(DCDOUT)}$, $V_{(BOUT)}$, $V_{(XPOUT)}$ and $V_{(XGSOUT)}$ – 0.3 V to VCCLOG + 0.3 V
Output voltage range, $V_O$ and $V_{(XDOWNn)}$ . . . . . – 0.3 V to 16 V
Storage temperature range, $T_{str}$ . . . . . –40°C to 150°C
Continuous total power dissipation at (or below) $T_A$ = 25°C . . . . . 4.7 W
Power dissipation rating at (or above) $T_A$ = 25°C . . . . . 38.2m W/°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GNDLOG terminal.

### recommended operating conditions

#### dc characteristics

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Logic supply voltage, $V_{CC(LOG)}$ | | 4.5 | 5 | 5.5 | V |
| Supply voltage for constant current circuit, $V_{CC(LED)}$ | | 4.5 | 5 | 5.5 | V |
| Analog power supply, $V_{CC(ANA)}$ | | 4.5 | 5 | 5.5 | V |
| Voltage between $V_{CC}$, $V_{(DIFF1)}$ | $V_{(DIFF1)}$ = $V_{CC(LOG)} - V_{CC(ANA)}$ $V_{CC(LOG)} - V_{CC(LED)}$ $V_{CC(ANA)} - V_{CC(LED)}$ | –0.3 | 0 | 0.3 | V |
| Voltage between GND, $V_{(DIFF2)}$ | $V_{(DIFF2)}$= GND(LOG) – GND(ANA) GND(LOG) – GND(LED) GND(ANA) – GND(LED) | –0.3 | 0 | 0.3 | V |
| Voltage applied to constant current output, $V_O$ | OUT0 to OUT15 off | | | 15 | V |
| High–level input voltage, $V_{IH}$ | | 0.8 $V_{CC(LOG)}$ | | $V_{CC(LOG)}$ | V |
| Low–level input voltage, $V_{IL}$ | | GND(LOG) | | 0.2 $V_{CC(LOG)}$ | V |
| High–level output current, $I_{OH}$ | $V_{CC(LOG)}$ = 4.5 V, DOUT0 to DOUT9, DCDOUT0 to DCDOUT5, BOUT, XGSOUT, XPOUT | | | –1 | mA |
| Low–level output current, $I_{OL}$ | $V_{CC(LOG)}$ = 4.5 V, DOUT0 to DOUT9, DCDOUT0 to DCDOUT5, BOUT, XGSOUT, XPOUT | | | 1 | mA |
| | $V_{(CCLOG)}$ = 4.5 V, XDOWN1, XDOWN2 | | | 5 | mA |
| Constant output current, $I_{OL(C)}$ | OUT0 to OUT15 | 5 | | 80 | mA |
| Operating free–air temperature range, $T_A$ | | –20 | | 85 | °C |
| PLL capacitance, $C_{(VCO)}$ | | | 1 | | µF |
| PLL resistor, $R_{(BIAS)}$ | At 16 MHz oscillation | | 22 | | kΩ |
| PLL resistor, $R_{(PD)}$ | | | 30 | | kΩ |

## recommended operating conditions (continued)

**ac characteristics, $V_{CC(LOG)}$ = $V_{CC(ANA)}$ = $V_{CC(LED)}$ = 4.5 V to 5.5 V, TA = – 20 to 85°C (unless otherwise noted)**

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| DCLK, DCCLK clock frequency, $f_{(DCLK)}$/$f_{(DCCLK)}$ | At single operation | | | 20 | MHz |
| | At cascade operation | | | 15 | |
| DCLK, DCCLK pulse duration (high- or low-level), $t_{w(h)}$/$t_{w(l)}$ | | 20 | | | ns |
| GSCLK clock frequency, $f_{(GSCLK)}$ | | | | 8 | MHz |
| GSCLK pulse duration (high- or low-level), $t_{w(h)}$/$t_{w(l)}$ | | 40 | | | ns |
| PLLCLK clock frequency, $f_{(PLLCLK)}$ | | | | 16 | MHz |
| WDT clock frequency, $f_{(WDT)}$ | | | | 8 | MHz |
| WDT pulse duration (high- or low-level), $t_{w(h)}$/$t_{w(l)}$ | | 40 | | | ns |
| XLATCH, XDCLAT pulse duration (high-level), $t_{w(h)}$ | | 30 | | | ns |
| Rise/fall time, $t_r$/$t_f$ | | | | 100 | ns |
| Setup time, $t_{su}$ | DINn – DCLK | 5 | | | ns |
| | DCDINn – DCCLK | 5 | | | |
| | BLANK – GSCLK | 10 | | | |
| | XENABLE – DCLK | 15 | | | |
| | XLATCH – DCLK | 10 | | | |
| | XLATCH – GSCLK | 10 | | | |
| | XDCLAT – DCCLK | 10 | | | |
| | RSEL – DCLK | 10 | | | |
| | RSEL – DCCLK | 15 | | | |
| | RSEL – XLATCH | 30 | | | |
| | RSEL – XDCLAT | 15 | | | |
| Hold time, $t_h$ | DINn – DCLK | 15 | | | ns |
| | DCDINn – DCCLK | 15 | | | |
| | XENABLE – DCLK | 20 | | | |
| | XLATCH – DCLK | 30 | | | |
| | XDCLAT – DCCLK | 20 | | | |
| | RSEL – DCLK | 20 | | | |
| | RSEL – DCCLK | 20 | | | |
| | RSEL – XLATCH | 20 | | | |
| | RSEL – XDCLAT | 10 | | | |

## electrical characteristics, LEDCHK = L, MIN/MAX: $V_{CC(LOG)} = V_{CC(ANA)} = V_{CC(LED)} = 4.5$ V to 5.5 V, $T_A = -20$ to 85°C, TYP: $V_{CC(LOG)} = V_{CC(ANA)} = V_{CC(LED)} = 5$ V, $T_A = 25$°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH} = -1$ mA, DOUTn, DCOUTn, XGSOUT, XPOUT, BOUT | $V_{CC(LOG)} - 0.5$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1 mA, DOUTn, DCOUTn, XGSOUT, XPOUT, BOUT | | | 0.5 | V |
| | | $I_{OL}$ = 5 mA, XDOWN1, XDOWN2 | | | 0.5 | |
| $I_I$ | Input current | $V_I = V_{CC(LOG)}$ or GND(LOG) | | | ±1 | µA |
| $I_{(LOG)}$ | Supply current (logic) | Input signal is static, TSENA = H, WDCAP = OPEN, No PLL is used | | | 1 | mA |
| | | Input signal is static, TSENA = H, WDCAP = OPEN, PLL multiple ratio = 1042 | | | 3 | mA |
| | | Data transfer, DCLK = 20 MHz, GSCLK = 8 MHz No PLL is used | | 35 | 45 | |
| | | Data transfer, DCLK = 20 MHz, GSCLK = 15 kHz PLL multiple ratio = 1042 | | 39 | 49 | mA |
| $I_{(ANA)}$ | Supply current (analog) | BLANK = L, $R_{(IREF)}$ = 1200 Ω | | 6.5 | 8 | mA |
| | | BLANK = L, $R_{(IREF)}$ = 600 Ω | | 13 | 15 | |
| $I_{(LED)}$ | Supply current (constant current driver) | LED turn off, $R_{(IREF)}$ = 1200 Ω | | 12 | 20 | mA |
| | | LED turn off, $R_{(IREF)}$ = 600 Ω | | 20 | 35 | |
| | | $V_O$ = 1 V, $R_{(IREF)}$ = 1200 Ω all output bits turn on | | 12 | 20 | |
| | | $V_O$ = 1 V, $R_{(IREF)}$ = 600 Ω all output bits turn on | | 20 | 35 | |
| $I_{OL(C1)}$ | Constant output current (includes error between bits) | $V_O$ = 1 V, $V_{(IREF)}$ = 1.2 V, $R_{(IREF)}$ = 1200 W | 35 | 40 | 45 | mA |
| $I_{OL(C2)}$ | Constant output current (includes error between bits) | $V_O$ = 0.7 V, $V_{(IREF)}$ = 1.2 V $R_{(IREF)}$ = 600 W | 70 | 80 | 90 | mA |
| $I_{OL(K)}$ | Constant output leakage current | OUT0 to OUT15 ($V_{OUTn}$ = 15 V) | | | 0.1 | µA |
| | | XDOWN1, 2 ($V_{XDOWNn}$ = 15 V) | | | 1 | µA |
| | | DOUTn, DCDOUTn ($V_{OUTn}$ = VCCLOG or GND) | | | 1 | µA |
| $\Delta I_{OL(C)}$ | Constant output current error between bit | $V_{CC(LOG)}=V_{CC(ANA)}=V_{CC(LED)}$ $V_O$ = 1 V, $R_{(IREF)}$ = 600 W All output bits turn on | | ± 1% | ± 4% | |
| $I_{\Delta OL(C1)}$ | Changes in constant output current depend on supply voltage | $V_O$ = 1 V, $R_{(IREF)}$ = 600 W, $V_{IREF}$ = 1.2 V | | ± 1% | ± 4% | V |
| $I_{\Delta OL(C2)}$ | Changes in constant output current depend on output voltage | $V_O$ = 1 V to 3 V, $R_{(IREF)}$ = 600 Ω, $V_{IREF}$ = 1.2 V, 1 bit output turn on | | ± 1% | ± 3% | V |
| $T_{(tsd)}$ | TSD detection temperature | Junction temperature | 150 | 160 | 170 | °C |
| $T_{(wdt)}$ | WDT detection temperature | No external capacitor | 5 | 10 | 15 | ms |
| $V_{(IREF)}$ | Voltage reference | BCENA = L, $R_{(IREF)}$ = 9.6 kΩ, | | 1.2 | | V |
| $V_{(LEDDET)}$ | Voltage applied to LED disconnection detection | | 0.2 | 0.3 | 0.4 | V |
| $P_{(LLJITTER)}$ | PLL jitter | $R_{(BIAS)}$ = 22 kΩ, $R_{(PD)}$ = 30 kΩ, $C_{(VCO)}$ = 0.1 µF | | 0.4% | 2% | |

**switching characteristics, $C_L$ = 15 pF, MIN/MAX: $V_{CC(LOG)}$ = $V_{CC(ANA)}$ = $V_{CC(LED)}$ = 4.5 V to 5.5 V, $T_A$ = –20 to 85°C, TYP: $V_{CC(LOG)}$ = $V_{CC(ANA)}$ = $V_{CC(LED)}$ = 5 V, $T_A$ = 25°C (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_r$ | Rise time | DOUTn, DCDOUTn | | 12 | 30 | ns |
| | | XGSOUT, BOUT, XPOUT | | 12 | 30 | |
| | | OUTn (see Figure 1) | | 110 | | |
| $t_f$ | Fall time | DOUTn, DCDOUTn | | 10 | 30 | ns |
| | | XGSOUT, BOUT, XPOUT | | 10 | 30 | |
| | | OUTn (see Figure 1) | | 130 | | |
| $t_d$ | Propagation delay time | OUTn+1 – OUTn | | 30 | 45 | ns |
| | | BLANK↑ – OUT0 | 40 | 50 | 70 | |
| | | BLANK – BOUT | 10 | 20 | 40 | |
| | | GSCLK – OUT0 (see Note 2) | | 7 | | |
| | | GSCLK – XGSOUT | 10 | 20 | 40 | |
| | | DCLK – DOUTn | 15 | 30 | 45 | |
| | | DCLK – DCDOUTn | 15 | 30 | 45 | |
| | | DCCLK – DCDOUTn | 15 | 30 | 45 | |
| | | XOE↓ – DOUTn (see Note 3) | 10 | 20 | 35 | |
| | | XOE↑ – DOUTn (see Note 3) | 10 | 15 | 25 | |
| | | RSEL – DOUTn | 10 | 20 | 40 | |
| | | LEDCHK – XDOWN2 | | | 1000 | |

NOTES: 2. MAG0 to MAG2 are all low level.
3. Until DOUT is turned on (drive) or turned off (Hi-Z).

## PARAMETER MEASUREMENT INFORMATION

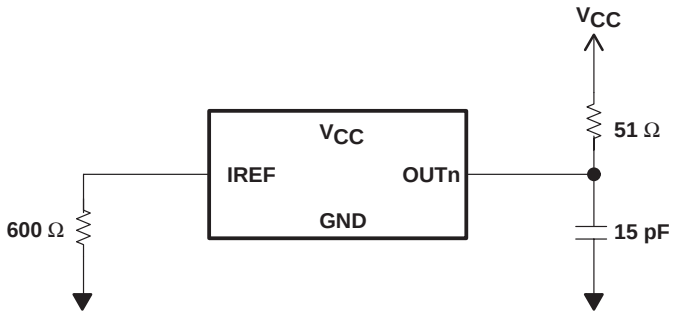



**Figure 1. Rise Time and Fall Time Test Circuit for OUTn**

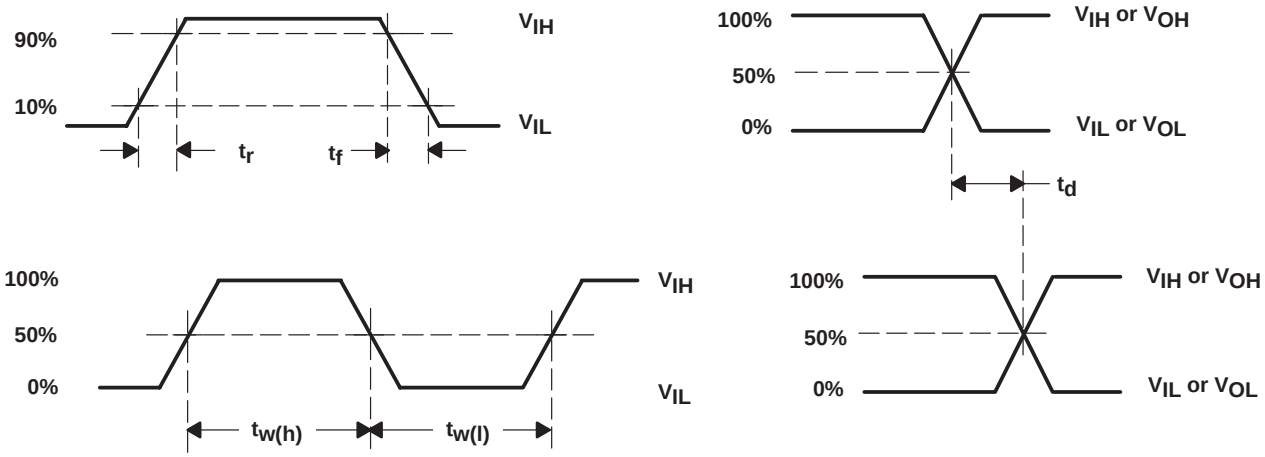



**Figure 2. Timing Requirements**

## PRINCIPLES OF OPERATION

### setting for output constant current value

On the constant current output terminals (OUT0–15), approximately 38 times the current which flows through the external resistor, $R_{(IREF)}$ (connected between IREF and GND), can flow. The external resistor value is calculated using the following equation:

$R_{(IREF)}$ ($\Omega$) $\cong$ 38 $\times$ 1.2 (V) / $I_{OL(C)}$(A) where both BCENA and DCENA are low.

Note that more current flows if IREF is connected to GND directly.

### constant output current operation

The constant current output turns on (sink constant current), if GSPOL is high and if all the gray scale data latched into the gray scale latch is not zero on the falling edge of the gray scale clock after the next rising edge of the gray scale clock when BLANK goes from high to low. After that, the number of the falling edge is counted by the 10-bit gray scale counter. Then, the output counted corresponding to the gray scale data is turned off (stop to sink constant current). The gray scale clock can be selected, as discussed in later section, from GSCLK or by internal PLL circuitry. If the shift register for the gray scale is updated during XLATCH high, the data on the gray scale data latch is also updated affecting the number of the gray scale of constant current output. Accordingly, during the on-state of the constant current output, XLATCH should be kept at a low level and the gray scale data latch should be held.

### input/output port and shift register selection

The TLC5911 supplies two parallel input ports such as DIN (10 bits : port A) and DCDIN (7 bits: port B). The DIN and DCDIN ports also supply DCLK and DCCLK for the shift clock, XLATCH and XDCLAT for latch, and DOUT and DCDOUT for output, respectively. The device has three kinds of shift register latchs such as the gray scale data, brightness control, and dot correction. The port and shift registers can be selected by RSEL0 and RSEL1. The selection of the shift registers will be done by RESL0 and RSEL1 as shown in Table 1. Note that the RSELn setting is done at DCLK low and DPOL high (DCLK is high when DPOL is low). When only port A is used, DCDIN, DCDOUT, DCCLK, and XDCLAT should be connected to GND.

**Table 1. Shift Register Latch Selection**

| | | SELECTED SHIFT REGISTER LATCH | | |
|---|---|---|---|---|
| | | PORT A | PORT B | |
| RSEL1 | RSEL0 | DIN, DCLK, XLATCH, DOUT | DCDIN, DCCLK, XDCLAT | DCDOUT |
| L | L | Gray scale data displayed | Dot correction | Dot correction |
| L | H | Brightness control | Dot correction | Dot correction |
| H | L | Dot correction (see Note 4) | Not connected | Dot correction |
| H | H | N/A (inhibit) | N/A (inhibit) | N/A (inhibit) |

NOTE 4: Zero is output to DOUT7 through DOUT9.

### shift register latch for gray scale data

The shift register latch for the gray scale data is configured with 16 $\times$ 10 bits. The gray scale data, configured with 10 bits, represents the time when constant current output is being turned on, and the data range is 0 to 1023 (00h to 3FFh). When the gray scale data is 0, the time is shortest, and the output is not turned on (light off). On the other hand, when the gray scale data is 1023, the time is longest, and it turns on during the time of the 1023 clocks from the gray scale clock. The configuration of the shift register and the latch for gray scale data is shown in Figure 3.

## PRINCIPLES OF OPERATION

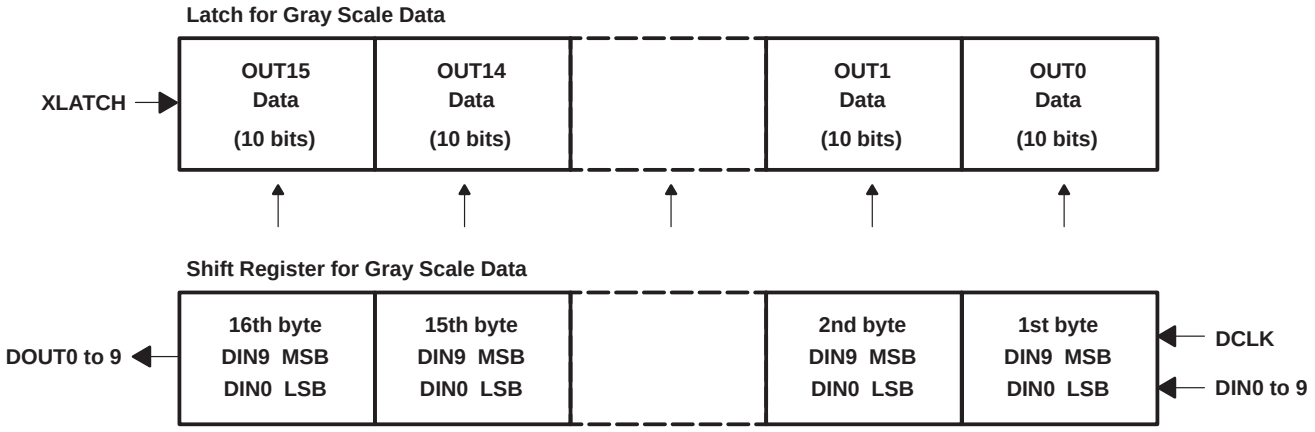
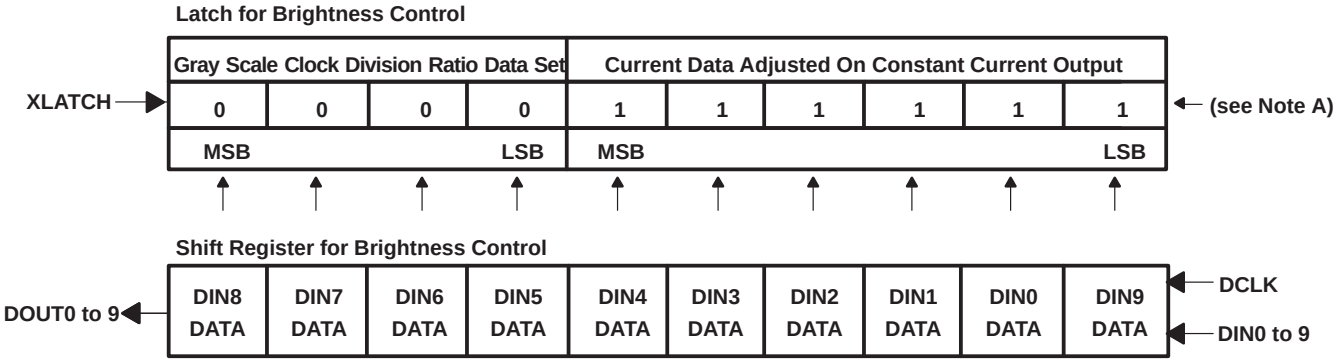



**Figure 3. Relationship Between Shift Register and Latch for Gray Scale Data**

### shift register latch for brightness control

The shift register latch for brightness control is configured with 1 × 10 bits. Using the shift register latch for the brightness control, the division ratio of the gray scale clock can be set and the output current value on constant current output can be adjusted. When powered up, the latch data is indeterminate and the shift register is not initialized. When these functions are used, data should be written to the shift register latch prior to lighting-on (BLANK=L). Also, it is prohibited from rewriting the latch value for the brightness control when the constant current output is turned on. When these functions are not used, the latch value can be set to the default value setting of BCENA at low level (connect to GND). Also, DIN9 is assigned to the LSB of the reference current control to maintain compatibility with the TLC5901/02/03 family. The configuration of the shift register and the latch for brightness control is shown in Figure 4.




NOTE A: Indicates default value at BCENA low.

**Figure 4. Relationship Between Shift Register and Latch for Brightness Control**

### shift register latch for dot correction

The shift register latch for dot correction is configured with 16 × 7 bits. Using the shift register latch for dot correction, the current value on the constant current output can be set individually. When powered up, the latch data is indeterminate and the shift register is not initialized. When these functions are used, data should be written to the shift register latch prior to lighting-on (BLANK=L). Also, rewriting the latch value for dot correction when the constant current output is turned on is inhibited. When these functions are not used, the latch value can be set to the default value setting of DCENA at low level (connect to GND). The configuration of the shift register and the latch for dot correction is shown in Figure 5.

## PRINCIPLES OF OPERATION

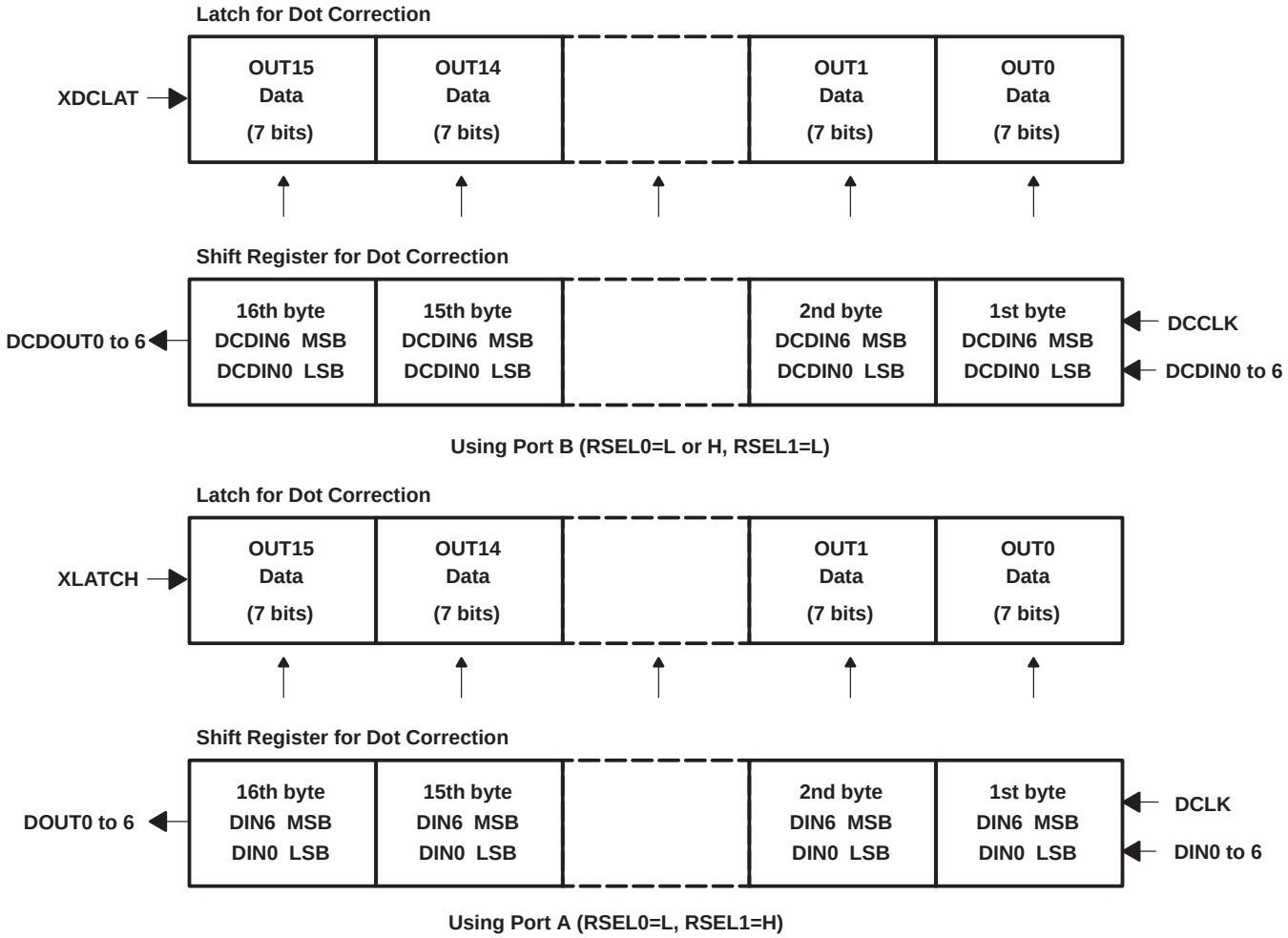



**Figure 5. Relationship Between the Shift Register and the Latch for Dot Correction**

### write data to shift register latch

The shift register latch written is selected using the RSEL0 and RSEL1 terminal. At port A, the data is applied to the DIN data input terminal, clocked into the shift register and synchronized to the rising edge of DCLK after XENABLE is pulled low. At port B, the data is applied to the DCDIN data input terminal, clocked into the shift register, and synchronized to the rising edge of DCCLK. The shift register for the gray scale data is configured with $16 \times 10$ bits and the shift register for dot correction is configured with $16 \times 7$ bits resulting in sixteen times DCLK. The shift register for the brightness control is configured with $1 \times 10$ bits resulting in one times DCLK. At the number of DCLK input for each case, data can be written into the shift register. In this condition, when the XLATCH at port A or the XDCLAT at port B is pulled high, data in the shift register is clocked into the latch (data through). When the XLATCH at port A or XDCLAT at port B is pulled low, data is held (latch).

## PRINCIPLES OF OPERATION

### brightness control function

By writing data into the brightness control latch, current on all the constant current outputs can be adjusted to control the variation of brightness between ICs. The division ratio for the gray scale clock can be set to control the variation of brightness for the total panel system. Furthermore, by writing data into the dot correction latch, current on each constant current output can be adjusted.

#### output current adjustment on all constant current outputs – brightness adjustment between ICs

By using the lower 6 bits of the brightness control latch, output current can be adjusted in 64 steps as 1 step of 0.8% of the current ratio between 100% and 50.8% when the output current is set to 100% of an external resistor (note that the current value is lower if the constant current output is corrected using the dot correction function). By using this function, the brightness control between modules (ICs) can be adjusted sending the desired data externally even if ICs are mounted on a print-circuit board. When BCENA is pulled low, the output current is set to 100%.

**Table 2. Relative Current Ratio For Total Constant Current Output**

| CURRENT RATIO % | 20 (mA) | 80 (mA) | CODE | $V_{IREF}$ (TYP) |
|---|---|---|---|---|
| 50.8 | 10.2 | 40.6 | MSB 000000 LSB | 0.60 |
| . . . . | . . . . | . . . . | . . . . | . . . . |
| 99.2 | 19.8 | 79.7 | 111110 | 1.19 |
| 100 | 20.0 | 80.0 | 111111† | 1.20 |

† BCENA is low.

#### frequency division ratio setting for gray scale clock – panel brightness adjustment

By using the upper 4 bits of the brightness control latch, the gray scale clock can be divided into 1/1 to 1/16. If the gray scale clock is set to 16 times the speed of frequency (1024×16=16384) during horizontal scanning time, the brightness can be adjusted in 16 steps by selecting the frequency division ratio. By using this function, the total panel brightness can be adjusted at once, and applied to the brightness of day or night. When BCENA is pulled low, the gray scale clock is not divided. When BCENA is pulled high, the brightness can be adjusted as shown in Table 3.

**Table 3. Relative Brightness Ratio For Total Constant Current Output**

| CODE | FREQUENCY DIVISION RATIO | RELATIVE BRIGHTNESS RATIO (%) |
|---|---|---|
| MSB 0000 LSB† | 1/1 | 6.3 |
| . . . . | . . . . | . . . . |
| 1110 | 1/15 | 93.8 |
| 1111 | 1/16 | 100 |

† BCENA is low.

## PRINCIPLES OF OPERATION

### output current adjustment on each constant current output – LED brightness adjustment

By using the dot correction latch, the output current on each constant current output can be adjusted in 128 steps as 1 step of 0.8% of the current ratio between 100% and 0% when the output current is set to 100% of an external resistor at 7Fh of the latched value and the lower 6 bits of the brightness control register. By using this function, the brightness deviation from the LED brightness variation can be minimized. When DCENA is pulled low, the output current is set to 100% without the dot correction.

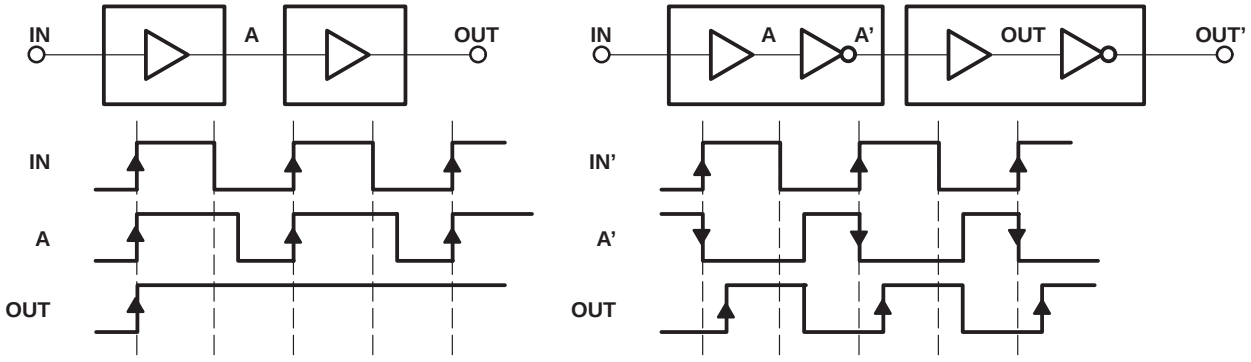
**Table 4. Relative Current Ratio By Constant Current Output**

| CODE | CURRENT RATIO % | $I_{OL(C)}$=40 (mA) |
|---|---|---|
| MSB 0000000 LSB | 0.0 | 0.0 |
| . . . . | . . . . | . . . . |
| 1111110 | 99.2 | 39.7 |
| 1111111† | 100 | 40 |

† DCENA is low.

### clock edge selection

The high speed clock signal is diminished due to the duty ratio change through the multiple stages of the IC or module as shown in Figure 6.




**a) Propagate through multiple stages buffer with slow falling edge**

**b) Insert inverter between buffers**

**Figure 6. Clock Edge Selection**

In Figure 6a, if the falling edge at the internal buffer is behind the rising edge, the clock will disappear if a multiple cascade connection is made. To resolve this problem, the duty ratio can be held unchanged using the connection as shown in Figure 6b if the valid clock edge can be selected (arrow in Figure 6). Note that the clock delay is not avoided even in this case.

The device incorporates the clock edge selection function for each DCLK and GSCLK. By using this function, the falling edge or rising edge for the valid edge can be selected depending on the status of DPOL and GSPOL, thus the degradation for the duty ratio can be reduced. The relationship between each signal is shown in Table 5.

## PRINCIPLES OF OPERATION

**Table 5. Valid Edge For DCLK and GSCLK**

| DPOL | DCLK valid edge | Operation at XENABLE = H |
|---|---|---|
| H | DCLK↑ | Pull DCLK to low level |
| L | DCLK↓ | Pull DCLK to high level |

| GSPOL | GSCLK valid edge | PLL operation |
|---|---|---|
| H | GSCLK↑ | Synchronize to the high level of DCLK |
| L | GSCLK↓ | Synchronize to the low level of DCLK |

The device supplies the XPOUT and XGSOUT output terminals for the cascade operation which inverts GSPOL and GSCLK respectively. It also supplies the BOUT output terminal as a buffered BLANK to make timing easy with GSCLK and XGSOUT.

### gray scale clock generation

When MAG<0:2> are all low, the clock input from the GSCLK terminal is used as the gray scale clock with no change, and except for this case the internal PLL generates the clock for the gray scale control clock. When using the PLL, the gray scale clock is generated by adjusting the clock to have the same number of pulses as the multiple ratio of the GSCLK reference period (when GSCLK and GSPOL are kept at the same level). The ratio in this case is determined depending on MAG0 through MAG2 as shown in Table 6.

When using the PLL, the internal PLLCLK is clocked out at the XGSOUT terminal. Therefore, the clock can be utilized for other devices on the same print-circuit board. Note that the number of ICs connected is limited depending on the frequency.

**Table 6. PLL Multiple Ratio**

| MAG2 | MAG1 | MAG0 | MULTIPLE RATIO | XGSOUT |
|---|---|---|---|---|
| L | L | L | 1 (Signal to control GSCLK by GSPOL) | Inverted GSCLK |
| L | L | H | $2^8$+6(=262) | PLLCLK (Gray scale clock is internally generated) |
| L | H | L | $2^9$+10(=522) | |
| L | H | H | $2^{10}$+18(=1042) | |
| H | L | L | $2^{11}$+34(=2082) | |
| H | L | H | $2^{12}$+66(=4162) | |
| H | H | L | $2^{13}$+130(=8322) | |
| H | H | H | $2^{14}$+258(=16642) | |

## PRINCIPLES OF OPERATION

### gray scale clock generation (continued)

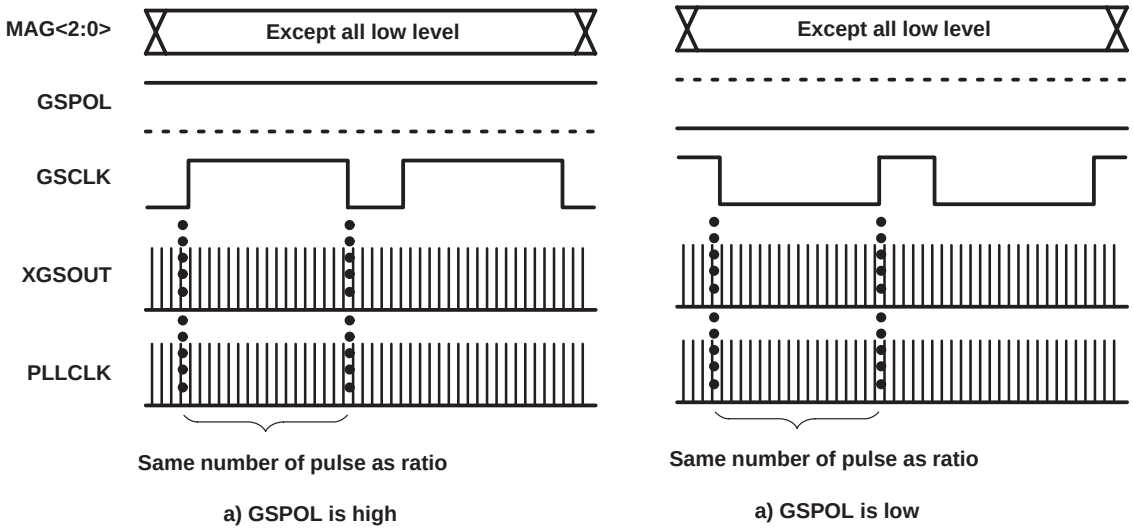


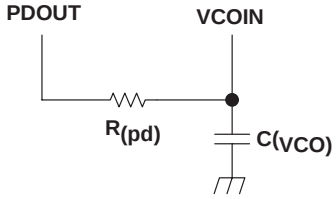

**Figure 7. Gray Scale Clock Generation**

The oscillation frequency bandwidth as referenced for the PLL can be set by an external resistor connected between RBIAS and GND. The relation between the external resistor and the oscillation frequency is shown in Table 7.

**Table 7. PLL Oscillation Frequency**

| RBIAS | 22 kΩ | 30 kΩ | 62 kΩ | 12 0kΩ |
|---|---|---|---|---|
| FREQUENCY | 13 to 16 MHz | 8 to 14 MHz | 4 to 9 MHz | 3 to 5 MHz |

Note that it takes 30 ms for the PLL to be stabilized. Furthermore, to make the PLL operation stabilized, a resistor and a capacitor connection is required between VCOIN, PDOUT and GND. The recommended values are shown in the Figure 8.




| | $C_{(VCO)}$ | $R_{(pd)}$ |
|---|---|---|
| Recommeded Value | 0.1 to 1 μF | 22 to 62 kΩ |

**Figure 8. Resistor and Capacitor Connection**

## PRINCIPLES OF OPERATION

### protection

This device incorporates WDT and TSD functions. If the WDT or TSD functions, the constant current output is stopped and XDOWN1 goes low. Therefore, by monitoring the XDOWN1 terminal, these failures can be detected immediately. Since the XDOWN1 output is configured as open collector, outputs of multiple ICs are brought together.

#### WDT (watchdog timer)

The constant current output is forced to turn off and XDOWN1 goes low when the fixed period elapsed after the signal applied to WDTRG has not been changed. Therefore, by connecting a scan signal (a signal to the control line displayed) to WDTRG, the stop of the scan signal can be detected and the constant current output is turned off preventing the LED from burning and damage caused by continuous LED turn on at the dynamic scanning operation. The detection time can be set using an external capacitor, C1. The typical value is approximately 10 ms without capacitor, 160 ms with a1000 pF capacitor, and 1500 ms with a 0.01 μF capacitor. During static operation, the WDT function is disabled connecting the WDCAP to GND (high or low level should be applied to WDTRG). Note that normal operations will be resumed changing the WDTRG level when WDT functions.

$$\text{WDT operational time T (ms)} \cong 10 + 0.15 \times \text{C1 (pF)}$$

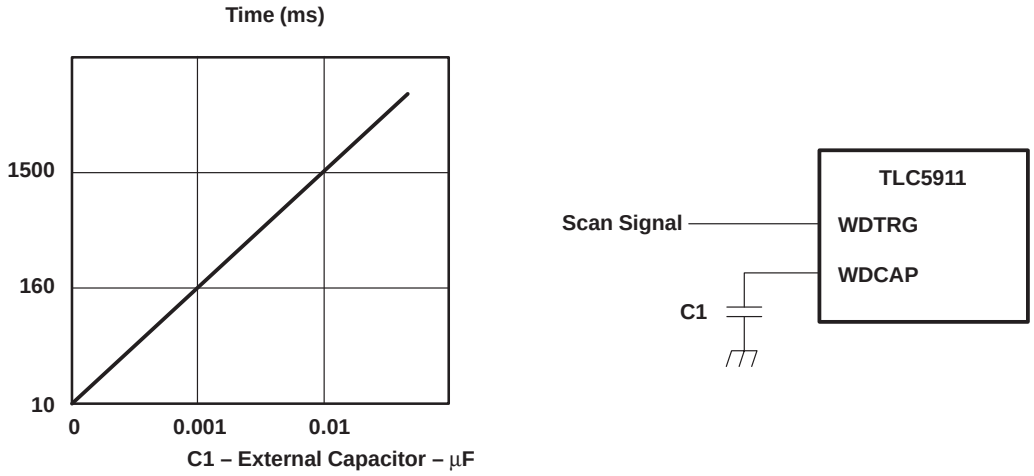



**Figure 9. WDT Operational Time and Usage Example**

#### TSD (thermal shutdown)

When the junction temperature exceeds the limit, TSD functions and turns the constant current output off, and XDOWN1 goes low. When TSD is used, TSENA is pulled high. When TSD is not used, TSENA is pulled low. To recover from the constant current output off-state to normal operations, the power supply should be turned off or TSENA should be pulled low once.

## PRINCIPLES OF OPERATION

### LOD function (LED open detection)

When LEDCHK is low, the LED disconnection detection function is disabled and XDOWN2 goes to a high-impedance state. When LEDCHK is high, the LED disconnection detection function is enabled, and XDOWN2 goes low if any LED is disconnected while monitoring the OUTn terminals to be turned on. This function is operational for sixteen OUTn terminals individually. To determine which constant current output is disconnected, the level of XDOWN2 is checked 16 times from OUT0 to OUT15 turning one constant current output on. The power supply voltage should be set so the constant current output applied is above 0.4 V when the LED is turned on normally. Also, since approximately 1000 ns is required from turning the constant current output on to XDOWN2 output, the gray scale data to be turned on during that period should be applied.

Table 8 is an example of XDOWN2 output status using four LEDs .

**Table 8. XDOWN2 Output Example**

| | | | | |
|---|---|---|---|---|
| **LED NUMBER** | 1 | 2 | 3 | 4 |
| **LED STATUS** | GOOD | NG | GOOD | NG |
| **OUTn** | ON | ON | ON | ON |
| **DETECTION RESULT** | GOOD | NG | GOOD | NG |
| **XDOWN2** | LOW (by case 2, 4) | | | |
| **LED NUMBER** | 1 | 2 | 3 | 4 |
| **LED STATUS** | GOOD | NG | GOOD | NG |
| **OUTn** | ON | ON | OFF | OFF |
| **DETECTION RESULT** | GOOD | NG | GOOD | GOOD |
| **XDOWN2** | LOW (by case 2) | | | |
| **LED NUMBER** | 1 | 2 | 3 | 4 |
| **LED STATUS** | GOOD | NG | GOOD | NG |
| **OUTn** | OFF | OFF | OFF | OFF |
| **DETECTION RESULT** | GOOD | GOOD | GOOD | GOOD |
| **XDOWN2** | HIGH-IMPEDANCE | | | |

### noise reduction

#### concurrent switching noise reduction

Concurrent switching noise has a potential to occur when multiple outputs turn on or off at the same time. To prevent this noise, the device has delay output terminals such as XGSOUT, BOUT for GSCLK (gray scale clock), and BLANK (blanking signal) respectively. By connecting these outputs to the GSCLK and BLANK terminals of next stage IC, it allows differences in the switching time between ICs. When GSCLK is output to GSOUT through the device, duty will be changed between input and output. The number of stages to be connected will be limited depending on the frequency.

#### delay between constant current output

The constant current output has a delay time of approximately 20 ns between outputs. It means approximately 300 ns delay time exists between OUT0 and OUT15. This time difference by delay is effective for the reduction of concurrent switching noise.

## PRINCIPLES OF OPERATION

### others

#### power supply

The following should be taken into consideration:

- VCCLOG, VCCANA and VCCLED should be supplied by a single power supply to minimize voltage differences between these terminals.
- The bypass capacitor should be located between the power supply and GND to eliminate the variation of power supply voltage.

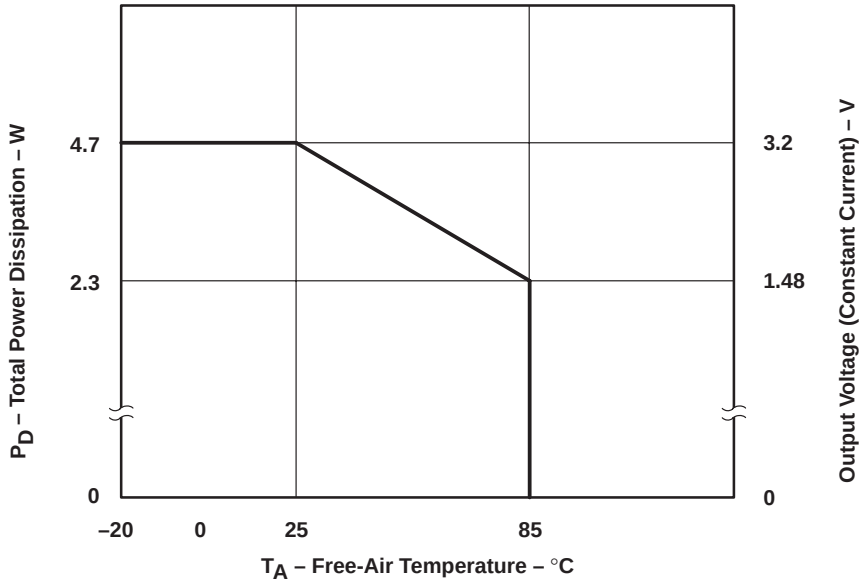
#### GND

Although GNDLOG, GNDANA, and GNDLED are internally tied together, these terminals should be externally connected to reduce noise influence.

#### thermal pad

The thermal pad should be connected to GND to eliminate the noise influence, since it is connected to the bottom side of IC chip. Also, the desired thermal effect will be obtained by connecting this pad to the PCB pattern with better thermal conductivity.

### power rating free-air temperature



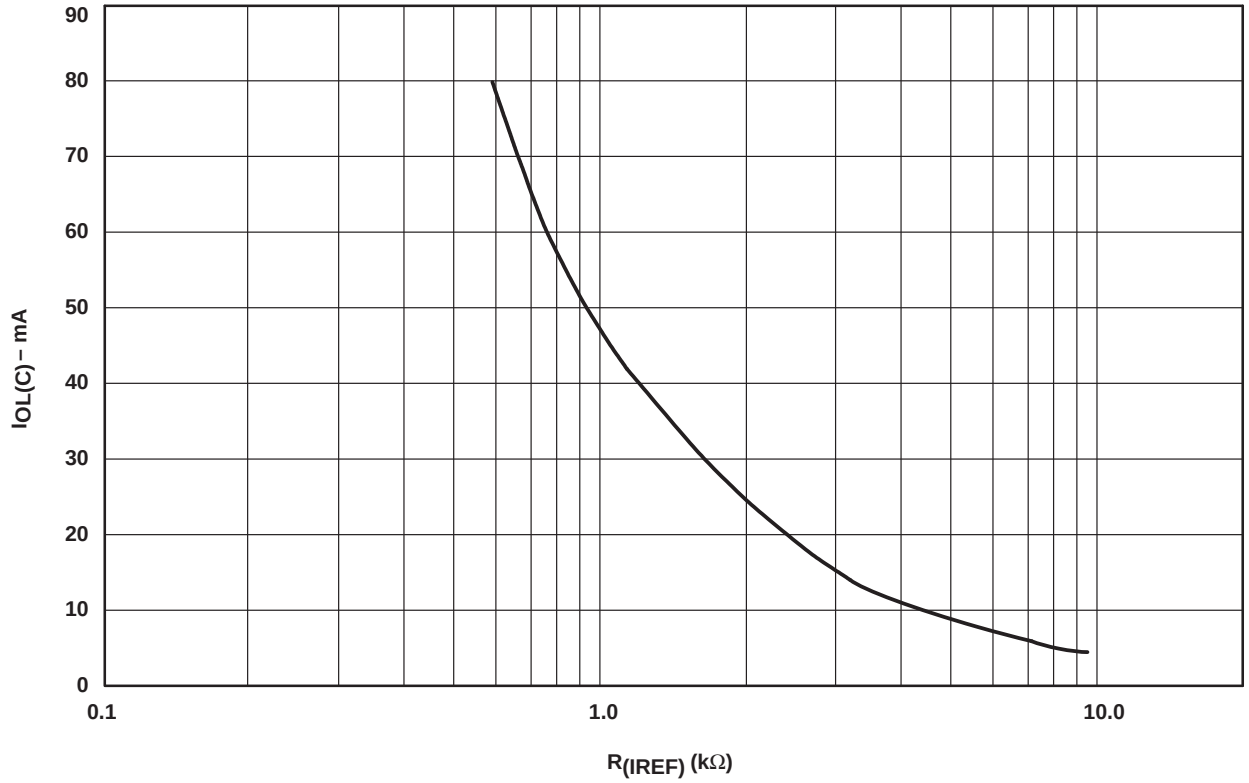

NOTES: A. The IC is mounted on PCB.
PCB size : $102 \times 76 \times 1.6$ [$mm^3$], four layers with the internal two layers being plane. The thermal pad is soldered to the PCB pattern of $10 \times 10$ [$mm^2$]. For operation above 25°C free-air temperature, derate linearly at the rate of 38.2 mW/°C.
$V_{CC(LOG)}=V_{CC(ANA)}=V_{CC(LED)}=5$ V, $I_{OL(C)}$ = 80 mA, $I_{CC}$ is a typical value.

B. The thermal impedance will be varied depending on the mounting conditions. Since the PZP package established a low thermal impedance by radiating heat from the thermal pad, the thermal pad should be soldered to the pattern with a low thermal impedance.

C. The material for the PCB should be selected considering the thermal characteristics since the temperature will rise around the thermal pad.

**Figure 10. Power Rating**

## PRINCIPLES OF OPERATION



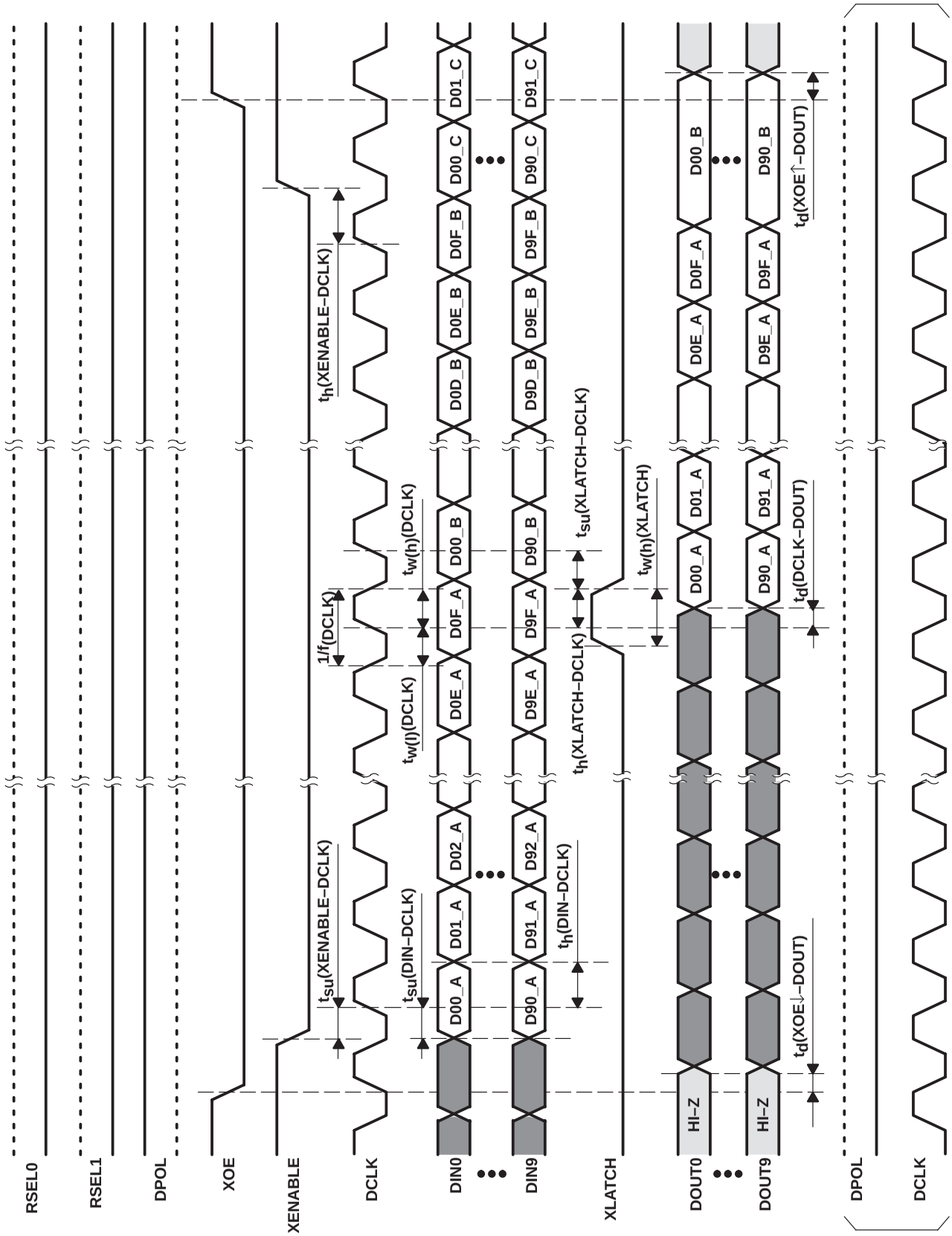

Conditions : $V_O$ = 1 V, $V_{(IREF)}$ = 1.2 V

$$I_{OL(C)}\,(mA) \cong \frac{V_{(IREF)}(V)}{R_{(IREF)}\,(k\Omega)} \times 38$$

$$R_{(IREF)}\,(k\Omega) \cong \frac{46}{I_{OL(C)}\,(mA)}$$

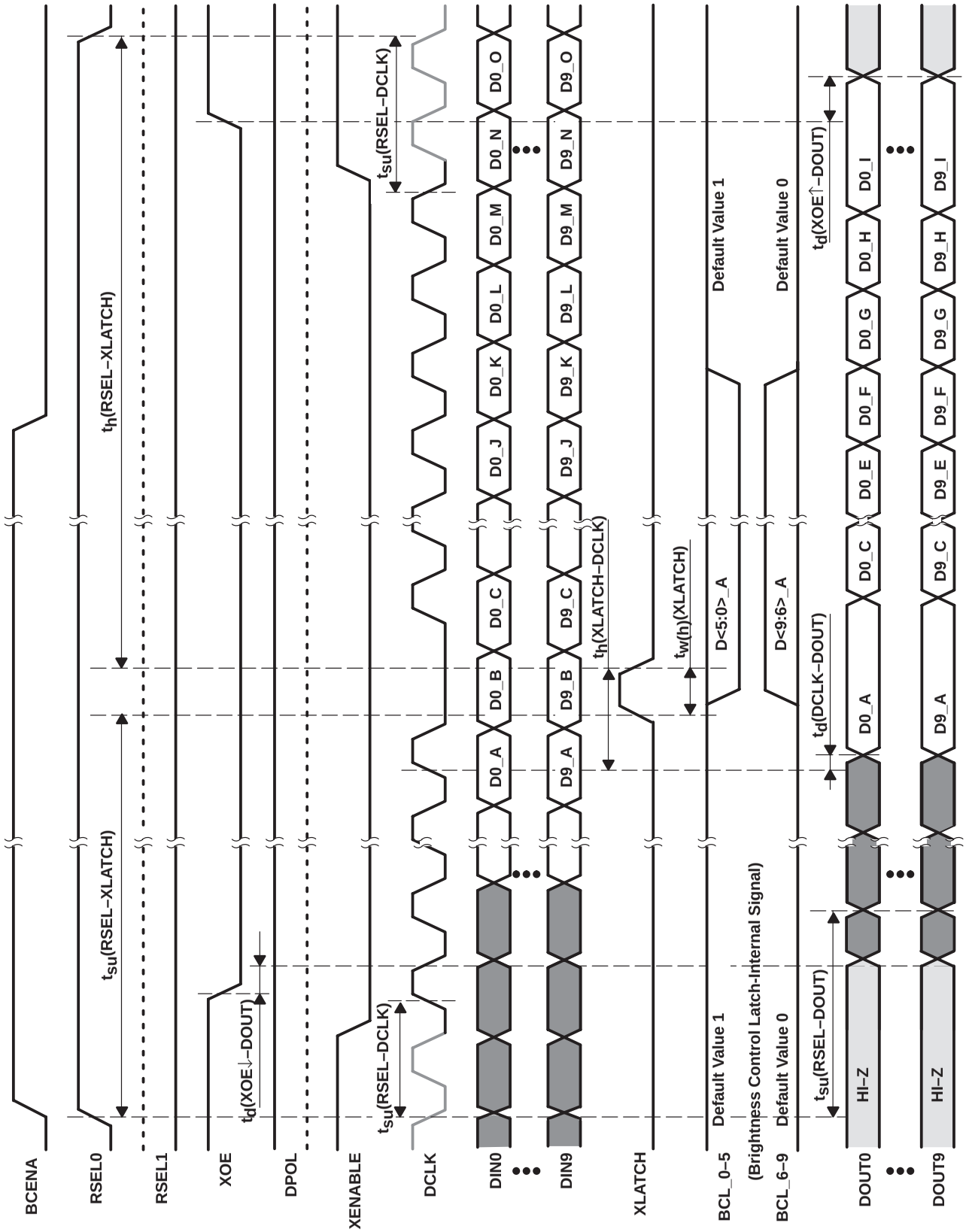
NOTE: The brightness control and dot corrected value are set at 100%.
The resistor, $R_{(IREF)}$, should be located as close as possible to the IREF terminal to avoid noise influence.

**Figure 11. Current on Constant Current Output vs External Resistor**



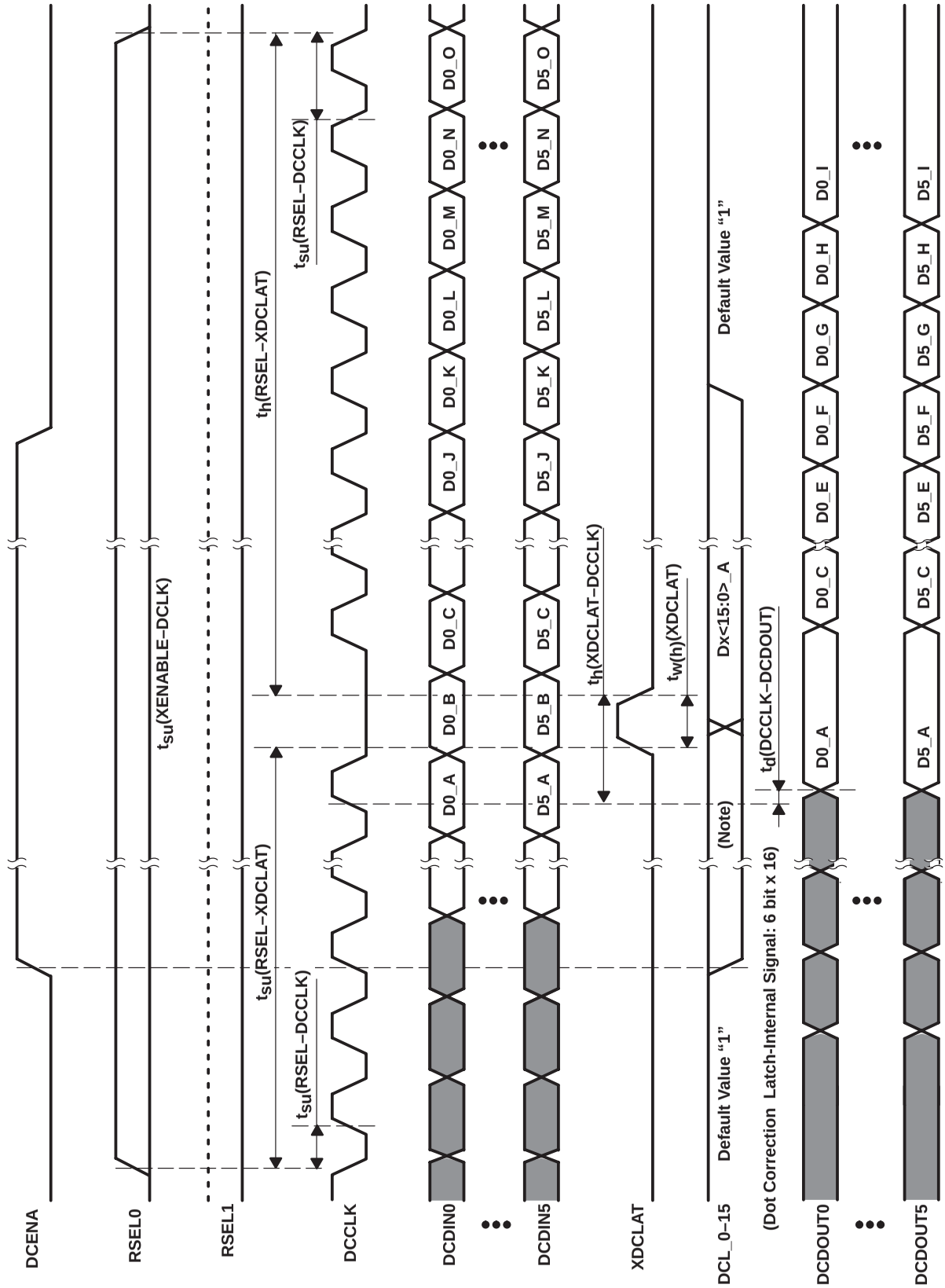

DPOL and DCLK can be replaced with the combination of these signals enclosed by the parenthesis (Both are inverted each other).

**Figure 12. Timing Diagram (Shift Register for Gray Scale Data)**



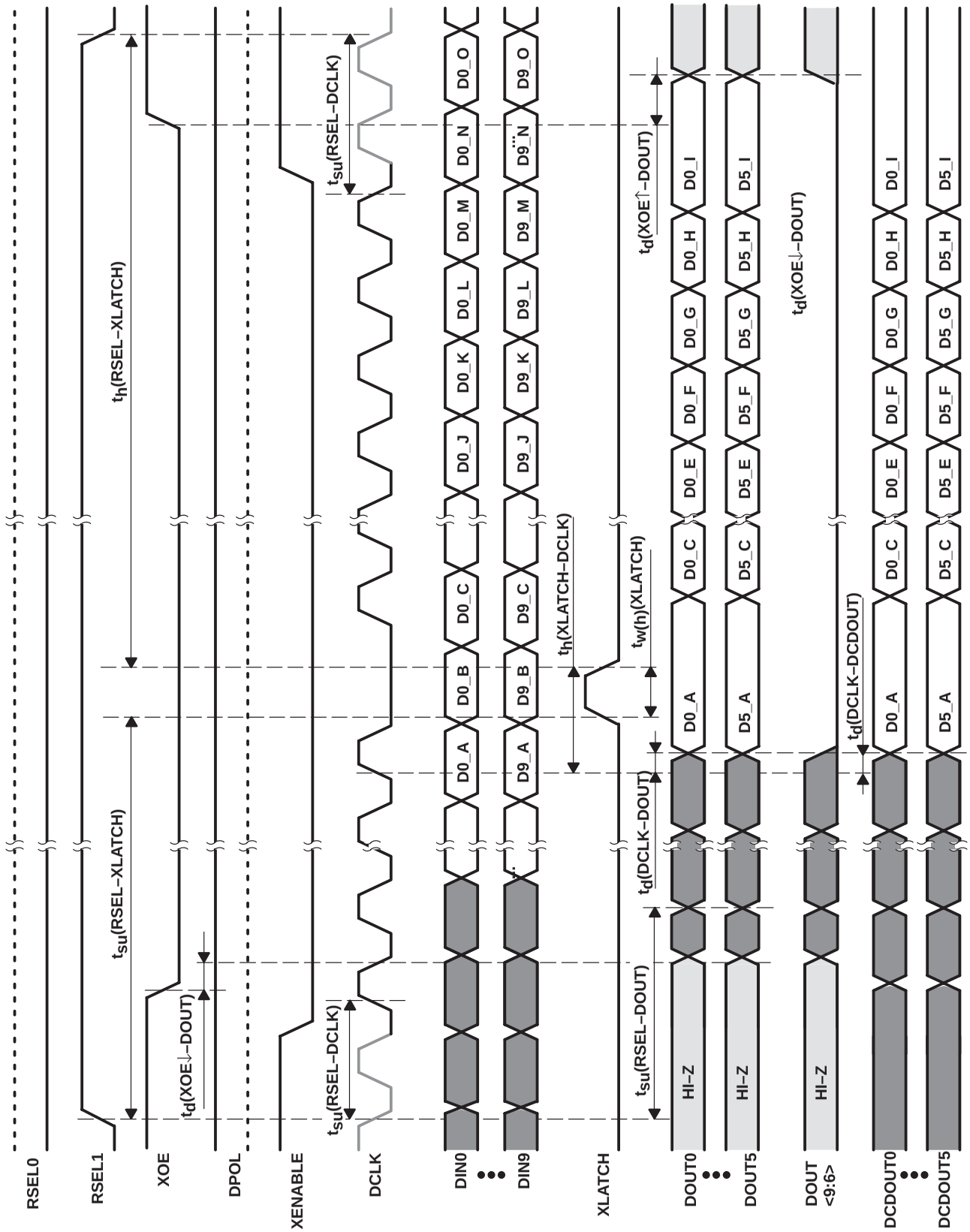

DPOL and DCLK can be replaced with signals inverted each other same as shift register for gray scale data.

**Figure 13. Timing Diagram (Shift Register for Brightness Control)**



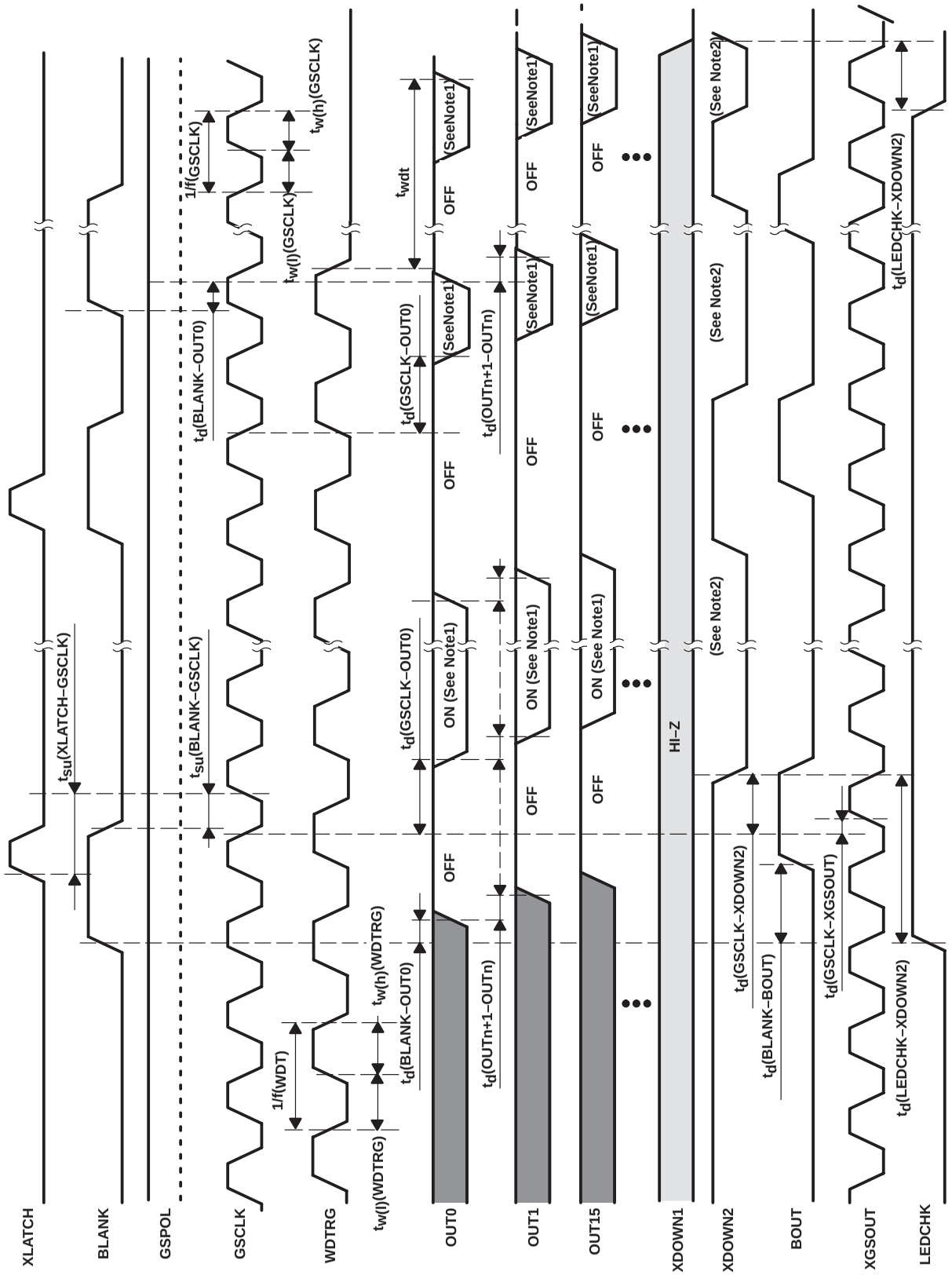

NOTE : Register value is immediately before DCLAT↓.

**Figure 14. Timing Diagram (Shift Register for Dot Correction: Using Port B)**




DPOL and DCLK can be replaced with signals inverted each other same as shift register for gray scale data.

**Figure 15. Timing Diagram (Shift Register for Dot Correction: Using Port A)**




GSPOL, GSCLK and XGSOUT can be replaced with signals inverted each other.

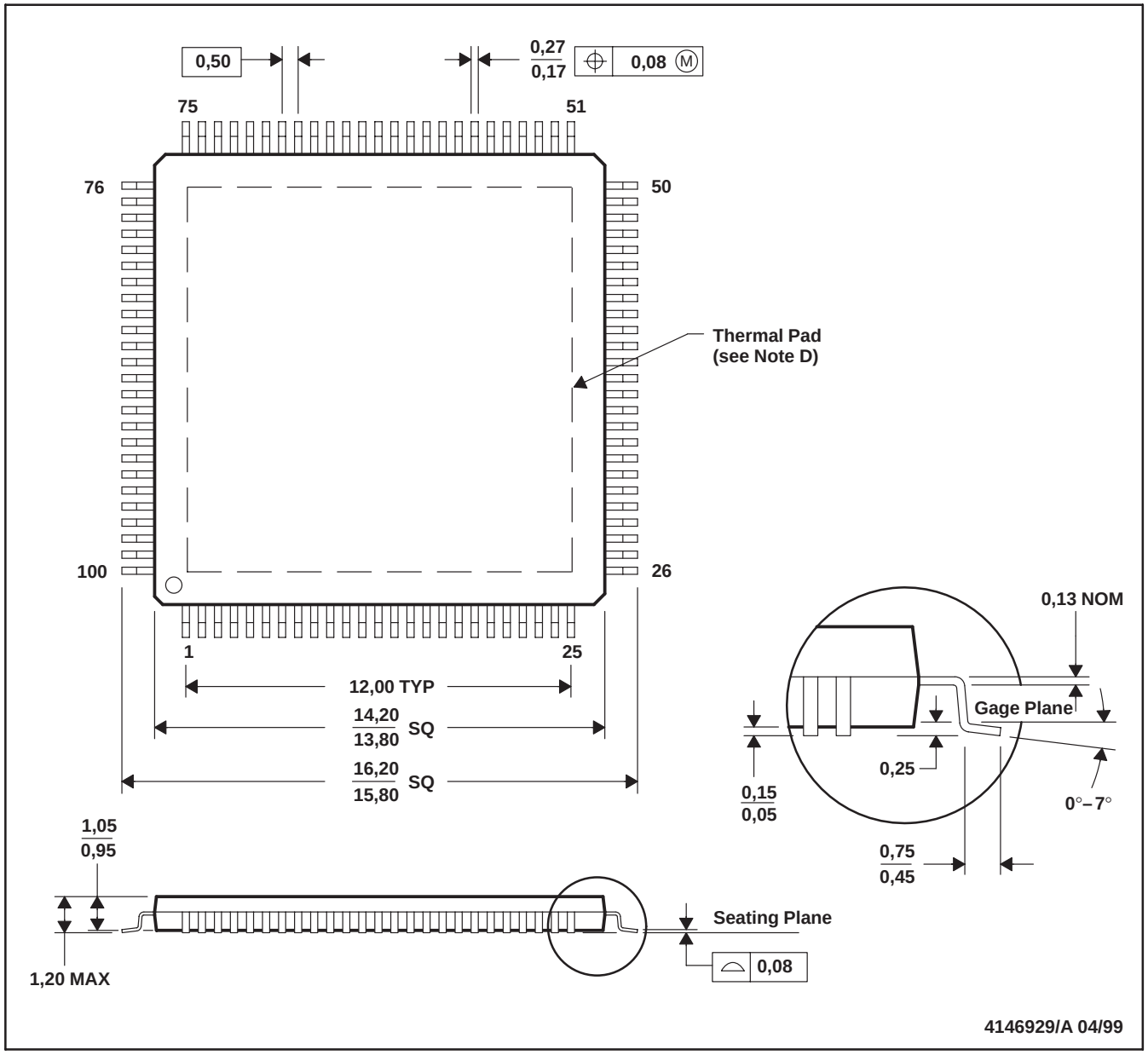
NOTE 1: ON or OFF, or ON time is varied depend on the gray scale data and BLANK.

NOTE 2: When LED is disconnected.

**Figure 16. Timing Diagram (Constant Current Output) – MAG0 to MAG2 Are All Zero**

## MECHANICAL DATA

**PZP (S-PQFP-G100)** **PowerPAD™ PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane.
This pad is electrically and thermally connected to the backside of the die and possibly selected leads. The dimensions of the thermal pad are 2 mm × 2 mm (maximum). The pad is centered on the bottom of the package.
E. Falls within JEDEC MS-026

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