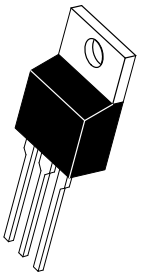
PNP
D45C

Complementary Silicon Power Transistor

. . . for general purpose driver or medium power output stages in CW or switching applications.

- Low Collector–Emitter Saturation Voltage — 0.5 V (Max)
- High f_t for Good Frequency Response
- Low Leakage Current

4.0 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 80 VOLTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Emitter Voltage	VCES	90	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak (1)	I_C	4.0 6.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_A = 25°C	P_D	30 1.67	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
DC Current Gain (V_{CE} = 1.0 Vdc, I_C = 0.2 Adc) (V_{CE} = 1.0 Vdc, I_C = 1.0 Adc) (V_{CE} = 1.0 Vdc, I_C = 2.0 Adc)	h_{FE}	 40 20 20	 120 — —	—

(REPLACES D44C)

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{BE} = 0)	I_{CES}	—	—	0.1	μA
Emitter Cutoff Current (V_{EB} = 5.0 Vdc)	I_{EBO}	—	—	10	μA
ON CHARACTERISTICS					
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 50 mAdc)	$V_{CE(sat)}$	—	0.135	0.5	Vdc
Base–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{BE(sat)}$	—	0.85	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, f = 1.0 MHz)	C_{cb}	—	125	—	pF
Gain Bandwidth Product (I_C = 20 mA, V_{CE} = 4.0 Vdc, f = 20 MHz)	f_T	—	40	—	MHz
SWITCHING TIMES					
Delay and Rise Times (I_C = 1.0 Adc, I_{B1} = 0.1 Adc)	$t_d + t_r$	—	50	75	ns
Storage Time (I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)	t_s	—	350	550	ns
Fall Time (I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)	t_f	—	50	75	ns

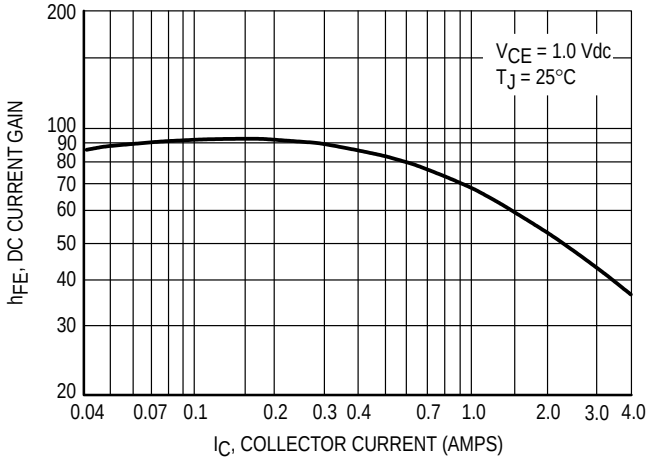


Figure 1. Typical DC Current Gain

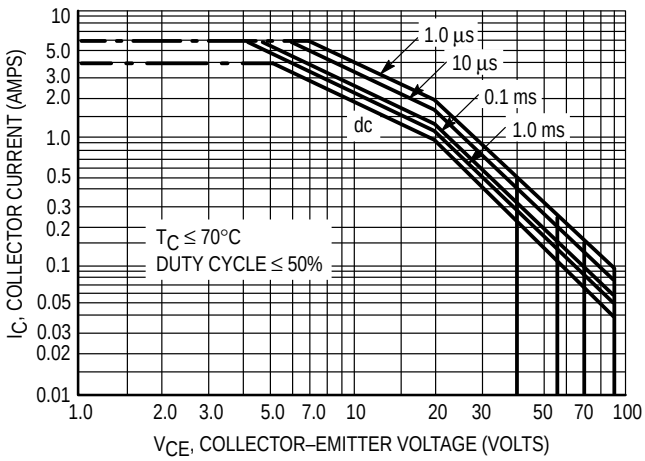
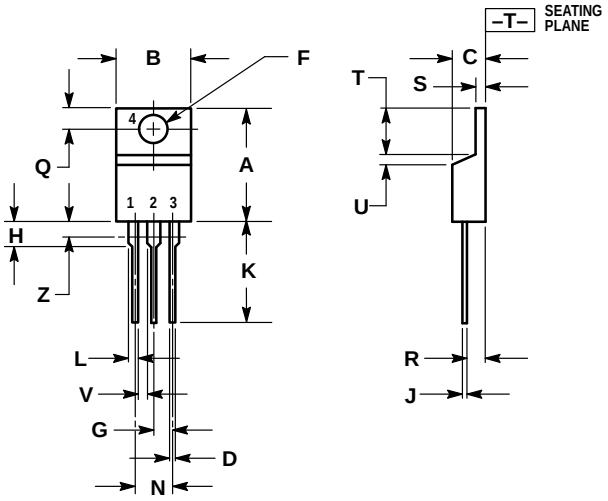


Figure 2. Maximum Rated Forward Bias Safe Operating Area

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A–06
TO–220AB
ISSUE Y

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