Data Sheet | June 1, 2006 | FN3955.5

330MHz, Low Power, Current Feedback Video Operational Amplifier with Output Disable

The HFA1145 is a high speed, low power current feedback amplifier built with Intersil's proprietary complementary bipolar UHF-1 process.

This amplifier features a TTL/CMOS compatible disable control, pin 8, which when pulled low reduces the supply current and forces the output into a high impedance state. This allows easy implementation of simple, low power video switching and routing systems. Component and composite video systems also benefit from this op amp's excellent gain flatness, and good differential gain and phase specifications.

Multiplexed A/D applications will also find the HFA1145 useful as the A/D driver/multiplexer.

The HFA1145 is a low power, high performance upgrade for the CLC410.

For Military grade product, please refer to the HFA1145/883 data sheet.

Ordering Information

PART NUMBER (BRAND)	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HFA1145IB	1145IB	-40 to 85	8 Ld SOIC	M8.15
HFA1145IBZ (Note)	1145IBZ	-40 to 85	8 Ld SOIC (Pb-free)	M8.15
HFA1145IP	HFA1145IP	-40 to 85	8 Ld PDIP	E8.3
HFA1145IPZ (Note)	HFA1145IPZ	-40 to 85	8 Ld PDIP* (Pb-free)	E8.3
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps Note: Requires a SOIC-to-DIP adapter. See "Evaluation Board" section inside.			

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Features

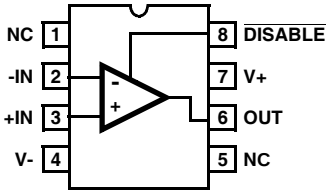
- Low Supply Current 5.8mA
- High Input Impedance 1MΩ
- Wide -3dB Bandwidth. 330MHz
- Very Fast Slew Rate. 1000V/μs
- Gain Flatness (to 75MHz) . . . . . ±0.1dB
- Differential Gain 0.02%
- Differential Phase. . . . . 0.03 Degrees
- Output Enable/Disable Time 180ns/35ns
- Pin Compatible Upgrade for CLC410
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Flash A/D Drivers
- Video Switching and Routing
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications

Pinout

HFA1145 (SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . . V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 1) . . . . . Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
ESD Rating . . . . . >600V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	170

Maximum Junction Temperature (Die Only) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/°C
Input Offset Voltage Common-Mode Rejection Ratio	ΔV_{CM} = ±1.8V	A	25	47	50	-	dB
	ΔV_{CM} = ±1.8V	A	85	45	48	-	dB
	ΔV_{CM} = ±1.2V	A	-40	45	48	-	dB
Input Offset Voltage Power Supply Rejection Ratio	ΔV_{PS} = ±1.8V	A	25	50	54	-	dB
	ΔV_{PS} = ±1.8V	A	85	47	50	-	dB
	ΔV_{PS} = ±1.2V	A	-40	47	50	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/°C
Non-Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	25	-	0.5	1	µA/V
	ΔV_{PS} = ±1.8V	A	85	-	0.8	3	µA/V
	ΔV_{PS} = ±1.2V	A	-40	-	0.8	3	µA/V
Non-Inverting Input Resistance	ΔV_{CM} = ±1.8V	A	25	0.8	1.2	-	MΩ
	ΔV_{CM} = ±1.8V	A	85	0.5	0.8	-	MΩ
	ΔV_{CM} = ±1.2V	A	-40	0.5	0.8	-	MΩ
Inverting Input Bias Current		A	25	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/°C
Inverting Input Bias Current Common-Mode Sensitivity	ΔV_{CM} = ±1.8V	A	25	-	3	6	µA/V
	ΔV_{CM} = ±1.8V	A	85	-	4	8	µA/V
	ΔV_{CM} = ±1.2V	A	-40	-	4	8	µA/V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	25	-	2	5	µA/V
	ΔV_{PS} = ±1.8V	A	85	-	4	8	µA/V
	ΔV_{PS} = ±1.2V	A	-40	-	4	8	µA/V
Inverting Input Resistance		C	25	-	60	-	Ω
Input Capacitance		C	25	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density (Note 6)	f = 100kHz	B	25	-	3.5	-	nV/√Hz
Non-Inverting Input Noise Current Density (Note 6)	f = 100kHz	B	25	-	2.5	-	pA/√Hz
Inverting Input Noise Current Density (Note 6)	f = 100kHz	B	25	-	20	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain	A_V = -1	C	25	-	500	-	kΩ
AC CHARACTERISTICS R_F = 510Ω, Unless Otherwise Specified							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Note 6)	A_V = +1, $+R_S$ = 510Ω	B	25	-	270	-	MHz
		B	Full	-	240	-	MHz
	A_V = -1, R_F = 425Ω	B	25	-	300	-	MHz
	A_V = +2	B	25	-	330	-	MHz
		B	Full	-	260	-	MHz
	A_V = +10, R_F = 180Ω	B	25	-	130	-	MHz
		B	Full	-	90	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P} at A_V = +2/-1, 4V_{P-P} at A_V = +1, Note 6)	A_V = +1, $+R_S$ = 510Ω	B	25	-	135	-	MHz
	A_V = -1	B	25	-	140	-	MHz
	A_V = +2	B	25	-	115	-	MHz
Gain Flatness (A_V = +2, V_{OUT} = 0.2V_{P-P}, Note 6)	To 25MHz	B	25	-	±0.03	-	dB
		B	Full	-	±0.04	-	dB
	To 75MHz	B	25	-	±0.11	-	dB
		B	Full	-	±0.22	-	dB
Gain Flatness (A_V = +1, $+R_S$ = 510Ω, V_{OUT} = 0.2V_{P-P}, Note 6)	To 25MHz	B	25	-	±0.03	-	dB
	To 75MHz	B	25	-	±0.09	-	dB
Minimum Stable gain		A	Full	-	1	-	V/V
OUTPUT CHARACTERISTICS A_V = +2, R_F = 510Ω, Unless Otherwise Specified							
Output Voltage Swing (Note 6)	A_V = -1, R_L = 100Ω	A	25	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current (Note 6)	A_V = -1, R_L = 50Ω	A	25, 85	50	60	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current		B	25	-	90	-	mA
Closed Loop Output Impedance (Note 6)	DC	B	25	-	0.08	-	Ω

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Second Harmonic Distortion (V_{OUT} = $2V_{P-P}$, Note 6)	10MHz	B	25	-	-48	-	dBc
	20MHz	B	25	-	-44	-	dBc
Third Harmonic Distortion (V_{OUT} = $2V_{P-P}$, Note 6)	10MHz	B	25	-	-50	-	dBc
	20MHz	B	25	-	-45	-	dBc
Reverse Isolation (S_{12}, Note 6)	30MHz	B	25	-	-55	-	dB
TRANSIENT CHARACTERISTICS A_V = +2, R_F = 510Ω, Unless Otherwise Specified							
Rise and Fall Times	V_{OUT} = $0.5V_{P-P}$	B	25	-	1.1	-	ns
		B	Full	-	1.4	-	ns
Overshoot (Note 4) (V_{OUT} = 0 to 0.5V, V_{IN} t_{RISE} = 1ns)	+OS	B	25	-	3	-	%
	-OS	B	25	-	5	-	%
Overshoot (Note 4) (V_{OUT} = $0.5V_{P-P}$, V_{IN} t_{RISE} = 1ns)	+OS	B	25	-	3	-	%
	-OS	B	25	-	11	-	%
Slew Rate (V_{OUT} = $4V_{P-P}$, A_V = +1, $+R_S$ = 510Ω)	+SR	B	25	-	1000	-	V/µs
		B	Full	-	975	-	V/µs
	-SR (Note 5)	B	25	-	650	-	V/µs
		B	Full	-	580	-	V/µs
Slew Rate (V_{OUT} = $5V_{P-P}$, A_V = +2)	+SR	B	25	-	1400	-	V/µs
		B	Full	-	1200	-	V/µs
	-SR (Note 5)	B	25	-	800	-	V/µs
		B	Full	-	700	-	V/µs
Slew Rate (V_{OUT} = $5V_{P-P}$, A_V = -1)	+SR	B	25	-	2100	-	V/µs
		B	Full	-	1900	-	V/µs
	-SR (Note 5)	B	25	-	1000	-	V/µs
		B	Full	-	900	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step, Note 6)	To 0.1%	B	25	-	15	-	ns
	To 0.05%	B	25	-	23	-	ns
	To 0.02%	B	25	-	30	-	ns
Overdrive Recovery Time	V_{IN} = ±2V	B	25	-	8.5	-	ns
VIDEO CHARACTERISTICS A_V = +2, R_F = 510Ω, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.02	-	%
	R_L = 75Ω	B	25	-	0.03	-	%
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.03	-	Degrees
	R_L = 75Ω	B	25	-	0.05	-	Degrees
DISABLE CHARACTERISTICS							
Disabled Supply Current	$V_{\overline{DISABLE}}$ = 0V	A	Full	-	3	4	mA
$\overline{DISABLE}$ Input Logic Low		A	Full	-	-	0.8	V
$\overline{DISABLE}$ Input Logic High		A	25, 85	2.0	-	-	V
		A	-40	2.4	-	-	V
$\overline{DISABLE}$ Input Logic Low Current	$V_{\overline{DISABLE}}$ = 0V	A	Full	-	100	200	µA

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
$\overline{\text{DISABLE}}$ Input Logic High Current	$V_{\overline{\text{DISABLE}}} = 5V$	A	Full	-	1	15	µA
Output Disable Time (Note 6)	$V_{IN} = \pm1V$, $V_{\overline{\text{DISABLE}}} = 2.4V$ to 0V	B	25	-	35	-	ns
Output Enable Time (Note 6)	$V_{IN} = \pm1V$, $V_{\overline{\text{DISABLE}}} = 0V$ to 2.4V	B	25	-	180	-	ns
Disabled Output Capacitance	$V_{\overline{\text{DISABLE}}} = 0V$	B	25	-	2.5	-	pF
Disabled Output Leakage	$V_{\overline{\text{DISABLE}}} = 0V$, $V_{IN} = \mp2V$, $V_{OUT} = \pm3V$	A	Full	-	3	10	µA
Off Isolation ($V_{\overline{\text{DISABLE}}} = 0V$, $V_{IN} = 1V_{P-P}$, Note 6)	At 5MHz	B	25	-	-75	-	dB
	At 25MHz	B	25	-	-60	-	dB
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current (Note 6)		A	25	-	5.8	6.1	mA
		A	Full	-	5.9	6.3	mA

NOTES:

3. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
4. Undershoot dominates for output signal swings below GND (e.g. $0.5V_{P-P}$), yielding a higher overshoot limit compared to the $V_{OUT} = 0$ to 0.5V condition. See the “Application Information” section for details.
5. Slew rates are asymmetrical if the output swings below GND (e.g. a bipolar signal). Positive unipolar output signals have symmetric positive and negative slew rates comparable to the +SR specification. See the “Application Information” section, and the pulse response graphs for details.
6. See Typical Performance Curves for more information.

Application Information

Optimum Feedback Resistor

Although a current feedback amplifier’s bandwidth dependency on closed loop gain isn’t as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier’s unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier’s bandwidth is inversely proportional to R_F. The HFA1145 design is optimized for $R_F = 510\Omega$ at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains, however, the amplifier is more stable so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For a gain of +1, a resistor ($+R_S$) in series with +IN is required to reduce gain peaking and increase stability.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	425	300
+1	510 ($+R_S = 510\Omega$)	270
+2	510	330
+5	200	300
+10	180	130

Non-inverting Input Source Impedance

For best operation, the DC source impedance seen by the non-inverting input should be ≥50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

$\overline{\text{DISABLE}}$ Input TTL Compatibility

The HFA1145 derives an internal GND reference for the digital circuitry as long as the power supplies are symmetrical about GND. With symmetrical supplies the digital switching threshold ($V_{TH} = (V_{IH} + V_{IL})/2 = (2.0 + 0.8)/2$) is 1.4V, which ensures the TTL compatibility of the $\overline{\text{DISABLE}}$ input. If asymmetrical supplies (e.g. +10V, 0V) are utilized, the switching threshold becomes:

$$V_{TH} = \frac{V+ + V-}{2} + 1.4V$$

and the V_{IH} and V_{IL} levels will be $V_{TH} \pm 0.6V$, respectively.

Optional GND Pad (Die Use Only) for TTL Compatibility

The die version of the HFA1145 provides the user with a GND pad for setting the disable circuitry GND reference. With symmetrical supplies the GND pad may be left unconnected, or tied directly to GND. If asymmetrical supplies (e.g. +10V, 0V) are utilized, and TTL compatibility is desired, die users must connect the GND pad to GND. With an external GND, the $\overline{\text{DISABLE}}$ input is TTL compatible regardless of supply voltage utilized.

Pulse Undershoot and Asymmetrical Slew Rates

The HFA1145 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased undershoot on the negative portion of the output waveform (See Figures 5, 8, and 11). This undershoot isn't present for small bipolar signals, or large positive signals. Another artifact of the composite device is asymmetrical slew rates for output signals with a negative voltage component. The slew rate degrades as the output signal crosses through 0V (See Figures 5, 8, and 11), resulting in a slower overall negative slew rate. Positive only signals have symmetrical slew rates as illustrated in the large signal positive pulse response graphs (See Figures 4, 7, and 10).

PC Board Layout

This amplifier's frequency response depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the device's input and output connections. Capacitance, parasitic or planned, connected to the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground at the amplifier's inverting input (-IN), as this capacitance causes gain peaking, pulse overshoot, and if large enough, instability. To reduce this capacitance, the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 270MHz (for A_V = +1). By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, the bandwidth decreases as the load capacitance increases. For example, at A_V = +1, R_S = 62Ω, C_L = 40pF, the overall bandwidth is limited to 180MHz, and bandwidth drops to 75MHz at A_V = +1, R_S = 8Ω, C_L = 400pF.

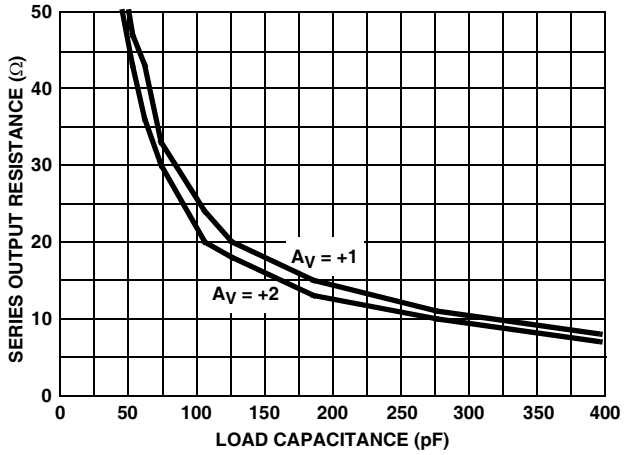


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1145 may be evaluated using the HFA11XX Evaluation Board and a SOIC to DIP adaptor like the Aries Electronics Part Number 14-350000-10. The layout and schematic of the board are shown in Figure 2.

The V_H connection may be used to exercise the $\overline{\text{DISABLE}}$ pin, but note that this connection has no 50Ω termination. To order evaluation boards (part number HFA11XXEVAL), please contact your local sales office.

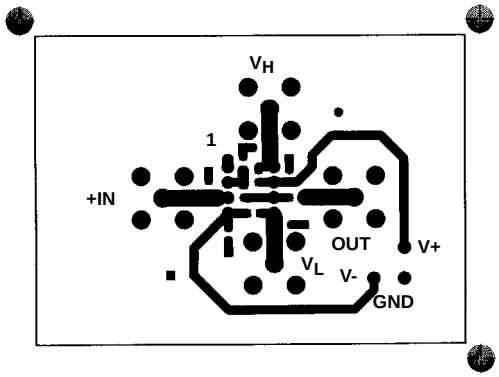


FIGURE 2A. TOP LAYOUT

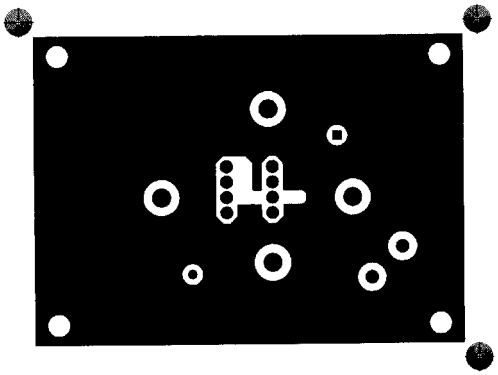


FIGURE 2B. TOP LAYOUT

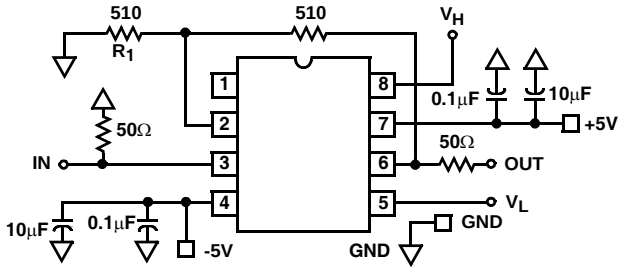


FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

Typical Performance Curves V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified

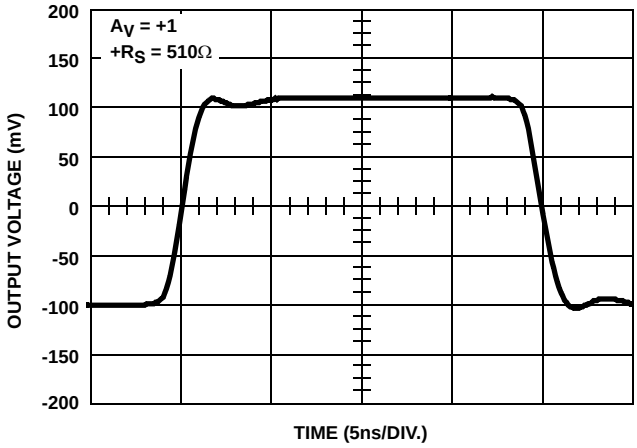


FIGURE 3. SMALL SIGNAL PULSE RESPONSE

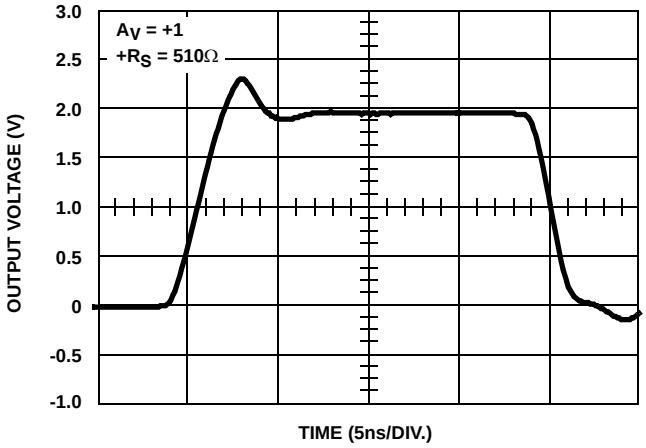


FIGURE 4. LARGE SIGNAL POSITIVE PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25°C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

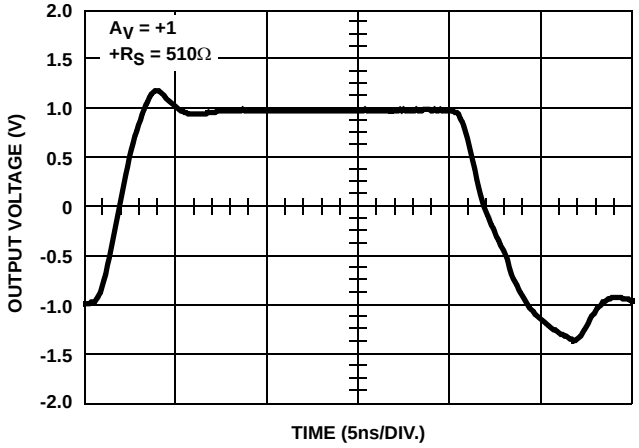


FIGURE 5. LARGE SIGNAL BIPOLAR PULSE RESPONSE

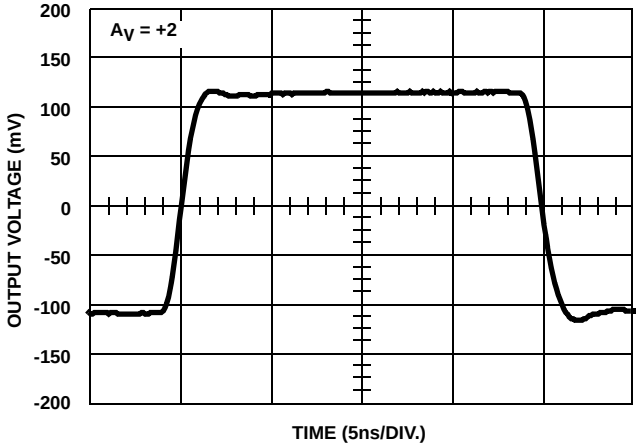


FIGURE 6. SMALL SIGNAL PULSE RESPONSE

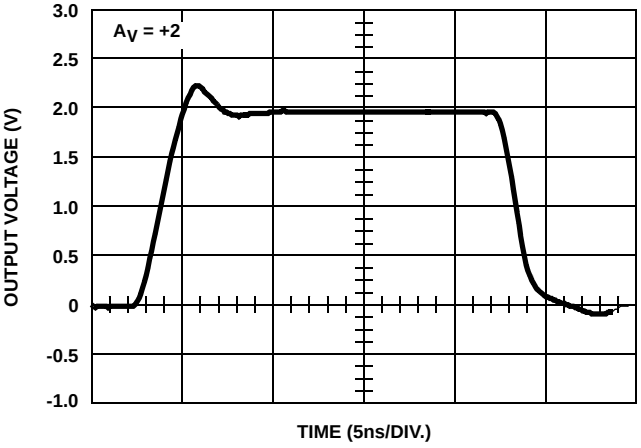


FIGURE 7. LARGE SIGNAL POSITIVE PULSE RESPONSE

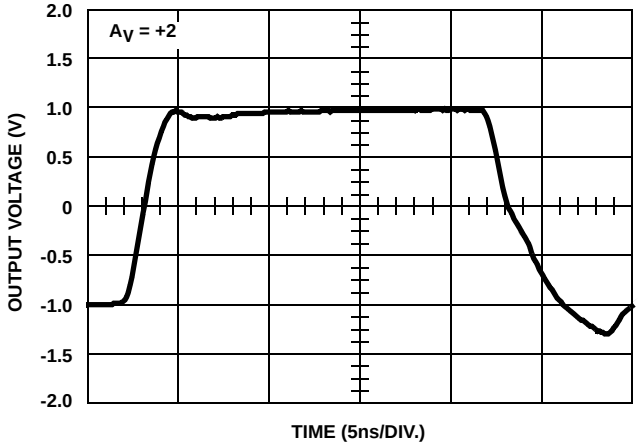


FIGURE 8. LARGE SIGNAL BIPOLAR PULSE RESPONSE

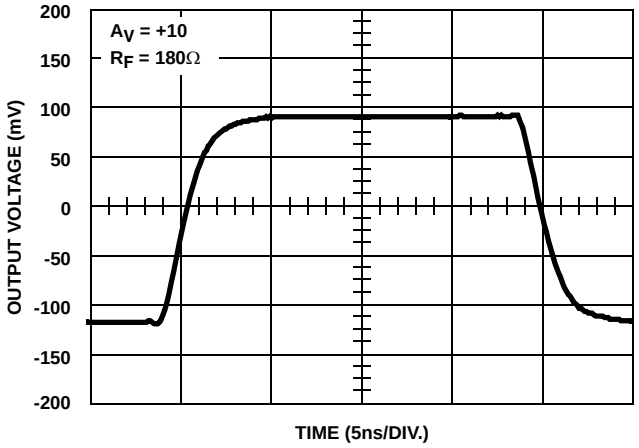


FIGURE 9. SMALL SIGNAL PULSE RESPONSE

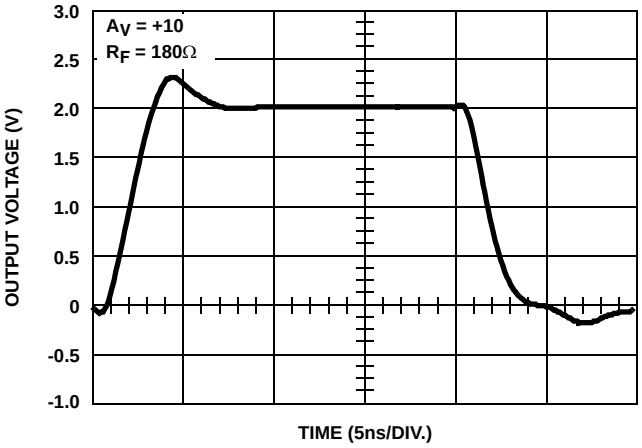


FIGURE 10. LARGE SIGNAL POSITIVE PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25°C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

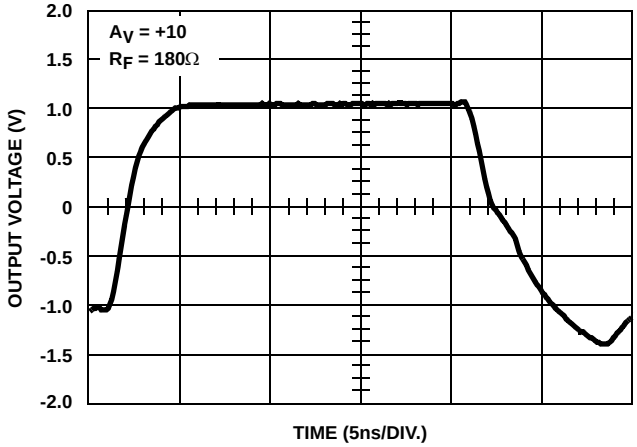


FIGURE 11. LARGE SIGNAL BIPOLAR PULSE RESPONSE

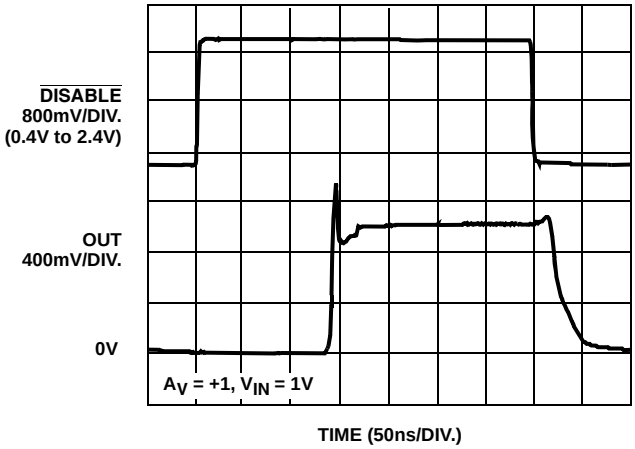


FIGURE 12. OUTPUT ENABLE AND DISABLE RESPONSE

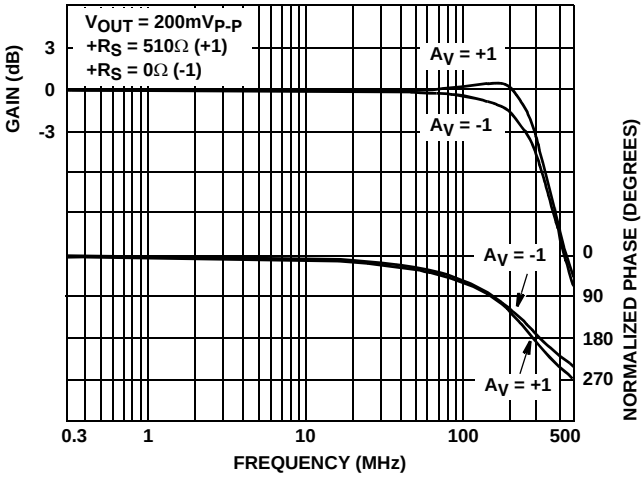


FIGURE 13. FREQUENCY RESPONSE

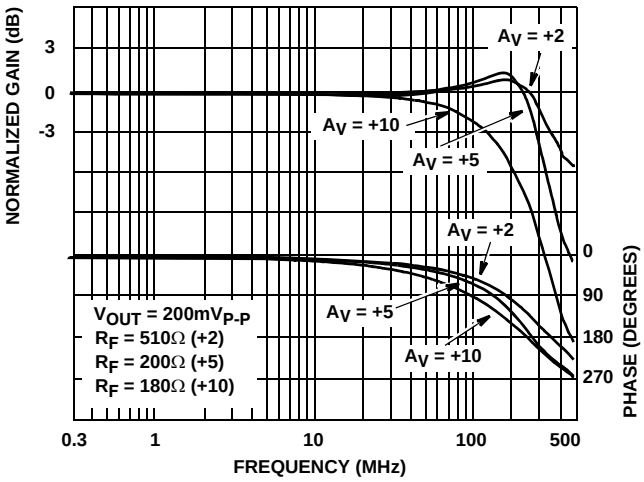


FIGURE 14. FREQUENCY RESPONSE

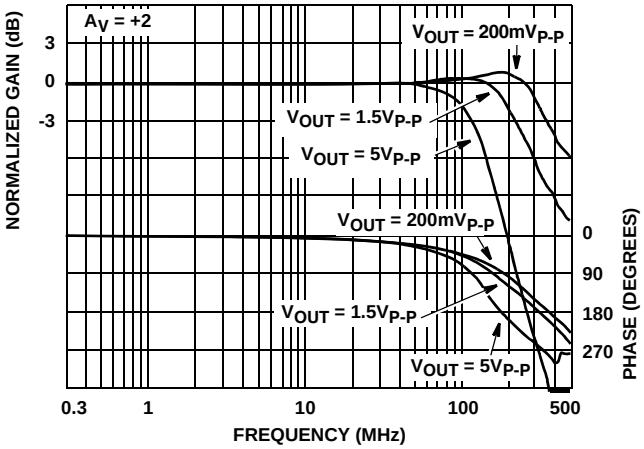


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

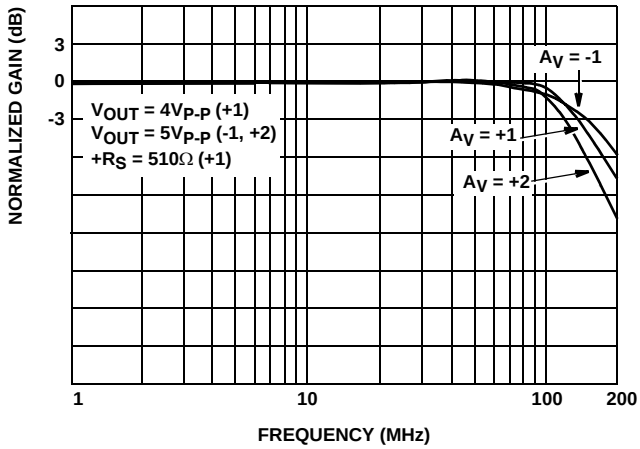


FIGURE 16. FULL POWER BANDWIDTH

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25°C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

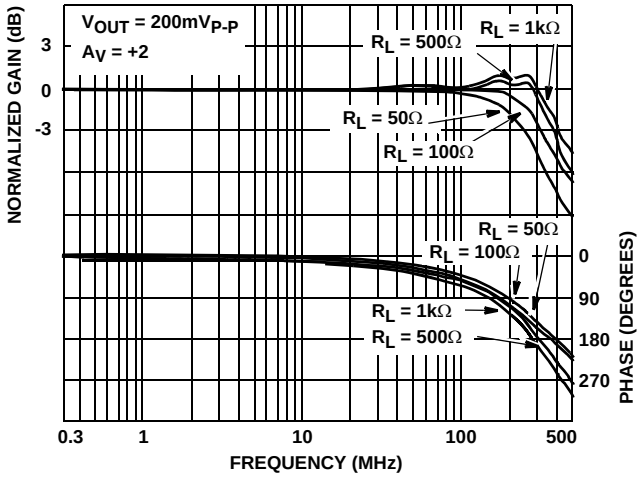


FIGURE 17. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

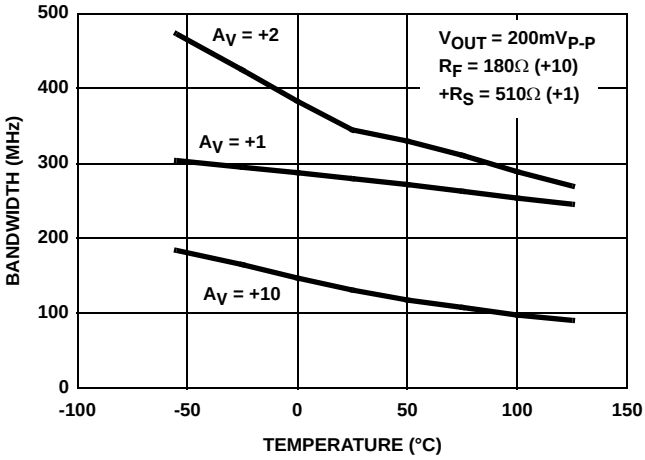


FIGURE 18. -3dB BANDWIDTH vs TEMPERATURE

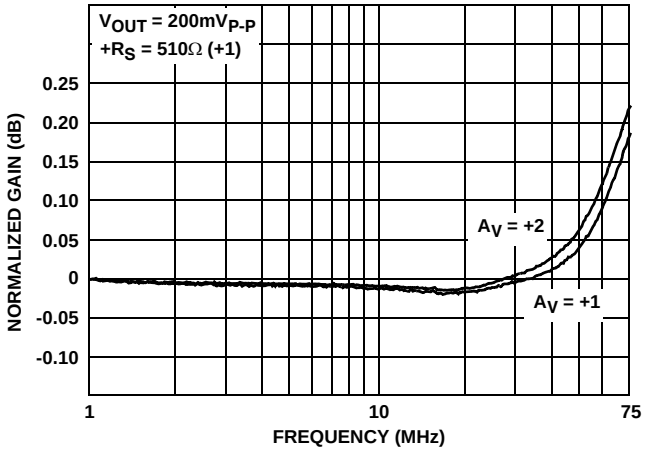


FIGURE 19. GAIN FLATNESS

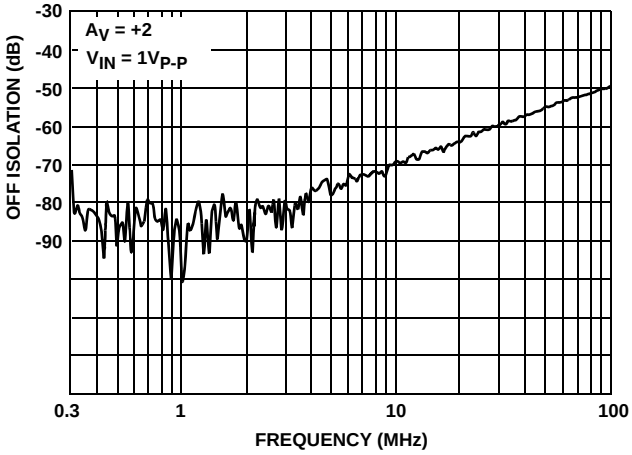


FIGURE 20. OFF ISOLATION

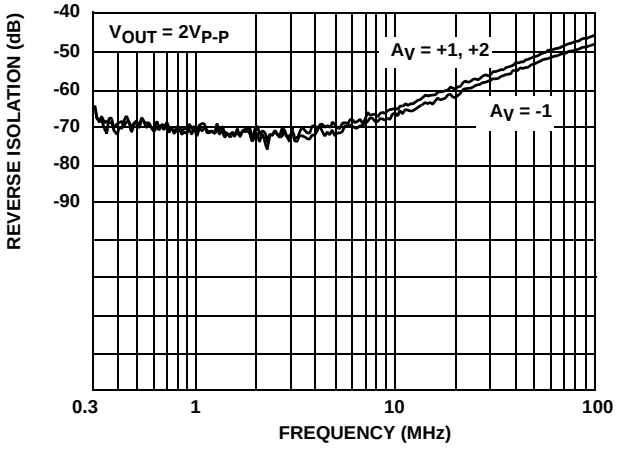


FIGURE 21. REVERSE ISOLATION (S_{12})

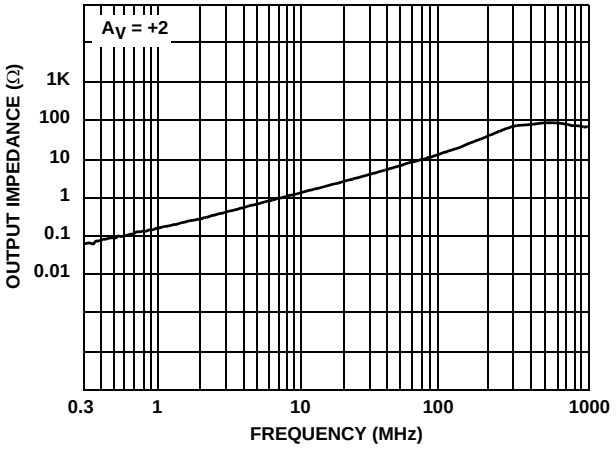


FIGURE 22. ENABLED OUTPUT IMPEDANCE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25°C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

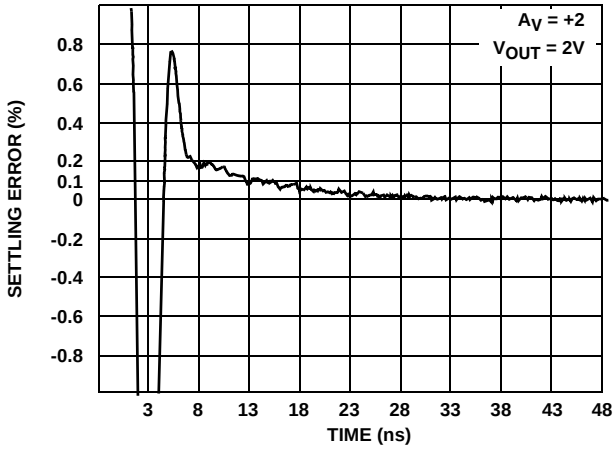


FIGURE 23. SETTLING RESPONSE

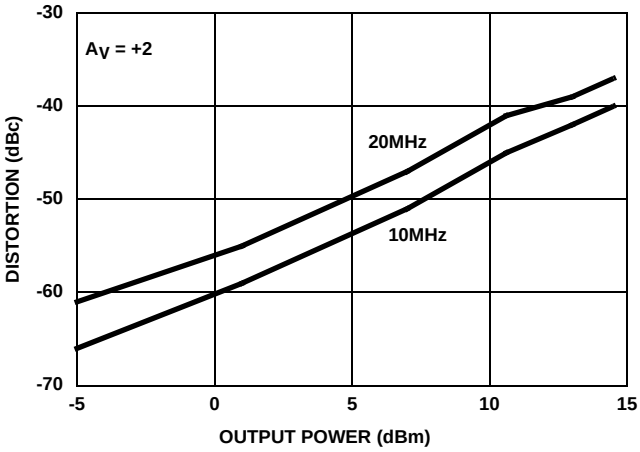


FIGURE 24. SECOND HARMONIC DISTORTION vs P_{OUT}

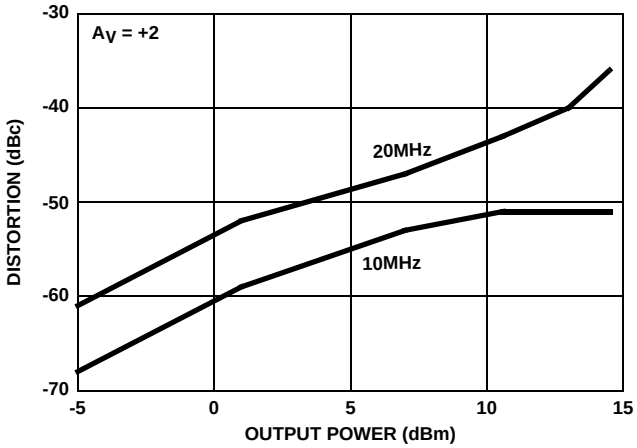


FIGURE 25. THIRD HARMONIC DISTORTION vs P_{OUT}

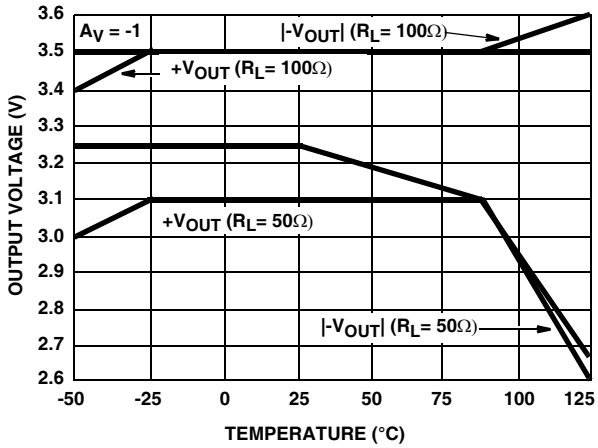


FIGURE 26. OUTPUT VOLTAGE vs TEMPERATURE

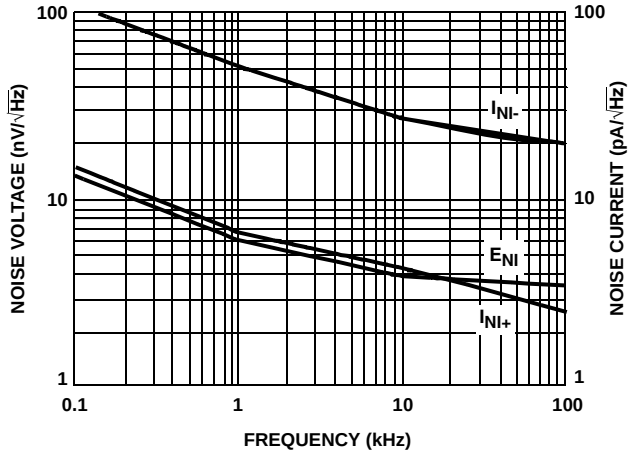


FIGURE 27. INPUT NOISE CHARACTERISTICS

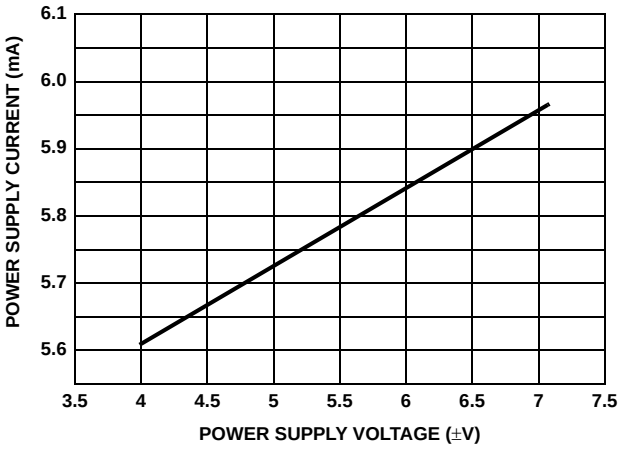


FIGURE 28. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

59 mils x 59 mils x 19 mils
1500µm x 1500µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

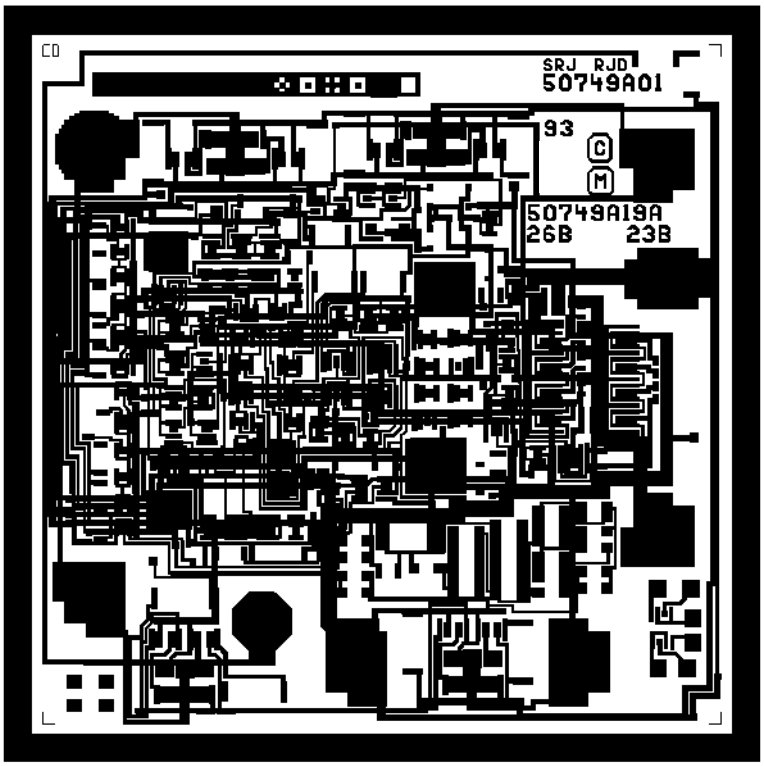
75

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1145



-IN

+IN

DISABLE

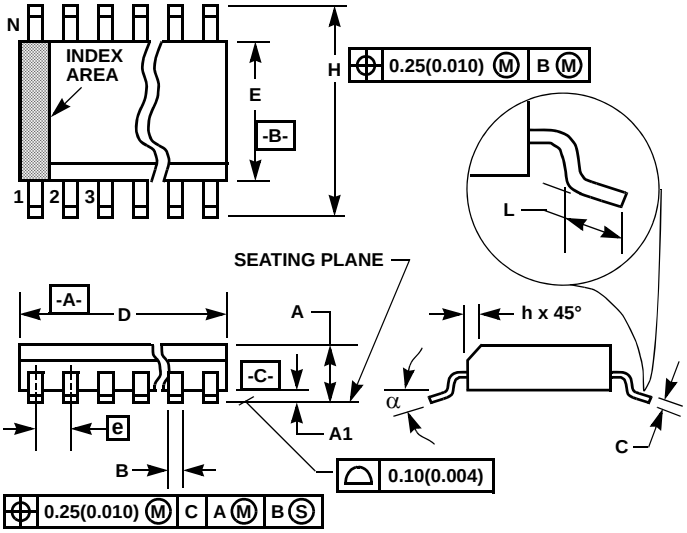
V+

OUT

V- OPTIONAL GND (NOTE)

NOTE: This pad is not bonded out on packaged units. Die users may set a GND reference, via this pad, to ensure the TTL compatibility of the $\overline{DIS}$ input when using asymmetrical supplies (e.g. V+ = 10V, V- = 0V). See the “Application Information” section for details.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

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