Active and Apparent Energy Metering IC with di/dt sensor interface

Preliminary Technical Data — ADE7753*

FEATURES

High Accuracy, supports IEC 61036 and IEC61268
On-Chip Digital Integrator enables direct interface with current sensors with di/dt output
The ADE7753 supplies Active, Reactive and Apparent Energy, Sampled Waveform, Current and Voltage RMS
Less than 0.1% error over a dynamic range of 1000 to 1
Positive only energy accumulation mode available
An On-Chip user Programmable threshold for line voltage surge and SAG, and PSU supervisory
Digital Power, Phase & Input Offset Calibration
An On-Chip temperature sensor (±3°C typical)
A SPI compatible Serial Interface
A pulse output with programmable frequency
An Interrupt Request pin (IRQ) and Status register
Proprietary ADCs and DSP provide high accuracy data over large variations in environmental conditions and time
Reference 2.4V±8% (20 ppm/°C typical) with external overdrive capability
Single 5V Supply, Low power (25mW typical)

GENERAL DESCRIPTION

The ADE7753 is an accurate active and apparent energy measurements IC with a serial interface and a pulse output. The ADE7753 incorporates two second order sigma delta ADCs, a digital integrator (on CH1), reference circuitry, temperature sensor, and all the signal processing required to perform RMS calculation on the voltage and current, active, reactive, and apparent energy measurement.

An on-chip digital integrator provides direct interface to di/dt current sensors such as Rogowski coils. The digital integrator eliminates the need for external analog integrator, and this solution provides excellent long-term stability and precise phase matching between the current and voltage channels. The integrator can be switched on and off based on the current sensor selected.

The ADE7753 contains an Active Energy register. It is capable of holding more than 200 seconds of accumulated power at full load. Data is read from the ADE7753 via the serial interface. The ADE7753 also provides a pulse output (CF) with output frequency is proportional to the active power.

In addition to rms calculation and active and apparent power information, the ADE7753 also accumulates the signed reactive energy. The ADE7753 also provides various system calibration features, i.e., channel offset correction, phase calibration and power calibration. The part also incorporates a detection circuit for short duration low or high voltage variations.

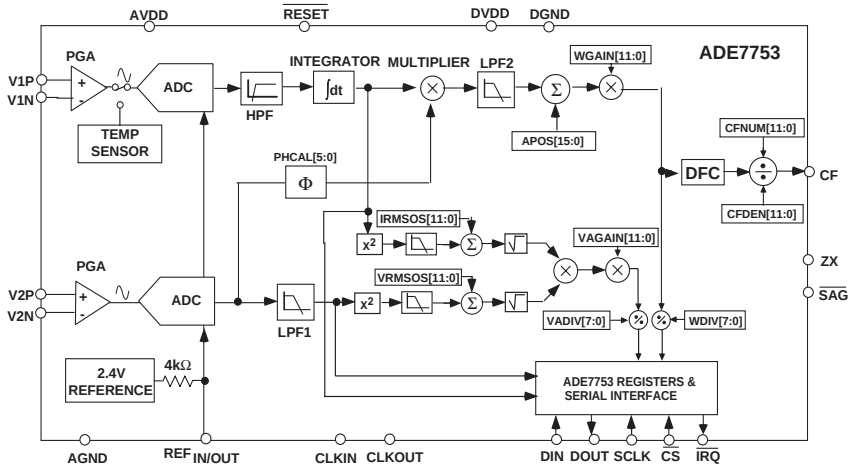
The ADE7753 has a positive only accumulation mode which gives the option to accumulate energy only when positive power is detected. An internal no-load threshold ensures that the part does not exhibit any creep when there is no load.

A zero crossing output (ZX) produces an output which is synchronized to the zero crossing point of the line voltage. This information is used in the ADE7753 to measure the line's period. The signal is also used internally to the chip in the line cycle Active and Apparent energy accumulation mode. This enables a faster and more precise energy accumulation and is useful during calibration. This signal is also useful for synchronization of relay switching with a voltage zero crossing.

The interrupt request output is an open drain, active low logic output. The Interrupt Status Register indicates the nature of the interrupt, and the Interrupt Enable Register controls which event produces an output on the $\overline{\text{IRQ}}$ pin.

The ADE7753 is available in 20-lead SSOP package.

FUNCTIONAL BLOCK DIAGRAM



*U.S. Patents 5,745,323; 5,760,617; 5,862,069; 5,872,469; others Pending.

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One Technology Way, P.O. Box 9106, Norwood. MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703
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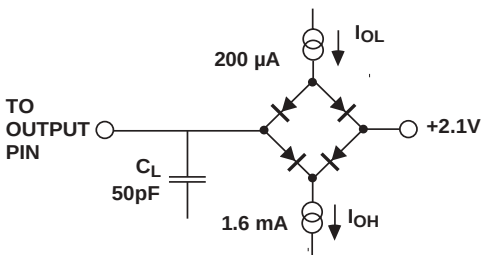
ADE7753–SPECIFICATIONS[1,3]

(AV_{DD} = DV_{DD} = 5V ± 5%, AGND = DGND = 0V, On-Chip Reference, CLKIN = 3.579545MHz XTAL, TMIN to TMAX = -40°C to +85°C)

Parameter	Spec	Units	Test Conditions/Comments
ENERGY MEASUREMENT ACCURACY			
Measurement Bandwidth	14	kHz	CLKIN = 3.579545 MHz
Measurement Error[1] on Channel 1			Channel 2 = 300mV rms/60Hz, Gain = 2
Channel 1 Range = 0.5V full-scale			
Gain = 1	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 2	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 4	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 8	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 16	0.2	% typ	Over a dynamic range 1000 to 1
Channel 1 Range = 0.25V full-scale			
Gain = 1	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 2	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 4	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 8	0.2	% typ	Over a dynamic range 1000 to 1
Gain = 16	0.2	% typ	Over a dynamic range 1000 to 1
Channel 1 Range = 0.125V full-scale			
Gain = 1	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 2	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 4	0.2	% typ	Over a dynamic range 1000 to 1
Gain = 8	0.2	% typ	Over a dynamic range 1000 to 1
Gain = 16	0.4	% typ	Over a dynamic range 1000 to 1
Phase Error[1] Between Channels	±0.05	° max	Line Frequency = 45Hz to 65Hz, HPF on
AC Power Supply Rejection[1]			AV_{DD} = DV_{DD} = 5V+175mV rms/ 120Hz
Output Frequency Variation (CF)	0.2	% typ	Channel 1 = 20mV rms, Gain = 16, Range = 0.5V Channel 2 = 300mV rms/60Hz, Gain = 1
DC Power Supply Rejection[1]			AV_{DD} = DV_{DD} = 5V ± 250mV dc
Output Frequency Variation (CF)	±0.3	% typ	Channel 1 = 20mV rms/60Hz, Gain = 16, Range = 0.5V Channel 2 = 300mV rms/60Hz, Gain = 1
ANALOG INPUTS			*See Analog Inputs Section*
Maximum Signal Levels	±0.5	V max	V1P, V1N, V2N and V2P to AGND
Input Impedance (dc)	390	kΩ min	
Bandwidth	14	kHz	CLKIN/256, CLKIN = 3.579545MHz
Gain Error[1,4]			External 2.5V reference, Gain = 1 on Channel 1 & 2
Channel 1			
Range = 0.5V full-scale	±4	% typ	V1 = 0.5V dc
Range = 0.25V full-scale	±4	% typ	V1 = 0.25V dc
Range = 0.125V full-scale	±4	% typ	V1 = 0.125V dc
Channel 2	±4	% typ	V2 = 0.5V dc
Gain Error Match[1]			External 2.5V reference
Channel 1			
Range = 0.5V full-scale	±0.3	% typ	Gain = 1, 2, 4, 8, 16
Range = 0.25V full-scale	±0.3	% typ	Gain = 1, 2, 4, 8, 16
Range = 0.125V full-scale	±0.3	% typ	Gain = 1, 2, 4, 8, 16
Channel 2	±0.3	% typ	Gain = 1, 2, 4, 8, 16
Offset Error[1]			
Channel 1	±10	mV max	Channel 1 Range = 0.5V
Channel 2	±10	mV max	Channel 2 Range = 0.5V
WAVEFORM SAMPLING			Sampling CLKIN/128, 3.579545MHz/128 = 27.9kSPS
Channel 1			*See Channel 1 Sampling*
Signal-to-Noise plus distortion	62	dB typ	150mV rms/60Hz, Range = 0.5V, Gain = 2
Bandwidth (-3dB)	14	kHz	CLKIN = 3.579545MHz
Channel 2			*See Channel 2 Sampling*
Signal-to-Noise plus distortion	52	dB typ	150mV rms/60Hz, Gain = 2
Bandwidth (-3dB)	140	Hz	CLKIN = 3.579545MHz

Parameter	Spec	Units	Test Conditions/Comments
REFERENCE INPUT			
$REF_{IN/OUT}$ Input Voltage Range	2.6	V max	2.4 V +8%
	2.2	V min	2.4V -8%
Input Capacitance	10	pF max	
ON-CHIP REFERENCE			Nominal 2.4V at $REF_{IN/OUT}$ pin
Reference Error	±200	mV max	
Current source	10	µA max	
Output Impedance	4	kΩ min	
Temperature Coefficient	20	ppm/°C typ	
CLKIN			Note all specifications CLKIN of 3.579545MHz
Input Clock Frequency	4	MHz max	
	1	MHz min	
LOGIC INPUTS			
$\overline{RESET}$, DIN, SCLK, CLKIN and $\overline{CS}$			
Input High Voltage, V_{INH}	2.4	V min	DV_{DD} = 5 V ± 10%
Input Low Voltage, V_{INL}	0.8	V max	DV_{DD} = 5 V ± 10%
Input Current, I_{IN}	±3	µA max	Typically 10nA, V_{IN} = 0V to DV_{DD}
Input Capacitance, C_{IN}	10	pF max	
LOGIC OUTPUTS[3]			
$\overline{SAG}$ & $\overline{IRQ}$			Open Drain outputs, 10kΩ pull up resistor
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5mA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 0.8mA
ZX & DOUT			
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5mA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 0.8mA
CF			
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5mA
Output Low Voltage, V_{OL}	1	V max	I_{SINK} = 7mA
POWER SUPPLY			For specified Performance
AV_{DD}	4.75	V min	5V - 5%
	5.25	V max	5V +5%
DV_{DD}	4.75	V min	5V - 5%
	5.25	V max	5V + 5%
AI_{DD}	3	mA max	Typically 2.0 mA
DI_{DD}	4	mA max	Typically 3.0 mA

NOTES:
[1]See Terminology Section for explanation of Specifications
[2]See Plots in Typical Performance Graphs
[3]Specifications subject to change without notice
[4]See Analog Inputs Section



Load Circuit for Timing Specifications

ORDERING GUIDE

MODEL	Package Option*
ADE7753ARS	RS-20
ADE7753ARSRL	RS-20
EVAL-ADE7753EB	ADE7753 evaluation board

* RS = Shrink Small Outline Package in tubes; RSRL = Shrink Small Outline Package in reel.

ADE7753

ADE7753 TIMING CHARACTERISTICS[1,2]

(AV_{DD} = DV_{DD} = 5V ± 5%, AGND = DGND = 0V, On-Chip Reference, CLKIN = 3.579545MHz XTAL, TMIN to TMAX = -40°C to +85°C)

Parameter	A, B Versions	Units	Test Conditions/Comments
Write timing			
t_1	20	ns (min)	$\overline{CS}$ falling edge to first SCLK falling edge
t_2	150	ns (min)	SCLK logic high pulse width
t_3	150	ns (min)	SCLK logic low pulse width
t_4	10	ns (min)	Valid Data Set up time before falling edge of SCLK
t_5	5	ns (min)	Data Hold time after SCLK falling edge
t_6	TBD	ns (min)	Minimum time between the end of data byte transfers.
t_7	TBD	ns (min)	Minimum time between byte transfers during a serial write.
t_8	100	ns (min)	$\overline{CS}$ Hold time after SCLK falling edge.
Read timing			
t_9	3.1	us (min)	Minimum time between read command (i.e. a write to Communication Reigster) and data read.
t_{10}	TBD	ns (min)	Minimum time between data byte transfers during a multibyte read.
t_{11}[3]	30	ns (min)	Data access time after SCLK rising edge following a write to the Communications Register
t_{12}[4]	100	ns (max)	Bus relinquish time after falling edge of SCLK.
	10	ns (min)	
t_{13}[4]	100	ns (max)	Bus relinquish time after rising edge of $\overline{CS}$.
	10	ns (min)	

NOTES

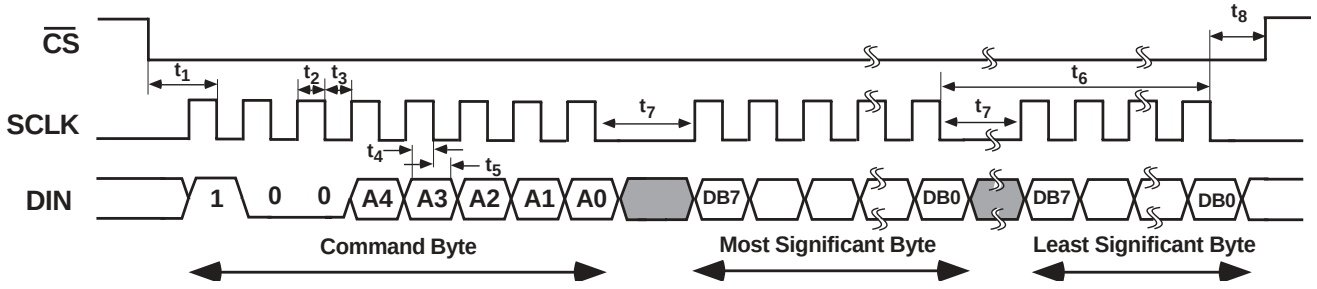
[1] Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are specified with tr = tf = 5ns (10% to 90%) and timed from a voltage level of 1.6V.

[2] See timing diagram below and Serial Interface section of this data sheet.

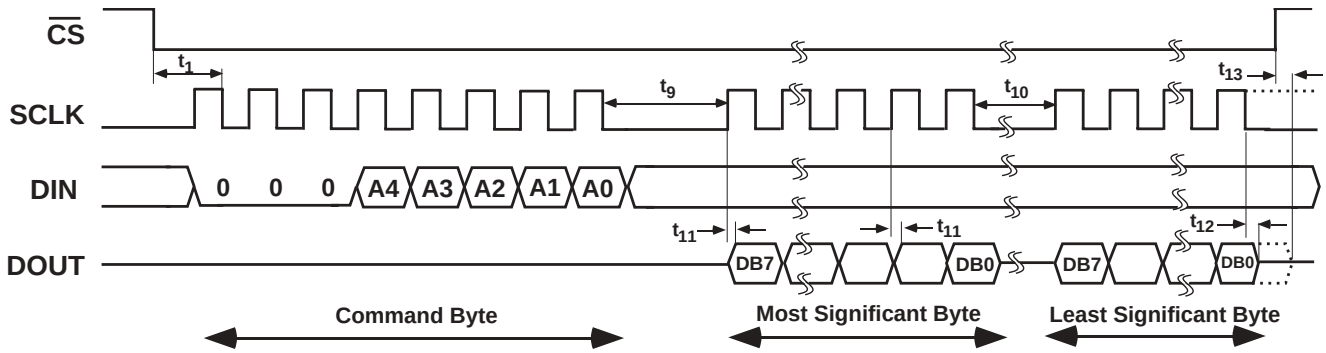
[3] Measured with the load circuit in Figure 1 and defined as the time required for the output to cross 0.8V or 2.4V.

[4] Derived from the measured time taken by the data outputs to change 0.5V when loaded with the circuit in Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50pF capacitor. This means that the time quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

Serial Write Timing



Serial Read Timing



ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
DV_{DD} toAV_{DD} ..... –0.3 V to +0.3 V
Analog Input Voltage to AGND
V_{1P}, V_{1N}, V_{2P} and V_{2N} ..... -6V to +6V
Reference Input Voltage to AGND .... –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Industrial ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
20 Pin SSOP, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 112°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADE7753 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Terminology

MEASUREMENT ERROR

The error associated with the energy measurement made by the ADE7753 is defined by the following formula:

$$Percentage\ Error = \left(\frac{Energy\ registered\ by\ ADE\,7753 - True\ Energy}{True\ Energy}\right)\times 100\%$$

PHASE ERROR BETWEEN CHANNELS

The digital integrator and the HPF (High Pass Filter) in Channel 1 have non-ideal phase response. To offset this phase response and equalize the phase response between channels, two phase correction network is placed in Channel 1: one for the digital integrator and the other for the HPF. Each phase correction network corrects the phase response of the corresponding component and ensures a phase match between Channel 1 (current) and Channel 2 (voltage) to within ±0.1° over a range of 45Hz to 65Hz and ±0.2° over a range 40Hz to 1kHz.

POWER SUPPLY REJECTION

This quantifies the ADE7753 measurement error as a percentage of reading when the power supplies are varied. For the AC PSR measurement a reading at nominal supplies (5V) is taken. A second reading is obtained with the same input signal levels when an ac (175mV rms/120Hz) signal is introduced onto the supplies. Any error introduced by this AC signal is expressed as a percentage of reading—see Measurement Error definition above.

For the DC PSR measurement a reading at nominal supplies (5V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied ±5%. Any error introduced is again expressed as a percentage of reading.

ADC OFFSET ERROR

This refers to the DC offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection - see characteristic curves. However, when HPF1 is switched on the offset is removed from Channel 1 (current) and the power calculation is not affected by this offset. The offsets may be removed by performing an offset calibration - see *Analog Inputs*.

GAIN ERROR

The gain error in the ADE7753 ADCs is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code - see Channel 1 ADC & Channel 2 ADC. It is measured for each of the input ranges on Channel 1 (0.5V, 0.25V and 0.125V). The difference is expressed as a percentage of the ideal code.

GAIN ERROR MATCH

The Gain Error Match is defined as the gain error (minus the offset) obtained when switching between a gain of 1 (for each of the input ranges) and a gain of 2, 4, 8, or 16. It is expressed as a percentage of the output ADC code obtained under a gain of 1. This gives the gain error observed when the gain selection is changed from 1 to 2, 4, 8 or 16.

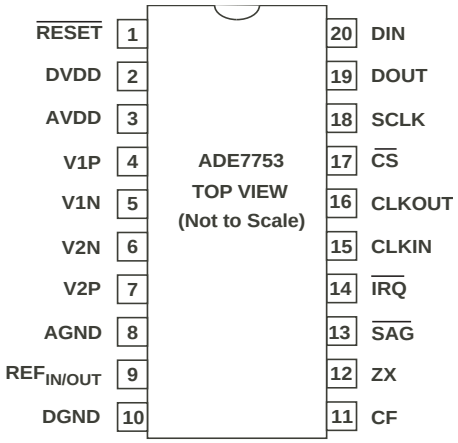
PIN FUNCTION DESCRIPTION

Pin No.	MNEMONIC	DESCRIPTION
1	$\overline{\text{RESET}}$	Reset pin for the ADE7753. A logic low on this pin will hold the ADCs and digital circuitry (including the Serial Interface) in a reset condition.
2	DV_{DD}	Digital power supply. This pin provides the supply voltage for the digital circuitry in the ADE7753. The supply voltage should be maintained at 5V ± 5% for specified operation. This pin should be decoupled to DGND with a 10µF capacitor in parallel with a ceramic 100nF capacitor.
3	AV_{DD}	Analog power supply. This pin provides the supply voltage for the analog circuitry in the ADE7753. The supply should be maintained at 5V ± 5% for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin by the use of proper decoupling. The typical performance graphs in this data sheet show the power supply rejection performance. This pin should be decoupled to AGND with a 10µF capacitor in parallel with a ceramic 100nF capacitor.
4,5	V1P, V1N	Analog inputs for Channel 1. This channel is intended for use with the di/dt current transducer such as Rogowski coil or other current sensor such as shunt or current transformer (CT). These inputs are fully differential voltage inputs with maximum differential input signal levels of ±0.5V, ±0.25V and ±0.125V, depending on the full scale selection - See *Analog Inputs*. Channel 1 also has a PGA with gain selections of 1, 2, 4, 8 or 16. The maximum signal level at these pins with respect to AGND is ±0.5V. Both inputs have internal ESD protection circuitry and in addition an overvoltage of ±6V can be sustained on these inputs without risk of permanent damage.
6,7	V2N, V2P	Analog inputs for Channel 2. This channel is intended for use with the voltage transducer. These inputs are fully differential voltage inputs with a maximum differential signal level of ±0.5V. Channel 2 also has a PGA with gain selections of 1, 2, 4, 8 or 16. The maximum signal level at these pins with respect to AGND is ±0.5V. Both inputs have internal ESD protection circuitry, and an overvoltage of ±6V can be sustained on these inputs without risk of permanent damage.
8	AGND	This pin provides the ground reference for the analog circuitry in the ADE7753, i.e. ADCs and reference. This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry, e.g. anti-aliasing filters, current and voltage transducers etc. In order to keep ground noise around the ADE7753 to a minimum, the quiet ground plane should only connected to the digital ground plane at one point. It is acceptable to place the entire device on the analog ground plane - see *Applications Information*.
9	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.4V ± 8% and a typical temperature coefficient of 20ppm/°C. An external reference source may also be connected at this pin. In either case this pin should be decoupled to AGND with a 1µF ceramic capacitor.
10	DGND	This provides the ground reference for the digital circuitry in the ADE7753, i.e. multiplier, filters and digital-to-frequency converter. Because the digital return currents in the ADE7753 are small, it is acceptable to connect this pin to the analog ground plane of the system - see *Applications Information*. However, high bus capacitance on the DOUT pin may result in noisy digital current which could affect performance.
11	CF	Calibration Frequency logic output. The CF logic output gives Active Power information. This output is intended to be used for operational and calibration purposes. The full-scale output frequency can be adjusted by writing to the CFDEN and CFNUM Register—see *Energy To Frequency Conversion*.
12	ZX	Voltage waveform (Channel 2) zero crossing output. This output toggles logic high and low at the zero crossing of the differential signal on Channel 2—see *Zero Crossing Detection*.
13	$\overline{\text{SAG}}$	This open drain logic output goes active low when either no zero crossings are detected or a low voltage threshold (Channel 2) is crossed for a specified duration. See *Line Voltage Sag Detection*.
14	$\overline{\text{IRQ}}$	Interrupt Request Output. This is an active low open drain logic output. Maskable interrupts include: Active Energy Register roll-over, Active Energy Register at half level, and arrivals of new waveform samples. See *ADE7753 Interrupts*.

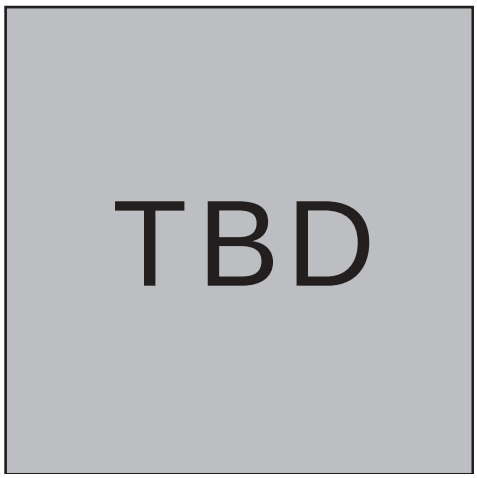
Pin No.	MNEMONIC	DESCRIPTION
15	CLKIN	Master clock for ADCs and digital signal processing. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7753. The clock frequency for specified operation is 3.579545MHz. Ceramic load capacitors of between 22pF and 33pF should be used with the gate oscillator circuit. Refer to crystal manufacturers data sheet for load capacitance requirements.
16	CLKOUT	A crystal can be connected across this pin and CLKIN as described above to provide a clock source for the ADE7753. The CLKOUT pin can drive one CMOS load when either an external clock is supplied at CLKIN or a crystal is being used.
17	$\overline{CS}$	Chip Select. Part of the four wire SPI Serial Interface. This active low logic input allows the ADE7753 to share the serial bus with several other devices. See *ADE7753 Serial Interface*.
18	SCLK	Serial Clock Input for the synchronous serial interface. All Serial data transfers are synchronized to this clock—see *ADE7753 Serial Interface*. The SCLK has a schmitt-trigger input for use with a clock source which has a slow edge transition time, e.g., opto-isolator outputs.
19	DOUT	Data Output for the Serial Interface. Data is shifted out at this pin on the rising edge of SCLK. This logic output is normally in a high impedance state unless it is driving data onto the serial data bus—see *ADE7753 Serial Interface*..
20	DIN	Data Input for the Serial Interface. Data is shifted in at this pin on the falling edge of SCLK—see *ADE7753 Serial Interface*..

PIN CONFIGURATION

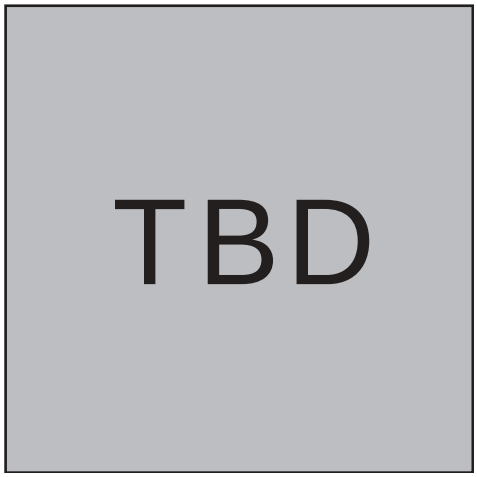
SSOP Packages



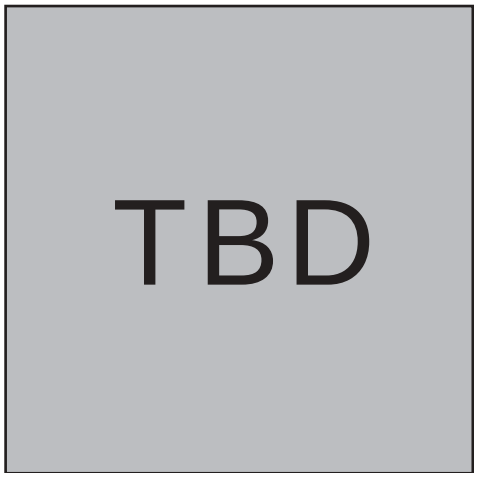
Typical Performance Characteristics-ADE7753



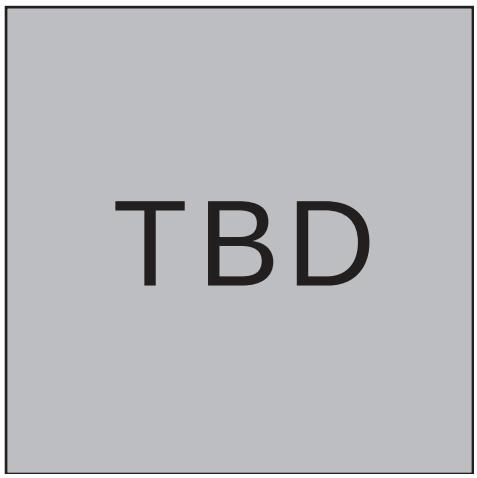
TPC 1— Error as a % of Reading (Gain=1)



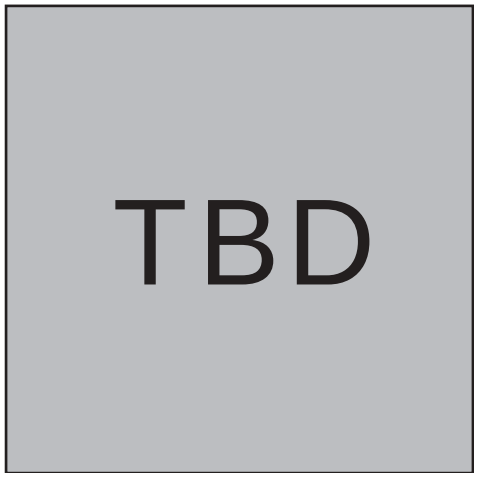
TPC 2— Error as a % of Reading (Gain=4)



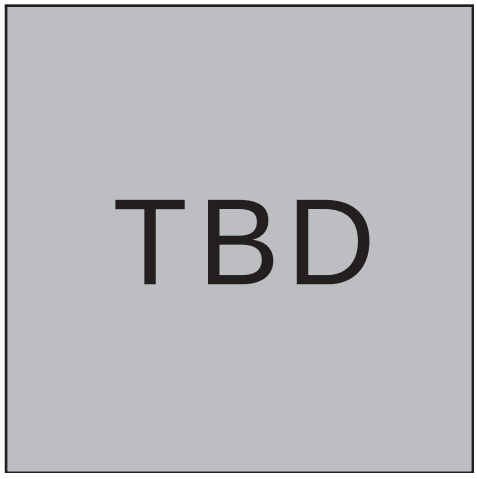
TPC 3— Error as a % of Reading (Gain=16)



TPC 4— Error as a % of Reading (Full-Scale input for Channel 1=0.25V, Gain=4)



TPC 5— Error as a % of Reading (Full-scale input for Channel 1=0.125V, Gain=8)



TPC 6— Test Circuits for Performance Curves

ANALOG INPUTS

The ADE7753 has two fully differential voltage input channels. The maximum differential input voltage for input pairs V1P/V1N and V2P/V2N are ±0.5V. In addition, the maximum signal level on analog inputs for V1P/V1N and V2P/V2N are ±0.5V with respect to AGND.

Each analog input channel has a PGA (Programmable Gain Amplifier) with possible gain selections of 1, 2, 4, 8 and 16. The gain selections are made by writing to the Gain register—see Figure 2. Bits 0 to 2 select the gain for the PGA in Channel 1 and the gain selection for the PGA in Channel 2 is made via bits 5 to 7. Figure 1 shows how a gain selection for Channel 1 is made using the Gain register.

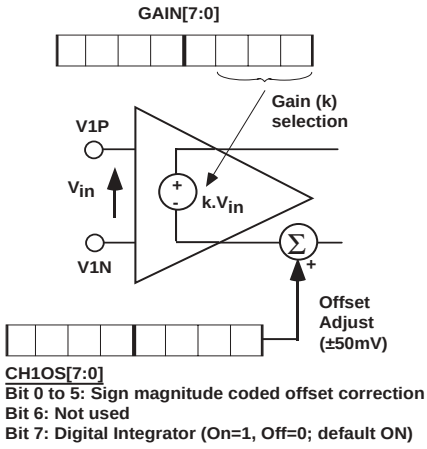


Figure 1— PGA in Channel 1

In addition to the PGA, Channel 1 also has a full scale input range selection for the ADC. The ADC analog input range selection is also made using the Gain register—see Figure 2. As mentioned previously the maximum differential input voltage is 1V. However, by using bits 3 and 4 in the Gain register, the maximum ADC input voltage can be set to 0.5V, 0.25V or 0.125V. This is achieved by adjusting the ADC reference—see *ADE7753 Reference Circuit*. Table I below summarizes the maximum differential input signal level on Channel 1 for the various ADC range and gain selections.

Table I

Maximum input signal levels for Channel 1

Max Signal Channel 1	ADC Input Range Selection 0.5V	0.25V	0.125V
0.5V	Gain = 1	—	—
0.25V	Gain = 2	Gain = 1	—
0.125V	Gain = 4	Gain = 2	Gain = 1
0.0625V	Gain = 8	Gain = 4	Gain = 2
0.0313V	Gain = 16	Gain = 8	Gain = 4
0.0156V	—	Gain = 16	Gain = 8
0.00781V	—	—	Gain = 16

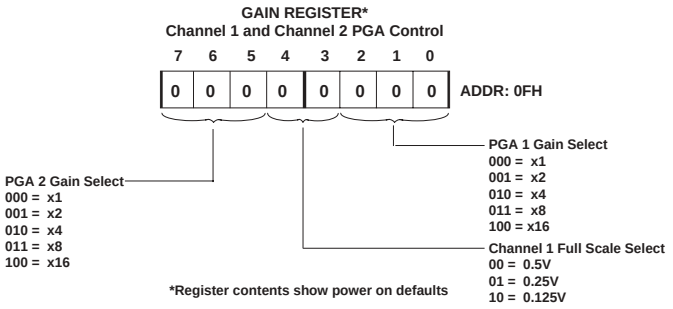


Figure 2— ADE7753 Analog Gain register

It is also possible to adjust offset errors on Channel 1 and Channel 2 by writing to the Offset Correction Registers (CH1OS and CH2OS respectively). These registers allow channel offsets in the range ±20mV to ±50mV (depending on the gain setting) to be removed. Note that it is not necessary to perform an offset correction in an Energy measurement application if HPF in Channel 1 is switched on. Figure 3 shows the effect of offsets on the real power calculation. As can be seen from Figure 3, an offset on Channel 1 and Channel 2 will contribute a dc component after multiplication. Since this dc component is extracted by LPF2 to generate the Active (Real) Power information, the offsets will have contributed an error to the Active Power calculation. This problem is easily avoided by enabling HPF in Channel 1. By removing the offset from at least one channel, no error component is generated at dc by the multiplication. Error terms at Cos(w.t) are removed by LPF2 and by integration of the Active Power signal in the Active Energy register (AENERGY[23:0]) – see *Energy Calculation*.

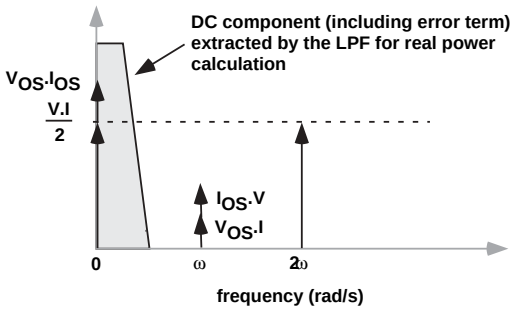


Figure 3— Effect of channel offsets on the real power calculation

The contents of the Offset Correction registers are 6-Bit, sign and magnitude coded. The weighting of the LSB size depends on the gain setting, i.e., 1, 2, 4, 8 or 16. Table II below shows the correctable offset span for each of the gain settings and the LSB weight (mV) for the Offset Correction registers. The maximum value which can be written to the offset correction registers is ±31 decimal —see Figure 4. Figure 4 shows the relationship between the Offset Correction register contents and the offset (mV) on the analog inputs for a gain setting of one. In order to perform an offset adjustment, The analog inputs should be first connected to AGND, and there should be no signal on either Channel 1 or Channel 2. A read from Channel 1 or Channel 2 using the

Table II
Offset Correction range

Gain	Correctable Span	LSB Size
1	±50mV	1.61mV/LSB
2	±37mV	1.19mV/LSB
4	±30mV	0.97mV/LSB
8	±26mV	0.84mV/LSB
16	±24mV	0.77mV/LSB

Waveform register will give an indication of the offset in the channel. This offset can be canceled by writing an equal and opposite offset value to the relevant offset register. The offset correction can be confirmed by performing another read. Note when adjusting the offset of Channel 1, one should disable the digital integrator and the HPF.

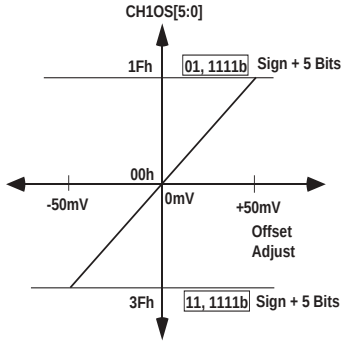


Figure 4– Channel Offset Correction Range (Gain = 1)

di/dt CURRENT SENSOR AND DIGITAL INTEGRATOR
di/dt sensor detects changes in magetic field caused by ac current. Figure 5 shows the principle of a di/dt current sensor.

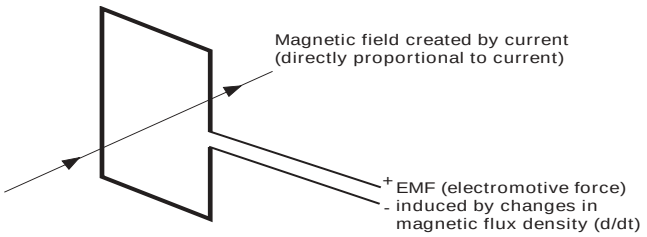


Figure 5– Principle of a di/dt current sensor

The flux density of a magnetic field induced by a current is directly proportional to the magnitude of the current. The changes in the magnetic flux density passing through a conductor loop generates an electromotive force (EMF) between the two ends of the loop. The EMF is a voltage signal which is proportional to the di/dt of the current. The voltage output from the di/dt current sensor is determined by the mutual inductance between the current carrying conductor and the di/dt sensor.

The current signal needs to be recovered from the di/dt signal before it can be used. An integrator is therefore necessary to restore the signal to its original form. The ADE7753 has a built-in digital integrator to recover the current signal from the di/dt sensor. The digital integrator on Channel 1 is switched off by default when the ADE7753 is powered up. Setting the MSB of CH1OS register will turn on the integrator. Figures 6 to 9 show the magnitude and phase response of the digital integrator.

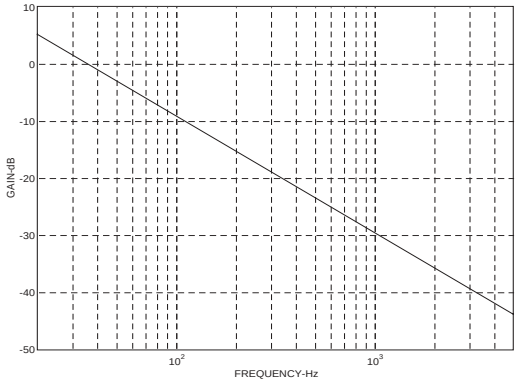


Figure 6– Combined gain response of the digital integrator and phase compensator

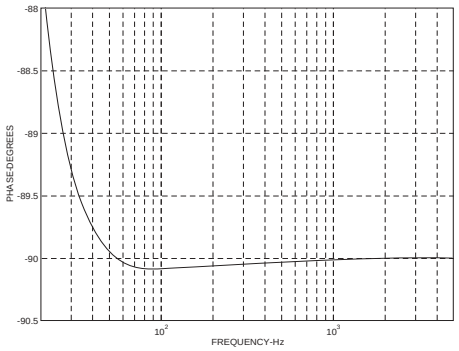


Figure 7– Combined phase response of the digital integrator and phase compensator

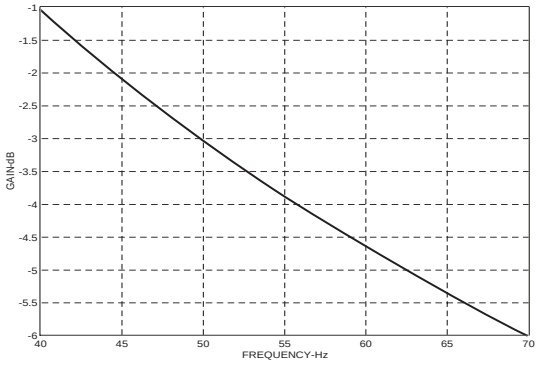


Figure 8– Combined gain response of the digital integrator and phase compensator (40Hz to 70Hz)

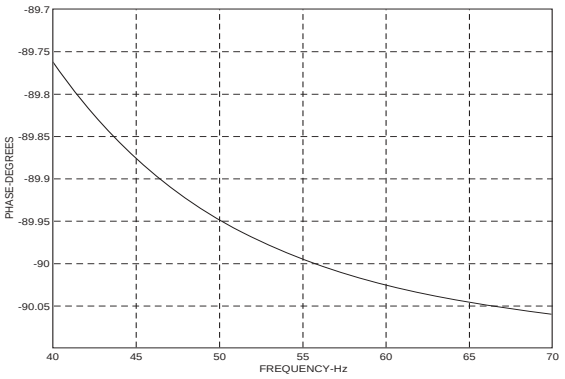


Figure 9– Combined phase response of the digital integrator and phase compensator (40Hz to 70Hz)

Note that the integrator has a -20dB/dec attenuation and approximately -90° phase shift. When combined with a di/dt sensor, the resulting magnitude and phase response should be a flat gain over the frequency band of interest. However, the di/dt sensor has a 20dB/dec gain associated with it, and generates significant high frequency noise, a more effective anti-aliasing filter is needed to avoid noise due to aliasing—see *Antialias Filter*.

When the digital integrator is switched off, the ADE7753 can be used directly with a conventional current sensor such as current transformer (CT) or a low resistance current shunt.

ZERO CROSSING DETECTION

The ADE7753 has a zero crossing detection circuit on Channel 2. This zero crossing is used to produce an external zero cross signal (ZX) and it is also used in the calibration mode - see *Energy Calibration*. The zero crossing signal is also used to initiate a temperature measurement on the ADE7753 - see *Temperature Measurement*.

Figure 10 shows how the zero cross signal is generated from the output of LPF1.

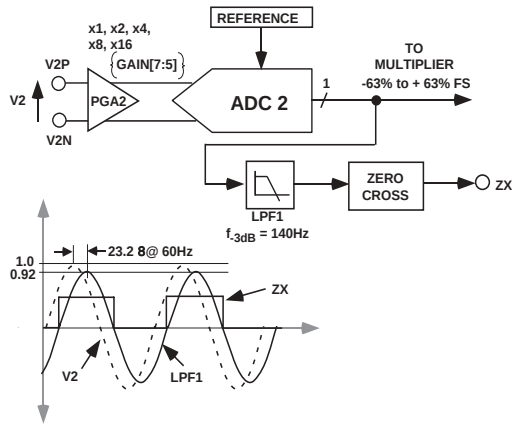


Figure 10– Zero cross detection on Channel 2

The ZX signal will go logic high on a positive going zero crossing and logic low on a negative going zero crossing on Channel 2. The zero crossing signal ZX is generated from the output of LPF1. LPF1 has a single pole at 156Hz (at CLKIN = 3.579545MHz). As a result there will be a phase lag between the analog input signal V2 and the output of LPF1. The phase response of this filter is shown in the *Channel 2 Sampling* section of this data sheet. The phase lag response of LPF1 results in a time delay of approximately 0.97ms (@ 60Hz) between the zero crossing on the analog inputs of Channel 2 and the rising or falling edge of ZX.

The zero-crossing detection also drives one flag bit in the interrupt status register. An active low in the IRQ output will also appear if the corresponding bit in the Interrupt Enable register is set to logic one.

The flag in the Interrupt status register as well as the IRQ output are reset to their default value when the Interrupt Status register with reset (RSTSTATUS) is read.

Zero Crossing Timeout

The zero crossing detection also has an associated time-out register ZXTOUT. This unsigned, 12-bit register is decremented (1 LSB) every 128/CLKIN seconds. The register is reset to its user programmed full scale value every time a zero crossing on Channel 2 is detected. The default power on value in this register is FFFh. If the register decrements to zero before a zero crossing is detected and the DISSAG bit in the Mode register is logic zero, the $\overline{\text{SAG}}$ pin will go active low. The absence of a zero crossing is also indicated on the $\overline{\text{IRQ}}$ pin if the ZXTO enable bit in the Interrupt Enable register is set to logic one. Irrespective of the enable bit setting, the ZXTO flag in the Interrupt Status register is always set when the ZXTOUT register is decremented to zero - see *ADE7753 Interrupts*.

The Zerocross Time-out register can be written/read by the user and has an address of 1Dh - see *Serial Interface* section. The resolution of the register is 128/CLKIN seconds per LSB. Thus the maximum delay for an interrupt is 0.15 second ($128/\text{CLKIN} \times 2^{12}$).

Figure 11 shows the mechanism of the zero crossing time out detection when the line voltage stays at a fixed DC level for more than CLKIN/128 x ZXTOUT seconds.

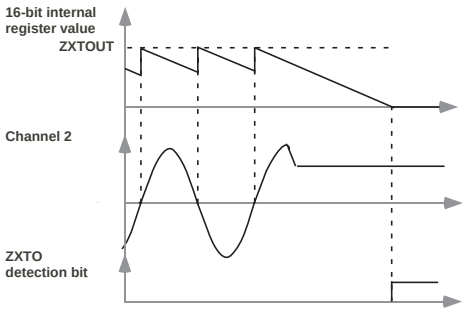


Figure 11 - Zero crossing Time out detection

PERIOD MEASUREMENT

The ADE7753 provides also the period measurement of the line. The period register is an unsigned 15-bit register and is updated every period.

The resolution of this register is 2.2ms/LSB when CLKIN=3.579545MHz, which represents 0.013% when the line frequency is 60Hz. When the line frequency is 60Hz, the value of the Period register is approximately 7576d. The length of the register enables the measurement of line frequencies as low as 13.9Hz.

POWER SUPPLY MONITOR

The ADE7753 also contains an on-chip power supply monitor. The Analog Supply (AV_{DD}) is continuously monitored by the ADE7753. If the supply is less than 4V ± 5% then the ADE7753 will go into an inactive state, i.e. no energy will be accumulated when the supply voltage is below 4V. This is useful to ensure correct device operation at power up and during power down. The power supply monitor has built-in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies.

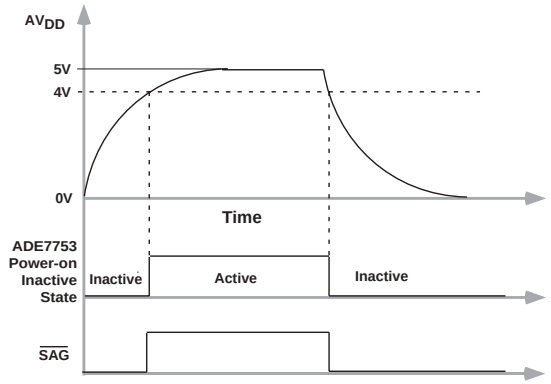


Figure 12 - On-Chip power supply monitor

As can be seen from Figure 12 the trigger level is nominally set at 4V. The tolerance on this trigger level is about ±5%. The $\overline{SAG}$ pin can also be used as a power supply monitor input to the MCU. The $\overline{SAG}$ pin will go logic low when the ADE7753 is in its inactive state. The power supply and decoupling for the part should be such that the ripple at AV_{DD} does not exceed 5V±5% as specified for normal operation.

LINE VOLTAGE SAG DETECTION

In addition to the detection of the loss of the line voltage signal (zero crossing), the ADE7753 can also be programmed to detect when the absolute value of the line voltage drops below a certain peak value, for a number of line cycles. This condition is illustrated in Figure 13 below.

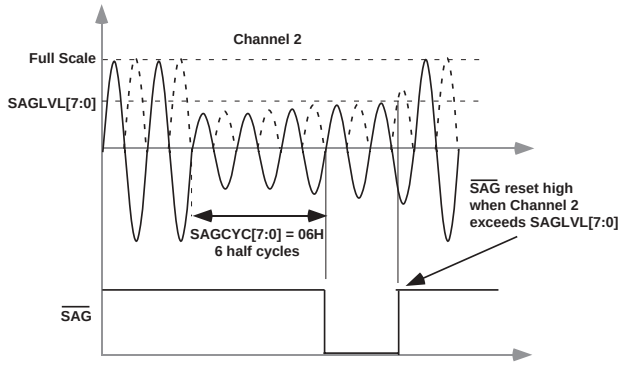


Figure 13– ADE7753 Sag detection

Figure 13 shows the line voltage fall below a threshold which is set in the Sag Level register (SAGLVL[7:0]) for five line cycles. Since the Sag Cycle register (SAGCYC[7:0]) contains 03h the $\overline{SAG}$ pin will go active low at the end of the fifth line cycle for which the line voltage falls below the threshold, if the DISSAG bit in the Mode register is logic zero. As is the case when zero-crossings are no longer detected, the sag event is also recorded by setting the SAG flag in the Interrupt Status register. If the SAG enable bit is set to logic one, the $\overline{IRQ}$ logic output will go active low - see *ADE7753 Interrupts*. The $\overline{SAG}$ pin will go logic high again when the absolute value of the signal on Channel 2 exceeds the sag level set in the Sag Level register. This is shown in Figure 13 when the $\overline{SAG}$ pin goes high during the tenth line cycle from the time when the signal on Channel 2 first dropped below the threshold level.

Sag Level Set

The contents of the Sag Level register (1 byte) are compared to the absolute value of the most significant byte output from LPF1, after it is shifted left by one bit. Thus for example the nominal maximum code from LPF1 with a full scale signal on Channel 2 is 2518h—see *Channel 2 sampling*. Shifting one bit left will give 4A30h. Therefore writing 4Ah to the SAG Level register will put the sag detection level at full scale. Writing 00h will put the sag detection level at zero. The Sag Level register is compared to the most significant byte of a waveform sample after the shift left and detection is made when the contents of the sag level register are greater.

PEAK DETECTION

The ADE7753 can also be programmed to detect when the absolute value of the voltage or the current channel of one phase exceeds a certain peak value. Figure 14 illustrates the behavior of the peak detection for the voltage channel.

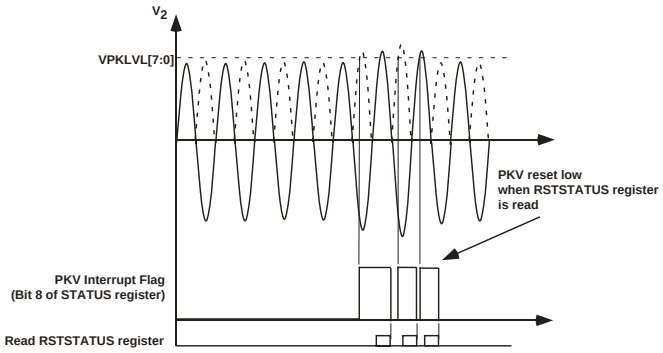


Figure 14 - ADE7753 Peak detection

Both channel 1 and channel 2 are monitored at the same time. Figure 14 shows a line voltage exceeding a threshold which is set in the Voltage peak register (VPKLVL[7:0]). The Voltage Peak event is recorded by setting the PKV flag in the Interrupt Status register. If the PKV enable bit is set to logic one in the Interrupt Mask register, the $\overline{IRQ}$ logic output will go active low. Similarly, the Current Peak event is recorded by setting the PKI flag in the Ineterrupt Status register—see *ADE7753 Interrupts.*

Peak Level Set

The contents of the VPKLVL and IPKLVL registers are respectively compared to the absolute value of channel 1 and channel 2, after they are multiplied by 2.

Thus, for example, the nominal maximum code from the channel 1 ADC with a full scale signal is 2851ECh —see *Channel 1 Sampling*. Multiplying by 2 will give 50A3D8h. Therefore, writing 50h to the IPKLVL register will put the channel 1 peak detection level at full scale and set the current peak detection to its least sensitive value.
Writing 00h will put the channel 1 detection level at zero. The detection is done when the content of the IPKLVL register is smaller than the incoming channel 1 sample.

Peak Level Record
The ADE7753 records the maximum absolute value reached by channel 1 and channel 2 in two different registers - IPEAK and VPEAK respectively. VPEAK and IPEAK are 24-bit unsigned registers. These registers are updated each time the absolute value of the Waveform sample from the corresponding channel is above the value stored in the VPEAK or IPEAK register. The contents of the VPEAK register corresponds to 2 times the maximum absolute value observed on the channel 2 input. The contents of IPEAK represents the max absolute value observed on the channel 1 input. Reading the RSTVPEAK and RSTIPEAK registers will clear their respective contents after the read operation.

ADE7753 INTERRUPTS
ADE7753 Interrupts are managed through the Interrupt Status register (STATUS[15:0]) and the Interrupt Enable register (IRQEN[15:0]). When an interrupt event occurs in the ADE7753, the corresponding flag in the Status register is set to a logic one - see Interrupt Status register. If the enable bit for this interrupt in the Interrupt Enable register is logic one, then the $\overline{IRQ}$ logic output goes active low. The flag bits in the Status register are set irrespective of the state of the enable bits.
In order to determine the source of the interrupt, the system master (MCU) should perform a read from the Status register with reset (RSTSTATUS[15:0]). This is achieved by carrying out a read from address 0Ch. The $\overline{IRQ}$ output will go logic high on completion of the Interrupt Status register read command—see *Interrupt timing*. When carrying out a read with reset, the ADE7753 is designed to ensure that no interrupt events are missed. If an interrupt event occurs just as the Status register is being read, the event will not be lost and the $\overline{IRQ}$ logic output is guaranteed to go high for the duration of the Interrupt Status register data transfer before going logic low again to indicate the pending interrupt. See the next section for a more detailed description.

Using the ADE7753 Interrupts with an MCU
Shown in Figure 15 is a timing diagram which shows a suggested implementation of ADE7753 interrupt management using an MCU. At time t_1 the $\overline{IRQ}$ line will go active low indicating that one or more interrupt events have occurred in the ADE7753. The $\overline{IRQ}$ logic output should be tied to a negative edge triggered external interrupt on the MCU. On detection of the negative edge, the MCU should be configured to start executing its Interrupt Service Routine (ISR). On entering the ISR, all interrupts should be disabled using the global interrupt enable bit. At this point the MCU external interrupt flag can be cleared in order to capture interrupt events which occur during the current ISR. When the MCU interrupt flag is cleared a read from the Status register with reset is carried out. This will cause the $\overline{IRQ}$ line to be reset logic high (t_2)—see *Interrupt timing*. The Status register contents are used to determine the source of the interrupt(s) and hence the appropriate action to be taken. If a subsequent interrupt event occurs during the ISR, that event will be recorded by the MCU external interrupt flag being set again (t_3). On returning from the ISR, the global interrupt mask will be cleared (same instruction cycle) and the external interrupt flag will cause the MCU to jump to its ISR once again. This will ensure that the MCU does not miss any external interrupts.

Interrupt timing
The *ADE7753 Serial Interface* section should be reviewed first before reviewing the interrupt timing. As previously de-

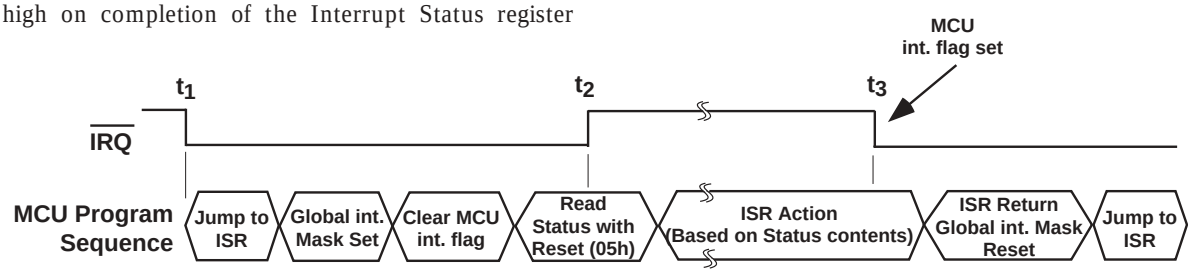


Figure 15– ADE7753 interrupt management

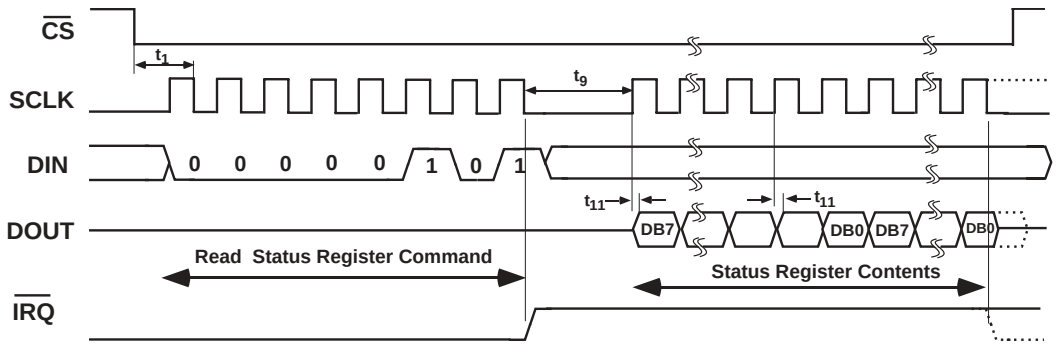


Figure 16– ADE7753 interrupt timing

scribed, when the $\overline{IRQ}$ output goes low the MCU ISR must read the Interrupt Status register in order to determine the source of the interrupt. When reading the Status register contents, the $\overline{IRQ}$ output is set high on the last falling edge of SCLK of the first byte transfer (read Interrupt Status register command). The $\overline{IRQ}$ output is held high until the last bit of the next 15-bit transfer is shifted out (Interrupt Status register contents)— see Figure 16. If an interrupt is pending at this time, the $\overline{IRQ}$ output will go low again. If no interrupt is pending the $\overline{IRQ}$ output will stay high.

TEMPERATURE MEASUREMENT

ADE7753 also includes an on-chip temperature sensor. A temperature measurement can be made by setting bit 5 in the Mode register. When bit 5 is set logic high in the Mode register, the ADE7753 will initiate a temperature measurement on the next zero crossing. When the zero crossing on Channel 2 is detected the voltage output from the temperature sensing circuit is connected to ADC1 (Channel 1) for digitizing. The resultant code is processed and placed in the Temperature register (TEMP[7:0]) approximately 26µs later (24 CLKIN cycles). If enabled in the Interrupt Enable register (bit 5), the $\overline{IRQ}$ output will go active low when the temperature conversion is finished. Please note that temperature conversion will introduce a small amount of noise in the energy calculation. If temperature conversion is performed frequently (e.g. multiple times per second), a noticeable error will accumulate in the resulting energy calculation over time.

The contents of the Temperature register are signed (2's complement) with a resolution of approximately 1 LSB/°C. The temperature register will produce a code of 00h when the ambient temperature is approximately 70°C. The temperature measurement is uncalibrated in the ADE7753 and has an offset tolerance that could be as high as ±20°C.

ADE7753 ANALOG TO DIGITAL CONVERSION

The analog-to-digital conversion in the ADE7753 is carried out using two second order sigma-delta ADCs. For simplicity reason, the block diagram in Figure 17 shows a first order sigma-delta ADC. The converter is made up of two parts: the sigma-delta modulator and the digital low pass filter.

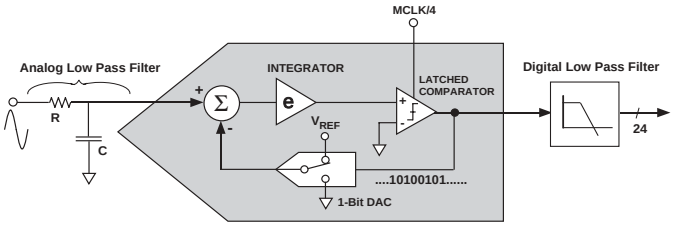


Figure 17– First Order Sigma-Delta (Σ–Δ) ADC

A sigma-delta modulator converts the input signal into a continuous serial stream of 1's and 0's at a rate determined by the sampling clock. In the ADE7753 the sampling clock is equal to CLKIN/4. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough the average value of the DAC output (and therefore the bit stream) will approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged will a meaningful result be obtained. This averaging is carried out in the second part of the ADC, the digital low pass filter. By averaging a large number of bits from the modulator the low pass filter can produce 24-bit data words which are proportional to the input signal level.

The sigma-delta converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is over-sampling. By over sampling we mean that the signal is sampled at a rate (frequency) which is many times higher than the bandwidth of interest. For example the sampling rate in the ADE7753 is CLKIN/4 (894kHz) and the band of interest is 40Hz to 2kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered—see Figure 18. However, oversampling alone is not an efficient enough method to improve the signal to noise ratio (SNR) in the band of interest. For example, an oversampling ratio of 4 is required just to increase the SNR by only 6dB (1-Bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. This is what happens in the sigma-delta modulator, the noise is shaped by the integrator which has a high pass type response for the quantization noise. The result is that most of the noise is at the higher frequencies where it can be removed by the digital low pass filter. This noise shaping is also shown in Figure 18.

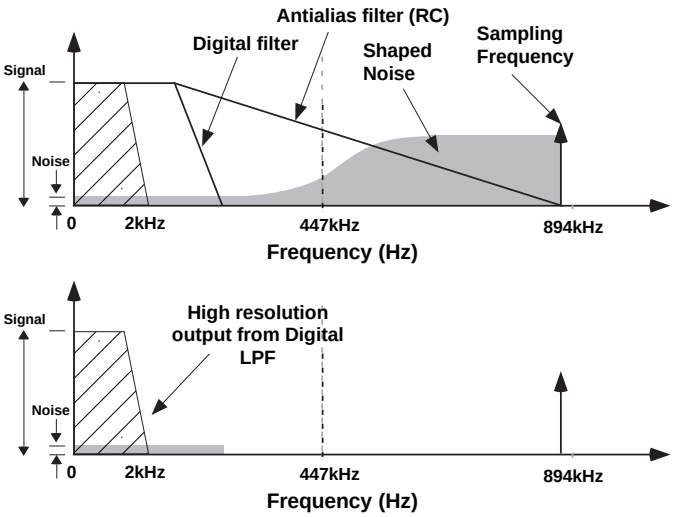


Figure 18– Noise reduction due to Oversampling & Noise shaping in the analog modulator

Antialias Filter

Figure 17 also shows an analog low pass filter (RC) on the input to the modulator. This filter is present to prevent aliasing. Aliasing is an artifact of all sampled systems. Basically it means that frequency components in the input signal to the ADC which are higher than half the sampling rate of the ADC will appear in the sampled signal at a

frequency below half the sampling rate. Figure 19 illustrates the effect. Frequency components (arrows shown in black) above half the sampling frequency (also know as the Nyquist frequency, i.e., 447kHz) get imaged or folded back down below 447kHz (arrows shown in grey). This will happen with all ADCs regardless of the architecture. In the example shown, only frequencies near the sampling frequency, i.e., 894kHz, will move into the band of interest for metering, i.e, 40Hz - 2kHz. This allows the usage of very simple LPF (Low Pass Filter) to attenuate high frequency (near 900kHz) noise and prevents distortion in the band of interest. For conventional current sensor, a simple RC filter (single pole LPF) with a corner frequency of 10kHz will produce an attenuation of approximately 40dBs at 894kHz—see Figure 18. The 20dB per decade attenuation is usually sufficient to eliminate the effects of aliasing for conventional current sensor.
For di/dt sensor such as Rogowski coil, however, the sensor has 20dB per decade gain. This will neutralize the -20dB per decade attenuation produced by the simple LPF. Therefore, when using a di/dt sensor, care should be taken to offset the 20dB per decade gain coming from the di/dt sensor. One simple approach is to cascade two RC filters to produce the -40dB per decade attenuation needed.

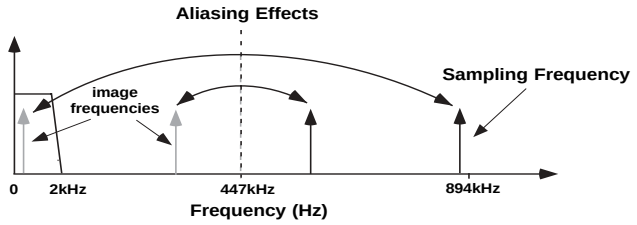


Figure 19 —ADC and signal processing in Channel 1

ADC transfer function
Below is an expression which relates the output of the LPF in the sigma-delta ADC to the analog input signal level. Both ADCs in the ADE7753 are designed to produce the same output code for the same input signal level.

$$Code\ (ADC) = 3.0492 \times \frac{V_{in}}{V_{out}} \times 262{,}144$$

Therefore with a full scale signal on the input of 0.5V and an internal reference of 2.42V, the ADC output code is nominally 165,151 or 2851Fh. The maximum code from the ADC is ±262,144, this is equivalent to an input signal level of ±0.794V. However for specified performance it is not recommended that the full-scale input signal level of 0.5V be exceeded.

ADE7753 Reference circuit
Shown below in Figure 20 is a simplified version of the reference output circuitry. The nominal reference voltage at the $REF_{IN/OUT}$ pin is 2.42V. This is the reference voltage used for the ADCs in the ADE7753. However, Channel 1 has three input range selections which are selected by dividing down the reference value used for the ADC in Channel 1. The reference value used for Channel 1 is divided down to ½ and ¼ of the nominal value by using an internal resistor divider as shown in Figure 20.

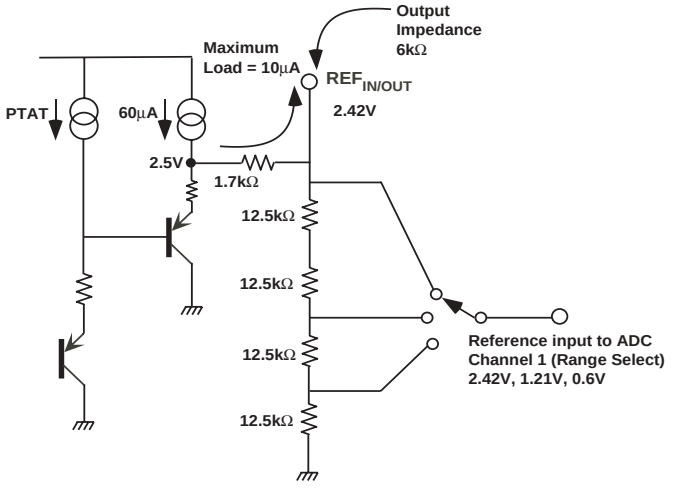


Figure 20 —ADE7753 Reference Circuit Ouput

The $REF_{IN/OUT}$ pin can be overdriven by an external source, e.g., an external 2.5V reference. Note that the nominal reference value supplied to the ADCs is now 2.5V not 2.42V. This has the effect of increasing the nominal analog input signal range by 2.5/2.42×100% = 3% or from 0.5V to 0.5165V.

The voltage of ADE7753 reference drifts slightly with temperature—see *ADE7753 Specifications* for the temperature coefficient specification (in ppm/°C) . The value of the temperature drift varies from part to part. Since the reference is used for the ADCs in both Channel 1 and 2, any *x*% drift in the reference will result in 2*x*% deviation of the meter accuracy. The reference drift resulting from temperature changes is usually very small and it is typically much smaller than the drift of other components on a meter. However, if guaranteed temperature performance is needed, one needs to use an external voltage reference. Alternatively, the meter can be calibrated at multiple temperatures. Real time compensation can be easily achieved using the on the on-chip temperature sensor.

CHANNEL 1 ADC
Figure 21 shows the ADC and signal processing chain for Channel 1. In waveform sampling mode the ADC outputs a signed 2's Complement 24-bit data word at a maximum of 27.9kSPS (CLKIN/128). With the specified full scale analog input signal of 0.5V (or 0.25V or 0.125V – see *Analog Inputs* section) the ADC will produce an output code which is approximately between 2851ECh (+2,642,412 Decimal) and D7AE14h (-2,642,412 Decimal). This is illustrated in Figure 21.

Channel 1 Sampling
The waveform samples may also be routed to the WAVEFORM register (MODE[14:13] = 1,0) to be read by the system master (MCU). In waveform sampling mode the WSMP bit (bit 3) in the Interrupt Enable register must also be set to logic one. The Active, Apparent Power and Energy calculation will remain uninterrupted during waveform sampling.
When in waveform sample mode, one of four output sample rates may be chosen by using bits 11 and 12 of the Mode register (WAVSEL1,0). The output sample rate may be 27.9kSPS, 14kSPS, 7kSPS or 3.5kSPS—see *Mode Register*. The interrupt request output $\overline{IRQ}$ signals a new sample

availability by going active low. The timing is shown in Figure 22. The 24-bit waveform samples are transferred from the ADE7753 one byte (8-bits) at a time, with the most significant byte shifted out first. The 24-bit data word is right justified - see *ADE7753 Serial Interface*.

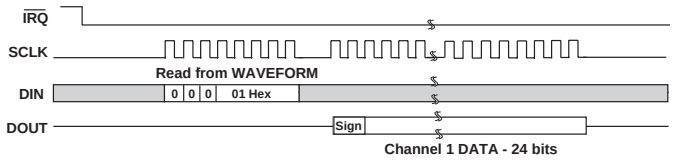


Figure 22 – Waveform sampling Channel 1

The interrupt request output IRQ stays low until the interrupt routine reads the Reset Status register - *see ADE7753 Interrupt*.

Channel 1 RMS calculation

Root Mean Square (RMS) value of a continuous signal V(t) is defined as:

$$V_{rms} = \sqrt{\frac{1}{T} \cdot \int_0^T V^2(t)dt} \quad (1)$$

For time sampling signals, rms calculation involves squaring the signal, taking the average and obtaining the square root:

$$V_{rms} = \sqrt{\frac{1}{N} \cdot \sum_{i=1}^{N} V^2(i)} \quad (2)$$

ADE7753 calculates simultaneously the RMS values for Channel 1 and Channel 2 in different register. Figure 23 shows the detail of the signal processing chain for the RMS calculation on channel 1. The channel 1 RMS value is processed from the samples used in the channel 1 waveform sampling mode. The channel 1 RMS value is stored in an unsigned 24-bit register (IRMS). One LSB of the channel 1 RMS register is equivalent to one LSB of a channel 1 waveform sample. The update rate of the channel 1 RMS measurement is CLKIN/4.

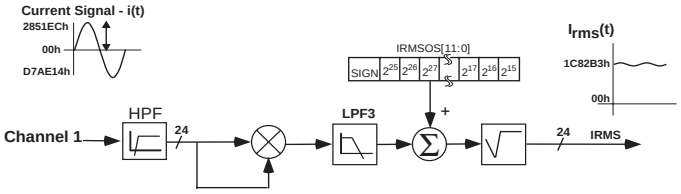


Figure 23 - Channel 1 RMS signal processing

With the specified full scale analog input signal of 0.5V, the ADC will produce an output code which is approximately ±2,642,412d—see *Channel 1 ADC*. The equivalent RMS values of a full-scale AC signal is 1,868,467d (1C82B3h).

Channel 1 RMS offset compensation

The ADE7753 incorporates a channel 1 RMS offset compensation register (IRMSOS). This is 12-bit signed registers which can be used to remove offset in the channel 1 RMS calculation. An offset may exist in the RMS calculation due to input noises that are integrated in the DC component of $V^2(t)$. The offset calibration will allow the content of the IRMS register to be maintained at zero when no input is present on channel 1.

1 LSB of the Channel 1 RMS offset are equivalent to 32,768 LSB of the square of the Channel 1 RMS register. Assuming that the maximum value from the Channel 1 RMS calculation is 1,868,467d with full scale AC inputs, then 1 LSB of the channel 1 RMS offset represents 0.46% of measurement error at -60dB down of full scale.

$$I_{rms} = \sqrt{I_{rms0}^2 + IRMSOS \times 32768}$$

where I_{rmso} is the RMS measurement without offset correction.

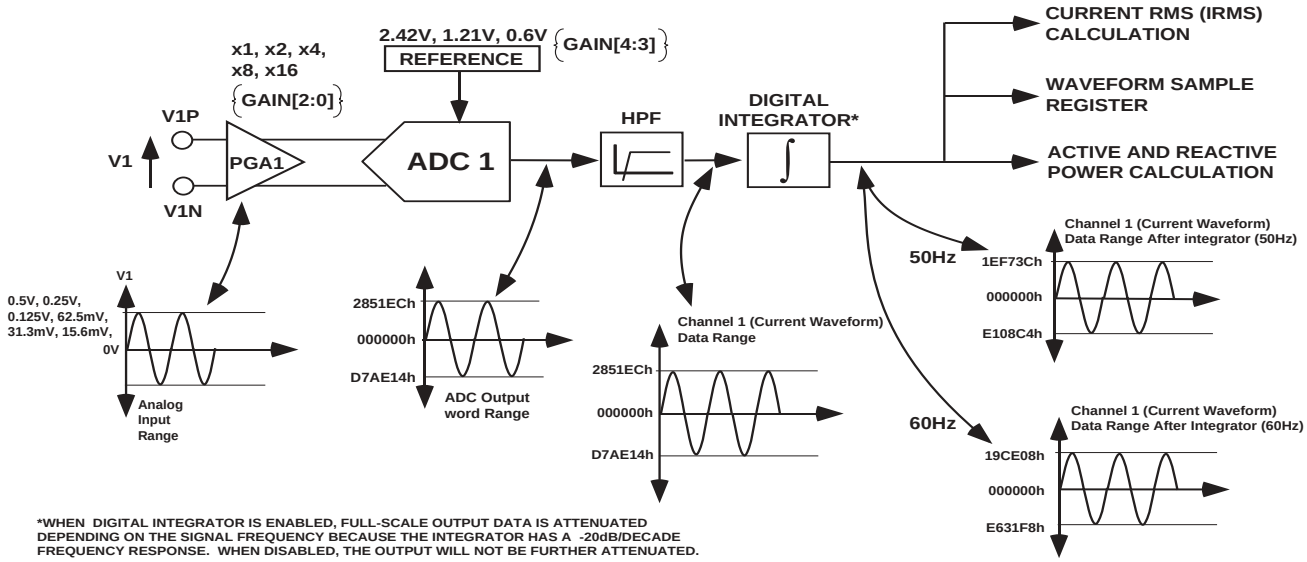


Figure 21 —ADC and signal processing in Channel 1

CHANNEL 2 ADC

Channel 2 Sampling

In Channel 2 waveform sampling mode (MODE[14:13] = 1,1 and WSMP = 1) the ADC output code scaling for Channel 2 is not the same as Channel 1. Channel 2 waveform sample is a 16-bit word and sign extended to 24 bits. For normal operation, the differential voltage signal between V2P and V2N should not exceed 0.5V. With maximum voltage input (±0.5V at PGA gain of 1), the outputs from the ADC swings between 2852h and D7AEh (±10,322 Decimal). However, before being passed to the Waveform register, the ADC output is passed through a single pole, low pass filter with a cutoff frequency of 140Hz. The plots in Figure 24 shows the magnitude and phase response of this filter.

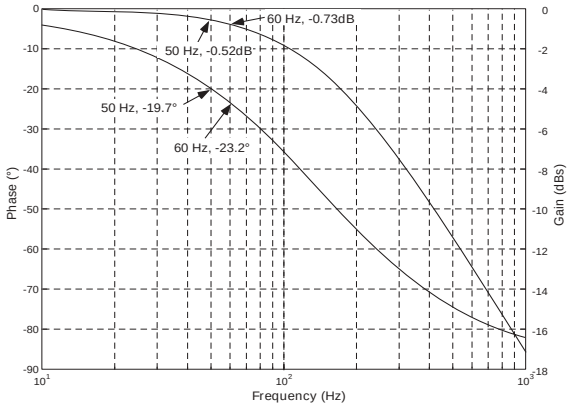


Figure 24 – Magnitude & Phase response of LPF1

The LPF1 has the effect of attenuating the signal. For example if the line frequency is 60Hz, then the signal at the output of LPF1 will be attenuated by about 8%.

$$|H(f)| = \frac{1}{\sqrt{1+\left(60Hz/140Hz\right)^2}} = 0.919 = -0.73dB$$

Note LPF1 does not affect the power calculation. The signal processing chain in Channel 2 is illustrated in Figure 25.

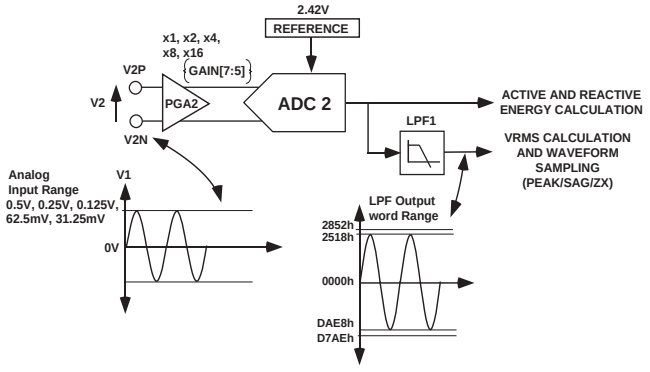


Figure 25 – ADC and Signal Processing in Channel 2

Unlike Channel 1, Channel 2 has only one analog input range (1V differential). However like Channel 1, Channel 2 does have a PGA with gain selections of 1, 2, 4, 8 and 16. For energy measurement, the output of the ADC is passed directly to the multiplier and is not filtered. A HPF is not required to remove any DC offset since it is only required to remove the offset from one channel to eliminate errors due to offsets in the power calculation. When in waveform sample mode, one of four output sample rates can be chosen by using bits 11 and 12 of the Mode register. The available output sample rates are 27.9kSPS, 14kSPS, 7kSPS or 3.5kSPS—see *Mode Register*. The interrupt request output $\overline{\text{IRQ}}$ signals a sample availability by going active low. The timing is the same as that for Channel 1 and is shown in Figure 22.

Channel 2 RMS calculation

Figure 26 shows the details of the signal processing chain for the RMS calculation on Channel 2. The channel 2 RMS value is processed from the samples used in the channel 2 waveform sampling mode. The RMS value will be slightly attenuated because of LPF1. Channel 2 RMS value is stored in the unsigned 24-bit VRMS register. The update rate of the channel 2 RMS measurement is CLKIN/4.

With the specified full scale AC analog input signal of 0.5V, the outputs from the LPF1 swings between 2518h and DAE8h at 60 Hz- see *Channel 2 ADC*. The equivalent RMS value of this full-scale AC signal is approximately 1,561,400 (17D338h) in the VRMS register.

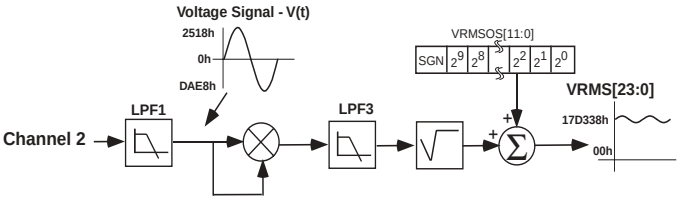


Figure 26 - Channel 2 RMS signal processing

Channel 2 RMS offset compensation

The ADE7753 incorporates a channel 2 RMS offset compensation register (VRMSOS). This is a 12-bit signed registers which can be used to remove offset in the channel 2 RMS calculation. An offset may exist in the RMS calculation due to input noises and dc offset in the input samples. The offset calibration allows the contents of the VRMS register to be maintained at zero when no voltage is applied.

1 LSB of the channel 2 RMS offset are equivalent to 1 LSB of the RMS register. Assuming that the maximum value from the channel 2 RMS calculation is 1,561,400d with full scale AC inputs, then 1 LSB of the channel 2 RMS offset represents 0.064% of measurement error at -60dB down of full scale.

$$V_{rms} = V_{rmso} + VRMSOS$$

where V_{rmso} is the RMS measurement without offset correction.

PHASE COMPENSATION

When the HPF is disabled, the phase error between Channel 1 and Channel 2 is zero from DC to 3.5kHz. When HPF is enabled, Channel 1 has a phase response illustrated in Figures 28 & 29. Also shown in Figure 30 is the magnitude response of the filter. As can be seen from the plots, the phase response is almost zero from 45Hz to 1kHz, This is all that is required in typical energy measurement applications.

However, despite being internally phase compensated the ADE7753 must work with transducers which may have inherent phase errors. For example a phase error of 0.1° to 0.3° is not uncommon for a CT (Current Transformer). These phase errors can vary from part to part and they must be corrected in order to perform accurate power calculations. The errors associated with phase mismatch are particularly noticeable at low power factors. The ADE7753 provides a means of digitally calibrating these small phase errors. The ADE7753 allows a small time delay or time advance to be introduced into the signal processing chain in order to compensate for small phase errors. Because the compensation is in time, this technique should only be used for small phase errors in the range of 0.1° to 0.5°. Correcting large phase errors using a time shift technique can introduce significant phase errors at higher harmonics.

The Phase Calibration register (PHCAL[5:0]) is a 2's complement signed single byte register which has values ranging from 21h (-31 in Decimal) to 1Fh (31 in Decimal). The register is centered at 0Dh, so that writing 0Dh to the register gives zero delay. By changing the PHCAL register, the time delay in the Channel 2 signal path can change from –100.8µs to +33.6µs (CLKIN = 3.579545MHz). One LSB is equivalent to 2.22µs time delay or advance. With a line frequency of 60Hz this gives a phase resolution of 0.048° at the fundamental (i.e., 360° × 2.22µs × 60Hz). Figure 27 illustrates how the phase compensation is used to remove a 0.1° phase lead in Channel 1 due to the external transducer. In order to cancel the lead (0.1°) in Channel 1, a phase lead must also be introduced into Channel 2. The resolution of the phase adjustment allows the introduction of a phase lead in increment of 0.048°. The phase lead is achieved by introducing a time advance into Channel 2. A time advance of 4.48µs is made by writing -2 (0Bh) to the time delay block, thus reducing the amount of time delay by 4.48µs, or equivalently, a phase lead of approximately 0.1° at line frequency of 60Hz. 0Bh represents -2 because the register is centered with zero at 0Dh.

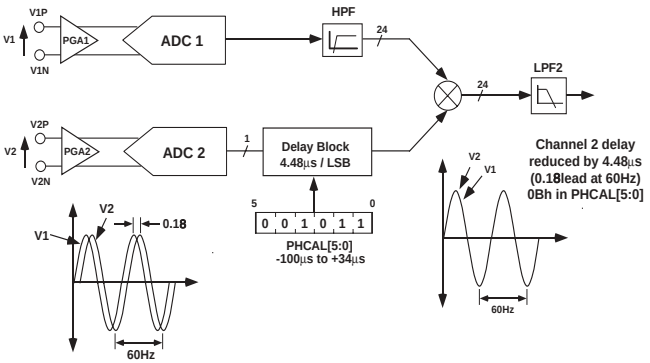


Figure 27 – *Phase Calibration*

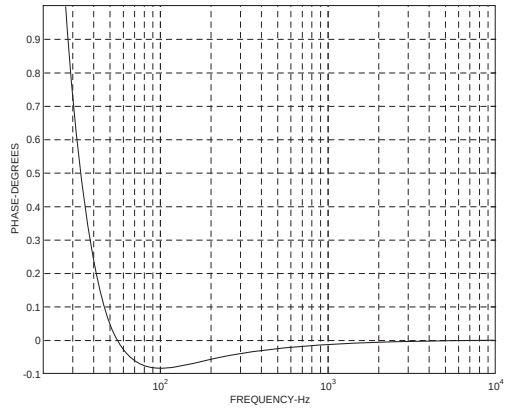


Figure 28 – Combined Phase Response of the HPF & Phase Compensation (10Hz to 1kHz)

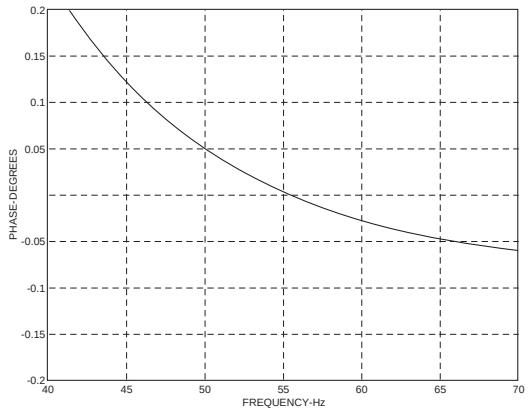


Figure 29 – Combined Phase Response of the HPF & Phase Compensation (40Hz to 70Hz)

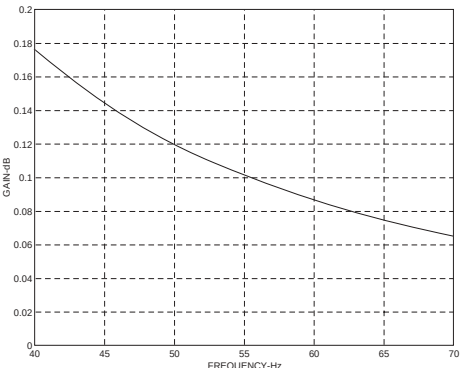


Figure 30 – Combined Gain Response of the HPF & Phase Compensation

ACTIVE POWER CALCULATION

Power is defined as the rate of energy flow from source to load. It is defined as the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal and it is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/

sec. Equation 3 gives an expression for the instantaneous power signal in an ac system.

$$v(t) = \sqrt{2}V \sin(\omega t) \quad (1)$$

$$i(t) = \sqrt{2}I \sin(\omega t) \quad (2)$$

where V = rms voltage,
I = rms current.

$$p(t) = v(t) \times i(t)$$
$$p(t) = VI - VI\cos(\omega t) \quad (3)$$

The average power over an integral number of line cycles (n) is given by the expression in Equation 4.

$$P = \frac{1}{nT}\int_0^{nT} p(t)dt = VI \quad (4)$$

where T is the line cycle period.
P is referred to as the Active or Real Power. Note that the active power is equal to the dc component of the instantaneous power signal *p(t)* in Equation 3 , i.e., VI. This is the relationship used to calculate active power in the ADE7753. The instantaneous power signal *p(t)* is generated by multiplying the current and voltage signals. The dc component of the instantaneous power signal is then extracted by LPF2 (Low Pass Filter) to obtain the active power information. This process is illustrated graphically in Figure 31.

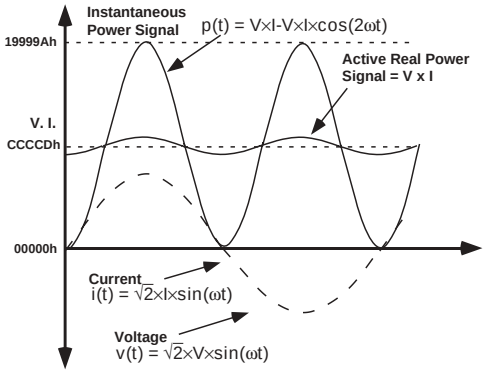


Figure 31– Active Power Calculation

Since LPF2 does not have an ideal "brick wall" frequency response—see Figure 32, the Active Power signal will have some ripple due to the instantaneous power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Since the ripple is sinusoidal in nature it will be removed when the Active Power signal is integrated to calculate Energy – see *Energy Calculation*.

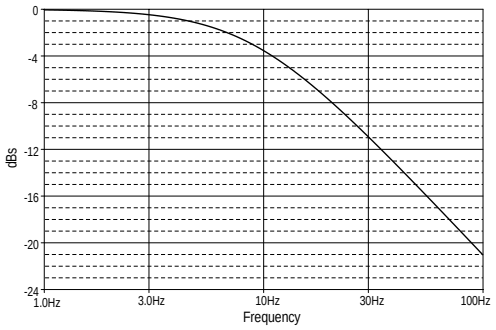


Figure 32 —Frequency Response of LPF2

Figure 33 shows the signal processing chain for the ActivePower calculation in the ADE7753. As explained, the Active Power is calculated by low pass filtering the instantaneous power signal. Note that for when reading the waveform samples from the output of LPF2,
The gain of the Active Energy can be adjusted by using the multiplier and Watt Gain register (WGAIN[11:0]). The gain is adjusted by writing a 2's complement 12-bit word to the Watt Gain register. Below is the expression that shows how the gain adjustment is related to the contents of the Watt Gain register.

$$Output\,WGAIN = \left(Active\ Power \times \left\{ 1 + \frac{WGAIN}{2^{12}} \right\} \right)$$

For example when 7FFh is written to the Watt Gain register the Power output is scaled up by 50%. 7FFh = 2047d, $2047/2^{12}$ = 0.5. Similarly, 800h = -2048 Dec (signed 2's Complement) and power output is scaled by –50%.
Shown in Figure 34 is the maximum code (in hex) output range for the Active Power signal (LPF2). Note that the output range changes depending on the contents of the Watt Gain register. The minimum output range is given when the Watt Gain register contents are equal to 800h, and the

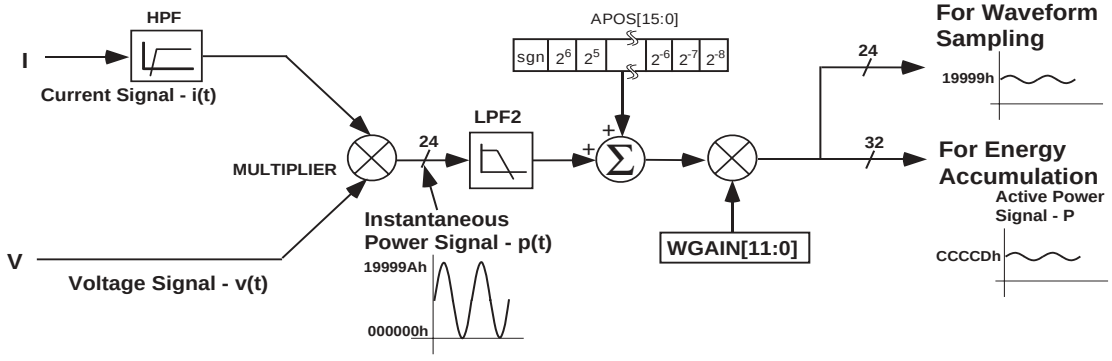


Figure 33– *Active Power Signal Processing*

maximum range is given by writing 7FFh to the Watt Gain register. This can be used to calibrate the Active Power (or Energy) calculation in the ADE7753.

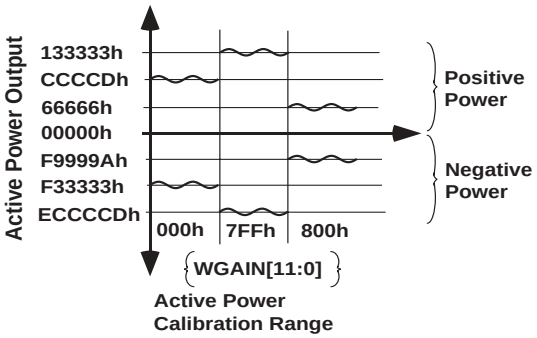


Figure 34 – Active Power Calculation Output Range

ENERGY CALCULATION

As stated earlier, power is defined as the rate of energy flow. This relationship can be expressed mathematically as Equation 5.

$$P = \frac{dE}{dt} \quad (5)$$

Where P = Power and E = Energy.
Conversely Energy is given as the integral of Power.

$$E = \int P dt \quad (6)$$

The ADE7753 achieves the integration of the Active Power signal by continuously accumulating the Active Power signal in an internal non-readable 56-bit Energy register. The Active Energy register (AENERGY[23:0]) represents the upper 24 bits of this internal register. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 7 below expresses the relationship

$$E = \int p(t)dt = \lim_{t \to 0} \left\{ \sum_{n=1}^{\infty} p(nT) \times T \right\} \quad (7)$$

Where n is the discrete time sample number and T is the sample period.

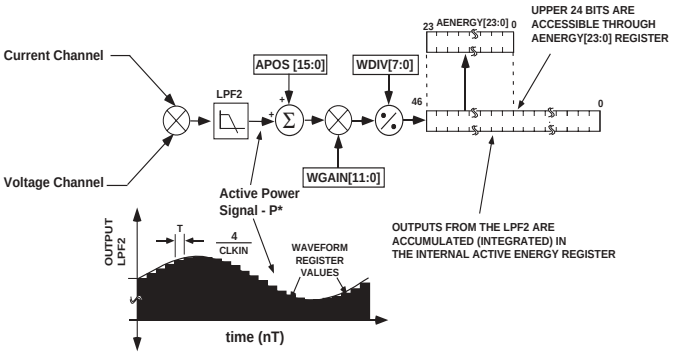


Figure 35 – *ADE7753 Active Energy Calculation*

The discrete time sample period (T) for the accumulation register in the ADE7753 is 1.1µs (4/CLKIN). As well as calculating the Energy this integration removes any sinusoidal components which may be in the Active Power signal.

Figure 35 shows a graphical representation of this discrete time integration or accumulation. The Active Power signal in the Waveform register is continuously added to the internal Active Energy register. This addition is a signed addition, therefore negative energy will be subtracted from the Active Energy contents.

The output of the multiplier is divided by WDIV. If the value in the WDIV register is equal to 0 then the internal Active Energy register is divided by 1. WDIV is an 8-bit unsigned register. After dividing by WDIV, the active energy is accumulated in a 48-bit internal energy accumulation register. The upper 24 bit of this register is accessible through a read to the Active Energy register (AENERGY[23:0]). A read to the RAENERGY register will return the content of the AENERGY register and the upper 24-bit of the internal register is clear after a read to AENERGY register.

As shown in Figure 35, the Active Power signal is accumulated in an internal 48-bit signed register. The Active Power signal can be read from the Waveform register by setting MODE[14:13] = 0,0 and setting the WSMP bit (bit 3) in the Interrupt Enable register to 1. Like the Channel 1 and Channel 2 waveform sampling modes the waveform date is available at sample rates of 27.9kSPS, 14kSPS, 7kSPS or 3.5kSPS—see Figure 22.

Figure 36 shows this energy accumulation for full scale signals (sinusoidal) on the analog inputs. The three curves displayed, illustrate the minimum period of time it takes the energy register to roll-over when the Active Power Gain register contents are 7FFh, 000h and 800h. The Watt Gain register is used to carry out power calibration in the ADE7753. As shown, the fastest integration time will occur when the Watt Gain register is set to maximum full scale, i.e., 7FFh.

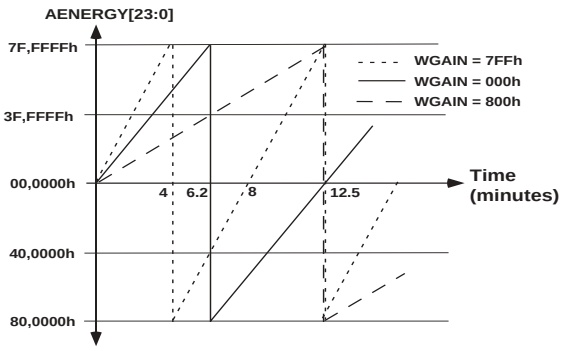


Figure 36 - Energy register roll-over time for full-scale power (Minimum & Maximum Power Gain)

Note that the energy register contents will roll over to full-scale negative (800000h) and continue increasing in value when the power or energy flow is positive - see Figure 36. Conversely if the power is negative the energy register would under flow to full scale positive (7FFFFFh) and continue decreasing in value.

By using the Interrupt Enable register, the ADE7753 can be configured to issue an interrupt ($\overline{IRQ}$) when the Active Energy register is half-full (positive or negative) or when an over/under flow occurs.

Integration time under steady load

As mentioned in the last section, the discrete time sample period (T) for the accumulation register is 1.1µs (4/CLKIN).

With full-scale sinusoidal signals on the analog inputs and the WGAIN register set to 000h, the average word value from each LPF2 is CCCCDh - see Figure 31. The maximum positive value which can be stored in the internal 47-bit register is 2^{46} - 1 or 7FFF,FFFF,FFFFh before it overflows, the integration time under these conditions with WDIV=0 is calculated as follows:

$$Time = \frac{3FFF,FFFF,FFFFh}{CCCCDh} \times 1.12\mu s = 187.5s = 3.12\min s$$

When WDIV is set to a value different from 0, the integration time varies as shown on Equation 8.

$$Time = Time_{WDIV=0} \times WDIV \qquad (8)$$

POWER OFFSET CALIBRATION

The ADE7753 also incorporates an Active Power Offset register (APOS[15:0]). This is a signed 2's complement 16-bit register which can be used to remove offsets in the active power calculation—*see Figure 33*. An offset may exist in the power calculation due to cross talk between channels on the PCB or in the IC itself. The offset calibration will allow the contents of the Active Power register to be maintained at zero when no power is being consumed.

Two hundred fifty six LSBs (APOS=0100h) written to the Active Power Offset register are equivalent to 1 LSB in the Waveform Sample register. Assuming the average value outputs from LPF2 is CCCCDh (838,861 in Decimal) when inputs on Channels 1 and 2 are both at full-scale. At -60dB down on Channel 1 (1/1000 of the Channel 1 full-scale input), the average word value outputs from LPF2 is 838.861 (838,861/1,000). 1 LSB in the LPF2 output has a measurement error of 1/838.861 × 100% = 0.119% of the average value. The Active Power Offset register has a resolution equal to 1/256 LSB of the Waveform register, hence the power offset correction resolution is 0.00047%/LSB (0.119%/256) at -60dB.

ENERGY TO FREQUENCY CONVERSION

ADE7753 also provides energy to frequency conversion for calibration purposes. After initial calibration at manufacturing, the manufacturer or end customer will often verify the energy meter calibration. One convenient way to verify the meter calibration is for the manufacturer to provide an output frequency which is proportional to the energy or active power under steady load conditions. This output frequency can provide a simple, single wire, optically isolated interface to external calibration equipment. Figure 37 illustrates the Energy-to-Frequency conversion in the ADE7753.

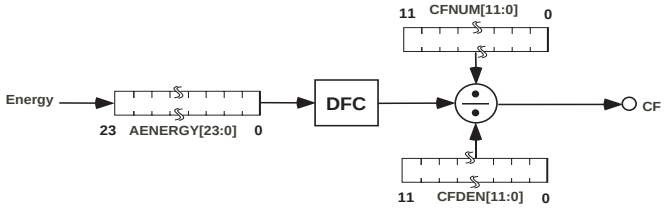


Figure 37– ADE7753 Energy to Frequency Conversion

A Digital to Frequency Converter (DFC) is used to generate the CF pulsed output. The DFC generates a pulse each time one LSB in the Active Energy register is accumulated. An output pulse is generated when (CFDEN+1)/(CFNUM+1) number of pulses are generated at the DFC output. Under steady load conditions the output frequency is proportional to the Active Power.

The maximum output frequency, with AC input signals at full-scale and CFNUM=00h & CFDEN=00h, is approximately 23 kHz.

The ADE7753 incorporates two registers, CFNUM[11:0] and CFDEN[11:0], to set the CF frequency. These are unsigned 12-bit registers which can be used to adjust the CF frequency to a wide range of values. These frequency scaling registers are 12-bit registers which can scale the output frequency by $1/2^{12}$ to 1 with a step of $1/2^{12}$.

If the value zero is written to any of these registers, the value one would be applied to the register. The ratio (CFNUM+1)/(CFDEN+1) should be smaller than one to assure proper operation. If the ratio of the registers (CFNUM+1)/(CFDEN+1) is greater than one, the register values would be adjust to a ratio (CFNUM+1)/(CFDEN+1) of one.

For example if the output frequency is 1.562kHz while the contents of CFDENare zero (000h), then the output frequency can be set to 6.1Hz by writing FFh to the CFDEN register. Note that for values where CFDEN>CFNUM, the performance of the CF frequency is not guaranteed. CFNUM should always be set to a value less than CFDEN.

The output frequency will have a slight ripple at a frequency equal to twice the line frequency. This is due to imperfect filtering of the instantaneous power signal to generate the Active Power signal – see *Active Power Calculation*. Equation 3 gives an expression for the instantaneous power signal. This is filtered by LPF2 which has a magnitude response given by Equation 9.

$$|H(f)| = \frac{1}{\sqrt{1+\frac{f^2}{8.9^2}}} \qquad (9)$$

The Active Power signal (output of LPF2) can be rewritten as.

$$p(t) = VI - \left\{\frac{VI}{\sqrt{1+\left(\frac{2f_l}{8.9}\right)^2}}\right\} \cdot \cos(4\pi f_l t) \qquad (10)$$

where f_l is the line frequency (e.g., 60Hz)

From Equation 6

$$E(t) = VIt - \left\{\frac{VI}{4\pi f_l \sqrt{1+\left(\frac{2f_l}{8.9}\right)^2}}\right\} \cdot \sin(4\pi f_l t) \qquad (11)$$

From Equation 11 it can be seen that there is a small ripple in the energy calculation due to a sin(2ωt) component. This is shown graphically in Figure 38. The Active Energy calculation is shown by the dashed straight line and is equal

to V x I x t. The sinusoidal ripple in the Active Energy calculation is also shown. Since the average value of a sinusoid is zero, this ripple will not contribute to the energy calculation over time. However, the ripple can be observed in the frequency output, especially at higher output frequencies. The ripple will get larger as a percentage of the frequency at larger loads and higher output frequencies. The reason is simply that at higher output frequencies the integration or averaging time in the Energy-to-Frequency conversion process is shorter. As a consequence some of the sinusoidal ripple is observable in the frequency output. Choosing a lower output frequency at CF for calibration can significantly reduce the ripple. Also averaging the output frequency by using a longer gate time for the counter will achieve the same results.

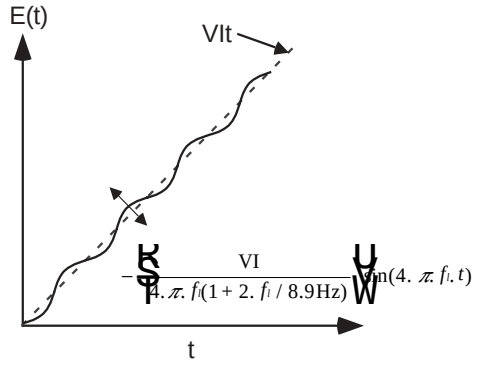


Figure 38 – Output frequency ripple

LINE CYCLE ENERGY ACCUMULATION MODE

In Line Cycle Energy Accumulation mode, the energy accumulation of the ADE7753 can be synchronized to the Channel 2 zero crossing so that active energy can be accumulated over an integral number of half line cycles. The advantage of summing the active energy over an integer number of half line cycles is that the sinusoidal component in the active energy is reduced to zero. This eliminates any ripple in the energy calculation. Energy is calculated more accurately and in a shorter time because integration period can be shortened. By using the line cycle energy accumulation mode, the energy calibration can be greatly simplified and the time required to calibrate the meter can be significantly reduced. The ADE7753 is placed in line cycle energy accumulation mode by setting bit 7 (CYCMODE) in the Mode register. In Line Cycle Energy Accumulation Mode the ADE7753 accumulates the active power signal in the LAENERGY register (Address 04h) for an integral number of line cycles, as shown in Figure 39. The number of half line cycles is specified in the LINECYC register (Address 1Ch). The ADE7753 can accumulate active power for up to 65,535 half line cycles. Because the active power is integrated on an integral number of line cycles, at the end of a line cycle energy accumulation cycle the CYCEND flag in the Interrupt Status register is set (bit 2). If the CYCEND enable bit in the Interrupt Enable register is enabled, the $\overline{IRQ}$ output will also go active low. Thus the $\overline{IRQ}$ line can also be used to signal the completion of the line cycle energy accumulation. Another calibration cycle will start as long as the CYCMODE bit in the Mode register is set. Note that the result of the first calibration is invalid and should be ignored. The result of all subsequent line cycle accumulation is correct.

From Equations 6 and 10.

$$E(t) = \int_0^{nT} VI\,dt - \left\{ \frac{VI}{\sqrt{1+\left(\frac{f}{8.9}\right)^2}} \right\} \cdot \int_0^{nT} \cos(2\pi\, f\, t)\,dt \qquad (12)$$

where n is a integer and T is the line cycle period. Since the sinusoidal component is integrated over a integer number of line cycles its value is always zero.

Therefore:

$$E = \int_0^{nT} VI dt + 0 \qquad (13)$$

$$E(t) = VInT \qquad (14)$$

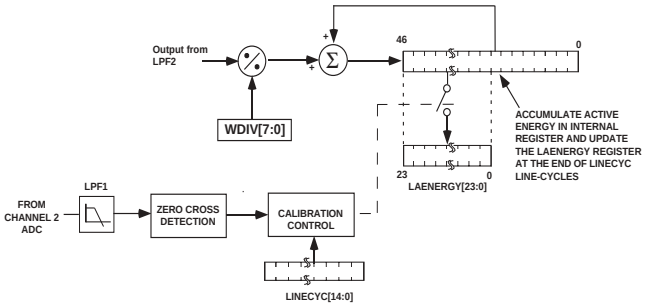


Figure 39 – Energy Calculation in Line Cycle Energy Accumulation Mode

Note that in this mode, the 16-bit LINECYC register can hold a maximum value of 65,535. In other words, the line energy accumulation mode can be used to accumulate active energy for a maximum duration over 65,535 half line cycles. At 60Hz line frequency, it translates to a total duration of 65,535 / 120Hz = 546 seconds.

POSITIVE ONLY ACCUMULATION MODE

In Positive Only Accumulation mode, the energy accumulation is done only for positive power, ignoring any occurrence of negative power above or below the no load threshold as shown in Figure 40. The ADE7753 is placed in positive only

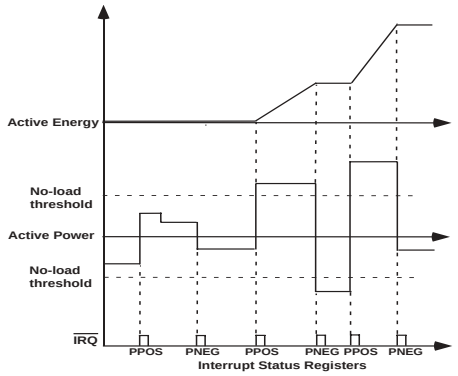


Figure 40 – Energy Accumulation in Positive Only Accumulation Mode

accumulation mode by setting the MSB of the MODE register (MODE[15]). The default setting for this mode is off. Transitions in the direction of power flow, going from negative to positive or positive to negative, set the IRQ pin to active low if the Interrupt Enable register is enabled. The Interrupt Status Registers, PPOS and PNEG, show which transition has occurred. *See ADE7753 Register Descriptions.*

NO LOAD THRESHOLD

The ADE7753 includes a "no load threshold" feature that will eliminate any creep effects in the meter. The ADE7753 accomplishes this by not accumulating energy if the multiplier output is below the "no load threshold". This threshold is 0.001% of the full-scale output frequency of the multiplier. Compare this value to the IEC1036 specification which states that the meter must start up with a load equal to or less than 0.4% Ib. This standard translates to .0167% of the full-scale output frequency of the multiplier.

REACTIVE POWER CALCULATION

Reactive power is defined as the product of the voltage and current waveforms when one of this signal is phase shifted by 90°. The resulting waveform is called the instantaneous reactive power signal. Equation 17 gives an expression for the instantaneous reactive power signal in an ac system when the phase of the current channel is shifted by +90°.

$$v(t) = \sqrt{2}\,V\,\sin(\omega t + \theta) \tag{15}$$

$$i(t) = \sqrt{2}\,I\,sin(\omega t) \qquad i'(t) = \sqrt{2}\,I\,sin(\omega t + \frac{\pi}{2}) \tag{16}$$

Where θ is the phase difference between the voltage and current channel, V = rms voltage and I = rms current.

$$Rp(t) = v(t) \times i'(t)$$
$$Rp(t) = VI\,\sin(\theta) + VI\,\sin(2\omega t + \theta) \tag{17}$$

The average power over an integral number of line cycles (n) is given by the expression in Equation 18.

$$RP = \frac{1}{nT}\int_0^{nT} Rp(t)dt = VI\,\sin(\theta) \tag{18}$$

where T is the line cycle period.

RP is referred to as the Reactive Power. Note that the reactive power is equal to the DC component of the instantaneous reactive power signal *Rp(t)* in Equation 17. This is the relationship used to calculate reactive power in the ADE7753. The instantaneous reactive power signal *Rp(t)* is generated by multiplying the channel 1 and channel 2. In this case, the phase of the channel 1 is shifted by +90°. The DC component of the instantaneous reactive power signal is then extracted by a low pass filter to obtain the reactive power information. Figure 41 shows the signal processing in the Reactive Power calculation in the ADE7753.

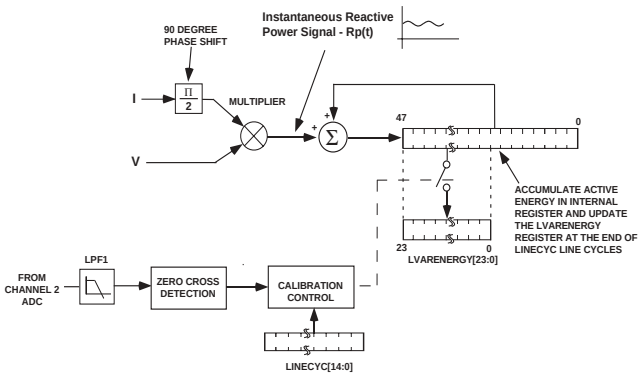


Figure 41 - Reactive Power Signal Processing

The features of the Reactive Energy accumulation are the same as the Line Active Energy accumulation. The number of half line cycles is specified in the LINECYC register. LINECYC is an unsigned 16-bit register. The ADE7754 can accumulate Reactive Power for up to 65535 combined half cycles. At the end of an energy calibration cycle the CYCEND flag in the Interrupt Status register is set. If the CYCEND mask bit in the Interrupt Mask register is enabled, the $\overline{\text{IRQ}}$ output will also go active low. Thus the $\overline{\text{IRQ}}$ line can also be used to signal the end of a calibration. The ADE7753 accumulates the Reactive Power signal in the LVARENERGY register for an integer number of half cycles, as shown in Figure 41.

The Reactive Energy accumulation in the ADE7753 not only provides the reactive energy calculated using the phase shift method, it is also useful to provide the sign of the reactive power if it is desirable to use triangular method to calculate reactive power. The ADE7753 also provides an accurate measurement of the apparent power. The user can choose to determine reactive energy through the mathematical relationship between apparent, active and reactive power. The sign of the reactive energy can be found by reading the result from the LVARENERGY register at the end of a reactive energy accumulation cycle.

$$\text{Reactive Energy} = sign(\text{Reactive Energy}) \times \sqrt{Apparent\,Energy^2 - Active\,Energy^2}$$

APPARENT POWER CALCULATION

Apparent power is defined as the amplitude of the vector sum of the Active and Reactive powers -see Figure 42. The angle θ between the Active Power and the Apparent Power generally represents the phase shift due to non-resistive loads. For single phase applications, θ represents the angle between the voltage and the current signals. Equation 20 gives an expression of the instantaneous power signal in an ac system with a phase shift.

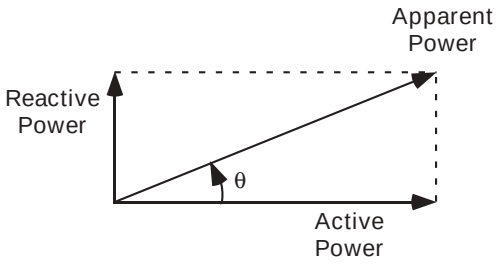


Figure 42 - Power triangle

$$v(t) = \sqrt{2}\ V_{rms}\ \sin(\omega t)$$
$$i(t) = \sqrt{2}\ I_{rms}\ \sin(\omega t + \theta) \quad (19)$$

$$p(t) = v(t) \times i(t)$$
$$p(t) = V_{rms}\ I_{rms}\ \cos(\theta) - V_{rms}\ I_{rms}\ \cos(2\omega t + \theta) \quad (20)$$

The Apparent Power (AP) is defined as V_{rms} x I_{rms}. This expression is independent from the phase angle between the current and the voltage.

Figure 43 illustrates graphically the signal processing in each phase for the calculation of the Apparent Power in the ADE7753.

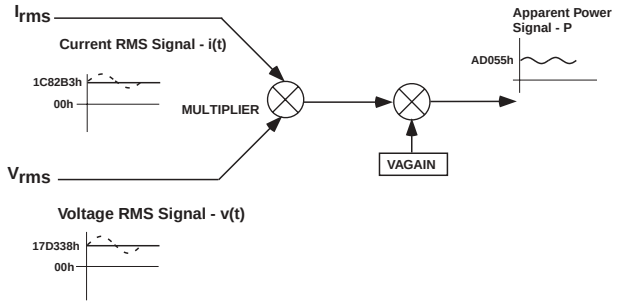


Figure 43 - Apparent Power Signal Processing

The gain of the Apparent Energy can be adjusted by using the multiplier and VA Gain register (VAGAIN[11:0]). The gain is adjusted by writing a 2's complement, 12-bit word to the VAGAIN register. Below is the expression that shows how the gain adjustment is related to the contents of the VA Gain register.

$$Output\ VAGAIN = \left(Apparent\ Power \times \left\{ 1 + \frac{VAGAIN}{2^{12}} \right\} \right)$$

For example when 7FFh is written to the VA Gain register the Power output is scaled up by 50%. 7FFh = 2047d, $2047/2^{12}$ = 0.5. Similarly, 800h = -2047 Dec (signed 2's Complement) and power output is scaled by –50%.

The Apparent Power is calculated with the Current and Voltage RMS values obtained in the RMS blocks of the ADE7753. Shown in Figure 44 is the maximum code (Hexadecimal) output range of the Apparent Power signal. Note that the output range changes depending on the contents of the Apparent Power Gain registers. The minimum output range is given when the Apparent Power Gain register content is equal to 800h and the maximum range is given by writing 7FFh to the Apparent Power Gain register. This can be used to calibrate the Apparent Power (or Energy) calculation in the ADE7753 -see *Apparent Power calculation*.

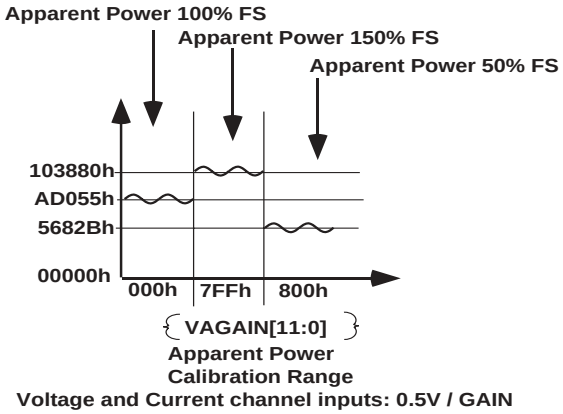


Figure 44- Apparent Power Calculation Output range

Apparent Power Offset Calibration

Each RMS measurement includes an offset compensation register to calibrate and eliminate the DC component in the RMS value -see *Channel 1 RMS calculation and Channel 2 RMS calculation*. The channel 1 and channel 2 RMS values are then multiplied together in the Apparent Power signal processing. As no additional offsets are created in the multiplication of the RMS values, there is no specific offset compensation in the Apparent Power signal processing. The offset compensation of the Apparent Power measurement is done by calibrating each individual RMS measurements.

APPARENT ENERGY CALCULATION

The Apparent Energy is given as the integral of the Apparent Power.

$$Apparent\ Energy = \int Apparent\ Power(t)\ dt \quad (21)$$

The ADE7753 achieves the integration of the Apparent Power signal by continuously accumulating the Apparent Power signal in an internal 48-bit register. The Apparent Energy register (VAENERGY[23:0]) represents the upper 24 bits of this internal register. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 23 below expresses the relationship

$$Apparent\ Energy = \underset{T \to 0}{Lim} \left\{ \sum_{n=0}^{\infty} Apparent\ Power(nT) \times T \right\} \quad (22)$$

Where n is the discrete time sample number and T is the sample period.

The discrete time sample period (T) for the accumulation register in the ADE7753 is 1.1µs (4/CLKIN).

Figure 44 shows a graphical representation of this discrete time integration or accumulation. The Apparent Power signal is continuously added to the internal register. This addition is a signed addition even if the Apparent Energy remains theoretically always positive.

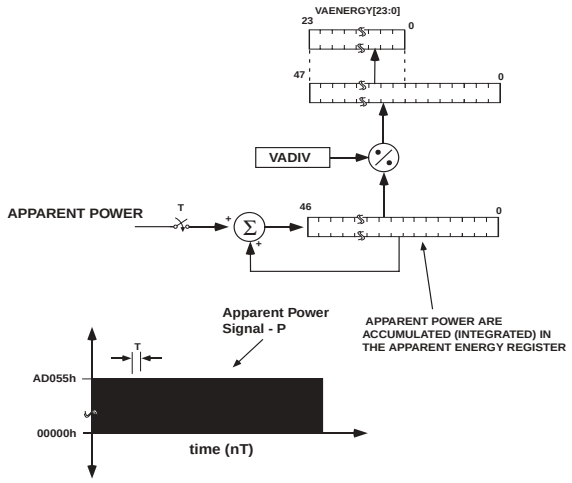


Figure 45- ADE7753 Apparent Energy calculation

The upper 52-bit of the internal register are divided by VADIV. If the value in the VADIV register is equal to 0 then the internal active Energy register is divided by 1. VADIV is an 8-bit unsigned register. The upper 24-bit are then written in the 24-bit Apparent Energy register (VAENERGY[23:0]). RVAENERGY register (24 bits long) is provided to read the Apparent Energy. This register is reset to zero after a read operation.

Figure 45 shows this Apparent Energy accumulation for full scale signals (sinusoidal) on the analog inputs. The three curves displayed, illustrate the minimum time it takes the energy register to roll-over when the VA Gain registers content is equal to 7FFh, 000h and 800h. The VA Gain register is used to carry out an apparent power calibration in the ADE7753. As shown, the fastest integration time will occur when the VA Gain register is set to maximum full scale, i.e., 7FFh.

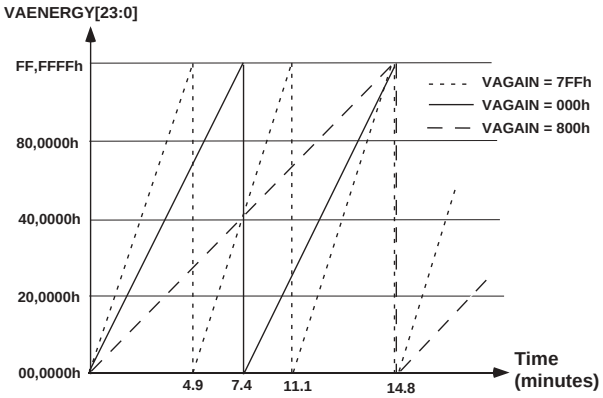


Figure 46- Energy register roll-over time for full-scale power (Minimum & Maximum Power Gain)

Note that the Apparent Energy register contents roll-over to full-scale negative (80,0000h) and continue increasing in value when the power or energy flow is positive - see Figure 46.

By using the Interrupt Enable register, the ADE7754 can be configured to issue an interrupt ($\overline{IRQ}$) when the Apparent Energy register is half full (positive or negative) or when an over/under flow occurs.

Integration times under steady load

As mentioned in the last section, the discrete time sample period (T) for the accumulation register is 1.1µs (4/CLKIN). With full-scale sinusoidal signals on the analog inputs and the VAGAIN register set to 000h, the average word value from Apparent Power stage is AD055h - see *Apparent Power output range*. The maximum value which can be stored in the Apparent Energy register before it over-flows is 2^{24} or FF,FFFFh. As the average word value is added to the internal register which can store 2^{48} - 1 or 7FFF,FFFF,FFFFh before it overflows, the integration time under these conditions with VADIV=0 is calculated as follows:

$$\text{Time} = \frac{7FFF,FFFF,FFFFh}{AD055h} \times 1.2\mu s = 888s = 14.8min$$

When VADIV is set to a value different from 0, the integration time varies as shown on Equation 23.

$$\text{Time} = \text{Time}_{WDIV=0} \text{ x VADIV} \qquad (23)$$

LINE APPARENT ENERGY ACCUMULATION

The ADE7753 is designed with a special Apparent Energy accumulation mode which simplifies the calibration process. By using the on-chip zero-crossing detection, the ADE7753 accumulates the Apparent Power signal in the LVAENERGY register for an integral number of half cycles, as shown in Figure 47. The line Apparent energy accumulation mode is always active.

The number of half line cycles is specified in the LINCYC register. LINCYC is an unsigned 16-bit register. The ADE7753 can accumulate Apparent Power for up to 65535 combined half cycles. Because the Apparent Power is integrated on the same integral number of line cycles as the Line Active Energy register, these two values can be compared easily. The active and apparent Energy are calculated more accurately because of this precise timing control and provide all the information needed for Reactive Power and Power Factor calculation. At the end of an energy calibration cycle the CYCEND flag in the Interrupt Status register is set. If the CYCEND mask bit in the Interrupt Mask register is enabled, the $\overline{IRQ}$ output will also go active low. Thus the $\overline{IRQ}$ line can also be used to signal the end of a calibration.

The Line Apparent Energy accumulation uses the same signal path as the Apparent Energy accumulation. The LSB size of these two registers is equivalent.

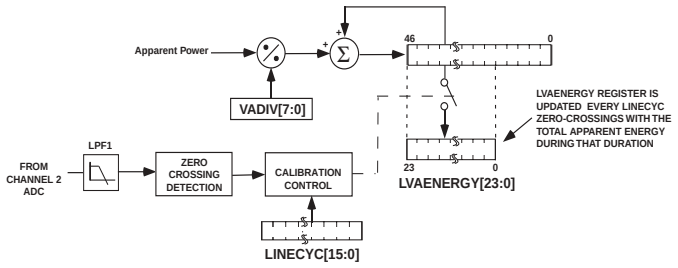


Figure 47 - ADE7753 Apparent Energy Calibration

CALIBRATING THE ENERGY METER

When calibrating the ADE7753, the first step is to calibrate the frequency on CF to some required meter constant, e.g., 3200 imp/kWh.

A convenient way to to determine the output frequency on CF is to use the line cycle energy accumulation mode. As shown in Figure 37, DFC generates a pulse each time a LSB in the LAENERGY register is accumulated. CF frequency (before the CF frequency divider) can be conveniently determined by the following expression:

$$CF\ Frequency = \frac{Content\ of\ LAENERGY[23:0]\ Register}{Elasped\ Time}$$

When the CYCMODE (bit 7) bit in the Mode register is set to a logic one, energy is accumulated over an integer number of half line cycles. If the line frequency is fixed and the number of half cycles of integration is specified, the total elasped time can be calculated by the following:

$$Elasped\ Time = \frac{1}{2 \times f_l} \times number\ of\ half\ cycles$$

For example, at 60Hz line frequency, the elasped time for 255 half cycles will be 2.125 seconds. Rewriting the above in terms of contents of various ADE7753 registers and line frequencies (*fl*):

$$CF\ Frequency = \frac{LAENERGY[23:0] \times 2 \times fl}{LINECYC[15:0]} \quad (24)$$

where *fl* is the line frequency.

Alternatively, CF frequency can be calculated based on the average LPF2 output.

$$\text{CF Frequency} = \frac{\text{Average LPF2 Output} \times \text{CLKIN}}{2^{27}} \quad (25)$$

Calibrating the Frequency at CF

When the frequency before frequency division is known, the pair of CF Frequency Divider registers (CFNUM and CFDEN) can be adjusted to produce the required frequency on CF. In this example a meter constant of 3200 imp/kWh is chosen as an appropriate constant. This means that under a steady load of 1kW, the output frequency on CF would be,

$$Frequency\ (CF) = \frac{3200\ imp/kWh}{60\,\text{min} \times 60\,\text{sec}} = \frac{3200}{3600} = 0.8888\ Hz$$

Assuming the meter is set up with a test current (basic current) of 20A and a line voltage of 220V for calibration, the load is calculated as 220V × 20A = 4.4kW. Therefore the expected output frequency on CF under this steady load condition would be 4.4 × 0.8888Hz = 3.9111Hz. Under these load conditions the transducers on Channel 1 and Channel 2 should be selected such that the signal on the voltage channel should see approximately half scale and the signal on the current channel about 1/8 of full scale (assuming a maximum current of 80A). Assuming at line frequency of 60Hz, energy is accumulated over FFh number of half line cycles, the resulting content of the LAENERGY register will be approximately 2971.4 (decimal). CF frequency is therefore calculated to be:

$$\text{Frequency (CF)} = \frac{2971.4 \times 2 \times 60}{255} = 1398.3\text{Hz}$$

Alternatively, the average value from LPF2 under this condition is approximately 1/16 of the full-scale level. As described previously, the average LPF2 output at full-scale ac input is CCCCD (hex) or 838,861 (decimal). At 1/16 of full-scale, the LPF2 output is then 52,428.81. Then using Digital to Frequency Conversion, the frequency under this load is calculated as:

$$\text{Frequency(CF)} = \frac{52428.81 \times 3.579545\text{MHz}}{2^{27}} = 1398.3\text{Hz}$$

This is the frequency with the contents of the CFNUM and CFDEN registers equal to 000h. The desired frequency out is 3.9111Hz. Therefore, the CF frequency must be divided by 2797/3.9111Hz or 357.5 decimal. This is achieved by loading the pair of CF Divider registers with the closest rational number. In this case, the closest rational number is found to be 1/358 (or 1h/166h). Therefore, 0h and 165h should be written to the CFNUM and CFDEN registers respectively. Note that the CF frequency is multiplied by the contents of (CFNUM + 1) / (CFDEN + 1). With the CF Divide registers contents equal to 1h/166h, the output frequency is given as 2797Hz / 358 = 3.905Hz. This setting has an error of -0.1%.

Calibrating CF is made easy by using the Calibration mode on the ADE7753. The critical part of this approach is that the line frequency needs to be exactly known. If this is not possible, the frequency can be measured by using the PERIOD register of the ADE7753.

Note that changing WGAIN[11:0] register will also affect the output frequency from CF. The WGAIN register has a gain adjustment of 0.0244% / LSB.

Determine the kWHr/LSB Calibration Coefficient

The Active Energy register (AENERGY) can be used to calculate energy. A full description of this register can be found in the *Energy Calculation* section. The AENERGY register gives the user both sign and magnitude information regarding energy consumption. On completion of the CF frequency output calibration, i.e., after adjusting the CF Frequency divider and the Watt Gain (WGAIN) register, the second stage of the calibration is to determine the kWh/LSB coefficient for the AENERGY register. Equation 26 below shows how LAENERGY can be used to calculate the calibration coefficient.

$$kWHr/LSB = \frac{Calibration\ Power\ (in\ kW)}{3600\ seconds/Hr} \times \frac{LINECYC[15:0]}{LAENERGY[23:0] \times 2 \times fl} \quad (26)$$

Once the coefficient is determined, the MCU can compute the energy consumption at any time by reading the AENERGY contents and multiplying by the coefficient to calculate kWh. In the above example, at 4.4kW, after 255 half cycles (at 60Hz), the resulting LAENERGY is approximately 2971 decimal. The kWHr/LSB can therefore be calculated to be 8.74×10^{-7} kWHr/LSB using the above equation.

CLKIN FREQUENCY

In this datasheet, the characteristics of the ADE7753 is shown with CLKIN frequency equals 3.579545 MHz. However, the ADE7753 is designed to have the same accuracy at any CLKIN frequency within the specified range. If the CLKIN frequency is not 3.579545MHz, various timing and filter characteristics will need to be redefined with the new CLKIN frequency. For example, the cut-off frequencies of all digital filters (LPF1, LPF2, HPF1, etc.) will shift in proportion to the change in CLKIN frequency according to the following equation:

$$New\ Frequency = Original\ Frequency \times \frac{CLKIN\ Frequency}{3.579545\ MHz} \quad (27)$$

The change of CLKIN frequency does not affect the timing characteristics of the serial interface because the data transfer is synchronized with serial clock signal (SCLK). But one needs to observe the read/write timing of the serial data transfer-see *ADE7753 Timing Characteristics*. Table III lists various timing changes that are affected by CLKIN frequency.

Table III

Frequency dependencies of the ADE7753 parameters

Parameter			CLKIN dependency
Nyquist frequency for CH 1&2 ADCs			CLKIN/8
PHCAL resolution (seconds per LSB)			4/CLKIN
Active Energy register update rate (Hz)			CLKIN/4
Waveform sampling rate (Number of samples per second)			
WAVSEL 1,0 =	0	0	CLKIN/128
	0	1	CLKIN/256
	1	0	CLKIN/512
	1	1	CLKIN/1024
Maximum ZXTOUT period			524,288/CLKIN

SUSPENDING THE ADE7753 FUNCTIONALITY

The analog and the digital circuit can be suspended separately. The analog portion of the ADE7753 can be suspended by setting the ASUSPEND bit (bit 4) of the Mode register to logic high—— See *Mode Register*. In suspend mode, all waveform samples from the ADCs will be set to zeros. The digital circuitry can be halted by stopping the CLKIN input and maintaining a logic high or low on CLKIN pin. The ADE7753 can be reactivated by restoring the CLKIN input and setting the ASUSPEND bit to logic low.

CHECKSUM REGISTER

The ADE7753 has a Checksum register (CHECKSUM[5:0]) to ensure the data bits received in the last serial read operation are not corrupted. The 6-bit Checksum register is reset before the first bit (MSB of the register to be read) is put on the DOUT pin. During a serial read operation, when each data bit becomes available on the rising edge of SCLK, the bit will be added to the Checksum register. In the end of the serial read operation, the content of the Checksum register will equal to the sum of all ones in the register previously read. Using the Checksum register, the user can determine if an error has occured during the last read operation.
Note that a read to the Checksum register will also generate a checksum of the Checksum register itself.

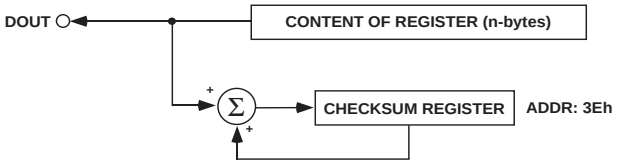


Figure 48– Checksum register for Serial Interface Read

ADE7753 SERIAL INTERFACE

All ADE7753 functionality is accessible via several on-chip registers – see Figure 49. The contents of these registers can be updated or read using the on-chip serial interface. After power-on or toggling the $\overline{\text{RESET}}$ pin low or a falling edge on $\overline{\text{CS}}$, the ADE7753 is placed in communications mode. In communications mode the ADE7753 expects a write to its Communications register. The data written to the communications register determines whether the next data transfer operation will be read or a write and also which register is accessed. Therefore all data transfer operations with the ADE7753, whether a read or a write, must begin with a write to the Communications register.

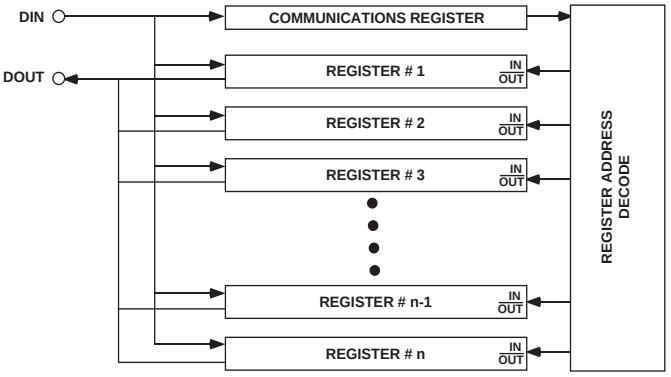


Figure 49– Addressing ADE7753 Registers via the Communications Register

The Communications register is an eight bit wide register. The MSB determines whether the next data transfer operation is a read or a write. The 5 LSBs contain the address of the register to be accessed. See *ADE7753 Communications Register* for a more detailed description.

Figure 50 and 51 show the data transfer sequences for a read and write operation respectively.

On completion of a data transfer (read or write) the ADE7753 once again enters communications mode.

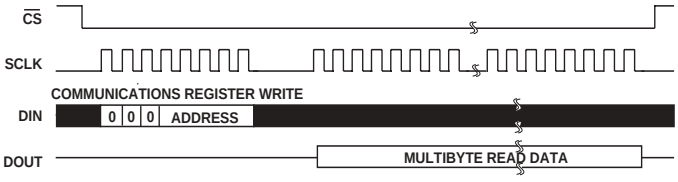


Figure 50– Reading data from the ADE7753 via the serial interface

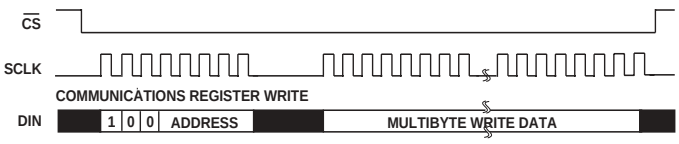


Figure 51– Writing data to the ADE7753 via the serial interface

A data transfer is complete when the LSB of the ADE7753 register being addressed (for a write or a read) is transferred to or from the ADE7753.

The Serial Interface of the ADE7753 is made up of four signals SCLK, DIN, DOUT and $\overline{\text{CS}}$. The serial clock for a data transfer is applied at the SCLK logic input. This logic input has a schmitt-trigger input structure, which allows slow rising (and falling) clock edges to be used. All data transfer operations are synchronized to the serial clock. Data is shifted into the ADE7753 at the DIN logic input on the falling edge of SCLK. Data is shifted out of the ADE7753 at the DOUT logic output on a rising edge of SCLK. The $\overline{\text{CS}}$ logic input is the chip select input. This input is used when multiple devices share the serial bus. A falling edge on $\overline{\text{CS}}$ also resets the serial interface and places the ADE7753 in communications mode. The $\overline{\text{CS}}$ input should be driven low for the entire data transfer operation. Bringing $\overline{\text{CS}}$ high during a data transfer operation will abort the transfer and place the serial bus in a high impedance state. The $\overline{\text{CS}}$ logic input may be tied low if the ADE7753 is the only device on the serial bus. However with $\overline{\text{CS}}$ tied low, all initiated data transfer operations must be fully completed, i.e., the LSB of each register must be transferred as there is no other way of bringing the ADE7753 back into communications mode without resetting the entire device, i.e., using $\overline{\text{RESET}}$.

ADE7753 Serial Write Operation

The serial write sequence takes place as follows. With the ADE7753 in communications mode (i.e. the $\overline{\text{CS}}$ input logic low), a write to the communications register first takes place. The MSB of this byte transfer is a 1, indicating that the data transfer operation is a write. The LSBs of this byte contain the address of the register to be written to. The ADE7753 starts shifting in the register data on the next falling edge of SCLK. All remaining bits of register data are shifted in on the falling edge of subsequent SCLK pulses – see Figure 51.

As explained earlier the data write is initiated by a write to the communications register followed by the data. During a data write operation to the ADE7753, data is transferred to all on-chip registers one byte at a time. After a byte is transferred into the serial port, there is a finite time before it is transferred to one of the ADE7753 on-chip registers. Although another byte transfer to the serial port can start while the previous byte is being transferred to an on-chip register, this second byte transfer should not finish until at least 4μs after the end of the previous byte transfer. This functionality is expressed in the timing specification t_6 - see Figure 51. If a write operation is aborted during a byte transfer ($\overline{\text{CS}}$ brought high), then that byte will not be written to the destination register.

Destination registers may be up to 3 bytes wide – see *ADE7753 Register Descriptions*. Hence the first byte shifted into the serial port at DIN is transferred to the MSB (Most significant Byte) of the destination register. If the addressed register is 12 bits wide, for example, a two-byte data transfer must take place. The data is always assumed to be right justified, therefore in this case, the four MSBs of the first byte would be ignored and the 4 LSBs of the first byte written to the ADE7753 would be the 4MSBs of the 12-bit word. Figure 52 illustrates this example.

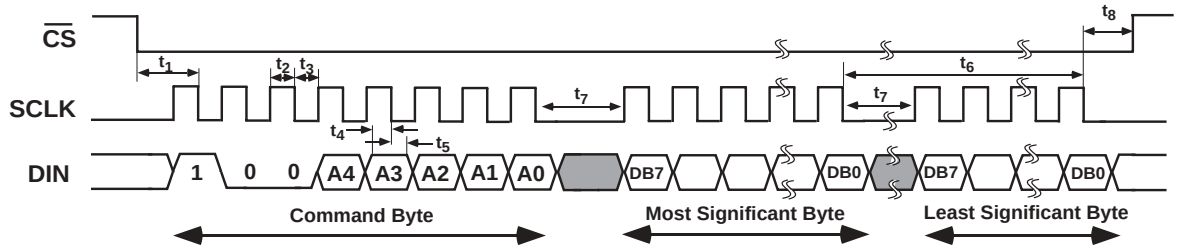


Figure 52 – Serial Interface Write Timing Diagram

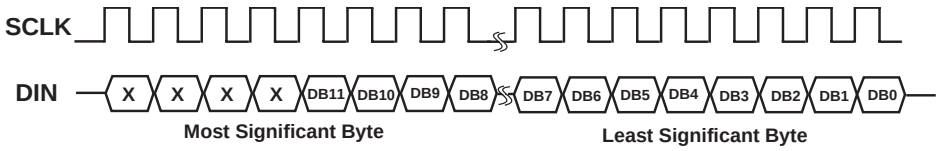


Figure 53—12 bit Serial Write Operation

ADE7753 Serial Read Operation

During a data read operation from the ADE7753 data is shifted out at the DOUT logic output on the rising edge of SCLK. As was the case with the data write operation, a data read must be preceded with a write to the Communications register.

With the ADE7753 in communications mode (i.e. $\overline{CS}$ logic low) an eight bit write to the Communications register first takes place. The MSB of this byte transfer is a 0, indicating that the next data transfer operation is a read. The LSBs of this byte contain the address of the register which is to be read. The ADE7753 starts shifting out of the register data on the next rising edge of SCLK – see Figure 54. At this point the DOUT logic output leaves its high impedance state and starts driving the data bus. All remaining bits of register data are shifted out on subsequent SCLK rising edges. The serial interface also enters communications mode again as soon as the read has been completed. At this point the DOUT logic output enters a high impedance state on the falling edge of the last SCLK pulse. The read operation may be aborted by bringing the $\overline{CS}$ logic input high before the data transfer is complete. The DOUT output enters a high impedance state on the rising edge of $\overline{CS}$.

When an ADE7753 register is addressed for a read operation, the entire contents of that register are transferred to the serial port. This allows the ADE7753 to modify its on-chip registers without the risk of corrupting data during a multi byte transfer.

Note when a read operation follows a write operation, the read command (i.e., write to communications register) should not happen for at least 4µs after the end of the write operation. If the read command is sent within 4µs of the write operation, the last byte of the write operation may be lost. The is given as timing specification t_9.

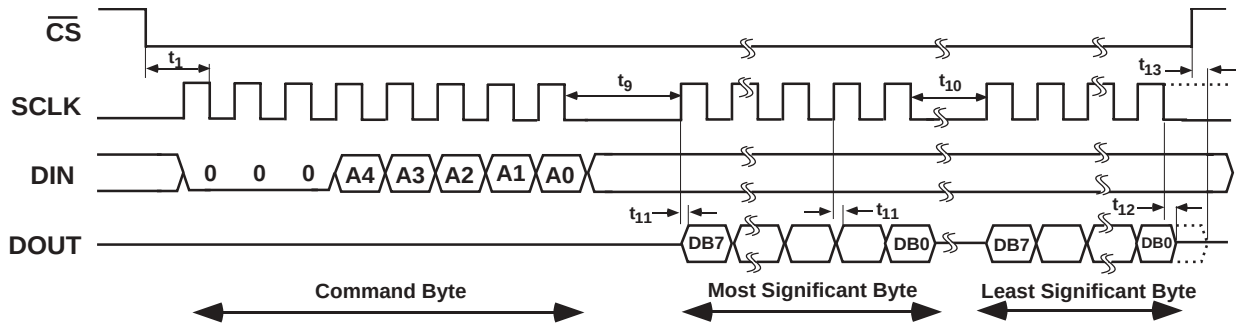


Figure 54– Serial Interface Read Timing Diagram

ADE7753 REGISTER LIST

Address	Name	R/W	# of Bits	Default	Description
01h	WAVEFORM	R	24 bits	0h	The Waveform register is a read-only register. This register contains the sampled waveform data from either Channel 1, Channel 2 or the Active Power signal. The data source and the length of the waveform registers are selected by data bits 14 and 13 in the Mode Register - see *Channel 1 & 2 Sampling*.
02h	AENERGY	R	24 bits	0h	The Active Energy register. Active Power is accumulated (Integrated) over time in this 24-bit, read-only register. The energy register can hold a minimum of 6 seconds of Active Energy information with full scale analog inputs before it overflows - see *Energy Calculation*.
03h	RAENERGY	R	24 bits	0h	Same as the Active Energy register except that the register is reset to zero following a read operation
04h	LAENERGY	R	24 bits	0h	Line Accumulation Active Energy register. The instantaneous active power is accumulated in this read-only register over the LINCYC number of half line cycles.
05h	VAENERGY	R	24 bits	0h	Apparent Energy register. Apparent power is accumulated over time in this read-only register.
06h	RVAENERGY	R	24 bits	0h	Same as the VAENERGY register except that the register is reset to zero following a read operation.
07h	LVAENERGY	R	24 bits	0h	Apparent Energy register. The instantaneous real power is accumulated in this read-only register over the LINECYC number of half line cycles
08h	LVARENERGY	R	24 bits	0h	Reactive Energy register. The instantaneous reactive power is accumulated in this read-only register over the LINECYC number of half line cycles.
09h	MODE	R/W	16 bits	000Ch	The Mode register. This is a 16-bit register through which most of the ADE7753 functionality is accessed. Signal sample rates, filter enabling and calibration modes are selected by writing to this register. The contents may be read at any time—see *Mode Register*.
0Ah	IRQEN	R/W	16 bits	40h	Interrupt Enable register. ADE7753 interrupts may be deactivated at any time by setting the corresponding bit in this 8-bit Enable register to logic zero. The Status register will continue to register an interrupt event even if disabled. However, the $\overline{\text{IRQ}}$ output will not be activated—see *ADE7753 Interrupts*.
0Bh	STATUS	R	16 bits	0h	The Interrupt Status register. This is an 8-bit read-only register. The Status Register contains information regarding the source of ADE7753 interrupts - see *ADE7753 Interrupts*.
0Ch	RSTSTATUS	R	16 bits	0h	Same as the Interrupt Status register except that the register contents are reset to zero (all flags cleared) after a read operation.
0Dh	CH1OS	R/W	8 bits	00h	Channel 1 Offset Adjust. Bit 6 is not used. Writing to bits 0 to 5 allows offsets on Channel 1 to be removed – see *Analog Inputs and CH1OS Register*. Writing a logic one to the MSB of this register enables the digital integrator on Channel 1, a zero disables the integrator. The default value of this bit is zero.
0Eh	CH2OS	R/W	8 bits	0h	Channel 2 Offset Adjust. Bit 6 and 7 not used. Writing to bits 0 to 5 of this register allows any offsets on Channel 2 to be removed - see *Analog Inputs*.
0Fh	GAIN	R/W	8 bits	0h	PGA Gain Adjust. This 8-bit register is used to adjust the gain selection for the PGA in Channel 1 and 2 - see *Analog Inputs*.

Address	Name	R/W	# of Bits	Default	Description
10h	PHCAL	R/W	6 bits	0Dh	Phase Calibration register. The phase relationship between Channel 1 and 2 can be adjusted by writing to this 6-bit register. The valid content of this 2's compliment register is between 1Dh to 21h. At line frequency of 60Hz, this is a range from -2.06 to +0.7 degrees. —see *Phase Compensation*.
11h	APOS	R/W	16 bits	0h	Active Power Offset Correction. This 16-bit register allows small offsets in the Active Power Calculation to be removed – see *Active Power Calculation*.
12h	WGAIN	R/W	12 bits	0h	Power Gain Adjust. This is a 12-bit register. The Active Power calculation can be calibrated by writing to this register. The calibration range is ±50% of the nominal full scale active power. The resolution of the gain adjust is 0.0244% / LSB—see *Channel 1 ADC Gain Adjust*.
13h	WDIV	R/W	8 bits	0h	Active Energy divider register. The internal active energy register is divided by the value of this register before being stored in the AENERGY register.
14h	CFNUM	R/W	12 bits	3Fh	CF Frequency Divider Numerator register. The output frequency on the CF pin is adjusted by writing to this 12-bit read/write register – see *Energy to Frequency Conversion*.
15h	CFDEN	R/W	12 bits	3Fh	CF Frequency Divider Denominator register. The output frequency on the CF pin is adjusted by writing to this 12-bit read/write register – see *Energy to Frequency Conversion*.
16h	IRMS	R	24 bits	0h	Channel 1 RMS value (current channel).
17h	VRMS	R	24 bits	0h	Channel 2 RMS value (voltage channel).
18h	IRMSOS	R/W	12 bits	0h	Channel 1 RMS offset correction register
19h	VRMSOS	R/W	12 bits	0h	Channel 2 RMS offset correction register
1Ah	VAGAIN	R/W	12 bits	0h	Apparent Gain register. Apparent power calculation can be calibrated by writing this register. The calibration range is 50% of the nominal full scale real power. The resolution of the gain adjust is 0.02444% / LSB.
1Bh	VADIV	R/W	8 bits	0h	Apparent Energy divider register. The internal apparent energy register is divided by the value of this register before being stored in the VAENERGY register.
1Ch	LINECYC	R/W	15 bits	FFFh	Line Cycle Energy Accumulation Mode Line-Cycle register. This 15-bit register is used during line cycle energy accumulation mode to set the number of half line cycles for energy accumulation - see *Line Cycle Energy Accumulation Mode*.
1Dh	ZXTOUT	R/W	12 bits	FFFh	Zero-cross Time Out. If no zero crossings are detected on Channel 2 within a time period specified by this 12-bit register, the interrupt request line ($\overline{\text{IRQ}}$) will be activated. The maximum time-out period is 0.15 second - see *Zero Crossing Detection*.
1Eh	SAGCYC	R/W	8 bits	FFh	Sag line Cycle register. This 8-bit register specifies the number of consecutive line cycles the signal on Channel 2 must be below SAGLVL before the $\overline{\text{SAG}}$ output is activated - see *Voltage Sag Detection*
1Fh	SAGLVL	R/W	8 bits	0h	Sag Voltage Level. An 8-bit write to this register determines at what peak signal level on Channel 2 the SAG pin will become active. The signal must remain low for the number of cycles specified in the SAGCYC register before the SAG pin is activated—see *Line Voltage Sag Detection*.
20h	IPKLVL	R/W	8 bits	FFh	Channel 1 Peak Level threshold (current channel). This register sets the level of the current peak detection. If the channel 1 input exceeds this level, the PKI flag in the status register is set.

Address	Name	R/W	# of Bits	Default	Description
21h	VPKLVL	R/W	8 bits	FFh	Channel 2 Peak Level threshold (voltage channel). This register sets the level of the voltage peak detection. If the channel 2 input exceeds this level, the PKV flag in the status register is set.
22h	IPEAK	R	24 bits	0h	Channel 1 peak register. The maximum input value of the Current channel since the last read of the register is stored in this register.
23h	RSTIPEAK	R	24 bits	0h	Same as Channel 1 peak register except that the register contents are reset to 0 after read.
24h	VPEAK	R	24 bits	0h	Channel 2 peak register. The maximum input value of the Voltage channel since the last read of the register is stored in this register.
25h	RSTVPEAK	R	24 bits	0h	Same as Channel 2 peak register except that the register contents are reset to 0 after a read.
26h	TEMP	R	8 bits	0h	Temperature register. This is an 8-bit register which contains the result of the latest temperature conversion – see *Temperature Measurement*.
27h	PERIOD	R	15 bits	0h	Period of the channel 2 (volatge channel) input estimated by Zero-crossing processing.
28h-3Ch					Reserved
3Dh	TMODE	R/W	8 bits	-	Test mode register
3Eh	CHKSUM	R	6 bits	0h	Checksum Register. This 6-bit read only register is equal to the sum of all the ones in the previous read – see *ADE7753 Serial Read Operation.*
3Fh	DIEREV	R	8 bits	-	Die Revision Register. This 8-bit read only register contains the revision number of the silicon.

ADE7753 REGISTER DESCRIPTIONS

All ADE7753 functionality is accessed via the on-chip registers. Each register is accessed by first writing to the communications register and then transferring the register data. A full description of the serial interface protocol is given in the *Serial Interface* section of this data sheet.

Communications Register

The Communications register is an 8-bit, write-only register which controls the serial data transfer between the ADE7753 and the host processor. All data transfer operations must begin with a write to the communications register. The data written to the communications register determines whether the next operation is a read or a write and which register is being accessed. Table IV below outlines the bit designations for the Communications register.

Table V. Communications Register

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W/$\overline{R}$	0	A5	A4	A3	A2	A1	A0

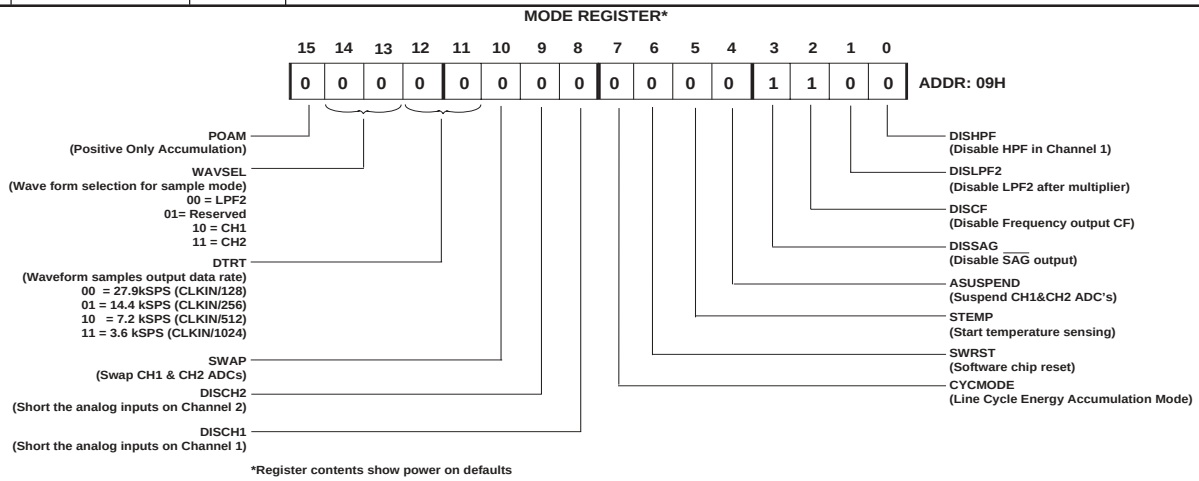
Bit Location	Bit Mnemonic	Description
0 to 5	A0 to A5	The six LSBs of the Communications register specify the register for the data transfer operation. Table III lists the address of each ADE7753 on-chip register.
6	RESERVED	This bit is unused and should be set to zero.
7	W/$\overline{R}$	When this bit is a logic one the data transfer operation immediately following the write to the Communications register will be interpreted as a write to the ADE7753. When this bit is a logic zero the data transfer operation immediately following the write to the Communications register will be interpreted as a read operation.

Mode Register (09H)

The ADE7753 functionality is configured by writing to the MODE register. Table VI below summarizes the functionality of each bit in the MODE register .

Table VI : Mode Register

Bit Location	Bit Mnemonic	Default Value	Description
0	DISHPF	0	The HPF (High Pass Filter) in Channel 1 is disabled when this bit is set.
1	DISLPF2	0	The LPF (Low Pass Filter) after the multiplier (LPF2) is disabled when this bit is set.
2	DISCF	1	The Frequency output CF is disabled when this bit is set
3	DISSAG	1	The line voltage Sag detection is disabled when this bit is set
4	ASUSPEND	0	By setting this bit to logic one, both ADE7753's A/D converters can be turned off. In normal operation, this bit should be left at logic zero. All digital functionality can be stopped by suspending the clock signal at CLKIN pin.
5	TEMPSEL	0	The Temperature conversion starts when this bit is set to one. This bit is automatically reset to zero when the Temperature conversion is finished.
6	SWRST	0	Software chip reset. A data transfer should not take place to the ADE7753 for at least 18µs after a software reset.
7	CYCMODE	0	Setting this bit to a logic one places the chip in line cycle energy accumulation mode.
8	DISCH1	0	ADC 1 (Channel 1) inputs are internally shorted together.
9	DISCH2	0	ADC 2 (Channel 2) inputs are internally shorted together.
10	SWAP	0	By setting this bit to logic 1 the analog inputs V2P and V2N are connected to ADC 1 and the analog inputs V1P and V1N are connected to ADC 2.
12, 11	DTRT1,0	00	These bits are used to select the Waveform Register update rate DTRT 1 DTRT0 Update Rate 0 0 27.9kSPS (CLKIN/128) 0 1 14kSPS (CLKIN/256) 1 0 7kSPS (CLKIN/512) 1 1 3.5kSPS (CLKIN/1024)
14, 13	WAVSEL1,0	00	These bits are used to select the source of the sampled data for the Waveform Register WAVSEL1,0 Length Source 0 0 24 bits Active Power signal (output of LPF2) 0 1 Reserved 1 0 24 bits Channel 1 1 1 24 bits Channel 2
15	POAM	0	Writing a logic one to this bit will allow only positive power to be accumulated in the ADE7753. The default value of this bit is 0.



Interrupt Status Register (0BH) / Reset Interrupt Status Register (0CH) / Interrupt Enable Register (0Ah)
The Status Register is used by the MCU to determine the source of an interrupt request ($\overline{IRQ}$). When an interrupt event occurs in the ADE7753, the corresponding flag in the Interrupt Status register is set logic high. If the enable bit for this flag is logic one in the Interrupt Enable register, the $\overline{IRQ}$ logic output goes active low. When the MCU services the interrupt it must first carry out a read from the Interrupt Status Register to determine the source of the interrupt.

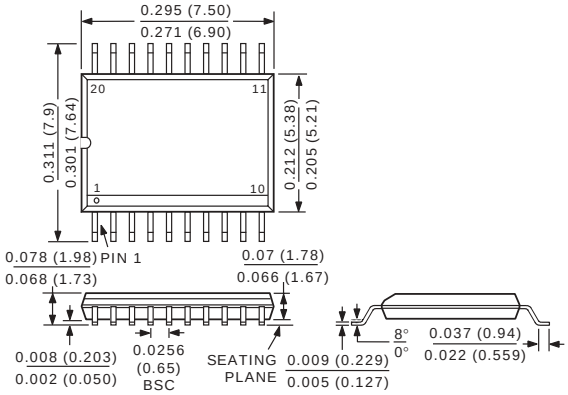
Table VII: Interrupt Status Register, Reset Interrupt Status Register & Interrupt Enable Register

Bit Location	Interrupt Flag	Description
0h	AEHF	Indicates that an interrupt was caused by the 0 to 1 transition of the MSB of the Active Energy register (i.e. the AENERGY register is half full)
1h	SAG	Indicates that an interrupt was caused by a SAG on the line voltage or no zero crossings were detected.
2h	CYCEND	Indicates the end of energy accumulation over an integer number of half line cycles as defined by the content of the LINECYC Register—see *Line Cycle Energy Accumulation Mode*
3h	WSMP	Indicates that new data is present in the Waveform Register.
4h	ZX	This status bit reflects the status of the ZX logic ouput—see *Zero Crossing Detection*
5h	TEMP	Indicates that a temperature conversion result is available in the Temperature Register.
6h	RESET	Indicates the end of a reset (for both software or hardware reset). The corresponding enable bit has no function in the Interrupt Enable Register, i.e. this status bit is set at the end of a reset, but it cannot be enabled to cause an interrupt.
7h	AEOF	Indicates that the Active Energy register has overflowed.
8h	PKV	Indicates that waveform sample from Channel2 has exceeded the VPKLVL value.
9h	PKI	Indicates that waveform sample from Channel1 has exceeded the IPKLVL value.
Ah	VAEHF	Indicates that an interrupt was caused by the 0 to 1 transition of the MSB of the Apparent Energy register (i.e. the VAENERGY register is half full)
Bh	VAEOF	Indicates that the Apparent Enrgy register has overflowed.
Ch	ZXTO	Indicates that an interrupt was caused by a missing zero crossing on the line voltage for the specified number of line cycles—see *Zero Crossing Time Out*
Dh	PPOS	Indicates that the power has gone from negative to positive.
Eh	PNEG	Indicates that the power has gone from positive to negative.
Fh	RESERVED	Reserved

OUTLINE DIMENSIONS

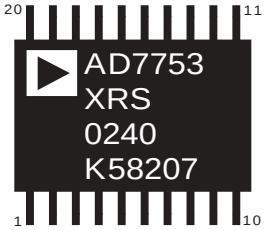
Dimensions shown in inches and (mm)

20-Shrink Small Outline Package
(RS-20)



ADE7753 ERRATA (REV 1.0)

The following is a list of known issues with the first revision of the ADE7753 silicon (rev 1.0). These issues will be resolved in the next version. Samples of this version of the silicon can be identified from the content of the DIEREV regsiter (Address 3Fh). The content of DIEREV register is 2 for Rev 1.2 silicon. In addition, the branding on top of the package for Rev 1.2 should be as shown below:



ERRATA

1. SAGCYC

The contents of SAGCYC register is equivalent to (SAGCYC-1). For example, if the desired number of linecycles for SAG detection is 20d line cycles, one should write 21d to the SAGCYC Register. This is not a silicon bug.

2. CFNUM and CFDEN

CFNUM should always be less than CFDEN. The behavior of the output frequency is not guaranteed for CF. This is not a silicon bug.

REVISION HISTORY

The main reason for revising the datasheet from version Pr.D to Pr.F is to correct some of the mistakes contained in the Pr.D and Pr.E version. In addition, changes were made to the silicon to fix bugs noted in the Errata list and to modify the product definition. The list below highlights the important changes from Pr.D to Pr.F. Note that all page numbers are referring to that of Pr.F.

Page 4

Read timing t_9 is determined to be 3.1us.

Page 12

The SAGCYC register value represents full-line cycles and not half-line cycles. The line voltage SAG detection section text was changed to reflect this design update. Figure 13 shows 3 line cycles, 3h in the SAGCYC register, changed from 6 half line cycles, 6h in the SAGCYC register. The section explaining Figure 13 has also changed accordingly.

Page 13

Peak Level record section was changed to show that the quantity stored in VPEAK register is 2 times the absolute value of the WAVEFORM register contents for CH2. IPEAK is 1 times the absolute value of the CH1 Waveform.

Page 18

1. The phase calibration register resolution has changed to 0.048 from 0.024. This section calculations have been changed to reflect this new resolution.

2. Figure 27 updated with new PHCAL range and delay block rate.

Page 20

Figure 36 Timing was updated.

Page 21

1. The internal active energy accumulation register is 47 bits instead of 53 bits. The equation also shows this change. This change is also implemented in the equations of page 25 as well as Figures 45 and 47 on page 25.

2. The maximum output frequency is changed to 23Hz.

3. Text added to explain CFNUM must be less than CFDEN.

Page 22

1. Figure 39 shows the actual internal register length to be 47 bits. This change is also on page 23, Figure 41.

2. Line Cycle Energy accumulation mode section changed to 15 bits for LINECYC Register.

Page 26

1. Equation 25 changed to have 2^27 bits for the denominator.

2. Content of LAENERGY register is 2971.4, and the CF frequency output in the example calculation is 1398.3 Hz.

3. The calculation of CFNUM and CFDEN changed according to the effect of the abovementioned changes.

Page 31

1. The definition of the SAGCYC a register has changed to full line cycles. LINECYC corrected to say 15 bits and remains half line cycles.

2. The PHCAL register description changed to reflect the new effective length and resolution of the register and default value of 0D.

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.