



## TPD4E1B06 4 通道超低泄露静电放电 (ESD) 保护器件

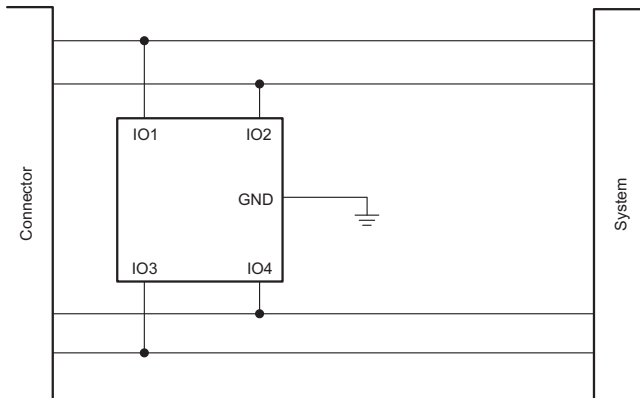
### 1 特性

- 超低泄漏电流 0.5nA (最大值)
- 针对 4 条输入输出 (I/O) 线路的瞬态保护
  - IEC 61000-4-2 接触放电  $\pm 12\text{kV}$
  - IEC 61000-4-2 空气间隙放电  $\pm 15\text{kV}$
  - IEC 61000-4-5 浪涌 3.0A (8/20 $\mu\text{s}$ )
- I/O 电容 0.7pF (典型值)
- 双向瞬态电压抑制器 (TVS) 二极管阵列
- 低 ESD 钳位电压
- 工业温度范围:  $-40^{\circ}\text{C}$  至  $125^{\circ}\text{C}$
- 小型、易于走线的 DRL 和 DCK 封装

### 2 应用范围

- 血糖仪
- 平板电脑
- 全球定位系统 (GPS)
- 便携式媒体播放器
- 电视
- 机顶盒

### 4 简化电路原理图



### 3 说明

TPD4E1B06 是一款 4 通道双向瞬态电压抑制器 (TVS) 二极管阵列。这款器件特有超低泄露电流 (0.5nA) 来实现精确模拟测量。  $\pm 12\text{kV}$  接触和  $\pm 15\text{kV}$  空气间隙 ESD 保护超过 IEC 61000-4-2 4 级要求。

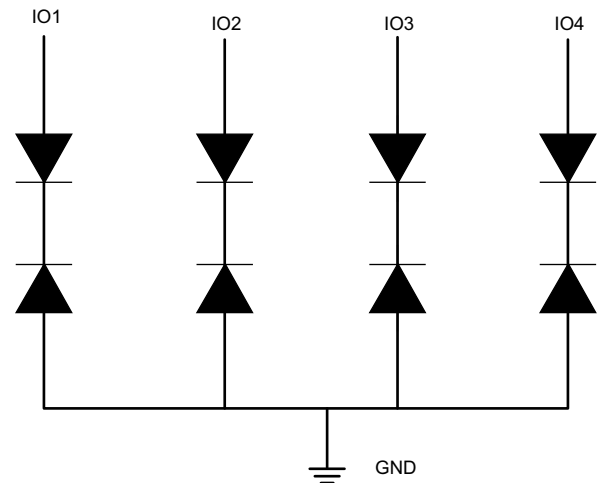
TPD4E1B06 的 0.7pF 线路电容值使得它非常适合于精密模拟, USB2.0, 以太网, SATA, 低压差分信令 (LVDS) 和 1394 接口。

#### 器件信息<sup>(1)</sup>

| 部件号       | 封装                 | 封装尺寸 (标称值)      |
|-----------|--------------------|-----------------|
| TPD4E1B06 | SC70 (6)           | 2.00mm x 2.10mm |
|           | 小外形尺寸晶体管 (SOT) (6) | 1.60mm x 1.60mm |

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

#### 功能方框图



## 目录

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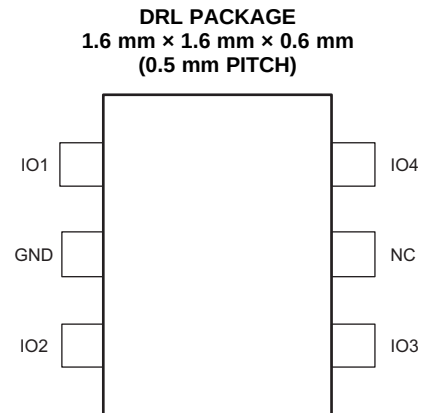
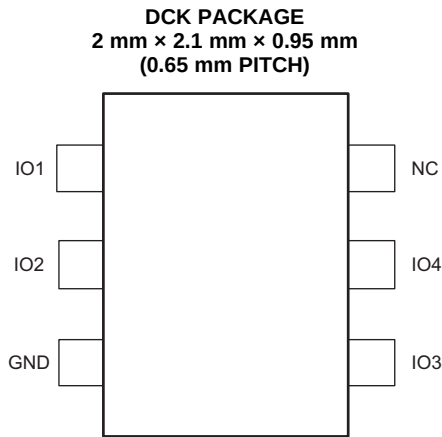
## 5 修订历史记录

| Changes from Revision B (May 2014) to Revision C           | Page |
|------------------------------------------------------------|------|
| • Changed 2 device names from TPD4E6B06 to TPD4E1B06 ..... | 8    |

| Changes from Revision A (January 2013) to Revision B                                      | Page |
|-------------------------------------------------------------------------------------------|------|
| • Changed $I_{PP}$ , peak pulse current from 3.5 A to 3.0 A .....                         | 4    |
| • Added Handling Ratings table. ....                                                      | 4    |
| • Added Recommended Operating Conditions table. ....                                      | 4    |
| • Changed Electrical Characteristics table to reflect operating conditions at 25 °C. .... | 4    |
| • Added MIN $V_{RWM}$ value of -5.5 V. ....                                               | 4    |
| • Changed $V_{CLAMP}$ at $I_{PP} = 1$ A from 10.5 V to 10.9 V. ....                       | 4    |
| • Changed Line Capacitance TYP value from 1 pF to 0.7 pF. ....                            | 4    |
| • Added Line Capacitance MAX value of 0.95 pF. ....                                       | 4    |
| • Changed $I_{LEAK}$ from MAX of 10 nA to 0.5 nA .....                                    | 4    |

| Changes from Original (December 2012) to Revision A                                                  | Page |
|------------------------------------------------------------------------------------------------------|------|
| • 已添加 DRL 封装到数据表。 ....                                                                               | 1    |
| • Fixed "f" units typo from GHz to MHz for $C_L$ parameter in ELECTRICAL CHARACTERISTICS table. .... | 4    |

## 6 Pin Configuration and Functions



### Pin Functions

| PIN  |     |     | TYPE | DESCRIPTION                                                                        |
|------|-----|-----|------|------------------------------------------------------------------------------------|
| NAME | NO. |     |      |                                                                                    |
|      | DCK | DRL |      |                                                                                    |
| IO1  | 1   | 1   | I/O  | ESD protected channel. Connect to data line as close to the connector as possible. |
| IO2  | 2   | 3   | I/O  | ESD protected channel. Connect to data line as close to the connector as possible. |
| IO3  | 4   | 4   | I/O  | ESD protected channel. Connect to data line as close to the connector as possible. |
| IO4  | 5   | 6   | I/O  | ESD protected channel. Connect to data line as close to the connector as possible. |
| GND  | 3   | 2   | GND  | Ground                                                                             |
| NC   | 6   | 5   | NC   | Not internally connected                                                           |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

|                                                                     | MIN | MAX | UNIT |
|---------------------------------------------------------------------|-----|-----|------|
| Operating temperature range                                         | –40 | 125 | °C   |
| $I_{PP}$ , peak pulse current ( $t_p = 8/20 \mu s$ ), IO pin to GND |     | 3.0 | A    |
| $P_{PP}$ , peak pulse power ( $t_p = 8/20 \mu s$ )                  |     | 45  | W    |

### 7.2 Handling Ratings

|                    |                           |                                                                                          | MIN  | MAX | UNIT |
|--------------------|---------------------------|------------------------------------------------------------------------------------------|------|-----|------|
| T <sub>stg</sub>   | Storage temperature range |                                                                                          | −65  | 155 | °C   |
| V <sub>(ESD)</sub> | Electrostatic discharge   | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | −4.0 | 4.0 | kV   |
|                    |                           | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | −1.5 | 1.5 |      |
|                    |                           | IEC 61000-4-2 contact ESD                                                                | −12  | 12  |      |
|                    |                           | IEC 61000-4-2 air-gap ESD                                                                | −15  | 15  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 4 kV may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 1.5 kV may actually have higher performance.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                                                                          | MIN  | MAX | UNIT |
|--------------------------------------------------------------------------|------|-----|------|
| $V_{IO}$ The voltage between any two device pins should not exceed 5.5 V | –5.5 | 5.5 | V    |
| $T_A$ Operating free-air temperature                                     | –40  | 125 | °C   |

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TPD4E1B06 |        | UNIT |
|-------------------------------|----------------------------------------------|-----------|--------|------|
|                               |                                              | DCK       | DRL    |      |
|                               |                                              | 6 PINS    | 6 PINS |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 227.3     | 233.4  | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 79.5      | 95.5   |      |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 72.1      | 68.1   |      |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 3.6       | 7.6    |      |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 70.4      | 67.9   |      |

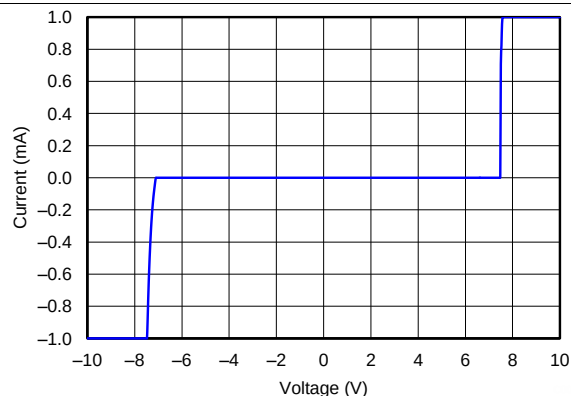
- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

### 7.5 Electrical Characteristics

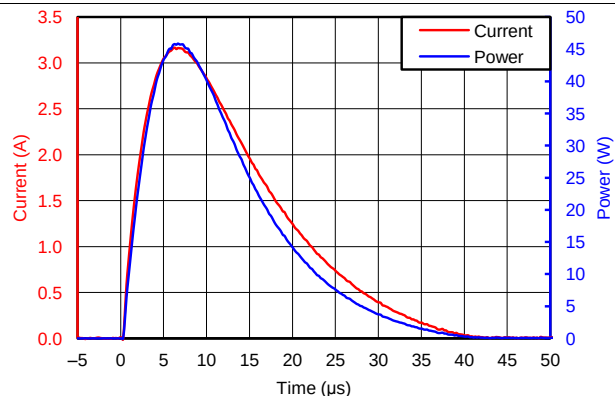
$T_A = 25^\circ\text{C}$

| PARAMETER   | TEST CONDITION                           | MIN                                                                                 | TYP | MAX      | UNIT     |
|-------------|------------------------------------------|-------------------------------------------------------------------------------------|-----|----------|----------|
| $V_{RWM}$   | Reverse stand-off voltage                | –5.5                                                                                |     | 5.5      | V        |
| $V_{CLAMP}$ | Clamp voltage with ESD strike, IO to GND | $I_{PP} = 1 \text{ A}$ , $t_p = 8/20 \mu\text{Sec}$ , from I/O to GND or GND to I/O |     | 10.9     | V        |
|             |                                          | $I_{PP} = 3 \text{ A}$ , $t_p = 8/20 \mu\text{Sec}$ , from I/O to GND or GND to I/O |     | 14.5     | V        |
| $R_{DYN}$   | Dynamic resistance                       | $I_{TLP} = 10 \text{ A to } 20 \text{ A}$ , I/O to GND                              |     | 1        | $\Omega$ |
|             |                                          | $I_{TLP} = 10 \text{ A to } 20 \text{ A}$ , GND to I/O                              |     | 0.8      |          |
| $C_L$       | Line capacitance                         | $f = 1 \text{ MHz}$ , $V_{BIAS} = 2.5 \text{ V}$                                    |     | 0.7 0.95 | pF       |
| $V_{BR}$    | Break-down voltage                       | $I_{IO} = 1 \text{ mA}$ , from I/O to GND or GND to I/O                             |     | 7 9.5    | V        |
| $I_{LEAK}$  | Leakage current                          | $V_{IO} = 2.5 \text{ V}$                                                            |     | 0.5      | nA       |

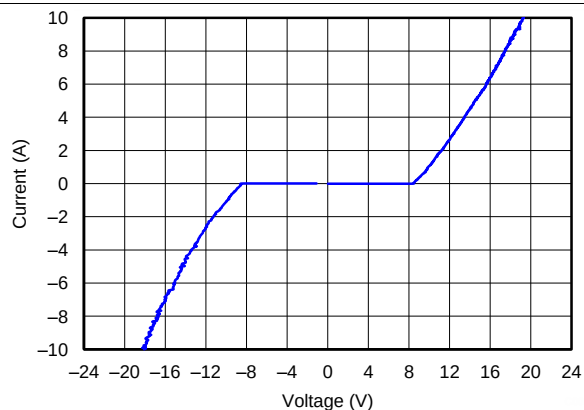
## 7.6 Typical Characteristics



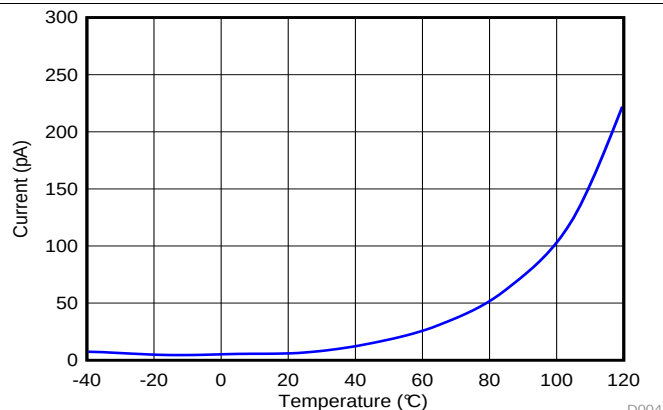
**Figure 1. DC Voltage Sweep I-V Curve**



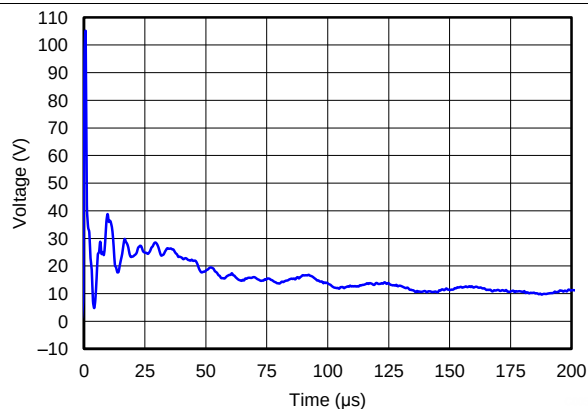
**Figure 2. Surge Curve ( $t_p = 8/20 \mu s$ ), Pin IO to GND**



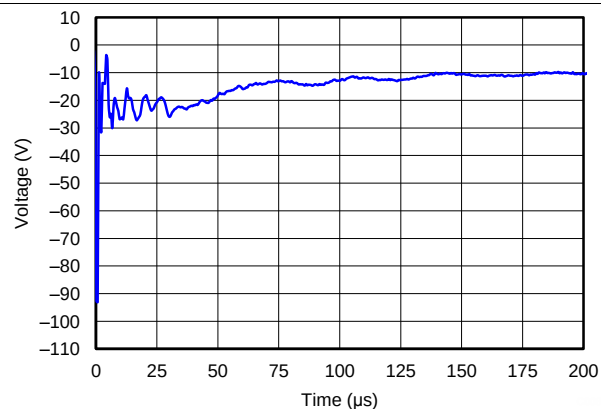
**Figure 3. TLP Plot IO to GND**



**Figure 4. Leakage vs Temperature**



**Figure 5. +8 kV IEC Waveform**



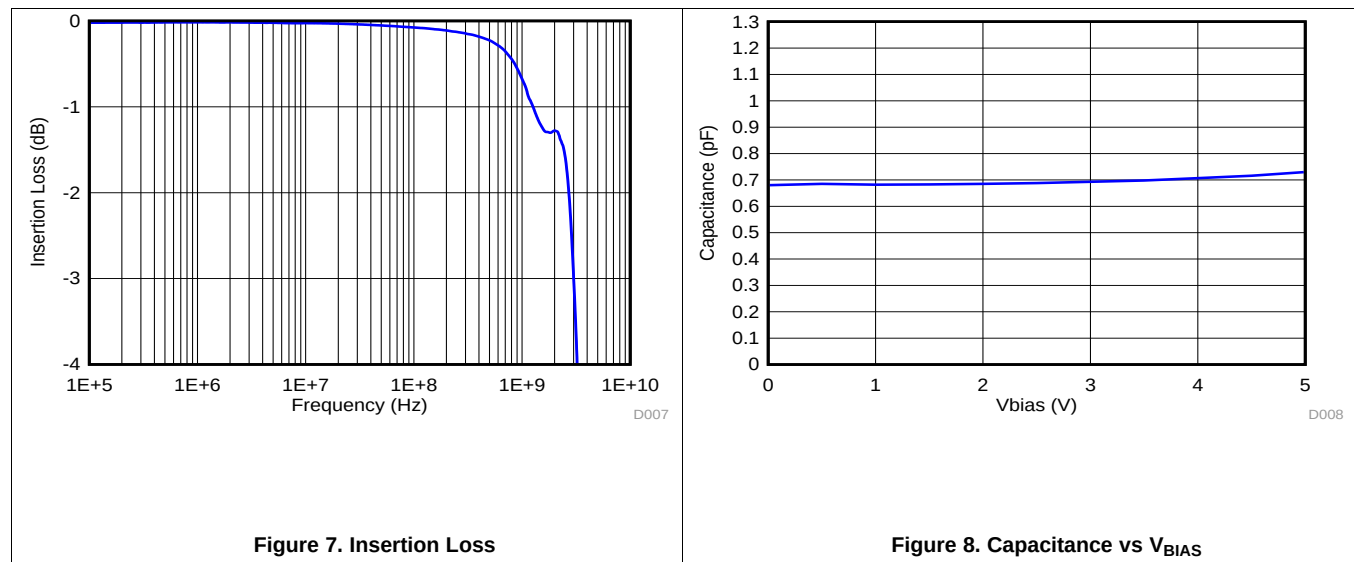
**Figure 6. -8 kV IEC Waveform**

## TPD4E1B06

ZHCSAP5C – DECEMBER 2012 – REVISED JULY 2014

[www.ti.com.cn](http://www.ti.com.cn)

### Typical Characteristics (continued)

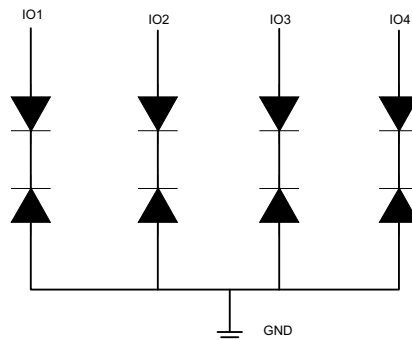


## 8 Detailed Description

### 8.1 Overview

The TPD4E1B06 is a 4-channel bi-directional Transient Voltage Suppressor (TVS) diode array. This device features ultra low leakage current (0.5 nA) for precision analog measurements. The  $\pm 12$  kV contact and  $\pm 15$  kV air gap ESD protection exceeds IEC 61000-4-2 level 4 requirements. The TPD4E1B06's 0.7 pF line capacitance makes it suitable for precision analog, USB2.0, Ethernet, SATA, LVDS, and 1394 interfaces.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The TPD4E1B06 is a 4-channel bi-directional Transient Voltage Suppressor (TVS) diode array. This device features ultra low leakage current (0.5 nA) for precision analog measurements. The  $\pm 12$  kV contact and  $\pm 15$  kV air gap ESD protection exceeds IEC 61000-4-2 level 4 requirements. The TPD4E1B06's 0.7 pF line capacitance makes it suitable for precision analog, USB2.0, Ethernet, SATA, LVDS, and 1394 interfaces.

#### 8.3.1 Ultra low Leakage Current 0.5 nA (Max)

TPD4E1B06 ultra-low leakage current supports long battery life and allows for precision analog measurements.

#### 8.3.2 Transient Protection for 4 I/O Lines

The four I/O pins of TPD4E1B06 can withstand ESD events up to  $\pm 12$  kV contact and  $\pm 15$  kV air gap per IEC61000-4-2.

#### 8.3.3 I/O Capacitance 0.7 pF (Typ)

TPD4E1B06 I/O pins present an ultra-low 0.7 pF capacitance to the protected signal lines, making it suitable for a wide range of applications.

#### 8.3.4 Bi-directional TVS diode array

TPD4E1B06 diode array structure uses back to back diode topology to accommodate bi-directional signaling between  $-5.5$  V and  $5.5$  V.

#### 8.3.5 Low ESD Clamping Voltage

TPD4E1B06 clamps ESD events to a safe level to protect system components.

### 8.4 Device Functional Modes

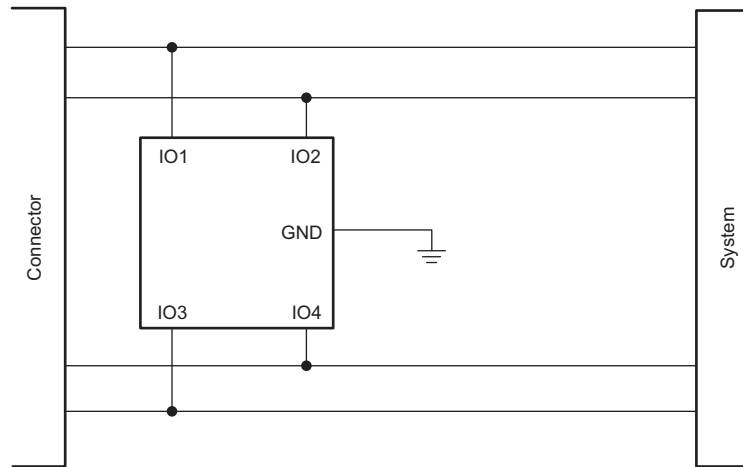
TPD4E1B06 is a passive integrated circuit that activates whenever fast transient voltages above  $V_{BR}$  or below  $-V_{BR}$  are present on the circuit being protected. During ESD events, voltages as high as  $\pm 12$  kV can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4E1B06 (usually within 10's of nano-seconds) the device reverts to passive.

## 9 Application and Implementation

### 9.1 Application Information

TPD4E1B06 is a TVS diode array which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS diode, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low  $R_{DYN}$  of the triggered TVS holds this voltage,  $V_{CLAMP}$ , to a safe level to the protected IC.

### 9.2 Typical Application



**Figure 9. Protecting a Pair of Bi-Directional Differential Data Lines**

The typical application of the TBD4E1B06 is to be placed in between the connector and the system. The low capacitance of the TBD4E1B06 gives flexibility in the end application, as it can be used on many different high speed interfaces.

#### 9.2.1 Design Requirements

**Table 1. Design Parameters**

| DESIGN PARAMETER                        | EXAMPLE VALUE   |
|-----------------------------------------|-----------------|
| Signal range on IO1, IO2, IO3, IO4 Pins | –5.5 V to 5.5 V |
| Operating frequency                     | 1.7 GHz         |

#### 9.2.2 Detailed Design Procedure

The designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency

##### 9.2.2.1 Signal Range on IO1, IO2, IO3, and IO4 Pins

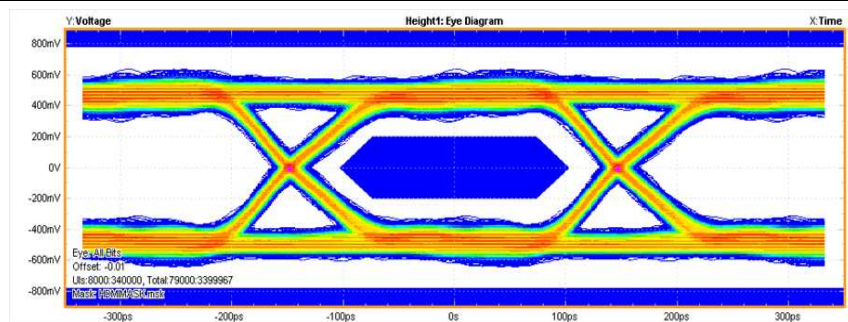
TPD4E1B06 has 4 protection channels for signal lines. Any I/O will support a signal range of –5.5 V to 5.5 V.

##### 9.2.2.2 Operating Frequency

The 0.7 pF capacitance of each I/O channel supports data rates up to 3.4 Gbps.



### 9.2.3 Application Curves



**Figure 10. 3.4 Gbps HDMI 1.4 Eye Diagram in DCK Package**

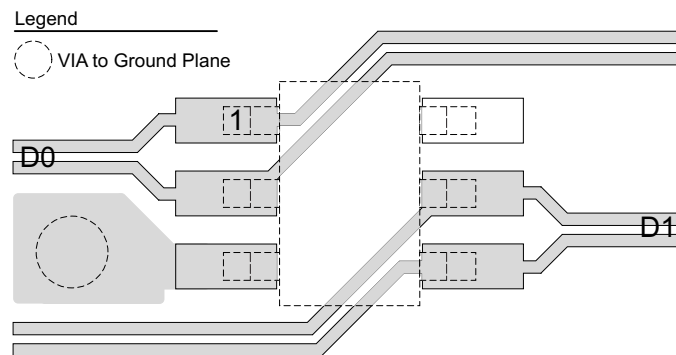
## 10 Layout

### 10.1 Layout Guidelines

- Place the device as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer should minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

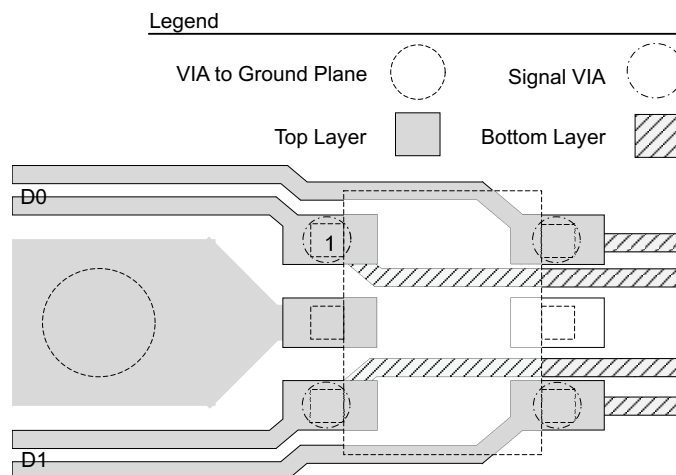
### 10.2 Layout Examples

Figure 11 shows a layout example for the TPD4E1B06DCK. Pins 1 & 2 and 4 & 5 are routed differentially. Pin 3 is routed to the ground plane. Pin 6 does not have an internal connection in the device and does not need to be routed anywhere on the board. It is also acceptable to connect pin 6 to the ground plane.



**Figure 11. DCK Layout Example Showing Two Data Pairs, D0 and D1**

Figure 12 shows a layout example for the TPD4E1B06DRL. Pins 1 & 6 and 3 & 4 are routed differentially. Pin 2 is routed to the ground plane. Pin 5 does not have an internal connection in the device and does not need to be routed anywhere on the board. It is also acceptable to connect pin 5 to the ground plane.



**Figure 12. DRL Layout Example Showing Two Data Pairs, D0 and D1**

## 11 器件和文档支持

### 11.1 商标

All trademarks are the property of their respective owners.

### 11.2 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.3 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

## 12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPD4E1B06DCKR    | ACTIVE        | SC70         | DCK                | 6    | 3000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | BYP                     | <a href="#">Samples</a> |
| TPD4E1B06DRLR    | ACTIVE        | SOT-5X3      | DRL                | 6    | 4000           | RoHS & Green    | NIPDAUAG                             | Level-1-260C-UNLIM   | -40 to 125   | (BYG, BYH)              | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

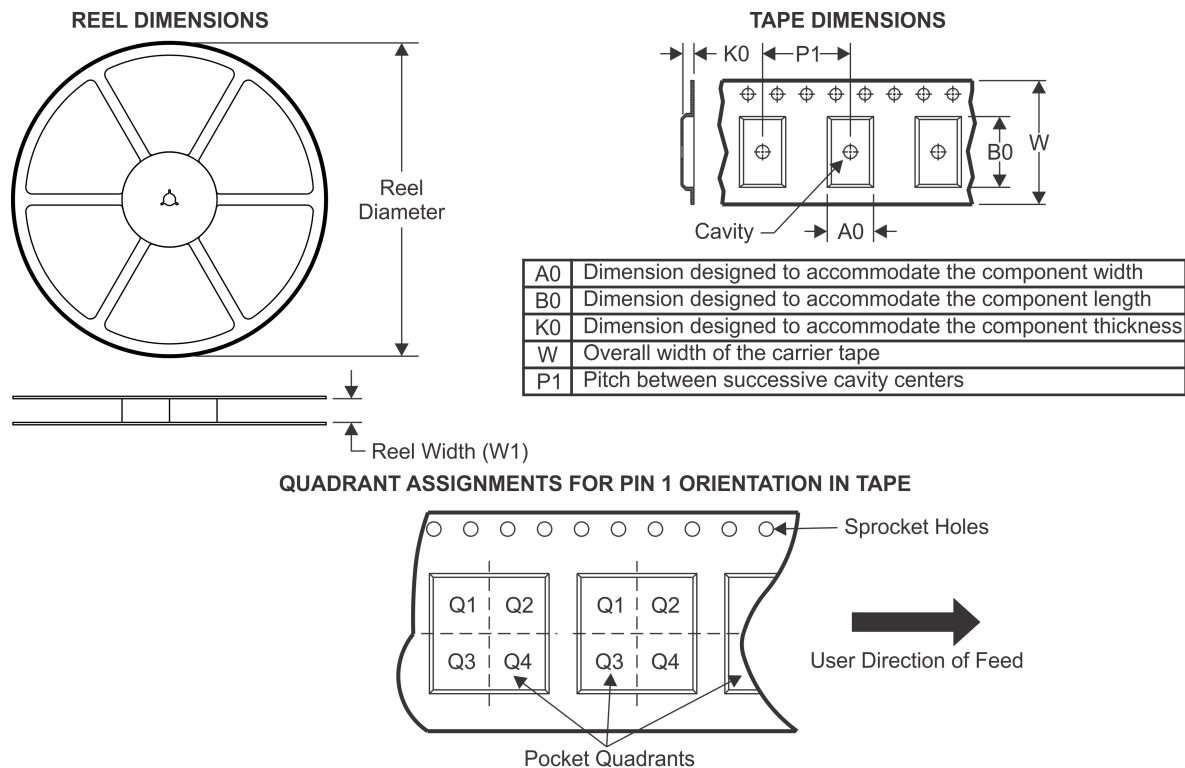
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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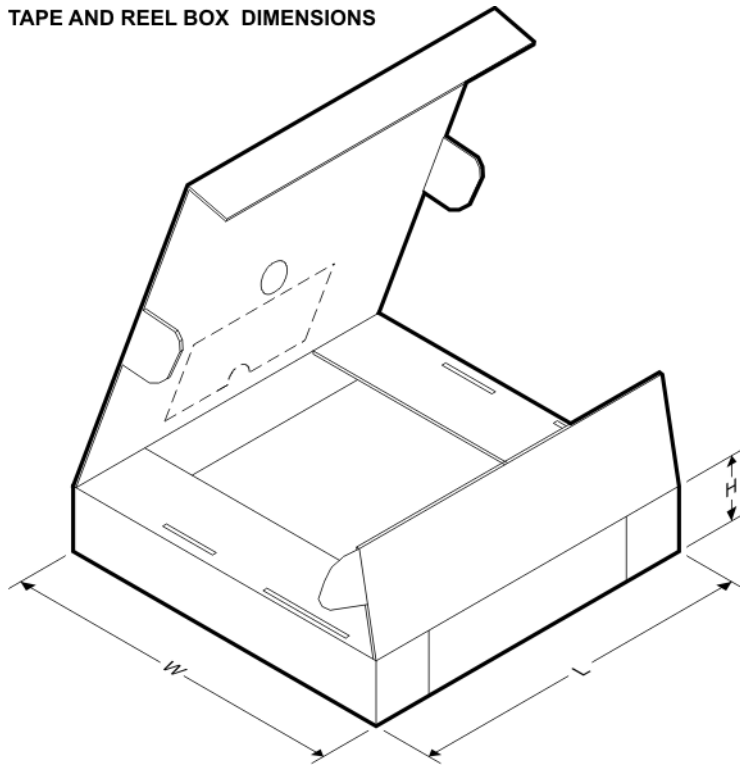


**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

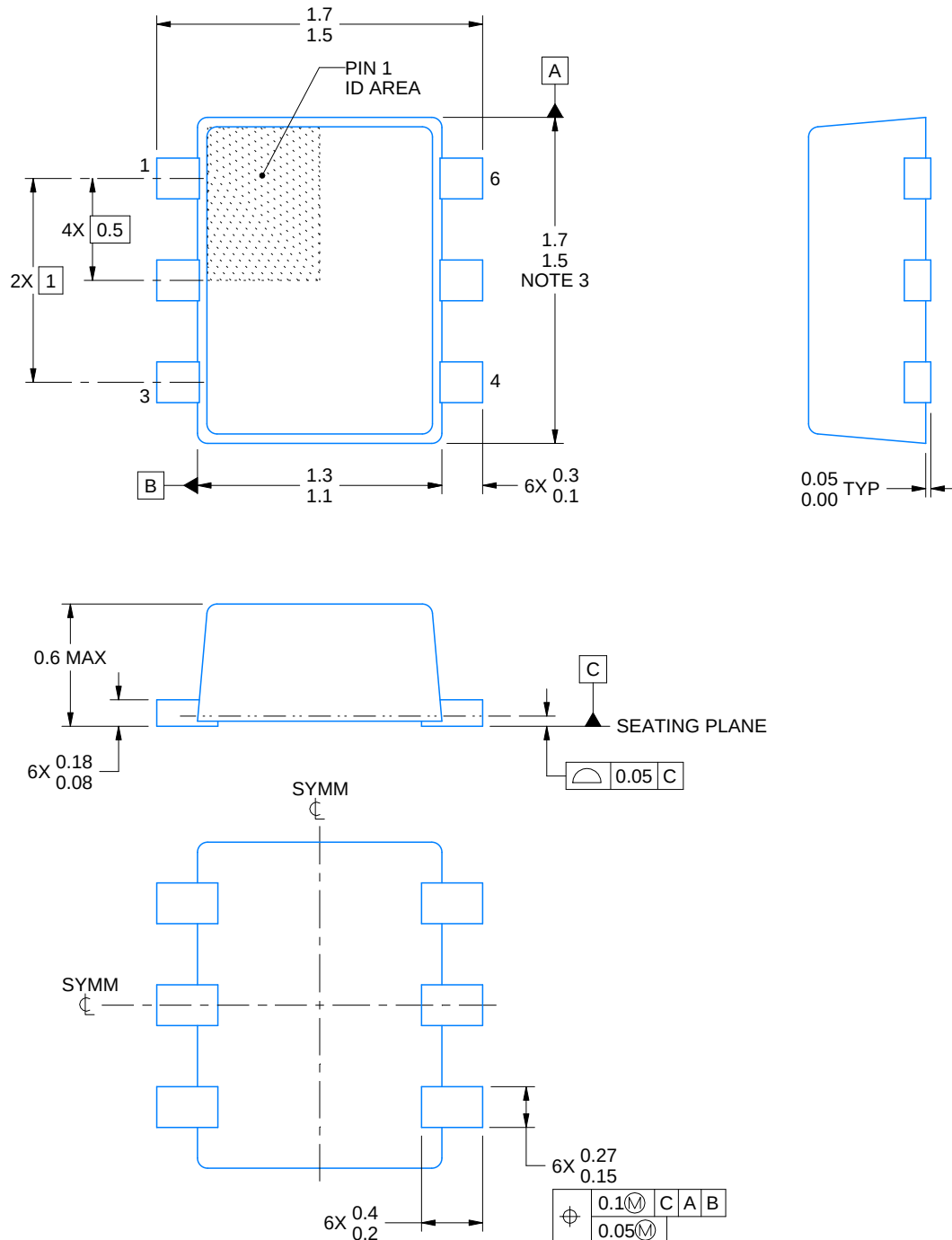
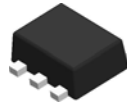
| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPD4E1B06DCKR | SC70         | DCK             | 6    | 3000 | 178.0              | 8.4                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| TPD4E1B06DRLR | SOT-5X3      | DRL             | 6    | 4000 | 180.0              | 8.4                | 1.98    | 1.78    | 0.69    | 4.0     | 8.0    | Q3            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPD4E1B06DCKR | SC70         | DCK             | 6    | 3000 | 180.0       | 180.0      | 18.0        |
| TPD4E1B06DRLR | SOT-5X3      | DRL             | 6    | 4000 | 183.0       | 183.0      | 20.0        |



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## NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-293 Variation UAAD

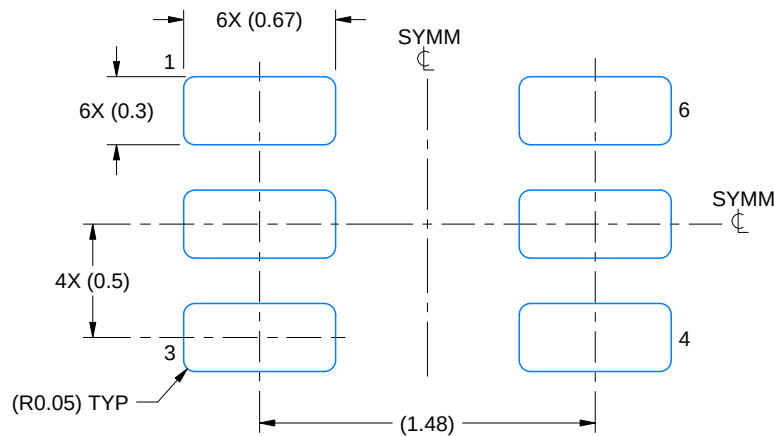


# EXAMPLE BOARD LAYOUT

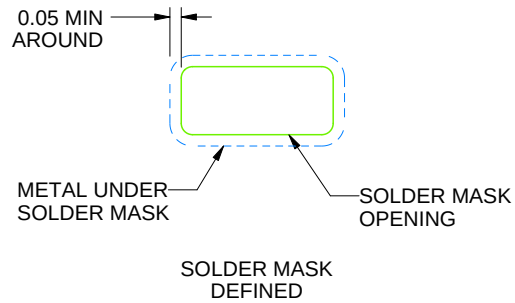
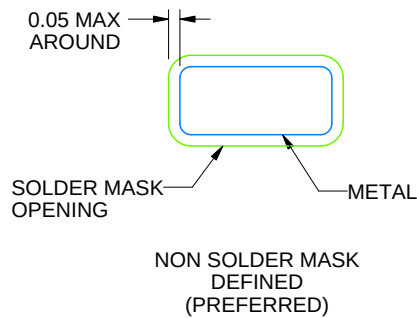
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

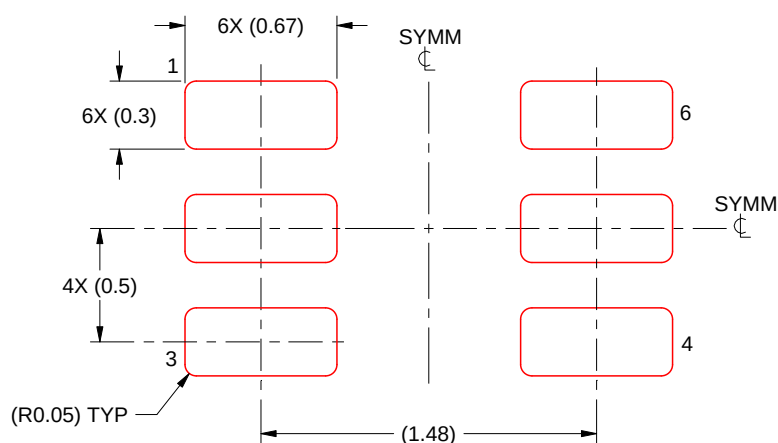
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

## EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

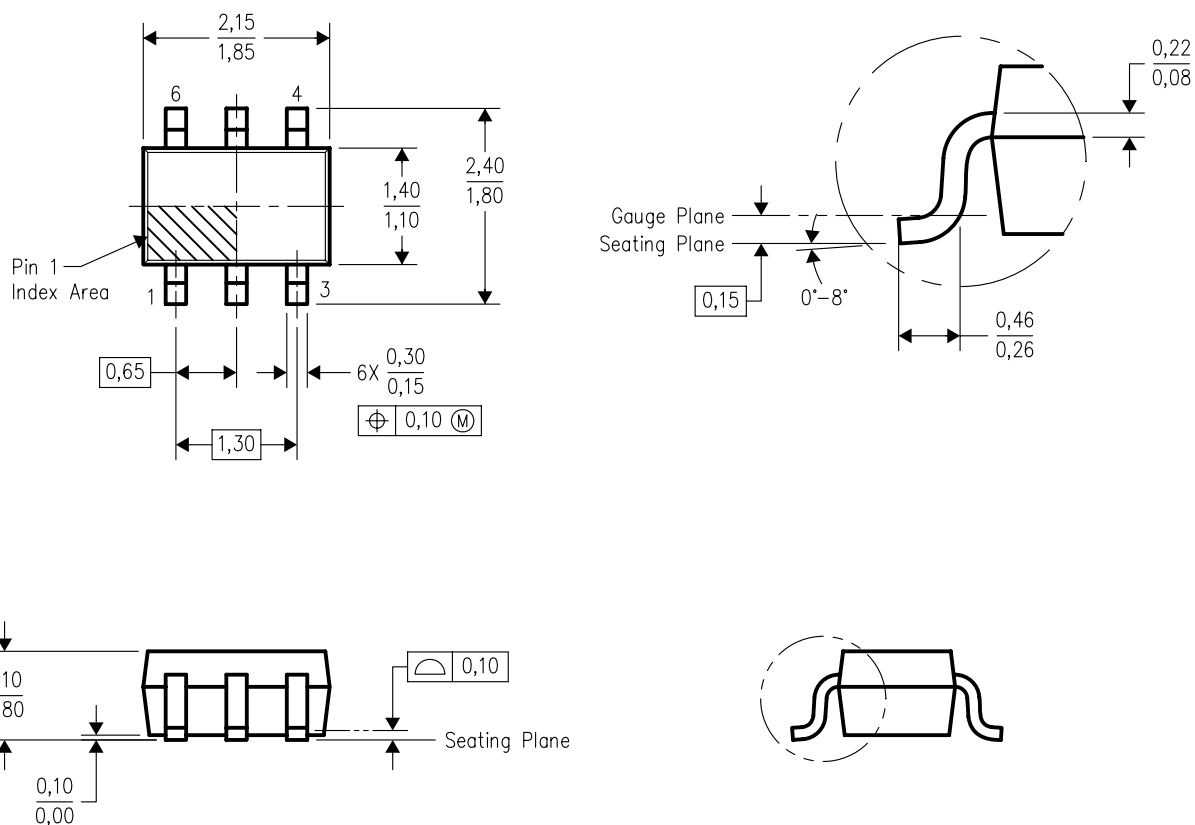
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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## DCK (R-PDSO-G6)

## PLASTIC SMALL-OUTLINE PACKAGE

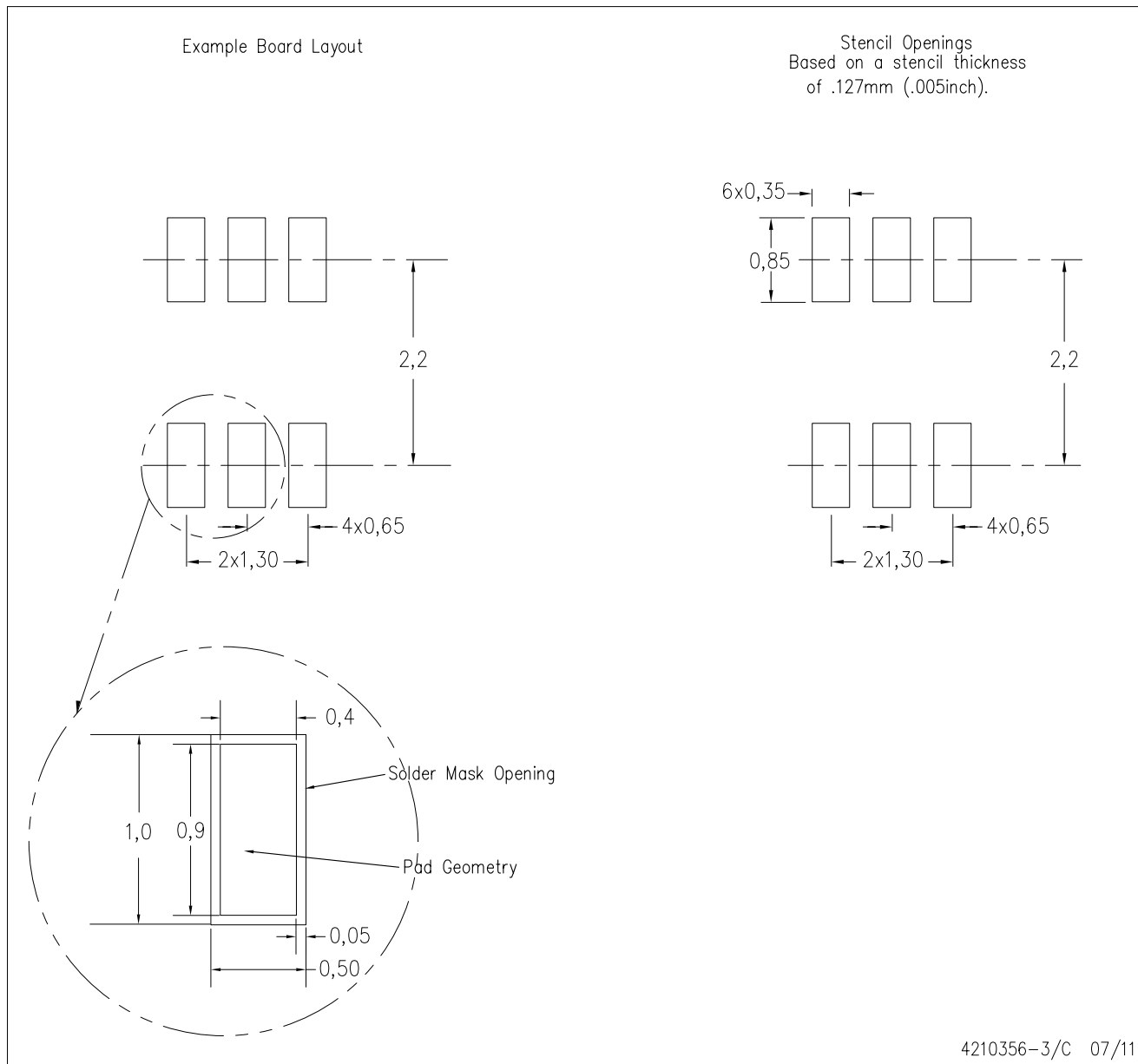


4093553-4/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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