

TL331B-Q1, TL391B-Q1 and TL331-Q1 Automotive Single Comparators

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
 - Device temperature grade 1: –40°C to 125°C ambient operating temperature range (B and Q versions)
 - Device temperature grade 3: –40°C to 85°C ambient operating temperature range (I version)
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C5
- NEW [TL331B-Q1](#) and [TL391B-Q1](#)
- Wide range of supply voltage, 2 V to 36 V
- Low supply-current drain independent of supply voltage:
0.43 mA Typ (B version)
- Low input bias current, 3.5 nA typ (B version)
- Low input offset voltage, 0.37 mV typ (B Version)
- Differential input voltage range equal to maximum-rated supply voltage, ±36 V
- Input range includes ground
- [TL391B-Q1](#) provides an [alternate pinout](#)
- Output compatible With TTL, MOS and CMOS

2 Applications

- [Automotive](#)
- [HEV/EV and power train](#)
- [Infotainment and cluster](#)
- [Body control module](#)

Family Comparison Table

| Specification | TL331B-Q1 TL391B-Q1 | TL331I-Q1 | TL331Q-Q1 | Units |
|--------------------------------------|--|-----------|------------|-------|
| Supply Voltage | 2 to 36 | 2 to 36 | 2 to 36 | V |
| Total Supply Current (5V to 36V max) | 0.43 | 0.7 | 0.7 | mA |
| Temperature Range | –40 to 125 | –40 to 85 | –40 to 125 | °C |
| ESD (HBM) | 2000 | 2000 | 2000 | V |
| Offset Voltage (Max over temp) | ± 4 | ± 9 | ± 9 | mV |
| Input Bias Current (typ / max) | 3.5 / 25 | 25 / 250 | 25 / 250 | nA |
| Response Time (typ) | 1 | 1.3 | 1.3 | µsec |

3 Description

The [TL331B-Q1](#) and [TL391B-Q1](#) devices are the next generation versions of the industry-standard TL331-Q1 comparator. These next generation devices provide outstanding value for cost-sensitive applications, with features including lower offset voltage, higher supply voltage capability, lower supply current, lower input bias current, lower propagation delay, dedicated ESD protection cells with improved negative input voltage handling. The TL331B-Q1 can drop-in replace both the TL331-Q1 "I" and "Q" versions. The [TL391B-Q1](#) provides an [alternate pinout](#) of the TL331B-Q1.

This device consists of a single voltage comparator designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible if the difference between the two supplies is 2 V to 36 V and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. To achieve wired-AND relationships, one can connect the output to other open-collector outputs.

Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) |
|--------------------------------------|------------------------|-------------------|
| TL331B-Q1, TL391B-Q1, TL331-Q1 | SOT-23 (5) | 2.90 mm × 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Table of Contents

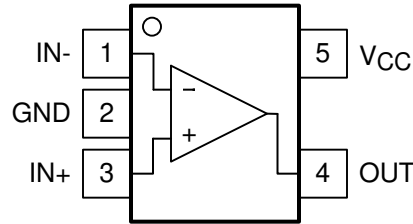
| | | | |
|--|----------|--|-----------|
| 1 Features | 1 | 7 Detailed Description | 15 |
| 2 Applications | 1 | 7.1 Overview..... | 15 |
| 3 Description | 1 | 7.2 Functional Block Diagram..... | 15 |
| Family Comparison Table | 1 | 7.3 Feature Description..... | 15 |
| 4 Revision History | 2 | 7.4 Device Functional Modes..... | 15 |
| 5 Pin Configuration and Functions | 3 | 8 Application and Implementation | 16 |
| 6 Specifications | 4 | 8.1 Application Information..... | 16 |
| 6.1 Absolute Maximum Ratings, TL331-Q1..... | 4 | 8.2 Typical Application..... | 16 |
| 6.2 Absolute Maximum Ratings, TL331B-Q1 and TL391B-Q1..... | 4 | 9 Power Supply Recommendations | 18 |
| 6.3 ESD Ratings, All Devices..... | 4 | 10 Layout | 18 |
| 6.4 Recommended Operating Conditions, TL331-Q1..... | 5 | 10.1 Layout Guidelines..... | 18 |
| 6.5 Recommended Operating Conditions, TL331B- Q1 and TL391B-Q1..... | 5 | 10.2 Layout Example..... | 18 |
| 6.6 Thermal Information..... | 5 | 11 Device and Documentation Support | 19 |
| 6.7 Electrical Characteristics, TL331B-Q1 and TL391B-Q1..... | 6 | 11.1 Documentation Support..... | 19 |
| 6.8 Switching Characteristics, TL331B-Q1 and TL391B-Q1..... | 6 | 11.2 Receiving Notification of Documentation Updates.. | 19 |
| 6.9 Electrical Characteristics, TL331-Q1..... | 7 | 11.3 Support Resources..... | 19 |
| 6.10 Switching Characteristics, TL331-Q1..... | 7 | 11.4 Trademarks..... | 19 |
| 6.11 Typical Characteristics, TL331-Q1..... | 8 | 11.5 Electrostatic Discharge Caution..... | 19 |
| 6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1..... | 9 | 11.6 Glossary..... | 19 |
| | | 12 Mechanical, Packaging, and Orderable Information | 19 |

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

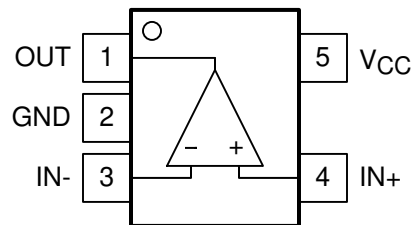
| | |
|--|-------------|
| Changes from Revision E (November 2020) to Revision F (January 2021) | Page |
| • Corrected front page link text to add missing "B"..... | 1 |
| Changes from Revision D (June 2020) to Revision E (November 2020) | Page |
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1 |
| • Changed TL331B-Q1 and TL391B-Q1 minimum recommended supply voltage to 2V throughout datasheet... | 1 |
| • Corrected supply voltages for all devices in Family Comparison Table..... | 1 |
| • Added TL331B-Q1 and TLV391B-Q1 Typical Graphs..... | 9 |
| Changes from Revision C (October 2013) to Revision D (June 2020) | Page |
| • Added B device. Updated to current TI datasheet format. Modified front page text to highlight B version..... | 1 |
| • Added Family Comparison Table..... | 1 |
| • Added Links to Family Table..... | 1 |
| Changes from Revision B (September 2012) to Revision C (October 2013) | Page |
| • Changed V_{ICR} in the Electrical Characteristics..... | 7 |
| • Changed test conditions of I_{OL} in the Electrical Characteristics..... | 7 |
| Changes from Revision A (July 2010) to Revision B (September 2012) | Page |
| • Changed V_{ICR} in the Electrical Characteristics..... | 7 |

5 Pin Configuration and Functions



Note reversed inputs compared to similar popular pinout

**Figure 5-1. TL331-Q1, TL331B-Q1 DBV Package
5-Pin SOT-23
Top View**



Note reversed inputs compared to similar popular pinout

**Figure 5-2. TL391B-Q1 DBV Package
5-Pin SOT-23
Top View**

Table 5-1. Pin Functions

| NAME | PIN | | TYPE | DESCRIPTION |
|-----------------|-------------------------------|------------------|------|-----------------------------|
| | TL331-Q1, TL331B-Q1 NO. | TL391B-Q1 NO. | | |
| IN+ | 3 | 4 | I | Positive Input |
| IN- | 1 | 3 | I | Negative Input |
| OUT | 4 | 1 | O | Open Collector/Drain Output |
| V _{CC} | 5 | 5 | — | Power Supply Input |
| GND | 2 | 2 | — | Ground |

6 Specifications

6.1 Absolute Maximum Ratings, TL331-Q1

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|-----------|-----|------|
| V _{CC} | Supply voltage ⁽²⁾ | 0 | 36 | V |
| V _{ID} | Differential input voltage ⁽³⁾ | -36 | 36 | V |
| V _I | Input voltage range (either input) | -0.3 | 36 | V |
| V _O | Output voltage | 0 | 36 | V |
| I _O | Output current | 0 | 20 | mA |
| | Duration of output short-circuit to ground ⁽⁴⁾ | Unlimited | | |
| T _J | Operating virtual junction temperature | 150 | | °C |
| T _{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 Absolute Maximum Ratings, TL331B-Q1 and TL391B-Q1

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|-----------|-----|------|
| V _{CC} | Supply voltage ⁽²⁾ | -0.3 | 38 | V |
| V _{ID} | Differential input voltage ⁽³⁾ | -38 | 38 | V |
| V _I | Input voltage range (either input) | -0.3 | 38 | V |
| V _O | Output voltage | -0.3 | 38 | V |
| I _O | Output current | | 20 | mA |
| | Duration of output short-circuit to ground ⁽⁴⁾ | Unlimited | | |
| I _{IK} | Input current ⁽⁵⁾ | | -50 | mA |
| T _J | Operating virtual junction temperature | -40 | 150 | °C |
| T _{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
- (5) Input current flows thorough parasitic diode to ground and will turn on parasitic transistors that will increase ICC and may cause output to be incorrect. Normal operation resumes when input current is removed.

6.3 ESD Ratings, All Devices

| | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2000 |
| | | Charged-device model (CDM), per AEC Q100-0111 | ±750 |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions, TL331-Q1

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-----------------|------------------------------------|-----|-----|------|
| V _{CC} | Supply voltage | 2 | 36 | V |
| T _J | Junction temperature, TL331IDBVRQ1 | -40 | 85 | °C |
| T _J | Junction temperature, TL331QDBVRQ1 | -40 | 125 | °C |

6.5 Recommended Operating Conditions, TL331B-Q1 and TL391B-Q1

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-----------------|----------------------|-----|-----|------|
| V _{CC} | Supply voltage | 2 | 36 | V |
| T _J | Junction temperature | -40 | 125 | °C |

6.6 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TL331-Q1 | TL331B-Q1, TL391B-Q1 | UNIT |
|-------------------------------|--|--------------|-------------------------|------|
| | | DBV (SOT-23) | DBV (SOT-23) | |
| | | 5 PINS | 5 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 218.3 | 211.7 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 87.3 | 133.6 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 44.9 | 79.9 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 4.3 | 56.4 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 44.1 | 79.6 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.7 Electrical Characteristics, TL331B-Q1 and TL391B-Q1

$V_S = 5\text{ V}$, $V_{CM} = (V-)$; $T_A = 25^\circ\text{C}$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|---|---|------|------------|------------|---------------|
| V_{IO} | Input offset voltage | $V_S = 5\text{ to }36\text{V}$ | -2.5 | ± 0.37 | 2.5 | mV |
| | | $V_S = 5\text{ to }36\text{V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ | -4 | | 4 | |
| I_B | Input bias current | | | -3.5 | -25 | nA |
| | | $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ | | | -50 | nA |
| I_{OS} | Input offset current | | -10 | ± 0.5 | 10 | nA |
| | | $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ | -25 | | 25 | nA |
| V_{CM} | Common mode range | $V_S = 3\text{ to }36\text{V}$ | (V-) | | (V+) - 1.5 | V |
| | | $V_S = 3\text{ to }36\text{V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ | (V-) | | (V+) - 2.0 | V |
| A_{VD} | Large signal differential voltage amplification | $V_S = 15\text{V}$, $V_O = 1.4\text{V to }11.4\text{V}$; $R_L \geq 15\text{k to } (V+)$ | 50 | 200 | | V/mV |
| V_{OL} | Low level output Voltage {swing from (V-)} | $I_{SINK} \leq 4\text{mA}$, $V_{ID} = -1\text{V}$ | | 110 | 400 | mV |
| | | $I_{SINK} \leq 4\text{mA}$, $V_{ID} = -1\text{V}$ $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ | | | 550 | mV |
| I_{OH-LKG} | High-level output leakage current | (V+) = $V_O = 5\text{ V}$; $V_{ID} = 1\text{V}$ | | 0.1 | 20 | nA |
| I_{OH-LKG} | High-level output leakage current | (V+) = $V_O = 36\text{V}$; $V_{ID} = 1\text{V}$; $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ | | | 1000 | nA |
| I_{OL} | Low level output current | $V_{OL} = 1.5\text{V}$; $V_{ID} = -1\text{V}$; $V_S = 5\text{V}$ | 6 | 18 | | mA |
| I_Q | Quiescent current | $V_S = 5\text{ V}$, no load | | 210 | 330 | μA |
| | | $V_S = 36\text{ V}$, no load, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ | | 275 | 430 | μA |

6.8 Switching Characteristics, TL331B-Q1 and TL391B-Q1

$V_S = 5\text{V}$, $V_O\text{ PULLUP} = 5\text{V}$, $V_{CM} = V_S/2$, $C_L = 15\text{pF}$, $R_L = 5.1\text{k Ohm}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|---|-----|------|-----|------|
| t_{response} | Propagation delay time, high-to-low; Small scale input signal (1) | Input overdrive = 5mV, Input step = 100mV | | 1000 | | ns |
| t_{response} | Propagation delay time, high-to-low; TTL input signal (1) | TTL input with $V_{\text{ref}} = 1.4\text{V}$ | | 300 | | ns |

(1) High-to-low and low-to-high refers to the transition at the input.

6.9 Electrical Characteristics, TL331-Q1

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | T_A | MIN | TYP | MAX | UNIT |
|-----------|---|--|----------------|-----|---------------------|------|------|
| V_{IO} | Input offset voltage | $V_{CC} = 5\text{ V to }30\text{ V}$, $V_O = 1.4\text{ V}$, $V_{IC} = V_{IC(min)}$ | 25°C | | 2 | 5 | mV |
| | | | -40°C to 125°C | | | 9 | |
| I_{IO} | Input offset current | $V_O = 1.4\text{ V}$ | 25°C | | 5 | 50 | nA |
| | | | -40°C to 125°C | | | 250 | |
| I_{IB} | Input bias current | $V_O = 1.4\text{ V}$ | 25°C | | -25 | -250 | nA |
| | | | -40°C to 125°C | | | -400 | |
| V_{ICR} | Common-mode input voltage range ⁽²⁾ | | 25°C | | 0 to $V_{CC} - 1.5$ | | V |
| | | | -40°C to 125°C | | 0 to $V_{CC} - 2$ | | |
| A_{VD} | Large-signal differential-voltage amplification | $V_{CC} = 15\text{ V}$, $V_O = 1.4\text{ V to }11.4\text{ V}$, $R_L \geq 15\text{ k}\Omega$ to V_{CC} | 25°C | | 50 | 200 | V/mV |
| I_{OH} | High-level output current | $V_{OH} = 5\text{ V}$, $V_{ID} = 1\text{ V}$ $V_{OH} = 30\text{ V}$, $V_{ID} = 1\text{ V}$ | 25°C | | 0.1 | 50 | nA |
| | | | -40°C to 125°C | | | | 1 |
| V_{OL} | Low-level output voltage | $I_{OL} = 4\text{ mA}$, $V_{ID} = -1\text{ V}$ | 25°C | | 150 | 400 | mV |
| | | | -40°C to 125°C | | | | |
| I_{OL} | Low-level output current | $V_{OL} = 1.5\text{ V}$, $V_{ID} = -1\text{ V}$ | 25°C | | 6 | | mA |
| I_{CC} | Supply current | $R_L = \infty$, $V_{CC} = 5\text{ V}$ | 25°C | | 0.4 | 0.7 | mA |

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

(2) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$ at 25°C, but either or both inputs can go to 30 V without damage.

6.10 Switching Characteristics, TL331-Q1

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

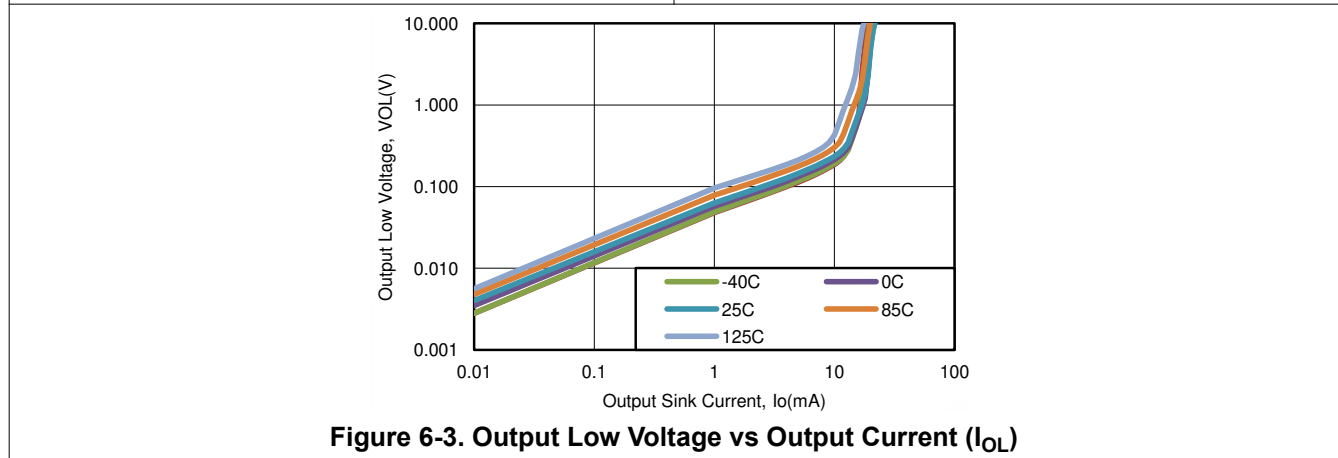
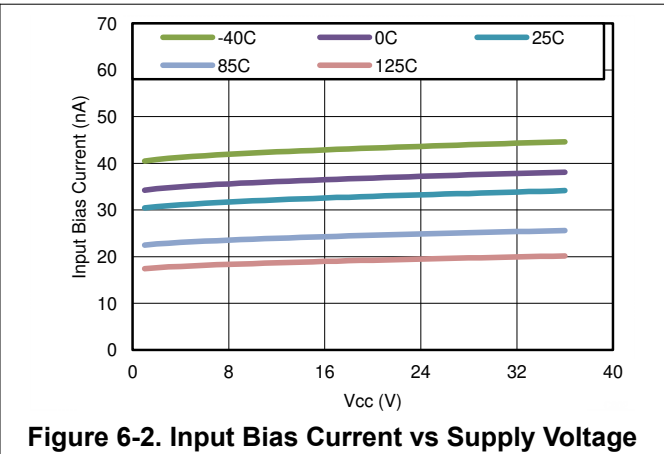
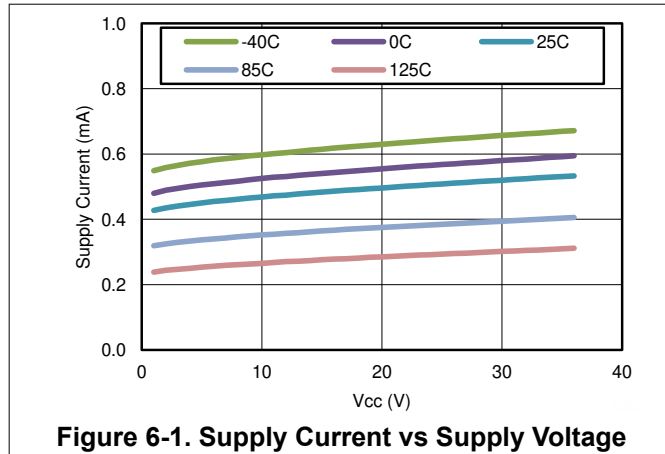
| PARAMETER | TEST CONDITIONS | TYP | UNIT | |
|---------------|---|---------------------------------------|------|---------------|
| Response time | R_L connected to 5 V through 5.1 k Ω , $C_L = 15\text{ pF}$ ^{(1) (2)} | 100-mV input step with 5-mV overdrive | 1.3 | μs |
| | | TTL-level input step | 0.3 | |

(1) C_L includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

6.11 Typical Characteristics, TL331-Q1

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $R_{\text{PULLUP}} = 5.1\text{k}$, $C_L = 15\text{pF}$, $V_{\text{CM}} = 0\text{V}$ unless otherwise noted.



6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{k}$, $C_L = 15\text{ pF}$, $V_{\text{CM}} = 0\text{ V}$, $V_{\text{UNDERDRIVE}} = 100\text{ mV}$, $V_{\text{OVERDRIVE}} = 100\text{ mV}$ unless otherwise noted.

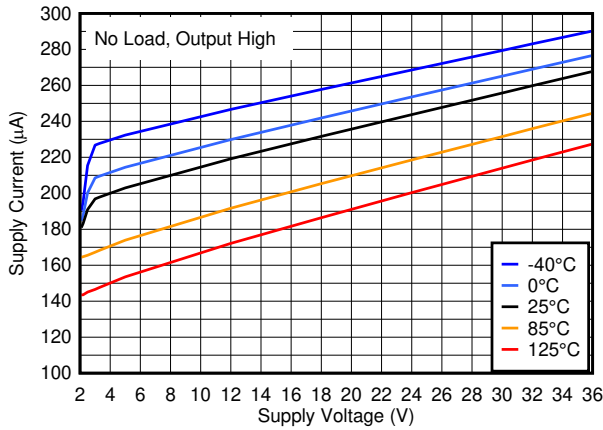


Figure 6-4. Supply Current vs. Supply Voltage

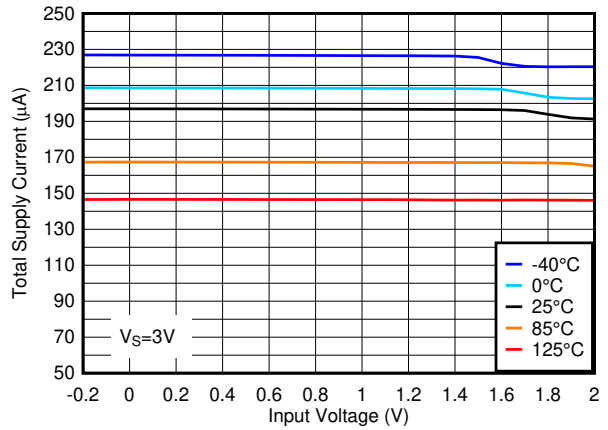


Figure 6-5. Total Supply Current vs. Input Voltage at 3V

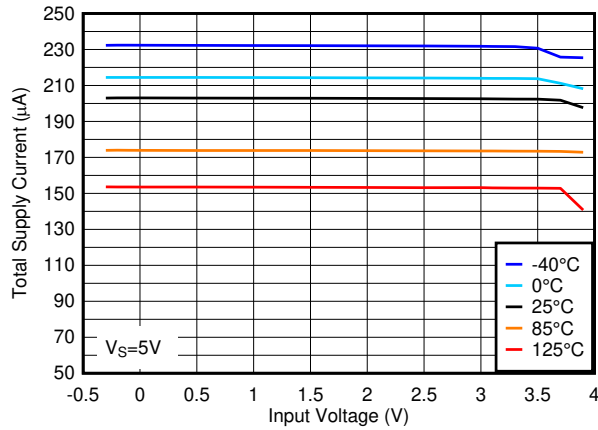


Figure 6-6. Total Supply Current vs. Input Voltage at 3.3V

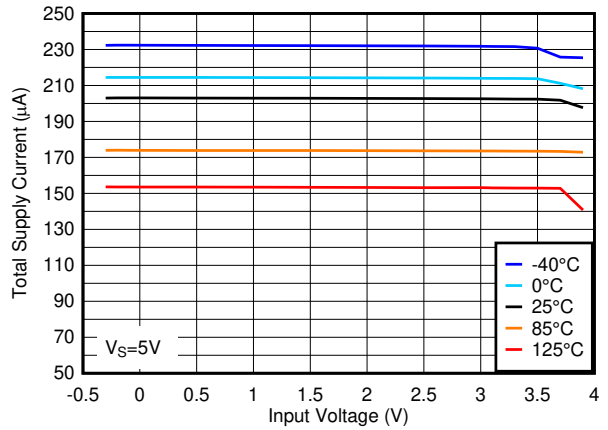


Figure 6-7. Total Supply Current vs. Input Voltage at 5V

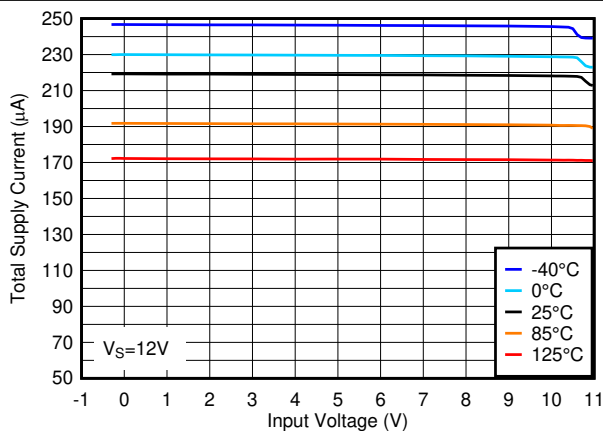


Figure 6-8. Total Supply Current vs. Input Voltage at 12V

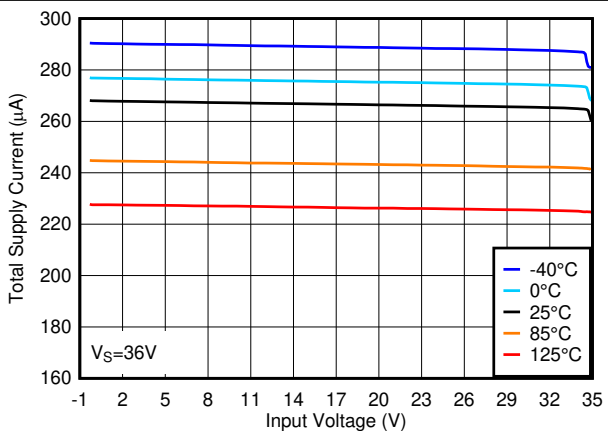


Figure 6-9. Total Supply Current vs. Input Voltage at 36V

6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}$, $C_L = 15\text{ pF}$, $V_{\text{CM}} = 0\text{ V}$, $V_{\text{UNDERDRIVE}} = 100\text{ mV}$, $V_{\text{OVERDRIVE}} = 100\text{ mV}$ unless otherwise noted.

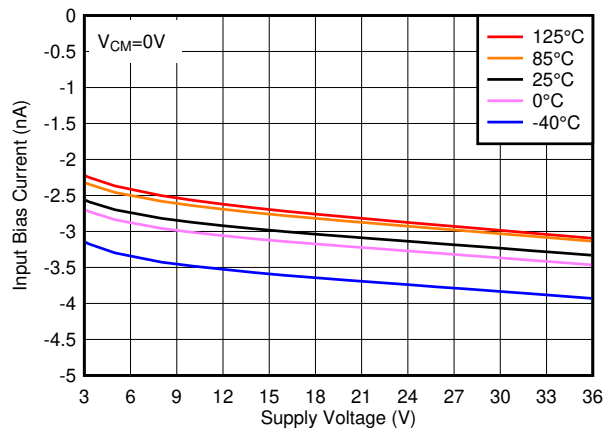


Figure 6-10. Input Bias Current vs. Supply Voltage

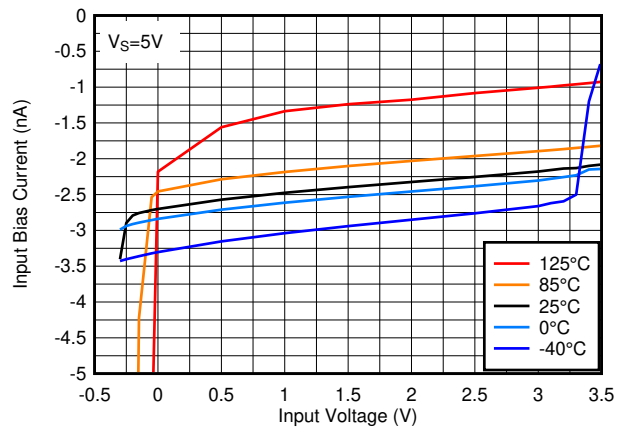


Figure 6-11. Input Bias Current vs. Input Voltage at 5V

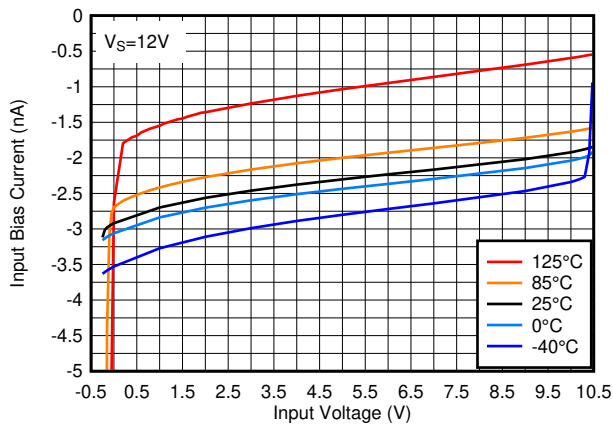


Figure 6-12. Input Bias Current vs. Input Voltage at 12V

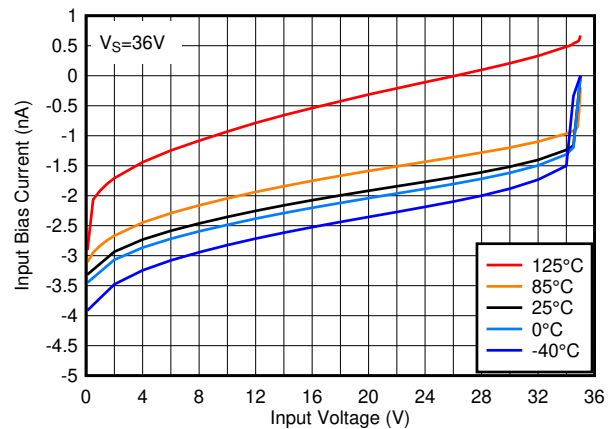


Figure 6-13. Input Bias Current vs. Input Voltage at 36V

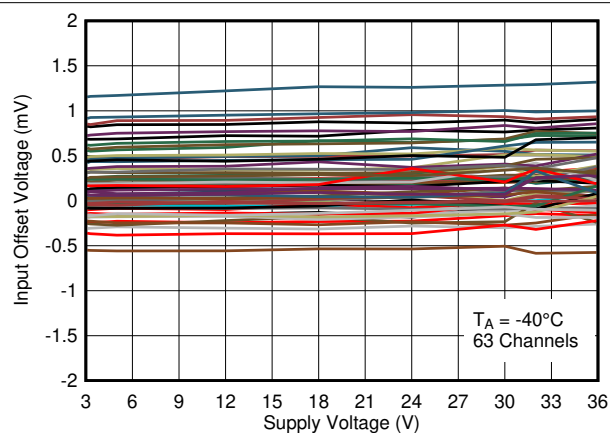


Figure 6-14. Input Offset Voltage vs. Supply Voltage at -40°C

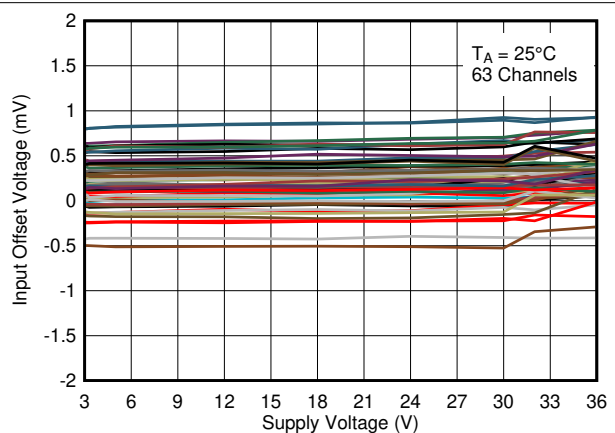


Figure 6-15. Input Offset Voltage vs. Supply Voltage at 25°C

6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}$, $C_L = 15\text{ pF}$, $V_{\text{CM}} = 0\text{ V}$, $V_{\text{UNDERDRIVE}} = 100\text{ mV}$, $V_{\text{OVERDRIVE}} = 100\text{ mV}$ unless otherwise noted.

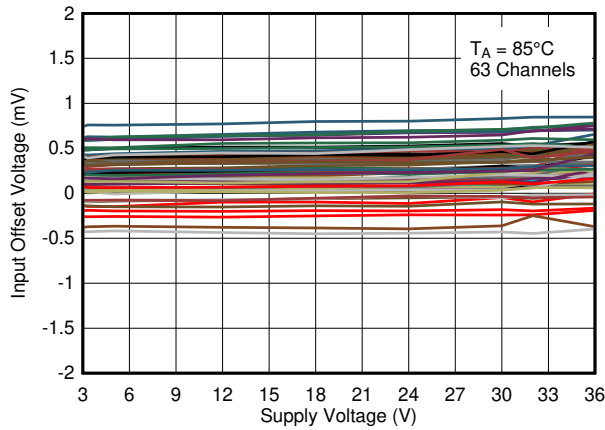


Figure 6-16. Input Offset Voltage vs. Supply Voltage at 85°C

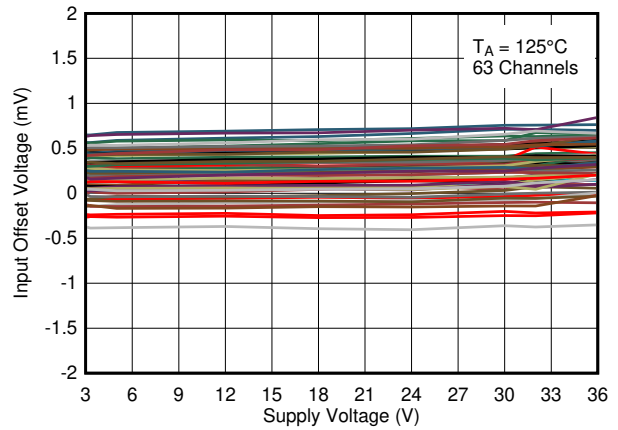


Figure 6-17. Input Offset Voltage vs. Supply Voltage at 125°C

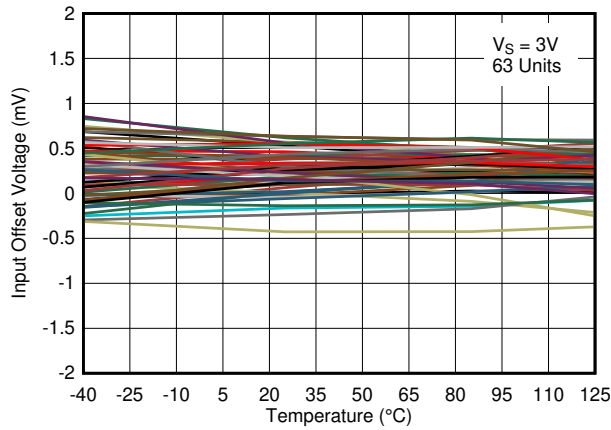


Figure 6-18. Input Offset Voltage vs. Temperature at 3V

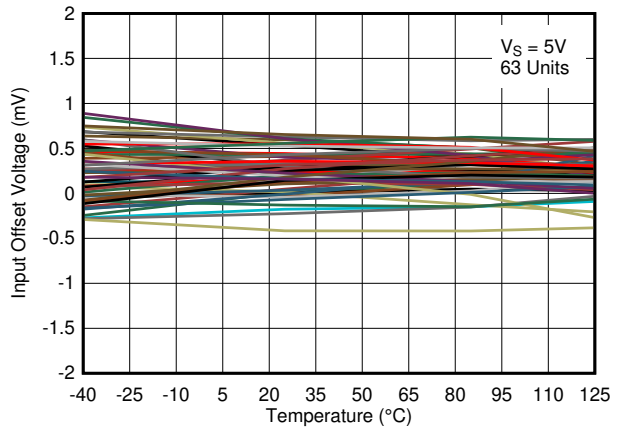


Figure 6-19. Input Offset Voltage vs. Temperature at 5V

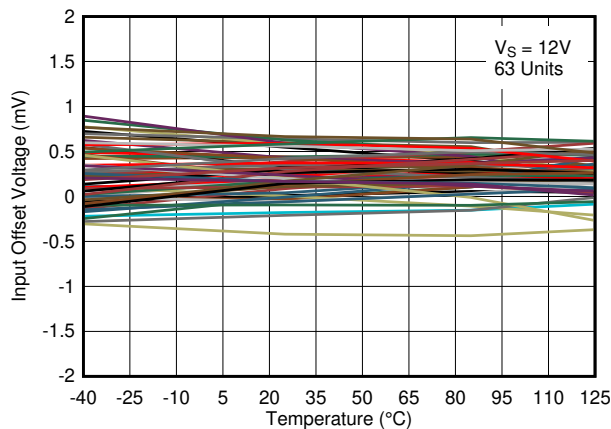


Figure 6-20. Input Offset Voltage vs. Temperature at 12V

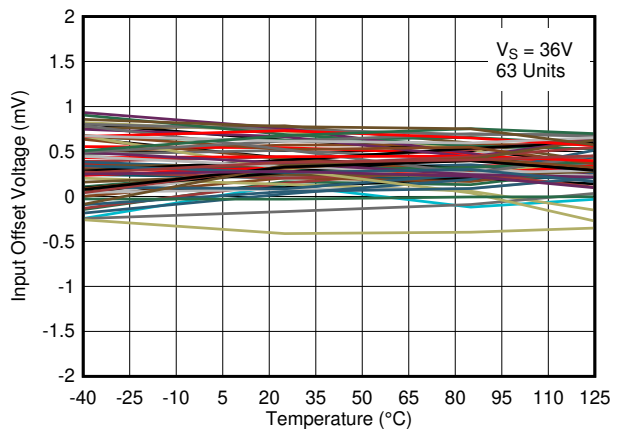


Figure 6-21. Input Offset Voltage vs. Temperature at 36V

6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}$, $C_L = 15\text{ pF}$, $V_{\text{CM}} = 0\text{ V}$, $V_{\text{UNDERDRIVE}} = 100\text{ mV}$, $V_{\text{OVERDRIVE}} = 100\text{ mV}$ unless otherwise noted.

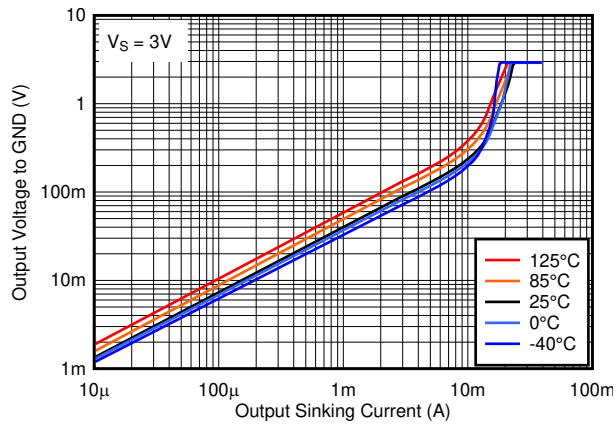


Figure 6-22. Output Low Voltage vs. Output Sinking Current at 3V

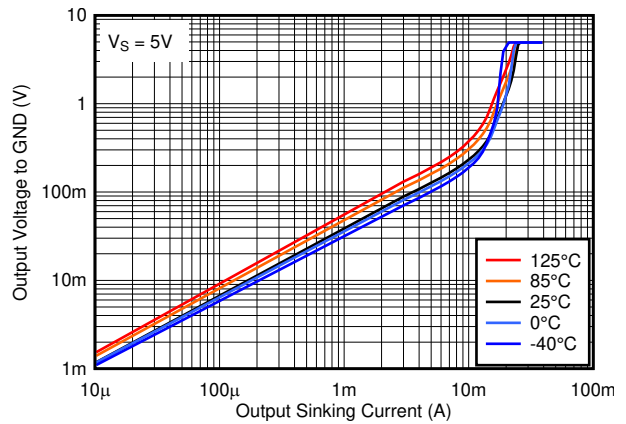


Figure 6-23. Output Low Voltage vs. Output Sinking Current at 5V

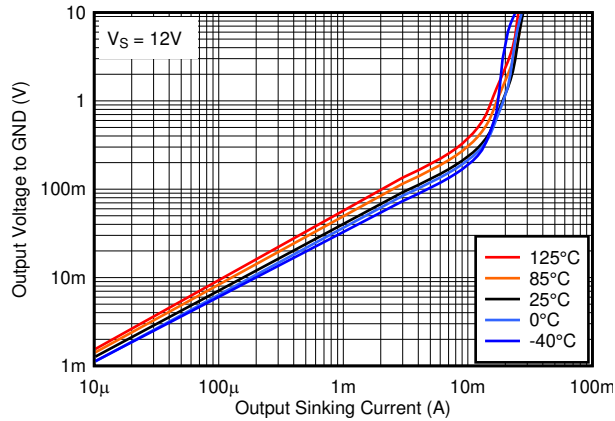


Figure 6-24. Output Low Voltage vs. Output Sinking Current at 12V

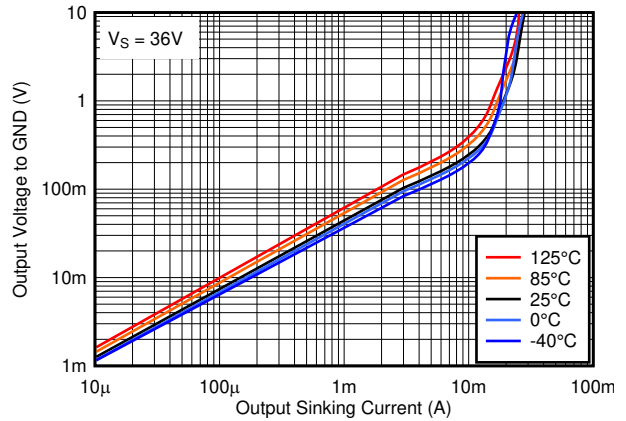


Figure 6-25. Output Low Voltage vs. Output Sinking Current at 36V

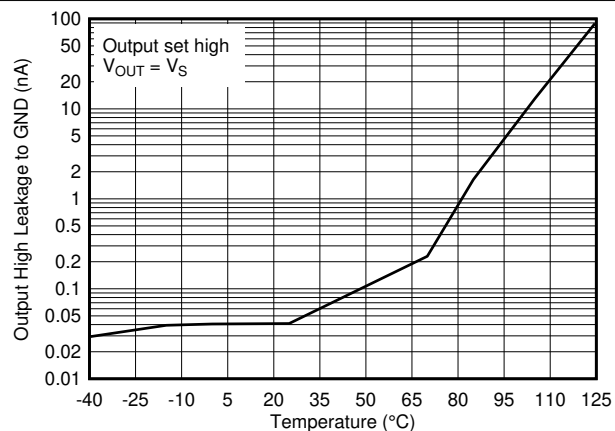


Figure 6-26. Output High Leakage Current vs. Temperature at 5V

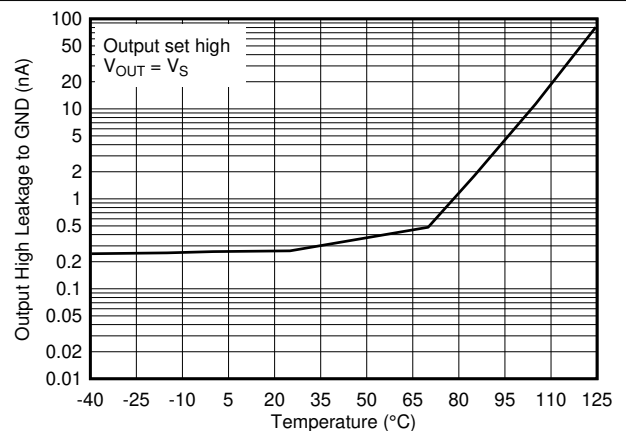


Figure 6-27. Output High Leakage Current vs. Temperature at 36V

6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}$, $C_L = 15\text{ pF}$, $V_{\text{CM}} = 0\text{ V}$, $V_{\text{UNDERDRIVE}} = 100\text{ mV}$, $V_{\text{OVERDRIVE}} = 100\text{ mV}$ unless otherwise noted.

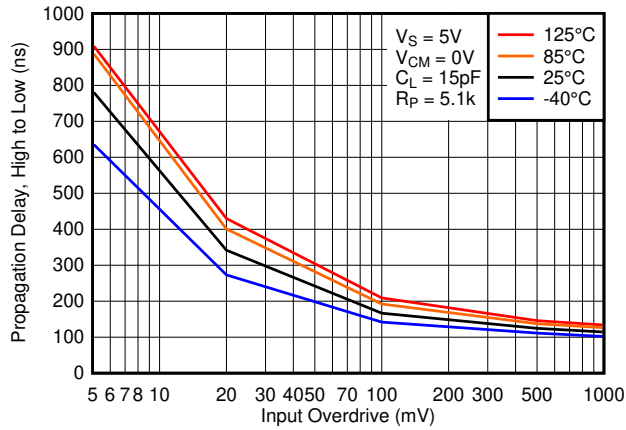


Figure 6-28. High to Low Propagation Delay vs. Input Overdrive Voltage, 5V

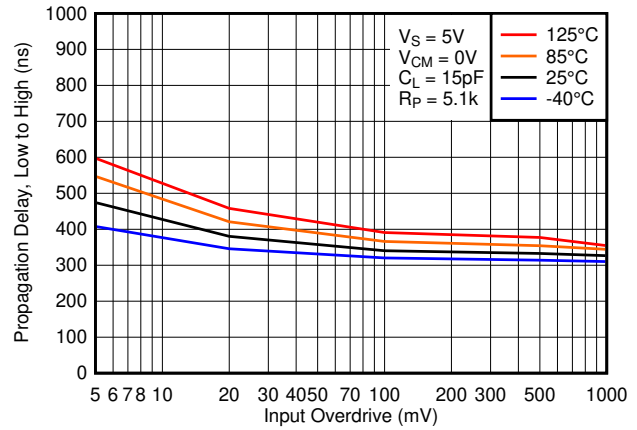


Figure 6-29. Low to High Propagation Delay vs. Input Overdrive Voltage, 5V

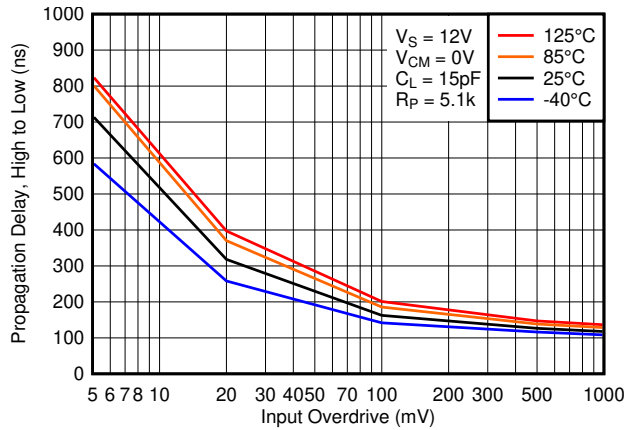


Figure 6-30. High to Low Propagation Delay vs. Input Overdrive Voltage, 12V

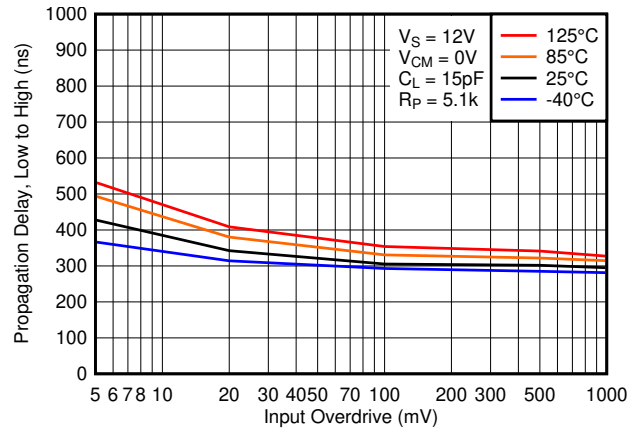


Figure 6-31. Low to High Propagation Delay vs. Input Overdrive Voltage, 12V

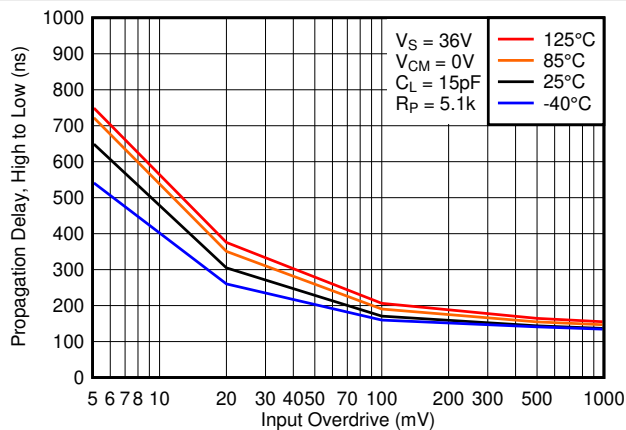


Figure 6-32. High to Low Propagation Delay vs. Input Overdrive Voltage, 36V

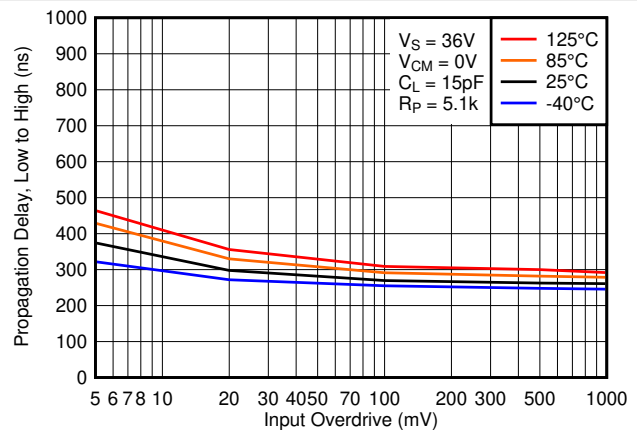


Figure 6-33. Low to High Propagation Delay vs. Input Overdrive Voltage, 36V

6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{k}$, $C_L = 15\text{ pF}$, $V_{\text{CM}} = 0\text{ V}$, $V_{\text{UNDERDRIVE}} = 100\text{ mV}$, $V_{\text{OVERDRIVE}} = 100\text{ mV}$ unless otherwise noted.

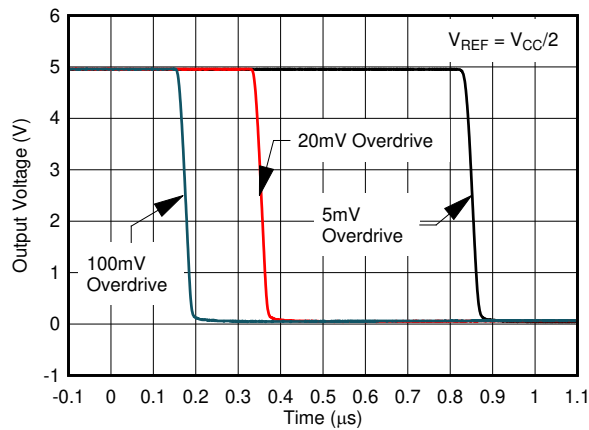


Figure 6-34. Response Time for Various Overdrives, High-to-Low Transition

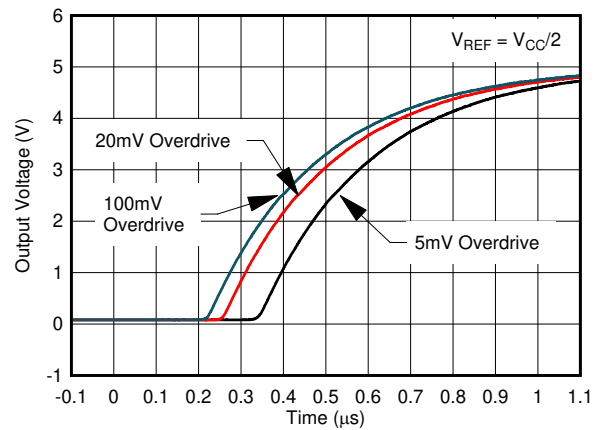


Figure 6-35. Response Time for Various Overdrives, Low-to-High Transition

7 Detailed Description

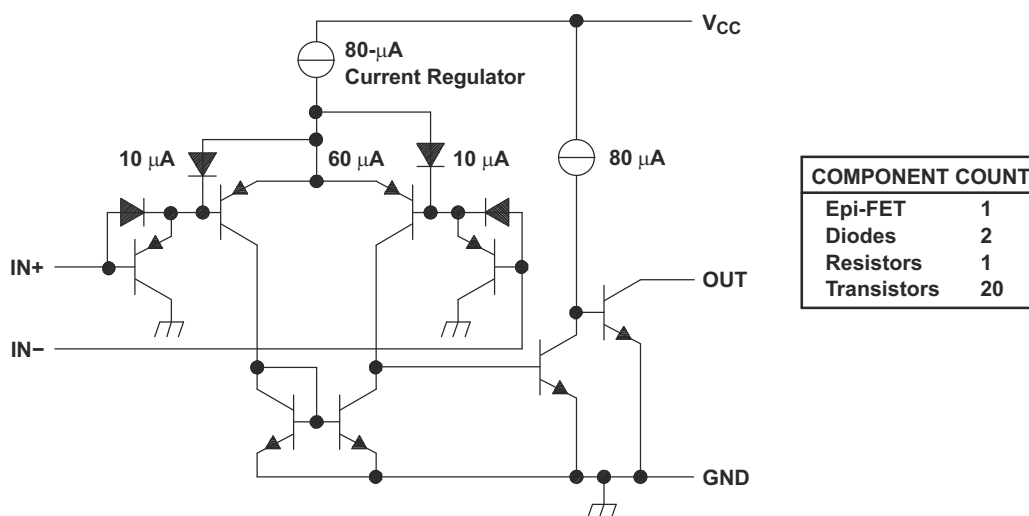
7.1 Overview

The TL331-Q1 is a single comparator with the ability to operate up to 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its very wide supply voltages range (2 V to 36 V), low I_q, and fast response.

The open-collector output allows the user to configure the output's logic low voltage (V_{OL}) and can be utilized to enable the comparator to be used in AND functionality.

The TL331B-Q1 and TL391B-Q1 are performance upgrades to industry standard TL331-Q1 using the latest semiconductor process technologies that allows for lower offset voltages, lower input bias and supply currents and faster response times. The TL331B can drop-in replace the "I" or "Q" versions of TL331-Q1. The TL391B-Q1 is an alternate pinout of the TL331B-Q1 for replacing competitive devices.

7.2 Functional Block Diagram



Current values shown are nominal.

7.3 Feature Description

The TL331-Q1 consists of a PNP Darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing TL331-Q1 to accurately function from ground to V_{CC} – 1.5 V differential input.

The output consists of an open collector NPN (pull-down or low side) transistor. The output NPN will sink current when the negative input voltage is higher than the positive input voltage and the offset voltage. The V_{OL} is resistive and will scale with the output current. Please see [Figure 6-3](#) for V_{OL} values with respect to the output current.

7.4 Device Functional Modes

7.4.1 Voltage Comparison

The TL331-Q1 operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pull-up) based on the input differential polarity.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

TL331-Q1 will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes TL331-Q1 optimal for level shifting to a higher or lower voltage.

8.2 Typical Application

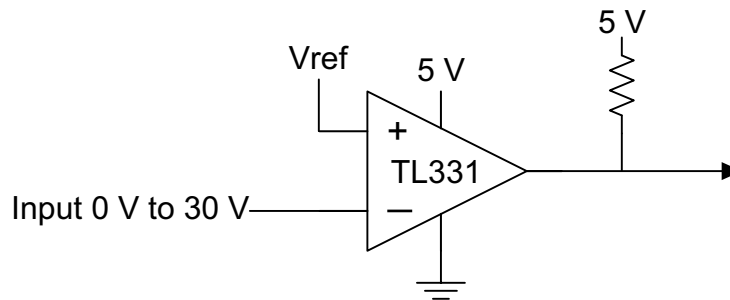


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 8-1](#) as the input parameters.

Table 8-1. Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE |
|--|-------------------------|
| Input Voltage Range | 0 V to $V_{CC} - 1.5$ V |
| Supply Voltage | 2 V to 36 V |
| Logic Supply Voltage (R_{PULLUP} Voltage) | 2 V to 36 V |
| Output Current (V_{LOGIC}/R_{PULLUP}) | 1 μ A to 4 mA |
| Input Overdrive Voltage | 100 mV |
| Reference Voltage | 2.5 V |
| Load Capacitance (C_L) | 15 pF |

8.2.2 Detailed Design Procedure

When using TL331-Q1 in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current
- Response time

8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is above or below 25°C the V_{ICR} can range from 0 V to $V_{CC} - 1.5$ V. This limits

the input voltage range to as high as $V_{CC} - 1.5\text{ V}$ and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

Below is a list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common mode range:
 - a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
 - b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common mode and IN- is within common mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common mode, the output is low and the output transistor is sinking current

8.2.2.2 TL331B-Q1 and TL391B-Q1 ESD Protection

The "B" versions add dedicated ESD protections on all the pins for improved ESD performance as well as improved negative input voltage handling. Please see Application Note [SNOAA35](#) for more information.

8.2.2.3 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). In order to make an accurate comparison the Overdrive Voltage (V_{OD}) should be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. [Figure 8-2](#) and [Figure 8-3](#) show positive and negative response times with respect to overdrive voltage.

8.2.2.4 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pull-up voltage. The output current will produce a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use [Figure 6-3](#) to determine V_{OL} based on the output current.

The output current can also effect the transient response. More is explained in the next section.

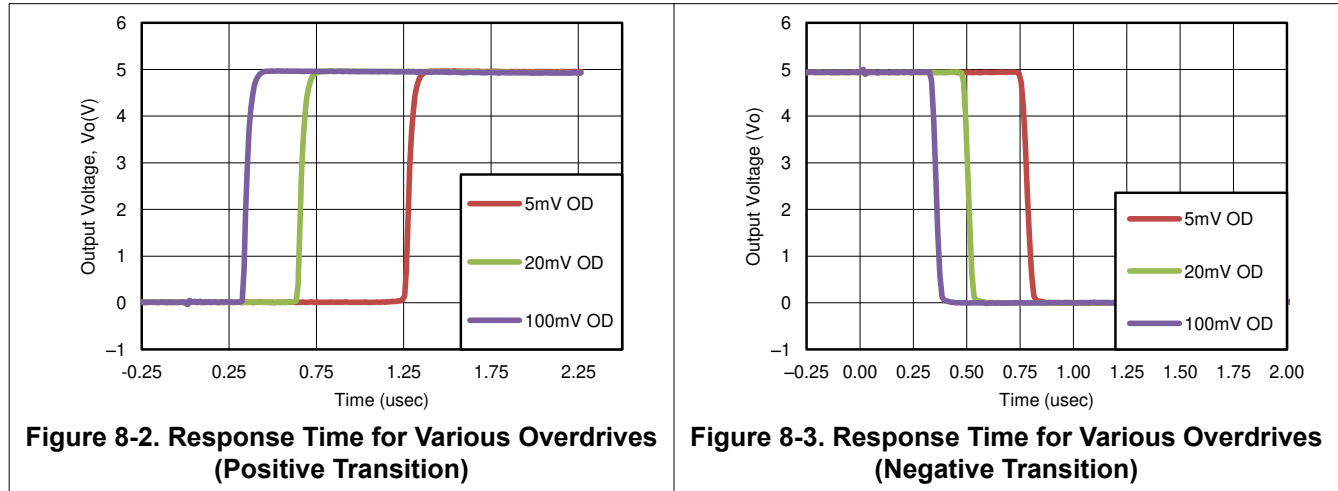
8.2.2.5 Response Time

Response time is a function of input over drive. See [Section 8.2.3](#) for typical response times. The rise and fall times can be determined by the load capacitance (C_L), load/pullup resistance (R_{PULLUP}), and equivalent collector-emitter resistance (R_{CE}).

- The rise time (T_R) is approximately $T_R \sim R_{PULLUP} \times C_L$
- The fall time (T_F) is approximately $T_F \sim R_{CE} \times C_L$
 - R_{CE} can be determined by taking the slope of [Figure 6-3](#) in its linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

8.2.3 Application Curves

The following curves were generated with 5 V on V_{CC} and V_{Logic} , $R_{PULLUP} = 5.1\text{ k}\Omega$, and 50 pF scope probe.



9 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, it is recommended to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can eat into the comparator's input common mode range and create an inaccurate comparison.

10 Layout

10.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches, which can affect the high level input common mode voltage range. In order to achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

10.2 Layout Example

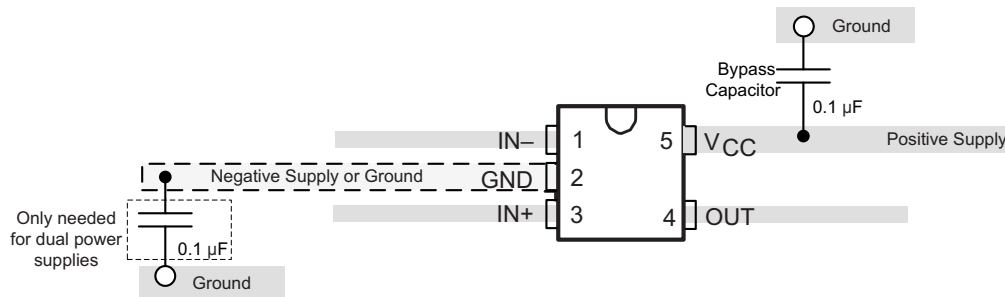


Figure 10-1. TL331-Q1 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

[Application Design Guidelines for LM339, LM393, TL331 Family Comparators](#) - SNOAA35

[Analog Engineers Circuit Cookbook: Amplifiers \(See Comparators section\)](#) - SLYY137

[Precision Design, Comparator with Hysteresis Reference Design](#)- TIDU020

[Window comparator circuit](#) - SBOA221

[Reference Design, Window Comparator Reference Design](#)- TIPD178

[Comparator with and without hysteresis circuit](#) - SBOA219

[Inverting comparator with hysteresis circuit](#) - SNOA997

[Non-Inverting Comparator With Hysteresis Circuit](#) - SBOA313

[Zero crossing detection using comparator circuit](#) - SNOA999

[A Quad of Independently Functioning Comparators](#) - SNOA654

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL331BQDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 31BQ | Samples |
| TL331IDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TQ1U | Samples |
| TL331QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T1RU | Samples |
| TL391BQDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 91BQ | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL331-Q1, TL331B-Q1, TL391B-Q1 :

- Catalog : [TL331](#), [TL331B](#), [TL391B](#)
- Enhanced Product : [TL331-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL331BQDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TL331IDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TL331QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TL391BQDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL331BQDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TL331IDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TL331QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TL391BQDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated