SupIRBuck™

HIGHLY EFFICIENT
INTEGRATED 8A SYNCHRONOUS BUCK REGULATOR

Features

- Greater than 96% Maximum Efficiency
- Wide Input Voltage Range 1.5V to 16V
- Wide Output Voltage Range 0.7V to 0.9*Vin
- Continuous 8A Load Capability
- Integrated Bootstrap-diode
- High Bandwidth E/A for excellent transient performance
- Programmable Switching Frequency up to 1.5MHz
- Programmable Over Current Protection (Hiccup)
- PGood output
- Precision Reference Voltage (0.7V, +/-1%)
- Programmable Soft-Start
- Enable Input with Voltage Monitoring Capability
- Enhanced Pre-Bias Start-up
- Seq input for Tracking applications
- -40ºC to 125ºC operating junction temperature
- Thermal Protection
- Pin compatible option for 4A and 12A devices
- 5mm x 6mm Power QFN Package, 0.9 mm height
- Lead-free, halogen-free and RoHS compliant

Description

The IR3841 ***SupIRBuck™*** is an easy-to-use, fully integrated and highly efficient DC/DC synchronous Buck regulator. The MOSFETs co-packaged with the on-chip PWM controller make IR3841 a space-efficient solution, providing accurate power delivery for low output voltage applications.

IR3841 is a versatile regulator which offers programmability of start up time, switching frequency and current limit while operating in wide input and output voltage range.

The switching frequency is programmable from 250kHz to 1.5MHz for an optimum solution.

It also features important protection functions, such as Pre-Bias startup, hiccup current limit and thermal shutdown to give required system level security in the event of fault conditions.

Applications

- Server Applications
- Storage Applications
- Embedded Telecom Systems
- Distributed Point of Load Power Architectures
- Netcom Applications
- Computing Peripheral Voltage Regulators
- General DC-DC Converters

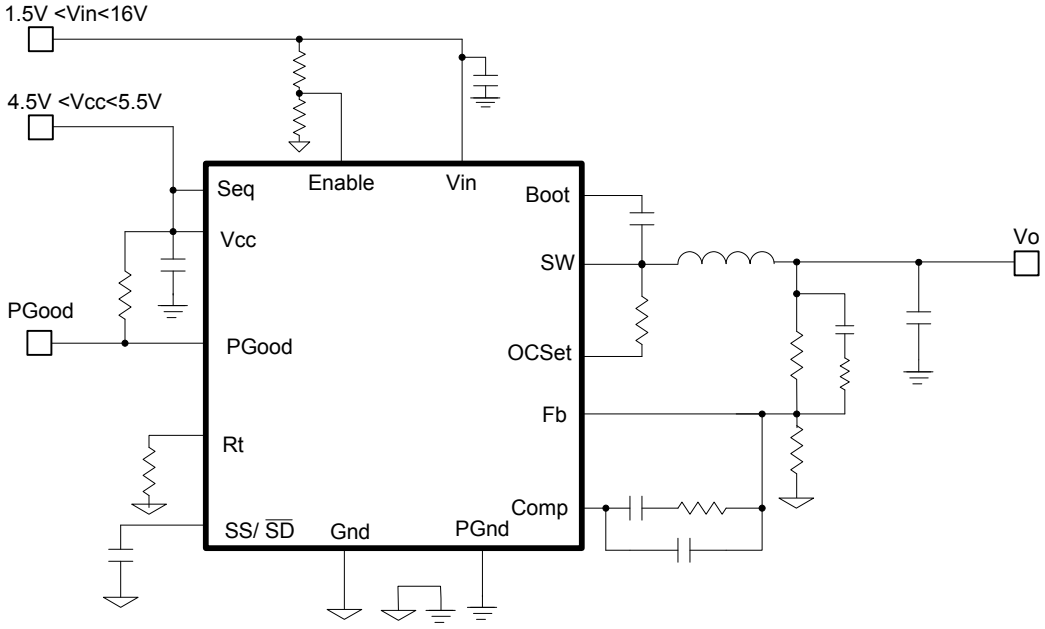


Fig. 1. Typical application diagram

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND unless otherwise specified)

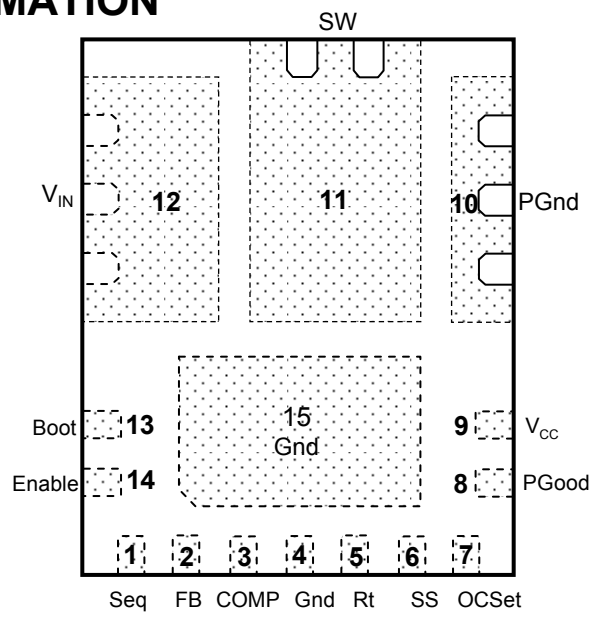
- Vin ..... -0.3V to 25V
- Vcc ..... -0.3V to 8V *(Note2)*
- Boot ..... -0.3V to 33V
- SW ..... -0.3V to 25V(DC), -4V to 25V(AC, 100ns)
- Boot to SW ..... -0.3V to Vcc+0.3V *(Note1)*
- OCSet ..... -0.3V to 30V, 30mA
- Input / output Pins ..... -0.3V to Vcc+0.3V *(Note1)*
- PGND to GND ..... -0.3V to +0.3V
- Storage Temperature Range ..... -55°C To 150°C
- Junction Temperature Range ..... -40°C To 150°C *(Note2)*
- ESD Classification ..... JEDEC Class 1C
- Moisture sensitivity level.....JEDEC Level 3@260 °C

Note1: *Must not exceed 8V*
Note2: *Vcc must not exceed 7.5V for Junction Temperature between -10°C and -40°C*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PACKAGE INFORMATION

5mm x 6mm POWER QFN



$\theta_{JA} = 35°C/W$

$\theta_{J\text{-}PCB} = 2°C/W$

ORDERING INFORMATION

PACKAGE DESIGNATOR	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER REEL
M	IR3841MTRPbF	15	4000
M	IR3841MTR1PbF	15	750

Block Diagram

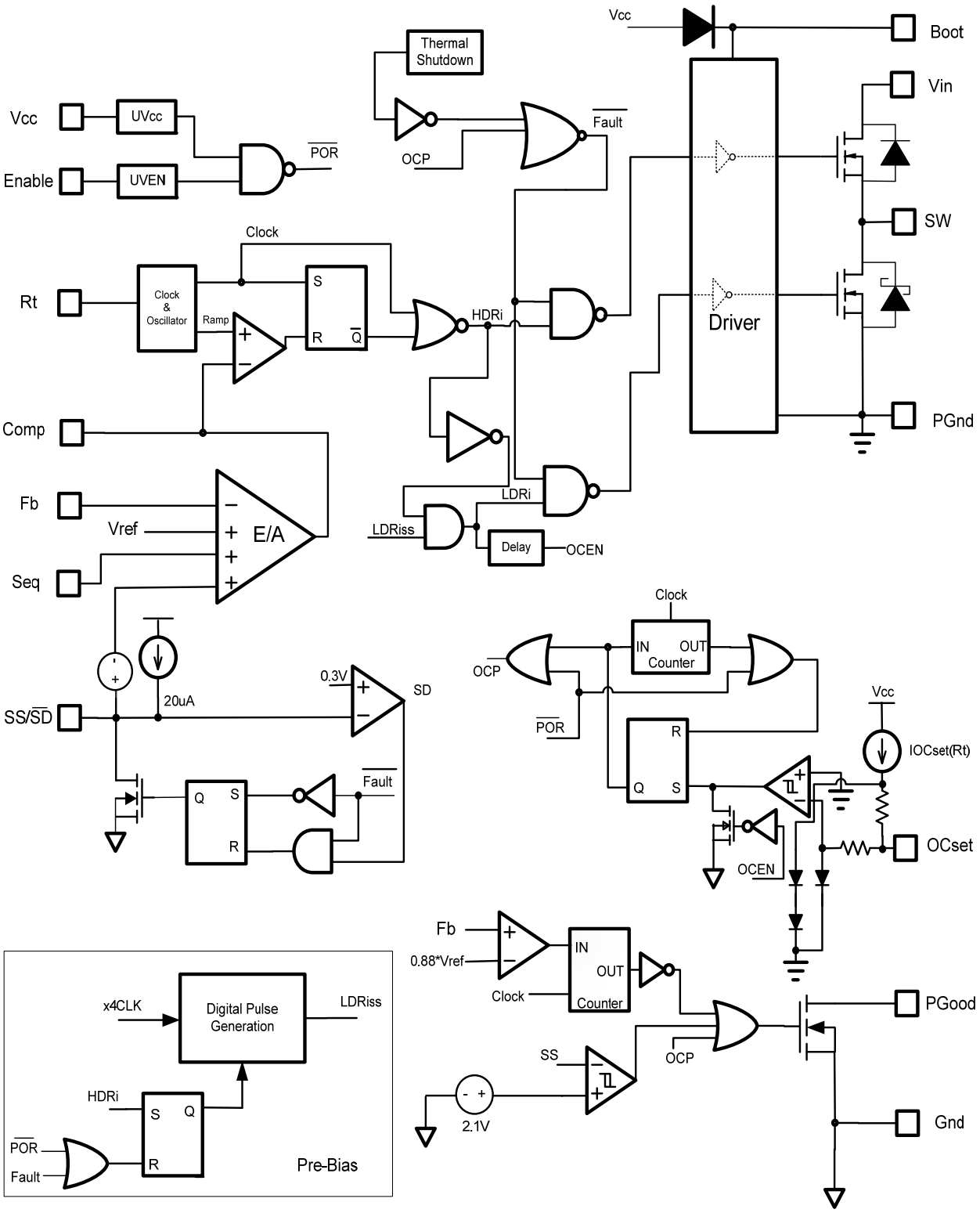


Fig. 2. Simplified block diagram of the IR3841

Pin Description

Pin	Name	Description
1	Seq	Sequence pin. Use two external resistors to set Simultaneous Power up sequencing. If this pin is not used connect to Vcc.
2	Fb	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator via resistor divider to set the output voltage and provide feedback to the error amplifier.
3	Comp	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to Fb pin to provide loop compensation.
4	Gnd	Signal ground for internal reference and control circuitry.
5	Rt	Set the switching frequency. Connect an external resistor from this pin to Gnd to set the switching frequency.
6	SS/$\overline{SD}$	Soft start / shutdown. This pin provides user programmable soft-start function. Connect an external capacitor from this pin to Gnd to set the start up time of the output voltage. The converter can be shutdown by pulling this pin below 0.3V.
7	OCSet	Current limit set point. A resistor from this pin to SW pin will set the current limit threshold.
8	PGood	Power Good status pin. Output is open drain. Connect a pull up resistor from this pin to Vcc. If unused, it can be left open.
9	V_{CC}	This pin powers the internal IC and the drivers. A minimum of 1uF high frequency capacitor must be connected from this pin to the power ground (PGnd).
10	PGnd	Power Ground. This pin serves as a separated ground for the MOSFET drivers and should be connected to the system's power ground plane.
11	SW	Switch node. This pin is connected to the output inductor.
12	V_{IN}	Input voltage connection pin.
13	Boot	Supply voltage for high side driver. A 0.1uF capacitor must be connected from this pin to SW.
14	Enable	Enable pin to turn on and off the device. Use two external resistors to set the turn on threshold (see Enable section). Connect this pin to Vcc if it is not used.
15	Gnd	Signal ground for internal reference and control circuitry.

Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
V_{in}	Input Voltage	1.5	16	V
V_{cc}	Supply Voltage	4.5	5.5	
Boot to SW	Supply Voltage	4.5	5.5	
V_o	Output Voltage	0.7	0.9*Vin	
I_o	Output Current	0	8	A
Fs	Switching Frequency	225	1650	kHz
T_j	Junction Temperature	-40	125	°C

Electrical Specifications

Unless otherwise specified, these specification apply over 4.5V< V_{cc}<5.5V, V_{in}=12V, 0°C<T_j< 125°C. Typical values are specified at T_a = 25°C.

Parameter	Symbol	Test Condition	Min	TYP	MAX	Units
Power Loss						
Power Loss	P_{loss}	Vcc=5V, V_{in}=12V, V_o=1.8V, I_o=8A, Fs=600kHz, L=1uH, *Note4*		1.6		W
MOSFET $R_{ds(on)}$						
Top Switch	$R_{ds(on)_Top}$	V_{Boot} -V_{sw} =5V, I_D=10A, Tj=25°C		16.7	23	mΩ
Bottom Switch	$R_{ds(on)_Bot}$	V_{cc}=5V, I_D=10A, Tj=25°C		8.7	12	
Reference Voltage						
Feedback Voltage	V_{FB}			0.7		V
Accuracy		0°C<Tj<125°C	-1.0		+1.0	%
		-40°C<Tj<125°C, *Note3*	-2.0		+2.0	
Supply Current						
V_{CC} Supply Current (Standby)	$I_{CC(Standby)}$	SS=0V, No Switching, Enable low			500	µA
V_{cc} Supply Current (Dyn)	$I_{CC(Dyn)}$	SS=3V, Vcc=5V, Fs=500kHz Enable high		12		mA
Under Voltage Lockout						
V_{CC}-Start-Threshold	V_{CC}_UVLO_Start	Vcc Rising Trip Level	4.06	4.26	4.46	V
V_{CC}-Stop-Threshold	V_{CC}_UVLO_Stop	Vcc Falling Trip Level	3.76	3.96	4.16	
V_{CC}-Hysteresis	Vcc-Hys	Supply ramping up and down	0.25	0.3	0.38	
Enable-Start-Threshold	Enable_UVLO_Start	Supply ramping up	1.14	1.2	1.36	
Enable-Stop-Threshold	Enable_UVLO_Stop	Supply ramping down	0.9	1.0	1.06	
Enable-Hysteresis	Enable_Hys	Supply ramping up and down	0.16	0.2	0.25	
Enable leakage current	Ien	Enable=3.3V			18	µA

Electrical Specifications (continued)

Unless otherwise specified, these specification apply over 4.5V< V_{cc}<5.5V, V_{in}=12V, 0°C<T_j< 125°C. Typical values are specified at T_a = 25°C.

Parameter	Symbol	Test Condition	Min	TYP	MAX	Units
Oscillator						
Rt Voltage			0.665	0.7	0.735	V
Frequency	F_S	Rt=59K	225	250	275	kHz
		Rt=28.7K	450	500	550	
		Rt=9.31K, *Note4*	1350	1500	1650	
Accuracy			-10		+10	%
Ramp Amplitude	Vramp	*Note4*		1.8		Vp-p
Ramp Offset	Ramp (os)	*Note4*		0.6		V
Min Pulse Width	Dmin(ctrl)	*Note4*		50		ns
Fixed Off Time		*Note4*		130	200	
Max Duty Cycle	Dmax	Fs=250kHz	92			%
Error Amplifier						
Input Offset Voltage	Vos	Vfb-Vseq, Vseq=0.8V	-10	0	+10	mV
Input Bias Current	IFb(E/A)		-1		+1	µA
Input Bias Current	IVp(E/A)		-1		+1	
Sink Current	Isink(E/A)		0.40	0.85	1.2	mA
Source Current	Isource(E/A)		8	10	13	
Slew Rate	SR	*Note4*	7	12	20	V/µs
Gain-Bandwidth Product	GBWP	*Note4*	20	30	40	MHz
DC Gain	Gain	*Note4*	100	110	120	dB
Maximum Voltage	Vmax(E/A)	*Vcc=4.5V*	3.4	3.5	3.7	V
Minimum Voltage	Vmin(E/A)			120	220	mV
Common Mode Voltage		*Note4*	0		1	V
Soft Start/SD						
Soft Start Current	ISS	Source	14	20	26	µA
Soft Start Clamp Voltage	Vss(clamp)		2.7	3.0	3.3	V
Shutdown Output Threshold	SD				0.3	
Over Current Protection						
OCSET Current	I_{OCSET}	Fs=250kHz	20.8	23.6	26.4	µA
		Fs=500kHz	43	48.8	54.6	
		Fs=1500kHz	136	154	172	
OC Comp Offset Voltage	V_{OFFSET}	*Note4*	-10	0	+10	mV
SS off time	SS_Hiccup			4096		Cycles
Bootstrap Diode						
Forward Voltage		I(Boot)=30mA	180	260	470	mV

Electrical Specifications (continued)

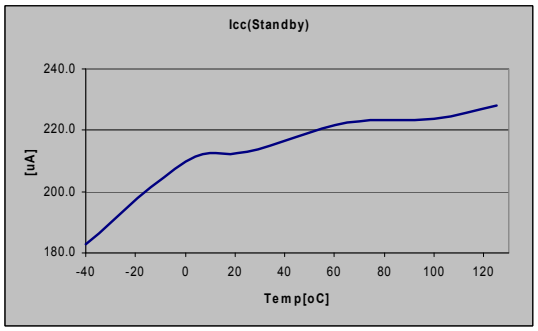
Unless otherwise specified, these specification apply over 4.5V< V_{cc}<5.5V, V_{in}=12V, 0°C<T_j< 125°C. Typical values are specified at T_a = 25°C.

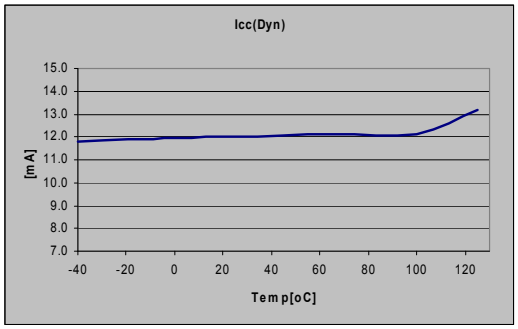
Parameter	SYM	Test Condition	Min	TYP	MAX	Units
Thermal Shutdown						
Thermal Shutdown		*Note4*		140		°C
Hysteresis		*Note4*		20		
Power Good						
Power Good upper Threshold	VPG+	Fb Rising	83	88	93	%Vref
Delay Comparator Threshold	PG(Delay)	Relative to charge voltage, SS rising	2	2.1	2.3	V
Delay Comparator Hysteresis	Delay(hys)	*Note4*	260	300	340	mV
PGood Voltage Low	PG(voltage)	I_{PGood}=-5mA			0.5	V
PGood Comparator Delay	PG(Delay)			256/Fs		s
Leakage Current	$I_{leakage}$			0	10	µA
Switch Node						
SW Bias Current	Isw	SW=0V, Enable=0V			3	µA
		SW=0V,Enable=high,SS=3V,Seq=0V, *Note4*			40	

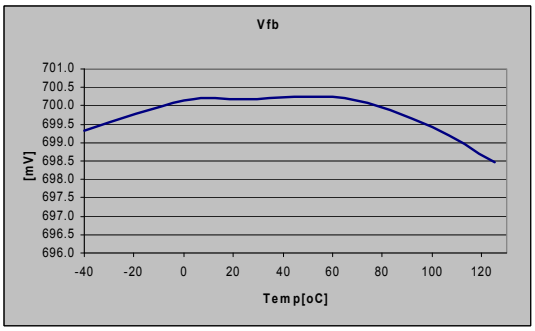
Note3: Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.

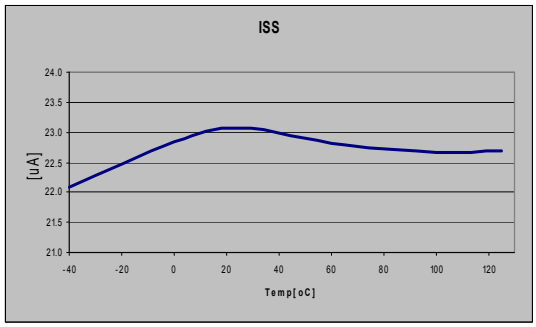
Note4: Guaranteed by Design but not tested in production.

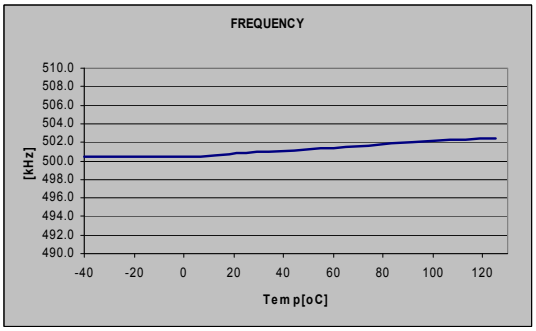
TYPICAL OPERATING CHARACTERISTICS (-40°C - 125°C)

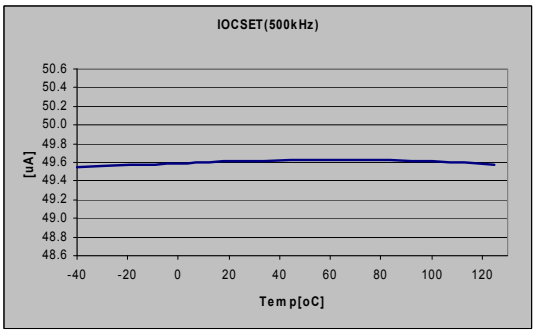


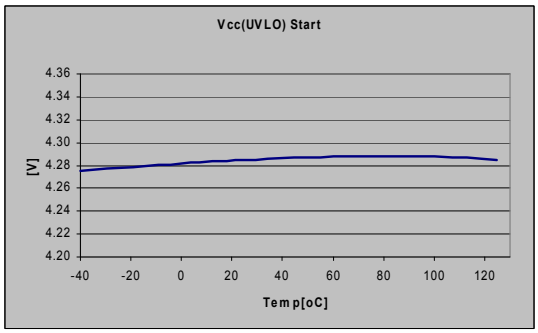


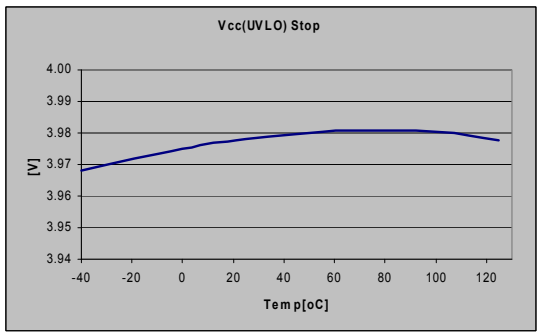


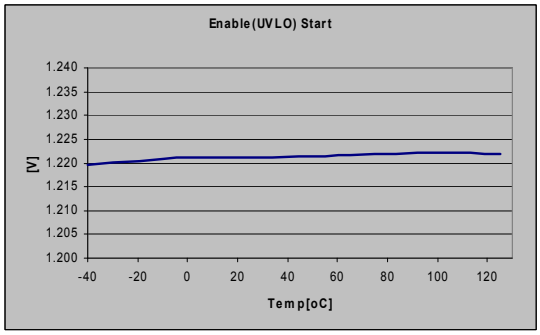


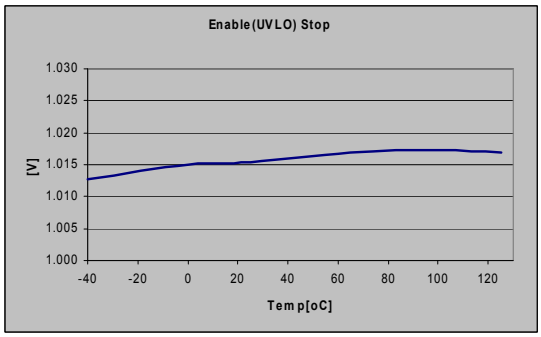








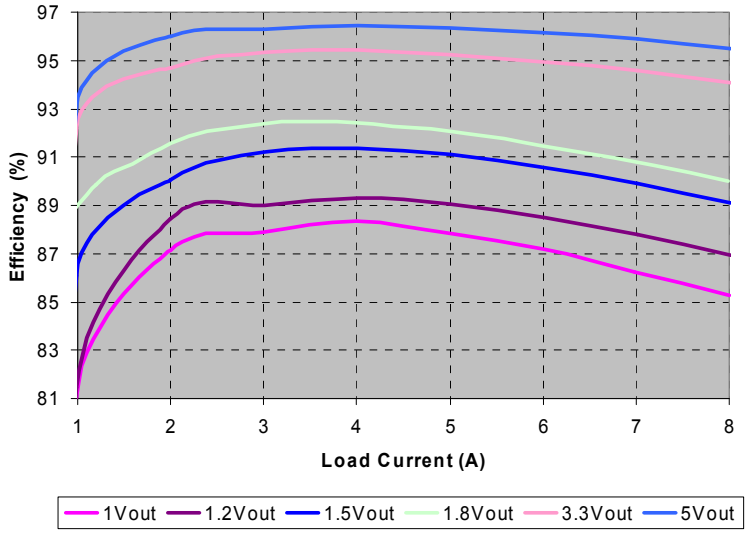


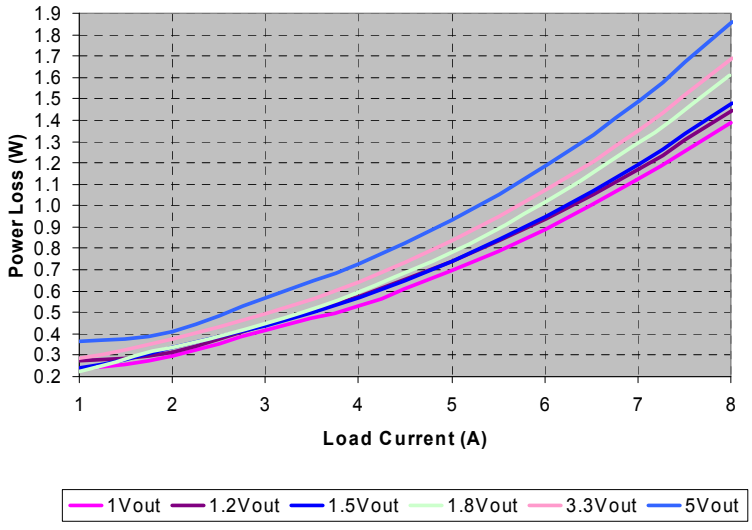


Typical Efficiency and Power Loss Curves
Vin=12V, Vcc=5V, Io=1A-8A, Room Temperature, No Air Flow

The table below shows the inductors used for each of the output voltages in the efficiency measurement.

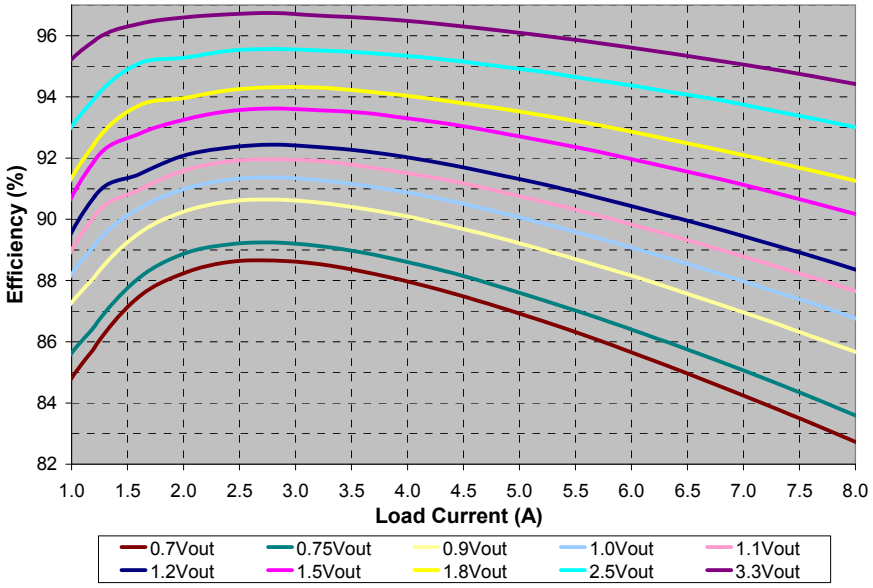
Vout (V)	L (uH)	P/N	DCR (mΩ)
1	0.36	ETQP4LR36WFC	1.1
1.2	0.36	ETQP4LR36WFC	1.1
1.5	0.36	ETQP4LR36WFC	1.1
1.8	1	MPL105-1R0	2.5
3.3	1	MPL105-1R0	2.5
5	1	MPL105-1R0	2.5

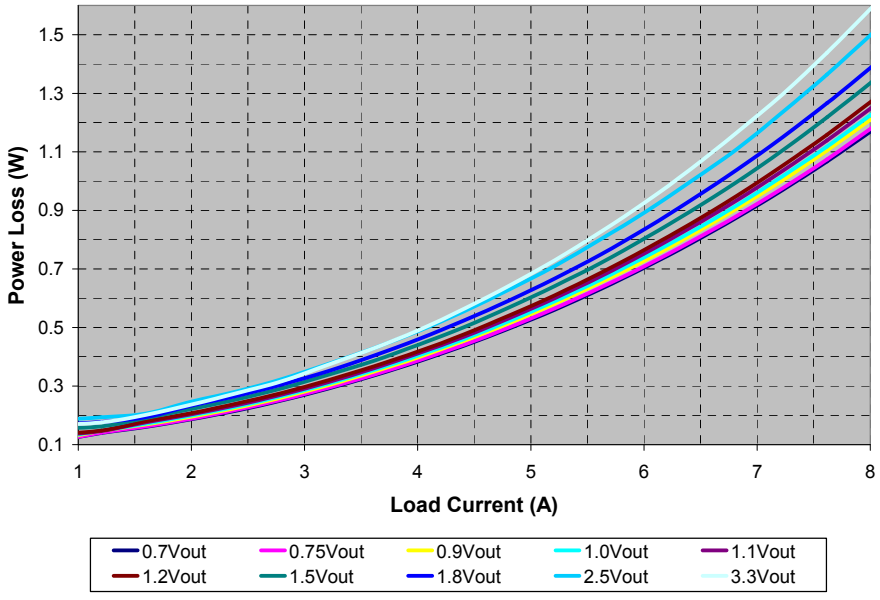




Typical Efficiency and Power Loss Curves
Vin=5V, Vcc=5V, Io=1A-8A, Fs=600kHz, Room Temperature, No Air Flow

For all the output voltages, L=0.51uH (DCR=0.29 mΩ, P/N: 59PR9876N)





Circuit Description

THEORY OF OPERATION

Introduction

The IR3841 uses a PWM voltage mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types.

The switching frequency is programmable from 250kHz to 1.5MHz and provides the capability of optimizing the design in terms of size and performance.

IR3841 provides precisely regulated output voltage programmed via two external resistors from 0.7V to 0.9*Vin.

The IR3841 operates with an external bias supply from 4.5V to 5.5V, allowing an extended operating input voltage range from 1.5V to 16V.

The device utilizes the on-resistance of the low side MOSFET as current sense element, this method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistor.

IR3841 includes two low $R_{ds(on)}$ MOSFETs using IR's HEXFET technology. These are specifically designed for high efficiency applications.

Under-Voltage Lockout and POR

The under-voltage lockout circuit monitors the input supply Vcc and the Enable input. It assures that the MOSFET driver outputs remain in the off state whenever either of these two signals drop below the set thresholds. Normal operation resumes once Vcc and Enable rise above their thresholds.

The POR (Power On Ready) signal is generated when all these signals reach the valid logic level (see system block diagram). When the POR is asserted the soft start sequence starts (see soft start section).

Enable

The Enable features another level of flexibility for start up. The Enable has precise threshold which is internally monitored by Under-Voltage Lockout (UVLO) circuit. Therefore, the IR3841 will turn on only when the voltage at the Enable pin exceeds this threshold, typically, 1.2V.

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the IR3841 does not turn on until the bus voltage reaches the desired level. Only after the bus voltage reaches or exceeds this level will the voltage at Enable pin exceed its threshold, thus enabling the IR3841. Therefore, in addition to being a logic input pin to enable the IR3841, the Enable feature, with its precise threshold, also allows the user to implement an Under-Voltage Lockout for the bus voltage V_{in}. This is desirable particularly for high output voltage applications, where we might want the IR3841 to be disabled at least until V_{in} exceeds the desired output voltage level.

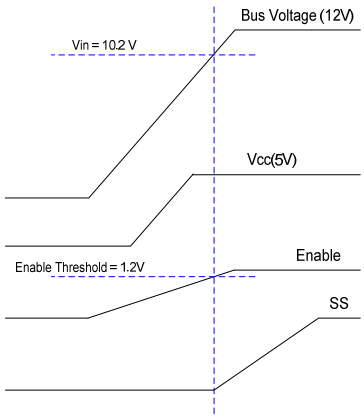


Fig. 3a. Normal Start up, Device turns on when the Bus voltage reaches 10.2V

Figure 3b. shows the recommended start-up sequence for the non-sequenced operation of IR3841, when Enable is used as a logic input.

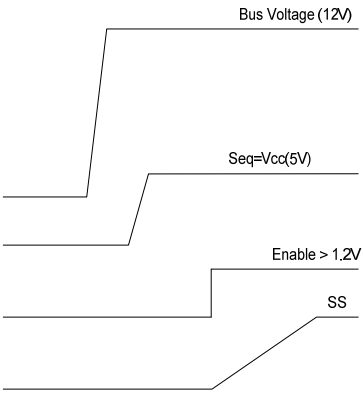


Fig. 3b. Recommended startup sequence, Non-Sequenced operation

Figure 3c. shows the recommended startup sequence for sequenced operation of IR3841 with Enable used as logic input.

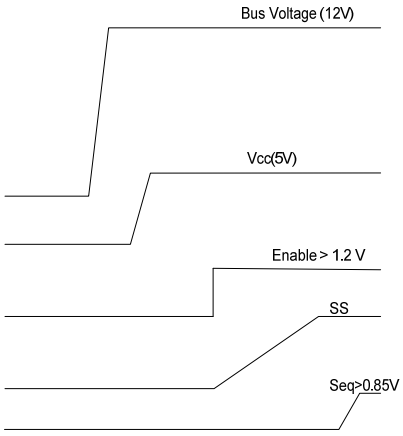


Fig. 3c. Recommended startup sequence, Sequenced operation

Pre-Bias Startup

IR3841 is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET off until the first gate signal for control MOSFET is generated. Figure 4 shows a typical Pre-Bias condition at start up.

The synchronous MOSFET always starts with a narrow pulse width and gradually increases its duty cycle with a step of 25%, 50%, 75% and 100% until it reaches the steady state value. The number of these startup pulses for the synchronous MOSFET is internally programmed. Figure 5 shows a series of 32, 16, 8 startup pulses.

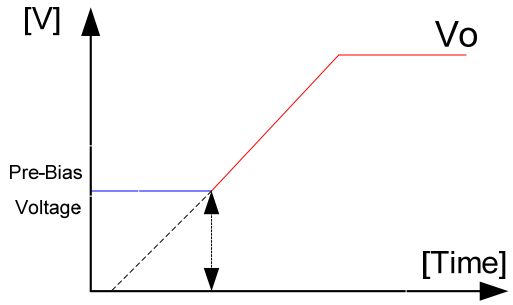


Fig. 4. Pre-Bias startup

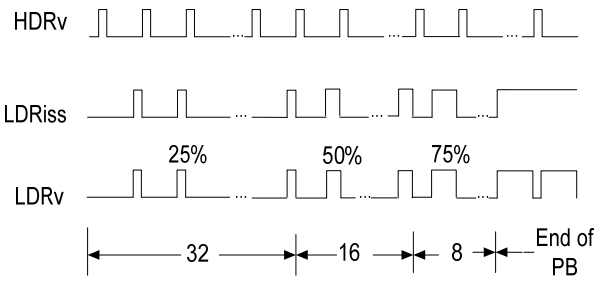


Fig. 5. Pre-Bias startup pulses

Soft-Start

The IR3841 has a programmable soft-start to control the output voltage rise and to limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Enable and Vcc rise above their UVLO thresholds and generate the Power On Ready (POR) signal. The internal current source (typically 20uA) charges the external capacitor C_{ss} linearly from 0V to 3V. Figure 6 shows the waveforms during the soft start.

The start up time can be estimated by:

$$T_{start} = \frac{(1.4 - 0.7) * C_{SS}}{20\mu A} \quad \text{----------(1)}$$

During the soft start the OCP is enabled to protect the device for any short circuit and over current condition.

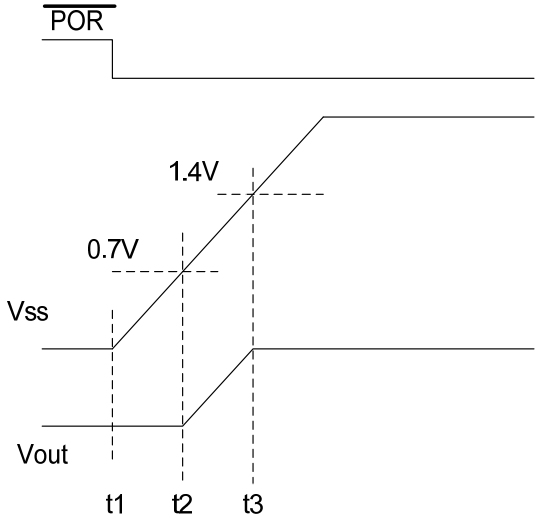


Fig. 6. Theoretical operation waveforms during soft-start

Operating Frequency

The switching frequency can be programmed between 250kHz – 1500kHz by connecting an external resistor from R_t pin to Gnd. Table 1 tabulates the oscillator frequency versus R_t.

Table 1. Switching Frequency and I_{OCSet} vs. External Resistor (R_t)

R_t (kΩ)	F_s (kHz)	I_{ocset} (µA)
47.5	300	29.4
35.7	400	39.2
28.7	500	48.7
23.7	600	59.07
20.5	700	68.2
17.8	800	78.6
15.8	900	88.6
14.3	1000	97.9
12.7	1100	110.2
11.5	1200	121.7
10.7	1300	130.8
9.76	1400	143.4
9.31	1500	150.3

Shutdown

The IR3841 can be shutdown by pulling the Enable pin below its 1 V threshold. This will tri-state both, the high side driver as well as the low side driver. Alternatively, the output can be shutdown by pulling the soft-start pin below 0.3V. In shutdown by this method, the high side driver is turned off, and the low side driver is turned on. Thus, in this method, the output voltage can be actively discharged through the synchronous FET. Normal operation is resumed by cycling the voltage at the Soft Start pin.

Over-Current Protection

The over current protection is performed by sensing current through the $R_{DS(on)}$ of low side MOSFET. This method enhances the converter's efficiency and reduces cost by eliminating a current sense resistor. As shown in figure 7, an external resistor (R_{OCSet}) is connected between OCSet pin and the switch node (SW) which sets the current limit set point.

An internal current source sources current (I_{OCSet}) out of the *OCSet* pin. This current is a function of the switching frequency and hence, of R_t.

$$I_{OCSet}(\mu A) = \frac{1400}{R_t(k\Omega)} \quad \text{.....(2)}$$

Table 1. shows I_{OCSet} at different switching frequencies. The internal current source develops a voltage across R_{OCSet}. When the low side MOSFET is turned on, the inductor current flows through the Q2 and results in a voltage at OCSet which is given by:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{DS(on)} * I_L) \quad \text{.....(3)}$$

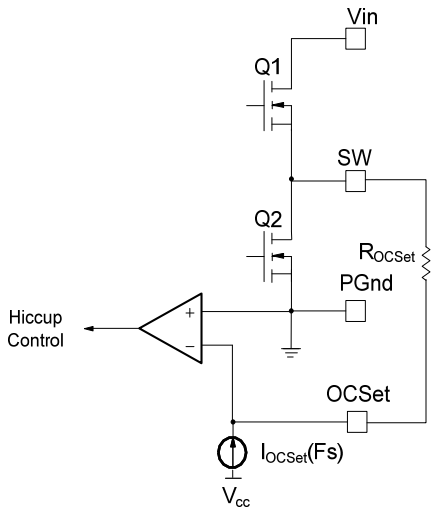


Fig. 7. Connection of over current sensing resistor

An over current is detected if the OCSet pin goes below ground. Hence, at the current limit threshold, V_{OCset}=0. Then, for a current limit setting I_{Limit}, R_{OCSet} is calculated as follows:

$$R_{OCSet} = \frac{R_{DS(on)} * I_{Limit}}{I_{OCSet}} \quad \text{.....(4)}$$

An overcurrent detection trips the OCP comparator, latches OCP signal and cycles the soft start function in hiccup mode.

The hiccup is performed by shorting the soft-start capacitor to ground and counting the number of switching cycles. The Soft Start pin is held low until 4096 cycles have been completed. The OCP signal resets and the converter recovers. After every soft start cycle, the converter stays in this mode until the overload or short circuit is removed.

The OCP circuit starts sampling current typically 160 ns after the low gate drive rises to about 3V. This delay functions to filter out switching noise.

Thermal Shutdown

Temperature sensing is provided inside IR3841. The trip threshold is typically set to 140ºC. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs and discharges the soft start capacitor.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20ºC hysteresis in the thermal shutdown threshold.

Output Voltage Sequencing

The IR3841 can accommodate user programmable sequencing options using Seq, Enable and Power Good pins.

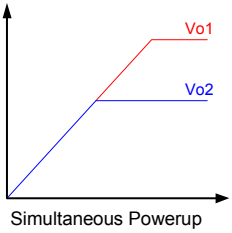


Fig. 8a. Simultaneous Power-up of the slave with respect to the master.

Through these pins, voltage sequencing such as simultaneous and sequential can be implemented. Figure 8. shows simultaneous sequencing configurations. In simultaneous power-up, the voltage at the Seq pin of the slave reaches 0.7V before the Fb pin of the master. For $R_E/R_F = R_C/R_D$, therefore, the output voltage of the slave follows that of the master until the voltage at the Seq pin of the slave reaches 0.7 V. After the voltage at the Seq pin of the slave exceeds 0.85V, the internal 0.7V reference of the slave dictates its output voltage.

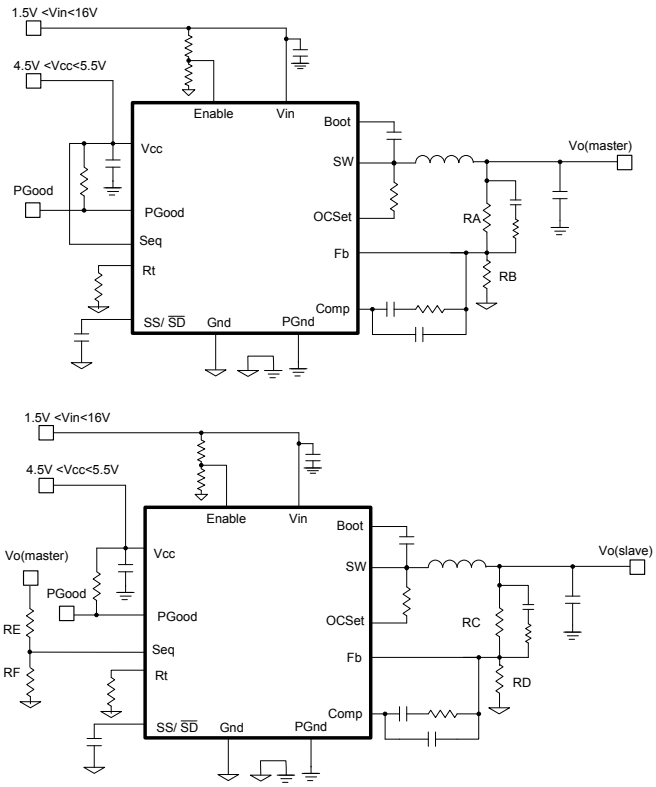


Fig. 8b. Application Circuit for Simultaneous Sequencing

Power Good Output

The IC continually monitors the output voltage via Feedback (Fb pin). The feedback voltage is compared to a fixed voltage. As soon as the Fb voltage reaches $0.88*V_{ref}$, the Power Good signal flags. This pin is open drain and it needs to be externally pulled high. High state indicates that output is in regulation. Fig 9. shows the timing diagram for the PGood function.

TIMING DIAGRAM OF PGOOD FUNCTION

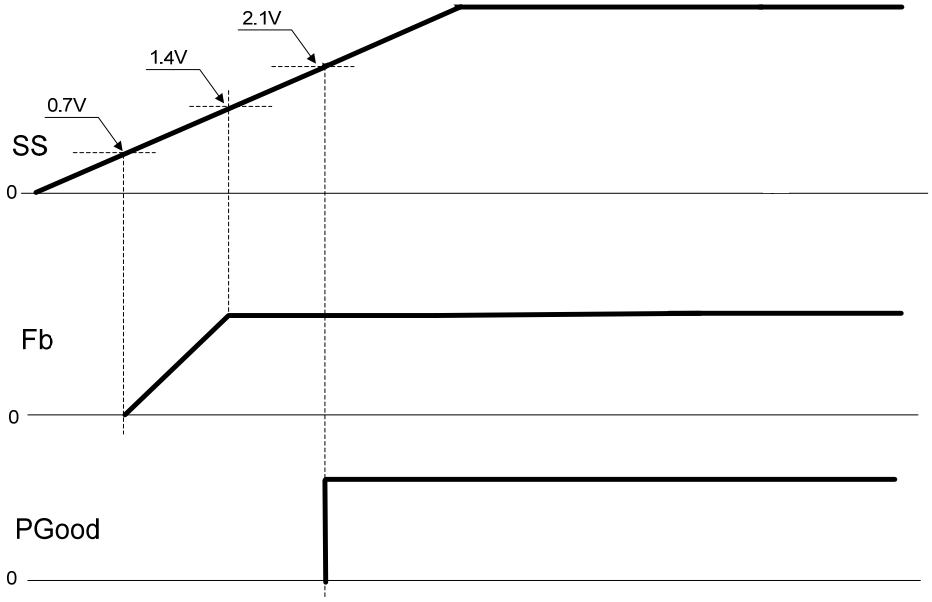


Fig.9a IR3841 Non-Sequenced Operation (Seq=Vcc)

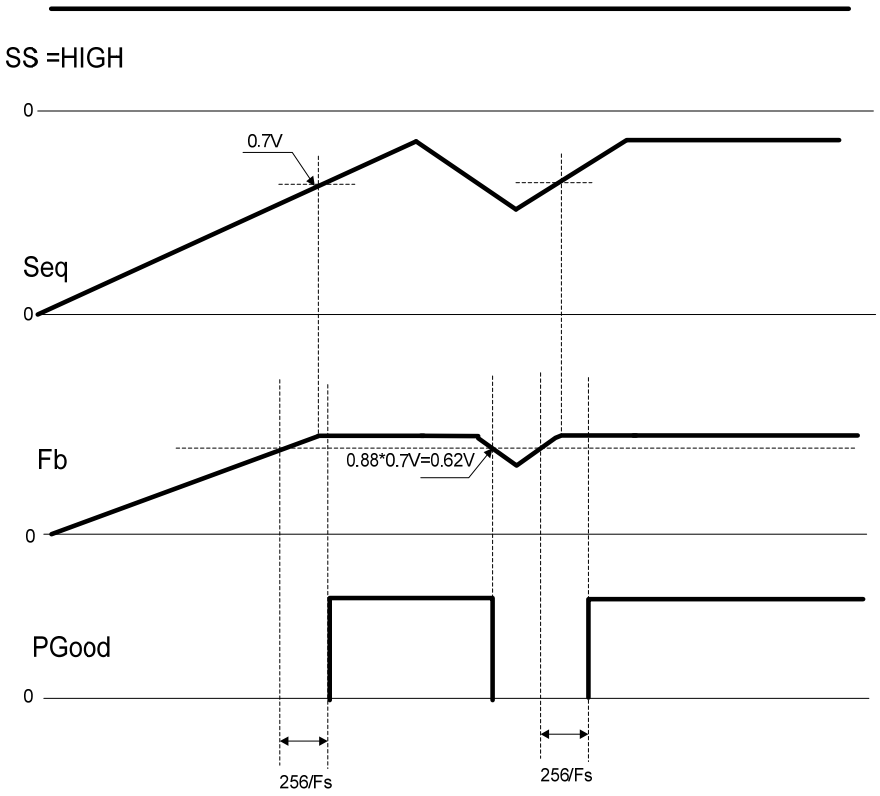


Fig.9b IR3841 Sequencing Operation

Minimum on time Considerations

The minimum ON time is the shortest amount of time for which the Control FET may be reliably turned on, and this depends on the internal timing delays. For the IR3841, the typical minimum on-time is specified as 50 ns.
Any design or application using the IR3841 must ensure operation with a pulse width that is higher than this minimum on-time and preferably higher than 100 ns. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{V_{in} \times F_s}$$

In any application that uses the IR3841, the following condition must be satisfied:

$$t_{on(min)} \le t_{on}$$

$$\therefore t_{on(min)} \le \frac{V_{out}}{V_{in} \times F_s}$$

$$\therefore V_{in} \times F_s \le \frac{V_{out}}{t_{on(min)}}$$

The minimum output voltage is limited by the reference voltage and hence $V_{out(min)}$ = 0.7 V. Therefore, for $V_{out(min)}$ = 0.7 V,

$$\therefore V_{in} \times F_s \le \frac{V_{out(min)}}{t_{on(min)}}$$

$$\therefore V_{in} \times F_s \le \frac{0.7\ V}{100\ ns} = 7 \times 10^6\ V/s$$

Therefore, at the maximum recommended input voltage 16V and minimum output voltage, the converter should be designed at a switching frequency that does not exceed 440 kHz. Conversely, for operation at the maximum recommended operating frequency 1.65 MHz and minimum output voltage, any voltage above 4.2 V may not be stepped down without pulse-skipping.

Maximum Duty Ratio Considerations

A fixed off-time of 200 ns maximum is specified for the IR3841. This provides an upper limit on the operating duty ratio at any given switching frequency. It is clear, that higher the switching frequency, the lower is the maximum duty ratio at which the IR3841 can operate. To allow some margin, the maximum operating duty ratio in any application using the IR3841 should still accommodate about 250 ns off-time. Fig 10. shows a plot of the maximum duty ratio v/s the switching frequency, with 250 ns off-time.

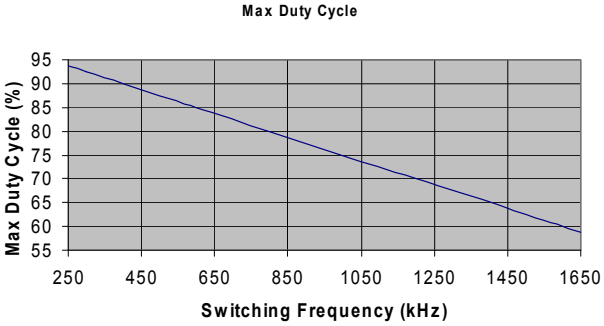


Fig. 10. Maximum duty cycle v/s switching frequency.

Application Information

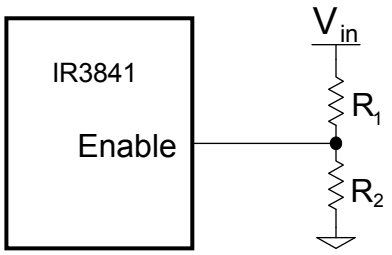
Design Example:

The following example is a typical application for IR3841. The application circuit is shown on page 23.

V_{in} = 12 V (13.2V max)
V_o = 1.8 V
I_o = 8 A
$\Delta V_o \leq$ 54mV
F_s = 600 kHz

Enabling the IR3841

As explained earlier, the precise threshold of the Enable lends itself well to implementation of a UVLO for the Bus Voltage.



For a typical Enable threshold of V_{EN} = 1.2 V

$$V_{in(\min)} * \frac{R_2}{R_1 + R_2} = V_{EN} = 1.2 \quad \text{..... (5)}$$

$$R_2 = R_1 \frac{V_{EN}}{V_{in(\min)} - V_{EN}} \quad \text{..... (6)}$$

For a $V_{in\ (min)}$=10.2V, R_1=4.99K and R_2=750 ohm is a good choice.

Programming the frequency

For F_s = 600 kHz, select R_t = 23.7 kΩ, using Table. 1.

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 0.7V. The divider is ratioed to provide 0.7V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_o = V_{ref} * \left(1 + \frac{R_8}{R_9}\right) \quad \text{.....(7)}$$

When an external resistor divider is connected to the output as shown in figure 11.
Equation (5) can be rewritten as:

$$R_9 = R_8 * \left(\frac{V_{ref}}{V_o - V_{ref}}\right) \quad \text{.....(8)}$$

For the calculated values of R8 and R9 see feedback compensation section.

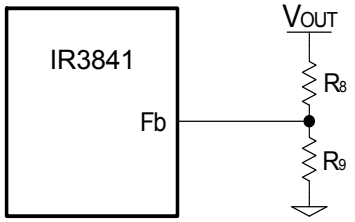


Fig. 11. Typical application of the IR3841 for programming the output voltage

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft-start capacitance value. From (1), for a desired start-up time of the converter, the soft start capacitor can be calculated by using:

$$C_{SS}(\mu F) = T_{start}\ (\text{ms}) \times 0.02857 \quad \text{..... (9)}$$

Where T_{start} is the desired start-up time (ms).
For a start-up time of 3.5ms, the soft-start capacitor will be 0.099µF. Choose a 0.1µF ceramic capacitor.

Bootstrap Capacitor Selection

To drive the Control FET, it is necessary to supply a gate voltage at least 4V greater than the voltage at the SW pin, which is connected the source of the Control FET . This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external bootstrap capacitor (C6). The operation of the circuit is as follows: When the lower MOSFET is turned on, the capacitor node connected to SW is pulled down to ground. The capacitor charges towards V_{cc} through the internal bootstrap diode, which has a forward voltage drop V_D. The voltage V_c across the bootstrap capacitor C6 is approximately given as

$$V_c \cong V_{cc} - V_D \quad \text{..... (10)}$$

When the upper MOSFET turns on in the next cycle, the capacitor node connected to SW rises to the bus voltage V_{in}. However, if the value of C6 is appropriately chosen,

the voltage *Vc* across C6 remains approximately unchanged and the voltage at the Boot pin becomes

$$V_{Boot} \cong V_{in} + V_{cc} - V_D \quad \text{.....(11)}$$

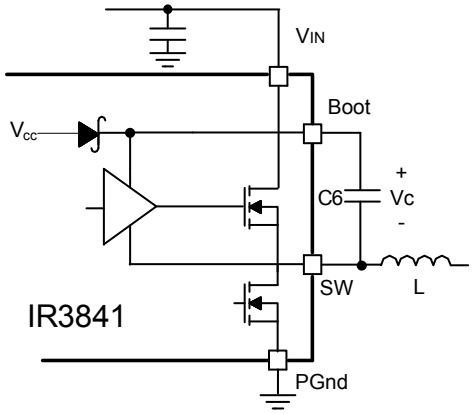


Fig. 12. Bootstrap circuit to generate Vc voltage

A bootstrap capacitor of value 0.1uF is suitable for most applications.

Input Capacitor Selection

The ripple current generated during the on time of the upper MOSFET should be provided by the input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_o * \sqrt{D*(1-D)} \quad \text{.....(12)}$$

$$D = \frac{V_o}{V_{in}} \quad \text{.....(13)}$$

Where:

D is the Duty Cycle

I_{RMS} is the RMS value of the input capacitor current.

Io is the output current.

For I_o=8A and *D* = 0.15, the I_{RMS} = 2.86A.

Ceramic capacitors are recommended due to their peak current capabilities. They also feature low ESR and ESL at higher frequency which enables better efficiency. For this application, it is advisable to have 4x10uF 16V ceramic capacitors ECJ-3YX1C106K from Panasonic. In addition to these, although not mandatory, a 1X330uF, 25V SMD capacitor EEV-FK1E331P may also be used as a bulk capacitor and is recommended if the input power supply is not located close to the converter.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor (Δi). The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$V_{in} - V_o = L * \frac{\Delta i}{\Delta t};\ \ \Delta t = D * \frac{1}{F_s}$$
$$L = (V_{in} - V_o) * \frac{V_o}{V_{in} * \Delta i * F_s} \quad \text{..... (14)}$$

Where:

V_{in} = Maximum input voltage

V_o = Output Voltage

Δi = Inductor ripple current

F_s = Switching frequency

Δt = Turn on time

D = Duty cycle

If $\Delta i \approx 35\%(I_o)$, then the output inductor is calculated to be 0.91µH. Select *L*=1 µH.

The MPL105-1R0 from Delta provides a compact, low profile inductor suitable for this application.

Output Capacitor Selection

The voltage ripple and transient requirements determine the output capacitors type and values. The criteria is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components. These components can be described as

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{o(ESR)} = \Delta I_L * ESR$$

$$\Delta V_{o(ESL)} = \left(\frac{V_{in} - V_o}{L}\right) * ESL$$

$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 * C_o * F_s} \quad \text{.....(15)}$$

ΔV_o = Output voltage ripple

ΔI_L = Inductor ripple current

Since the output capacitor has a major role in the overall performance of the converter and determines the result of transient response, selection of the capacitor is critical. The IR3841 can perform well with all types of capacitors.

As a rule, the capacitor must have low enough ESR to meet output ripple and load transient requirements.

The goal for this design is to meet the voltage ripple requirement in the smallest possible capacitor size. Therefore it is advisable to select ceramic capacitors due to their low ESR and ESL and small size. Six of the Panasonic ECJ-2FB0J226ML (22uF, 6.3V, 3mOhm) capacitors is a good choice.

Feedback Compensation

The IR3841 is a voltage mode controller. The control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed-loop transfer function with the highest 0 dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see figure 13). The resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2 * \pi \sqrt{L_o * C_o}} \quad \text{.....(16)}$$

Figure 13 shows gain and phase of the LC filter. Since we already have 180° phase shift from the output filter alone, the system runs the risk of being unstable.

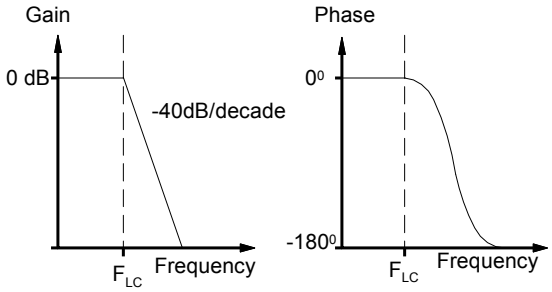


Fig. 13. Gain and Phase of LC filter

The IR3841 uses a voltage-type error amplifier with high-gain (110dB) and wide-bandwidth. The output of the amplifier is available for DC gain control and AC phase compensation.

The error amplifier can be compensated either in type II or type III compensation.

Local feedback with Type II compensation is shown in Fig. 14.

This method requires that the output capacitor should have enough ESR to generate a zero typically at 5kHz to 50kHz, which is essential for an acceptable phase margin and to satisfy stability requirements.

$$F_{ESR} = \frac{1}{2 * \pi * ESR * C_o} \quad \text{.....(17)}$$

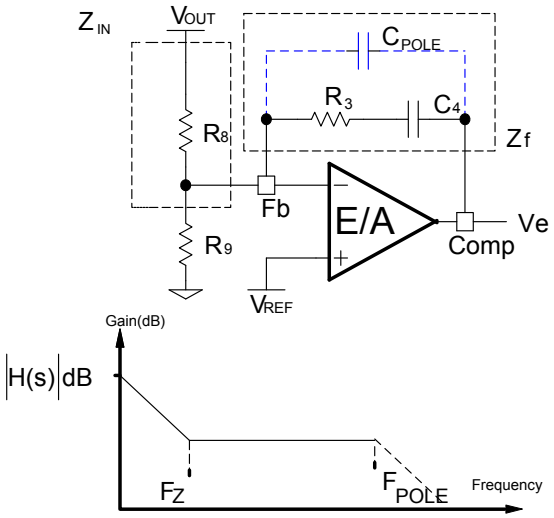


Fig. 14. Type II compensation network and its asymptotic gain plot

The transfer function (V_e/V_o) is given by:

$$\frac{V_e}{V_o} = H(s) = -\frac{Z_f}{Z_{IN}} = -\frac{1+sR_3C_4}{sR_8C_4} \quad \text{.....(18)}$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = \frac{R_3}{R_8} \quad \text{.....(19)}$$

$$F_z = \frac{1}{2\pi * R_3 * C_4} \quad \text{.....(20)}$$

First select the desired zero-crossover frequency (F_o):

$$F_o > F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10) * F_s$$

Use the following equation to calculate R3:

$$R_3 = \frac{V_{osc} * F_o * F_{ESR} * R_8}{V_{in} * F_{LC}^2} \quad \text{.....(21)}$$

Where:
V_{in} = Maximum Input Voltage
V_{osc} = Oscillator Ramp Voltage
F_o = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_8 = Feedback Resistor

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_z = 75\% F_{LC}$$

$$F_z = 0.75 * \frac{1}{2\pi\sqrt{L_o * C_o}} \quad \text{.....(22)}$$

Use equations (20), (21) and (22) to calculate C4.
One more capacitor is sometimes added in parallel with C4 and R3. This introduces one more pole which is mainly used to suppress the switching noise.
The additional pole is given by:

$$F_P = \frac{1}{2\pi * R_3 * \frac{C_4 * C_{POLE}}{C_4 + C_{POLE}}} \quad \text{.....(23)}$$

The pole sets to one half of the switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi * R_3 * F_s - \frac{1}{C_4}} \cong \frac{1}{\pi * R_3 * F_s} \quad \text{.....(24)}$$

For a general solution for unconditional stability for any type of output capacitors, and a wide range of ESR values, we should implement local feedback with a type III compensation network. The typically used compensation network for voltage-mode controller is shown in figure 15.

Again, the transfer function is given by:

$$\frac{V_e}{V_o} = H(s) = -\frac{Z_f}{Z_{IN}}$$

By replacing Z_{in} and Z_f according to figure 15, the transfer function can be expressed as:

$$H(s) = -\frac{(1+sR_3C_4)\left[1+sC_7(R_8+R_{10})\right]}{sR_8(C_4+C_3)\left[1+sR_3\left(\frac{C_4*C_3}{C_4+C_3}\right)\right](1+sR_{10}C_7)} \quad \text{....(25)}$$

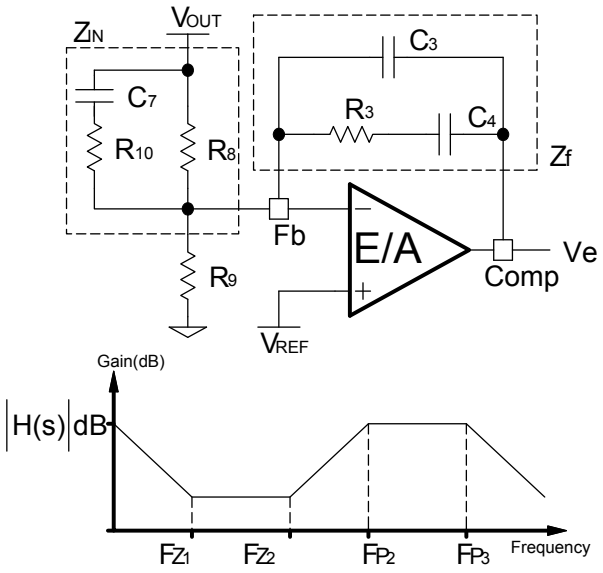


Fig.15. Type III Compensation network and its asymptotic gain plot

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0 \quad \text{.....(26)}$$

$$F_{P2} = \frac{1}{2\pi * R_{10} * C_7} \quad \text{.....(27)}$$

$$F_{P3} = \frac{1}{2\pi * R_3 \left(\frac{C_4 * C_3}{C_4 + C_3} \right)} \cong \frac{1}{2\pi * R_3 * C_3} \quad \text{.....(28)}$$

$$F_{Z1} = \frac{1}{2\pi * R_3 * C_4} \quad \text{.....(29)}$$

$$F_{Z2} = \frac{1}{2\pi * C_7 * (R_8 + R_{10})} \cong \frac{1}{2\pi * C_7 * R_8} \quad \text{.....(30)}$$

Cross over frequency is expressed as:

$$F_o = R_3 * C_7 * \frac{V_{in}}{V_{osc}} * \frac{1}{2\pi * L_o * C_o} \quad \text{.....(31)}$$

Based on the frequency of the zero generated by the output capacitor and its ESR, relative to crossover frequency, the compensation type can be different. The table below shows the compensation types and location of the crossover frequency.

Compensator Type	F_{ESR} vs F_o	Output Capacitor
Type II	$F_{LC}<F_{ESR}<F_o<F_s/2$	Electrolytic Tantalum
Type III	$F_{LC}<F_o<F_{ESR}$	Tantalum Ceramic

The higher the crossover frequency, the potentially faster the load transient response. However, the crossover frequency should be low enough to allow attenuation of switching noise. Typically, the control loop bandwidth or crossover frequency is selected such that

$$F_o \le (1/5 \sim 1/10) * F_s$$

The DC gain should be large enough to provide high DC-regulation accuracy. The phase margin should be greater than 45° for overall stability.

For this design we have:
V_{in}=12V
V_o=1.8V
V_{osc}=1.8V
V_{ref}=0.7V
L_o=1uH
C_o=6x22uF, ESR=3mOhm each

It must be noted here that the value of the capacitance used in the compensator design must be the small signal value. For instance, the small signal capacitance of the 22uF capacitor used in this design is 12uF at 1.8 V DC bias and 600 kHz frequency. It is this value that must be used for all computations related to the compensation. The small signal value may be obtained from the manufacturer's datasheets, design tools or SPICE models. Alternatively, they may also be inferred from measuring the power stage transfer function of the converter and measuring the double pole frequency F_{LC} and using equation (16) to compute the small signal C_o.

These result to:
***F_{LC}*=18.76 kHz**
***F_{ESR}*=4.4 MHz**
***$F_s/2$*=300 kHz**

Select crossover frequency: ***F_o*=100 kHz**
Since $F_{LC}<F_o<F_s/2<F_{ESR}$, TypeIII is selected to place the pole and zeros.

Detailed calculation of compensation TypeIII

Desired Phase Margin $\Theta = 70^{o}$

$$F_{Z2} = F_o\sqrt{\frac{1-\sin\Theta}{1+\sin\Theta}} = 17.63\text{kHz}$$

$$F_{P2} = F_o\sqrt{\frac{1+\sin\Theta}{1-\sin\Theta}} = 567.1\text{kHz}$$

Select $F_{Z1} = 0.5 * F_{Z2} = 8.82$ kHz and

$F_{P3} = 0.5 * F_s = 300$ kHz

Select $C_7 = 2.2\text{nF}$

Calculate R_3, C_3 and C_4 :

$$R_3 = \frac{2\pi * F_o * L_o * C_o * V_{osc}}{C_7 * V_{in}}; R_3 = 3.05\ \text{k}\Omega$$

Select $R_3 = 3.01\text{k}\Omega$

$$C_4 = \frac{1}{2\pi * F_{Z1} * R_3}; C_4 = 6\ \text{nF},\ \text{Select}\ C_4 = 10\ \text{nF}$$

$$C_3 = \frac{1}{2\pi * F_{P3} * R_3}; C_3 = 176.25\,\text{pF},\ \text{Select}\, C_3 = 150\,\text{pF}$$

Calculate R_{10}, R_8 and R_9 :

$$R_{10} = \frac{1}{2\pi * C_7 * F_{P2}};\ R_{10} = 128\,\Omega,\ \text{Select}\, R_{10} = 130\,\Omega$$

$$R_8 = \frac{1}{2\pi * C_7 * F_{Z2}} - R_{10};\ R_8 = 3.97\text{k}\Omega,$$

Select $R_8 = 4.02\text{k}\Omega$

$$R_9 = \frac{V_{ref}}{V_o - V_{ref}} * R_8; R_9 = 2.56\text{k}\Omega\ \text{Select}\, R_9 = 2.55\text{k}\Omega$$

Programming the Current-Limit

The Current-Limit threshold can be set by connecting a resistor (R_{OCSET}) from the SW pin to the OCSet pin. The resistor can be calculated by using equation (4). This resistor ROCSET must be placed close to the IC.

The $R_{DS(on)}$ has a positive temperature coefficient and it should be considered for the worst case operation.

$$I_{SET} = I_{L(critical)} = \frac{R_{OCSet} * I_{OCSet}}{R_{DS(on)}} \quad \text{.....(32)}$$

$R_{DS(on)} = 8.7\ \text{m}\Omega * 1.5 = 13.05\,\text{m}\Omega$

$I_{SET} \cong I_{o(LIM)} = 8\,\text{A} * 1.5 = 12\,\text{A}$

(50% over nominal output current)

$I_{OCSet} = 59.07\,\mu\text{A}$ (at $F_s = 600\text{kHz}$)

$R_{OCSet} = 2.65\,\text{k}\Omega$ Select $R_7 = 2.67\,\text{k}\Omega$

Setting the Power Good Threshold

Power Good threshold is internally set at 88% of Vref. When the voltage at the FB pin exceeds the threshold, PGood is asserted.

The PGood is an open drain output. Hence, it is necessary to use a pull up resistor R_{PG} from PGood pin to Vcc. The value of the pull-up resistor must be chosen such as to limit the current flowing into the PGood pin, when the output voltage is not in regulation, to less than 5 mA. A typical value used is 4.7kΩ.

Application Diagram:

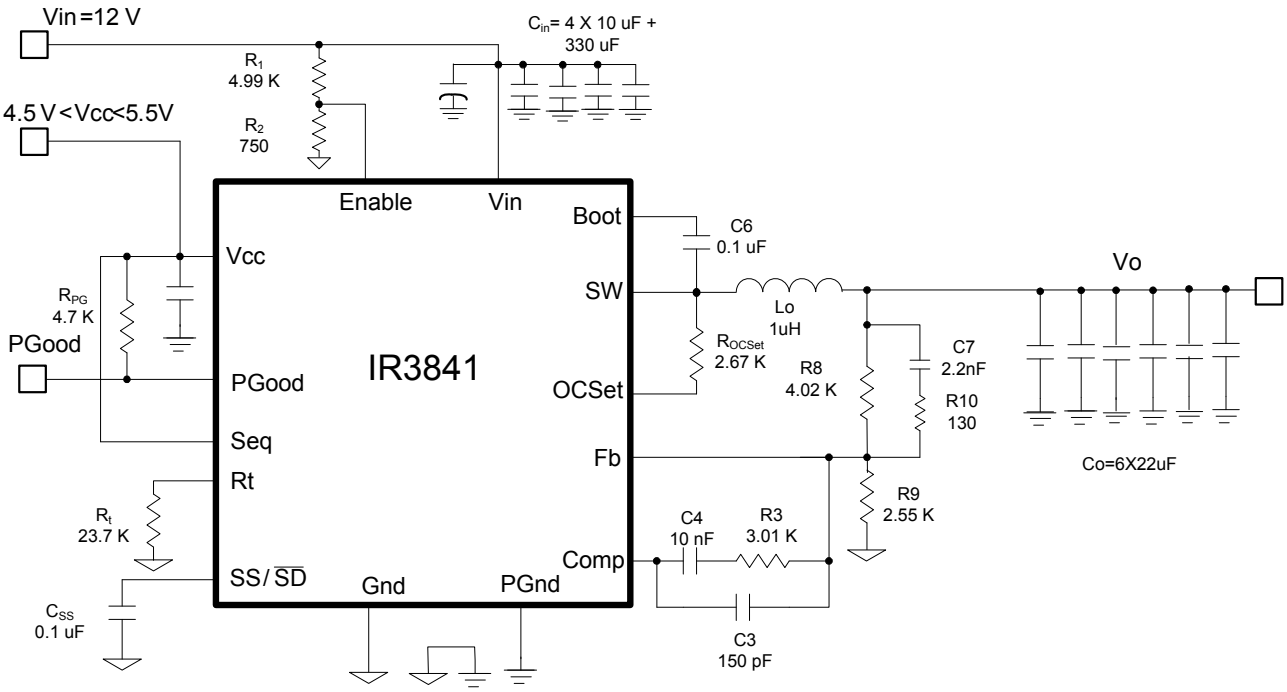


Fig. 16. Application circuit diagram for a 12V to 1.8 V, 8 A Point Of Load Converter

Suggested Bill of Materials for the application circuit:

Part Reference	Quantity	Value	Description	Manufacturer	Part Number
Cin	1	330uF	SMD Elecrolytic, Fsize, 25V, 20%	Panasonic	EEV-FK1E331P
	4	10uF	1206, 16V, X7R, 20%	Panasonic - ECG	ECJ-3YX1C106K
Lo	1	1.0uH	11.5x10x5mm, 20%, 2.34mOhm	Delta	MPL105-1R0
Co	6	22uF	0805, 6.3V, X5R, 20%	Panasonic- ECG	ECJ-2FB0J226ML
R1	1	4.99K	Thick Film, 0603,1/10 W,1%	Rohm	MCR03EZPFX4991
R2	1	750	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX7500
R_t	1	23.7k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX2372
R_{OCSet}	1	2.67k	Thick Film, 0603,1/10 W,1%	Rohm	MCR03EZPFX2671
R_{PG}	1	4.7K	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX4701
C_{ss}	1	0.1uF	0603, 25V, X7R, 10%	Panasonic - ECG	ECJ-1VB1E104K
R3	1	3.01k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX3011
C3	1	150pF	50V, 0603, NPO, 5%	Panasonic- ECG	ECJ-1VC1H151J
C4	1	10000pF	0603, 50V, X7R, 10%	Panasonic - ECG	ECJ-1VB1H103K
R8	1	4.02K	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX4021
R9	1	2.55K	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX2551
R10	1	130	Thick Film, 0603,1/10W,1%	Panasonic - ECG	ERJ-3EKF1300V
C7	1	2200pF	0603, 50V, X7R, 10%	Panasonic - ECG	ECJ-1VB1H222K
U1	1	IR3841	SupIRBuck PQFN 5x6mm	International Rectifier	IR3841MPbF

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vcc=5V, Vo=1.8V, Io=0-8A, Room Temperature, No Air Flow

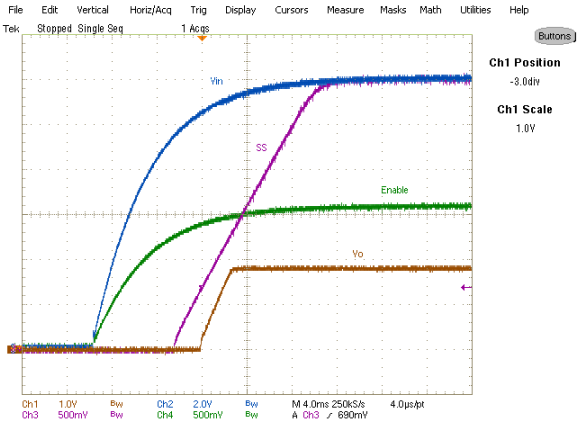


Fig. 17. Start up at 8A Load
Ch_1:V_o, Ch_2:V_{in}, Ch_3:V_{ss}, Ch_4:Enable

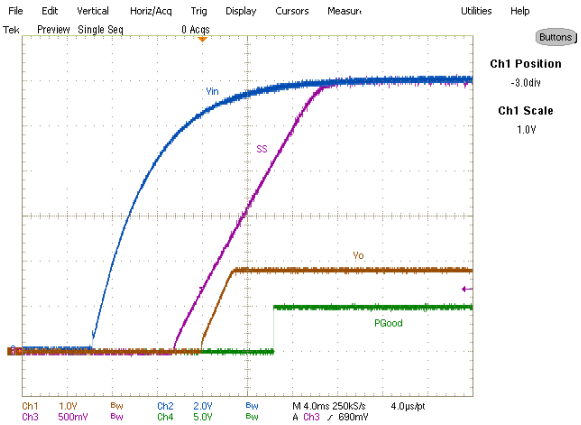


Fig. 18. Start up at 8A Load,
Ch_1:V_o, Ch_2:V_{in}, Ch_3:V_{ss}, Ch_4:V_{PGood}

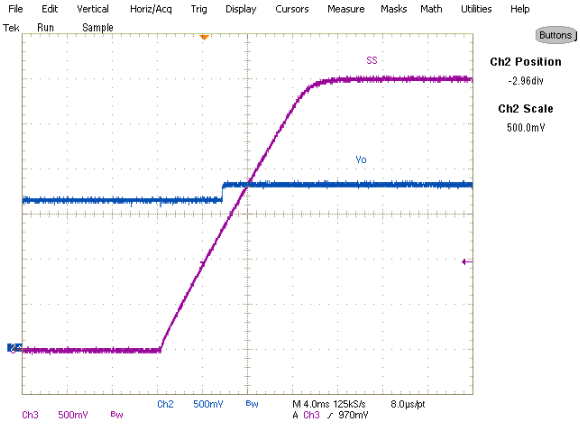


Fig. 19. Start up with 1.62V Pre Bias, 0A Load, Ch_2:V_o, Ch_3:V_{SS}

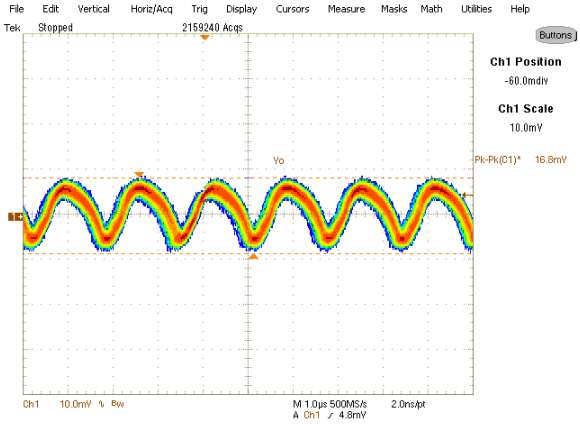


Fig. 20. Output Voltage Ripple, 8A load
Ch_1: V_{out} ,

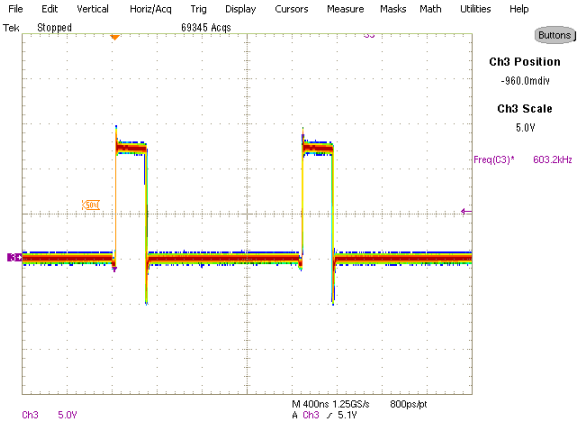


Fig. 21. Inductor node at 8A load
Ch_3:LX

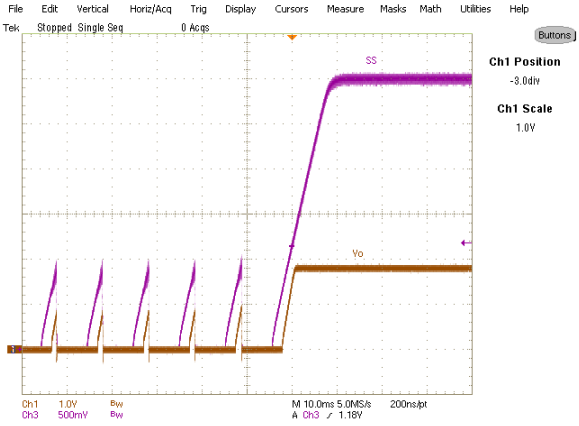


Fig. 22. Short (Hiccup) Recovery
Ch_1:V_{out} , Ch_2:V_{ss}

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc=5V, Vo=1.8V, Io=0-8A, Room Temperature, No Air Flow

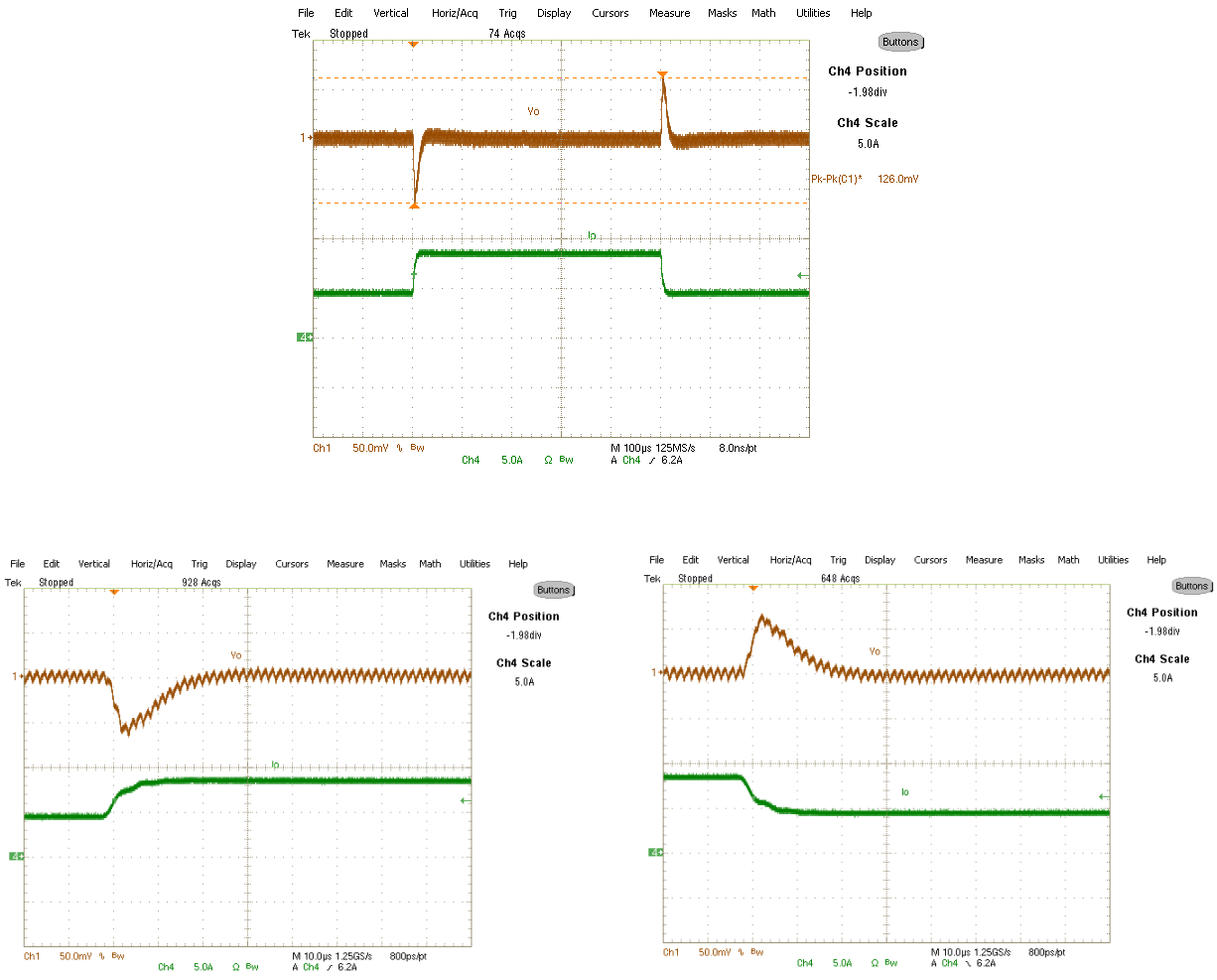


Fig. 23. Transient Response, 4A to 8A step
Ch_1:V_{out}, Ch_4:I_{out}

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc=5V, Vo=1.8V, Io=8A, Room Temperature, No Air Flow

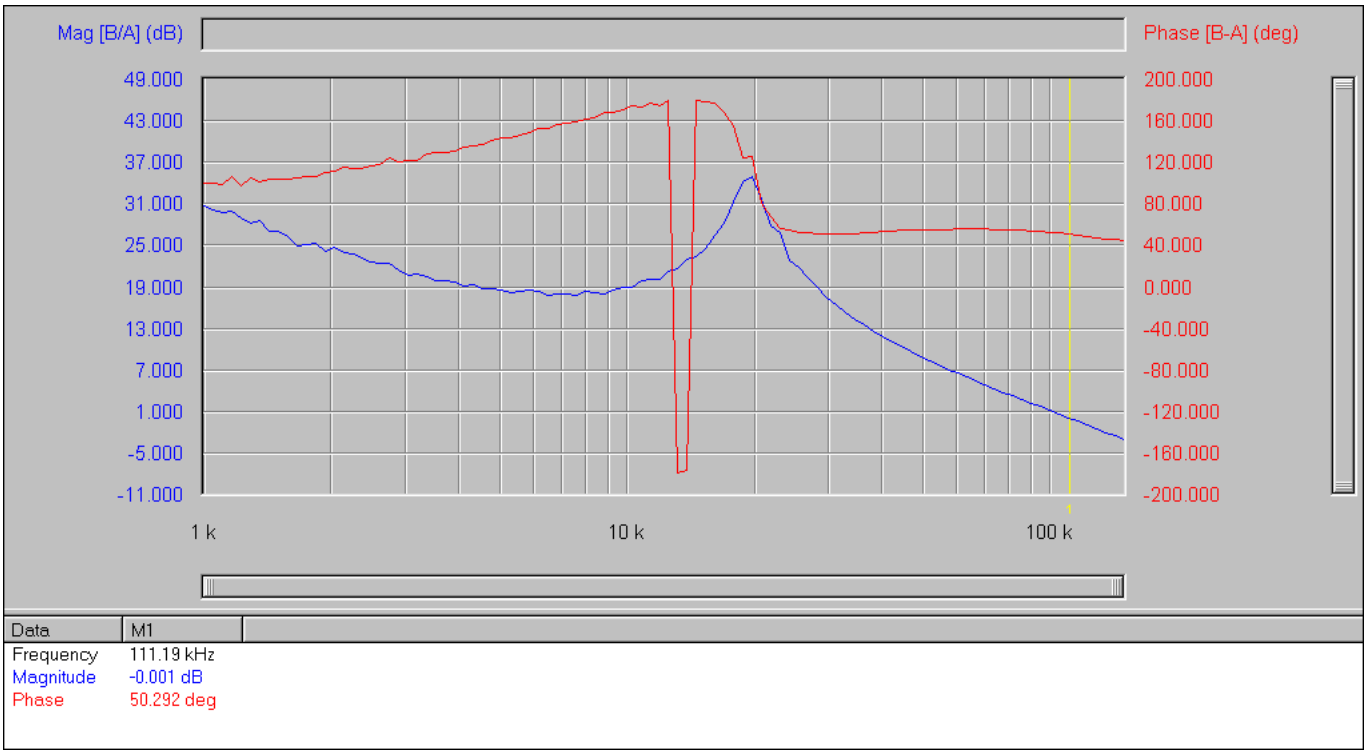


Fig. 24. Bode Plot at 8A load shows a bandwidth of 111kHz and phase margin of 50 degrees

Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Make all the connections for the power components in the top layer with wide, copper filled areas or polygons. In general, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

The inductor, output capacitors and the IR3841 should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place the input capacitor directly at the Vin pin of IR3841.

The feedback part of the system should be kept away from the inductor and other noise sources.

The critical bypass components such as capacitors for Vcc should be close to their respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

The connection between the OCSet resistor and the Sw pin should not share any trace with the connection between the bootstrap capacitor and the Sw pin. Instead, it is recommended to use a Kelvin connection of the trace from the OCSet resistor and the trace from the bootstrap capacitor at the Sw pin.

In a multilayer PCB use one layer as a power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

The Power QFN is a thermally enhanced package. Based on thermal performance it is recommended to use at least a 4-layers PCB. To effectively remove heat from the device the exposed pad should be connected to the ground plane using vias. Figure 25 illustrates the implementation of the layout guidelines outlined above, on the IRDC3841 4 layer demoboard.

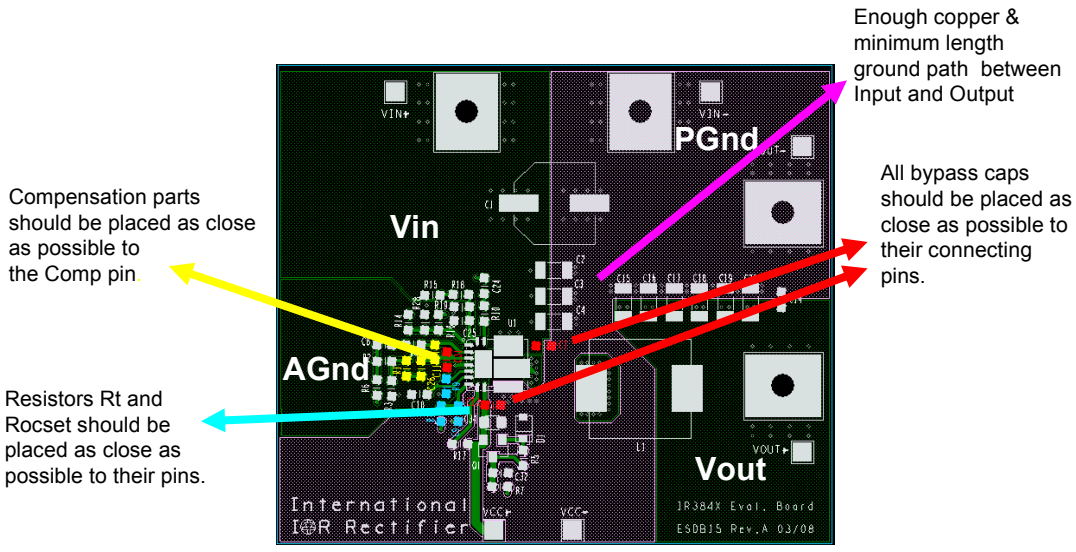


Fig.25a. IRDC3841 demoboard layout considerations – Top Layer

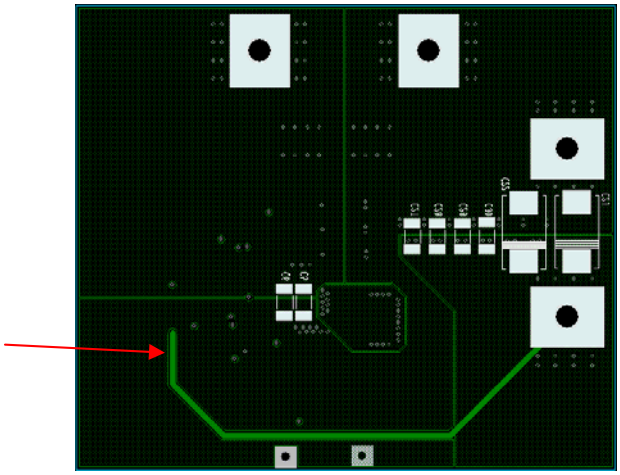


Fig.25b. IRDC3841 demoboard layout considerations – Bottom Layer

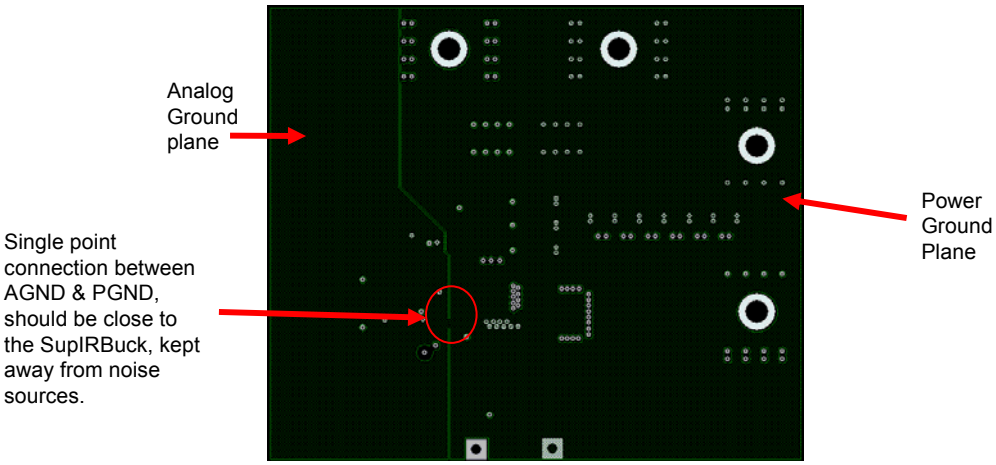


Fig.25c. IRDC3841 demoboard layout considerations – Mid Layer 1

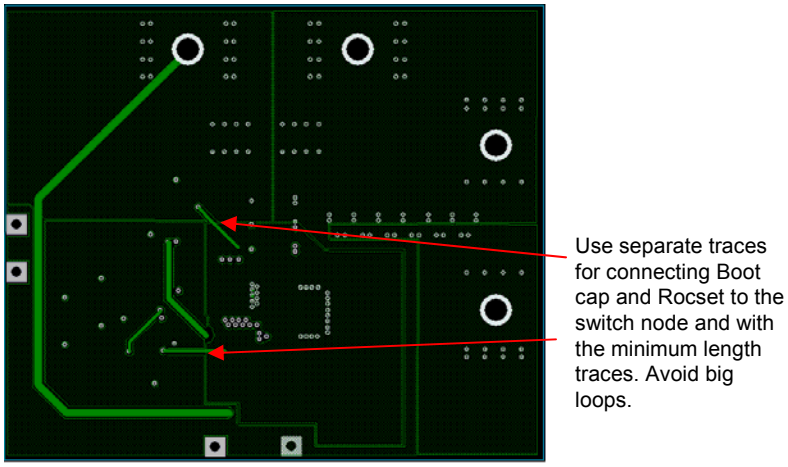


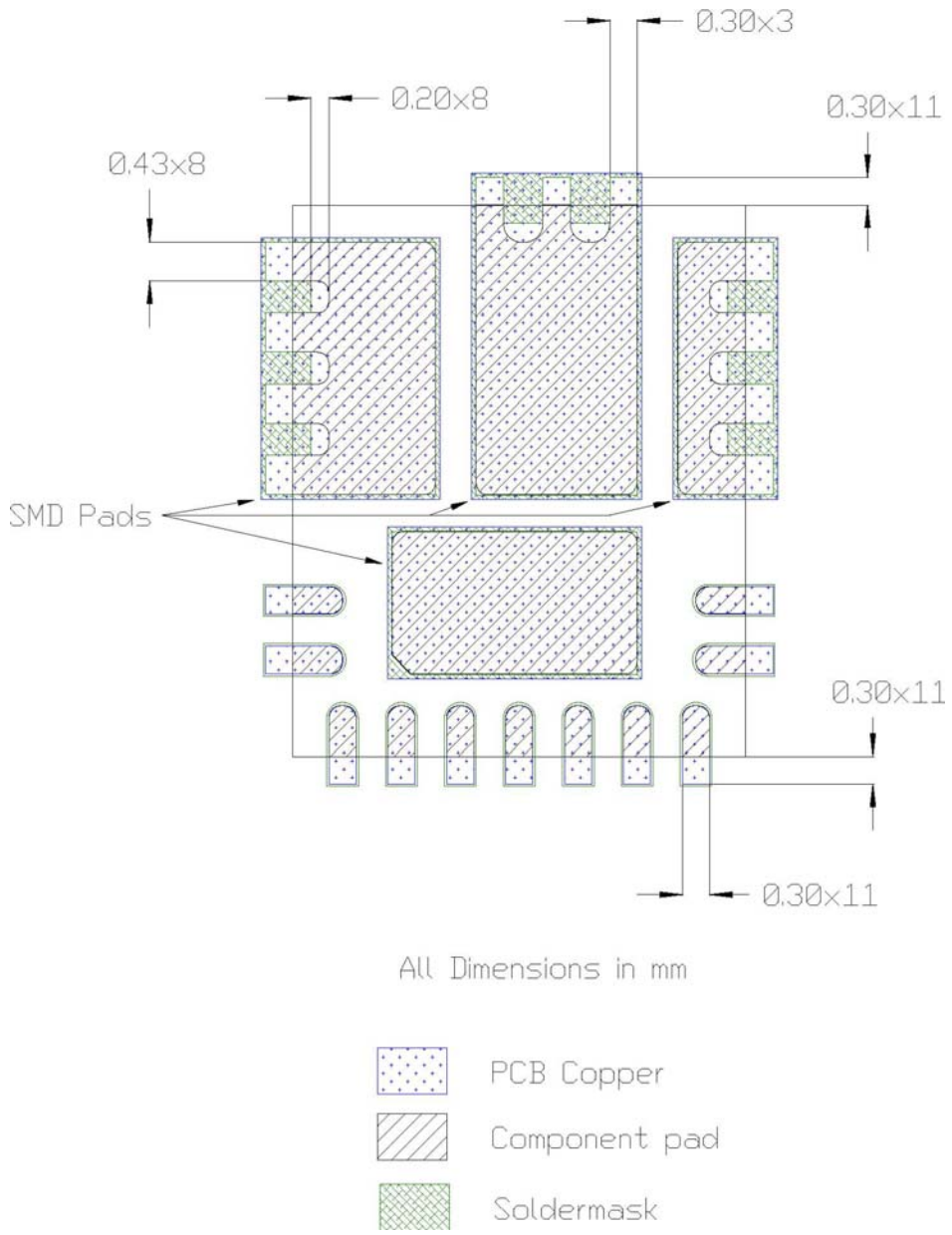
Fig.25d. IRDC3841 demoboard layout considerations – Mid Layer 2

PCB Metal and Components Placement

Lead lands (the 11 IC pins) width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.

Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large and inspectable toe fillet.

Pad lands (the 4 big pads other than the 11 IC pins) length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be no less than 0.17mm for 2 oz. Copper; no less than 0.1mm for 1 oz. Copper and no less than 0.23mm for 3 oz. Copper.

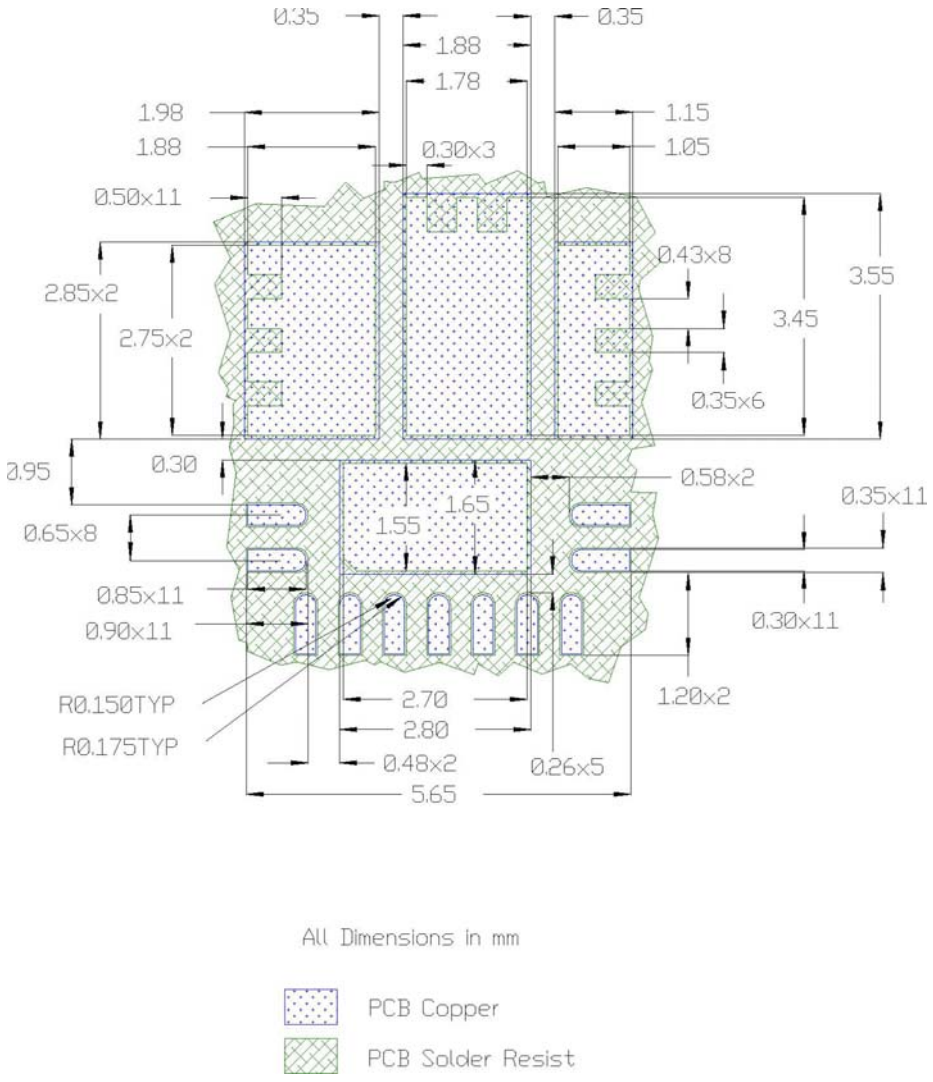


Solder Resist

It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

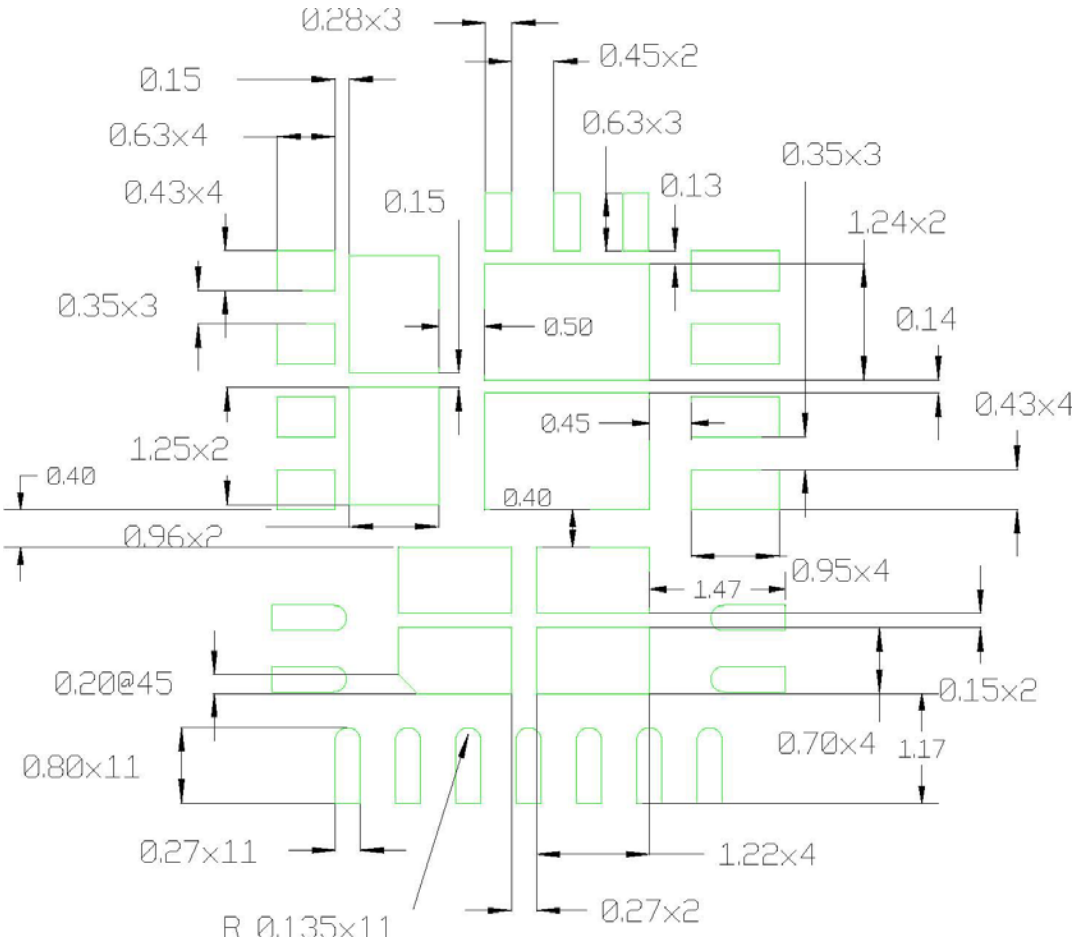
The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist mis-alignment.

Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

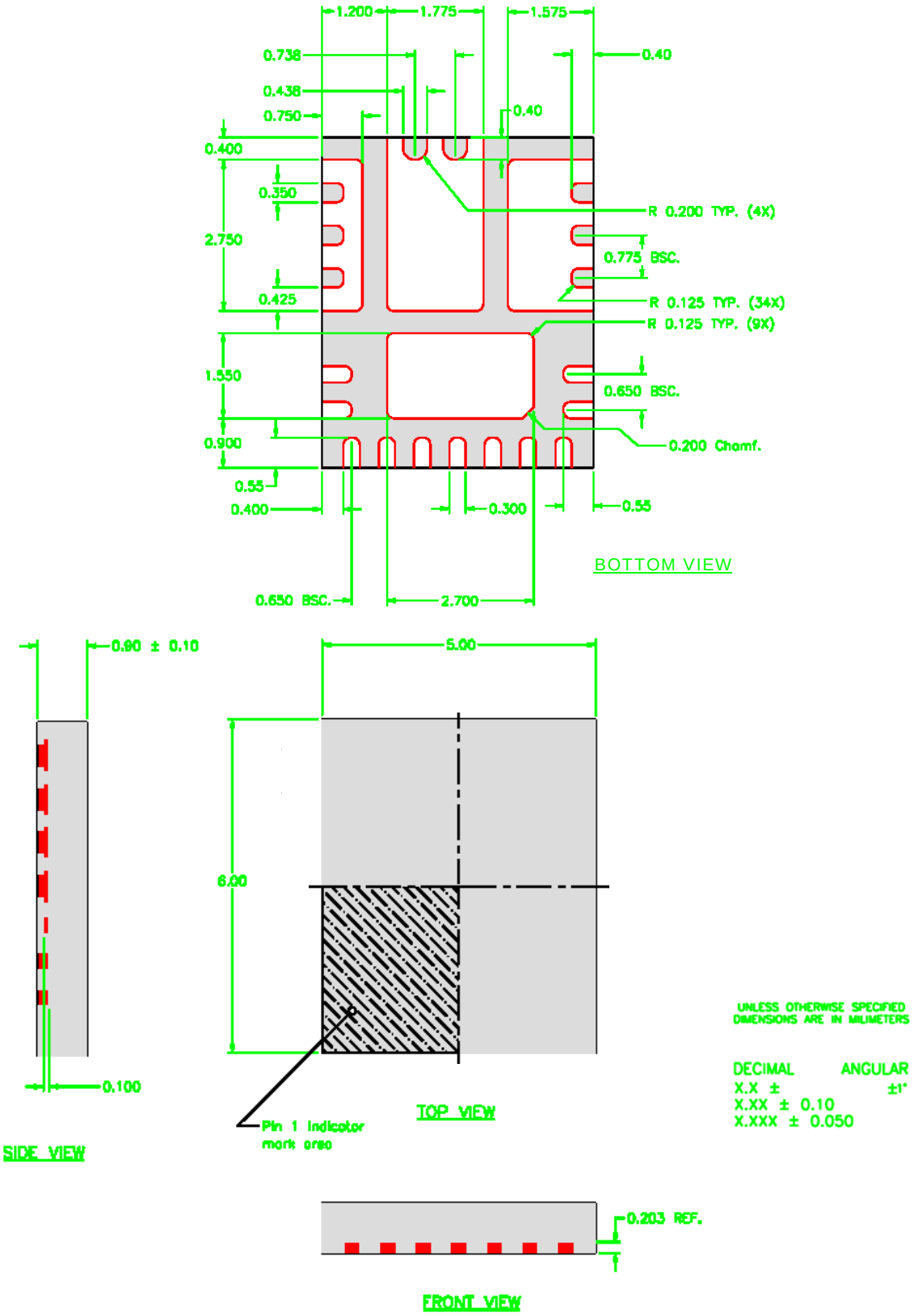


Stencil Design

- The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lads. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm



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