# MAX17690

# 60V, No-Opto Isolated Flyback Controller

## General Description

The MAX17690 is a peak current mode, fixed-frequency switching controller specifically designed for the isolated flyback topology operating in Discontinuous Conduction Mode (DCM). The device senses the isolated output voltage directly from the primary-side flyback waveform during the off-time of the primary switch. No auxiliary winding or optocoupler is required for output voltage regulation.

The MAX17690 is designed to operate over a wide supply range from 4.5V to 60V. The switching frequency is programmable from 50kHz to 250kHz. A EN/UVLO pin allows the user to turn on/off the power supply precisely at the desired input voltage. The MAX17690 provides an input overvoltage protection through the OVI pin. The 7V internal LDO output of the MAX17690 makes it suitable for switching both logic-level and standard MOSFETs used in flyback converters. With 2A/4A source/sink currents, the MAX17690 is ideal for driving low $R_{DS(ON)}$ power MOSFETs with fast gate transition times. The MAX17690 provides an adjustable soft-start feature to limit the inrush current during startup.

The MAX17690 provides temperature compensation for the output diode forward voltage drop. The MAX17690 has robust hiccup-protection and thermal protection schemes, and is available in a space-saving 16-pin 3mm x 3mm TQFN package with a temperature range from -40°C to 125°C.

## Benefits and Features

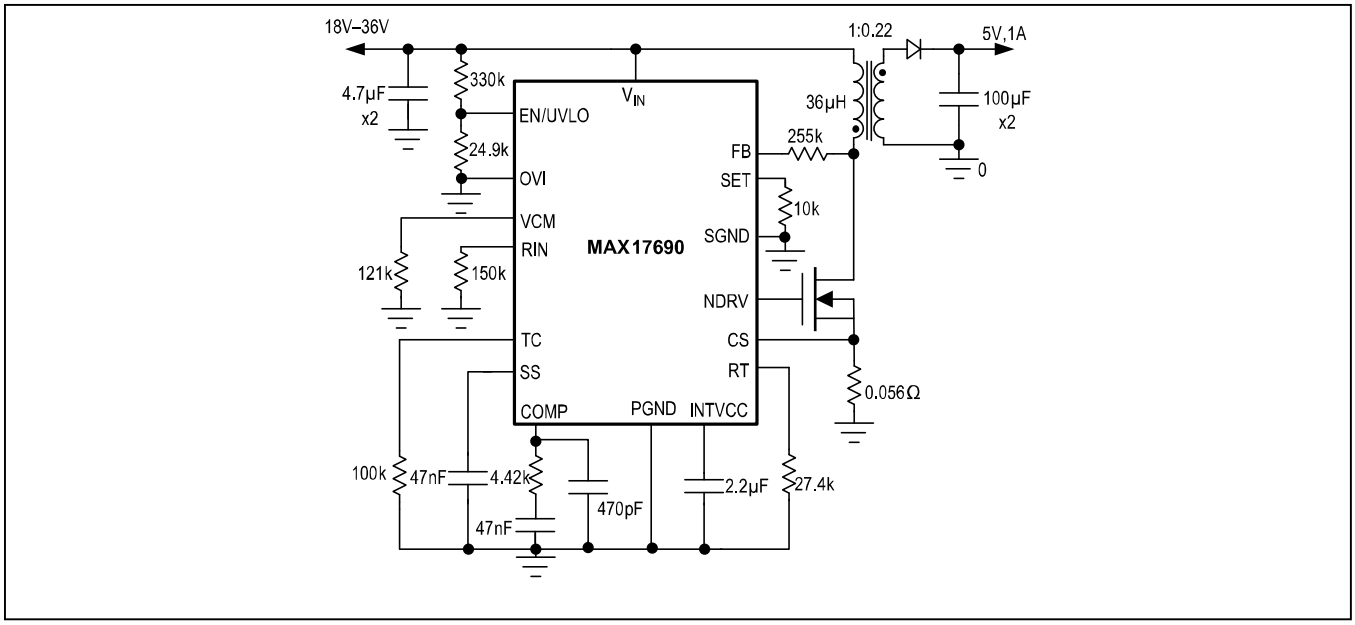
- 4.5V to 60V Input Voltage Range
- No Optocoupler or Third Winding Required to Derive Feedback Signal Across Isolation Boundary
- 2A/4A Peak Source/Sink Gate Drive Currents
- 50kHz to 250kHz Programmable Switching Frequency
- Input EN/UVLO Feature
- Input Overvoltage Protection
- Programmable Soft-Start
- Hiccup-Mode Short-Circuit Protection
- Thermal Shutdown Protection
- -40°C to 125°C Operating Temperature Range
- Space-Saving, 16-Pin 3 x 3 TQFN Package

## Applications

- Isolated Flyback Converters
- Wide-Range DC-Input Isolated Power Supplies
- Industrial and Telecom Applications
- PLC I/O modules

*Ordering Information* **appears at end of data sheet.**

## Application Circuit






maxim integrated™

## Absolute Maximum Ratings

INTVCC to SGND.....-0.3V to +16V
$V_{IN}$, EN/UVLO to SGND .....-0.3V to +70V
$V_{IN}$ to FB .....-0.3V to +0.3V
OVI to SGND .....-0.3V to +6V
RIN, RT, VCM, COMP, SS,
SET, TC and CS to SGND .....-0.3V to +6V
NDRV to PGND..... -0.3V to $V_{INTVCC}$ + 0.3V

Continuous Power Dissipation (single-layer board)
($T_A$ = +70°C, derate 15.6mW/°C above +70°C).....1250mW
Continuous Power Dissipation (multilayer board)
($T_A$ = +70°C, Derate 20.8mW/°C above +70°C)....1666.7mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Thermal Characteristics (Note 1)

Single-Layer Board
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) .....64°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$).....7°C/W

Four-Layer Board
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$).....48°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$).....7°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## Electrical Characteristics

($V_{IN}$ = 24V, $V_{EN/UVLO}$ = 2V, $V_{OVI}$ = 0V, $R_{RT}$ = 49.9kΩ, $C_{INTVCC}$ = 2.2µF to PGND; $V_{PGND}$ = $V_{SGND}$ = 0V, NDRV = SS = VCM = COMP = OPEN, CS = PGND, $V_{IN}$ to FB = 0V, $R_{SET}$ = 10kΩ, $R_{TC}$ = 27.5K, $R_{RIN}$ = 60kΩ,$T_A$ = $T_J$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = $T_J$ = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT VOLTAGE ($V_{IN}$)** | | | | | | |
| $V_{IN}$ Voltage Range | $V_{IN}$ | | 4.5 | | 60 | V |
| Input Supply Shutdown Current | IIN_SH | $V_{EN/UVLO}$ = 0V (shutdown mode) | | 2.5 | 4 | µA |
| | | $V_{IN}$ = 60V | | 3.5 | | µA |
| Input Switching Current | $I_{SW}$ | No capacitor at NDRV | | 1.8 | | mA |
| **ENABLE (EN/UVLO)** | | | | | | |
| EN/UNVO Threshold | $V_{ENR}$ | $V_{EN}$ rising | 1.19 | 1.215 | 1.24 | V |
| | $V_{ENF}$ | $V_{EN}$ falling | 1.07 | 1.1 | 1.12 | V |
| True Shutdown EN/UVLO Threshold | $V_{ENSHDN}$ | | | 0.7 | | V |
| EN/UVLO Input Leakage Current | $I_{ENLKG}$ | $V_{EN/UVLO}$ = 2V, $T_A$ = $T_J$ = +25°C | -100 | | +100 | nA |
| **INTVCC LDO** | | | | | | |
| INTVCC Output Voltage Range | $V_{INTVCC}$ | $V_{IN}$ = 8V, 1mA ≤ $I_{INTVCC}$ ≤ 25mA | 6.65 | 7.0 | 7.35 | V |
| | | 8V ≤ $V_{IN}$ ≤ 60V, $I_{INTVCC}$ = 1mA | 6.65 | 7.0 | 7.35 | V |
| INTVCC Current Limit | $I_{INTVCCMAX}$ | $V_{IN}$ = 8V, INTVCC = 6V | 26 | 60 | | mA |
| INTVCC Dropout | $V_{INTVCC-DO}$ | $V_{IN}$ = 4.5V, $I_{INTVCC}$ = 10mA | 4.1 | | | V |
| INTVCC ULVO | $V_{INTVCC-UVR}$ | Rising | 4.2 | 4.32 | 4.45 | V |
| | $V_{INTVCC-UVF}$ | Falling | 3.9 | 4.03 | 4.15 | V |
| **OVI** | | | | | | |
| OVI Threshold | $V_{OVIR}$ | $V_{OVI}$ rising | 1.19 | 1.215 | 1.24 | V |
| | $V_{OVIF}$ | $V_{OVI}$ falling | 1.07 | 1.1 | 1.12 | V |
| OVI Input Leakage Current | $I_{OVILKG}$ | $V_{OVI}$ = 2V, $T_A$ = $T_J$ = +25°C | -100 | | +100 | nA |

## Electrical Characteristics (continued)

($V_{IN}$ = 24V, $V_{EN/UVLO}$ = 2V, $V_{OVI}$ = 0V, $R_{RT}$ = 49.9kΩ, $C_{INTVCC}$ = 2.2µF to PGND; $V_{PGND}$ = $V_{SGND}$ = 0V, NDRV = SS = VCM = COMP = OPEN, CS = PGND, $V_{IN}$ to FB = 0V, $R_{SET}$ = 10kΩ, $R_{TC}$ = 27.5K, $R_{RIN}$ = 60kΩ,$T_A$ = $T_J$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = $T_J$ = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **NDRV** | | | | | | |
| RT Bias Voltage | $V_{RT}$ | | | 1.215 | | V |
| NDRV Switching Frequency Range | $F_{SW}$ | | 50 | | 250 | kHz |
| NDRV Switching Frequency Accuracy | | | -6 | | +6 | % |
| Maximum Duty Cycle | | | 66 | 69 | 71 | % |
| Minimum NDRV On-Time | $T_{ON\_MIN}$ | | | 200 | 235 | ns |
| Minimum NDRV Off-Time | $T_{OFF\_MIN}$ | | | 430 | 490 | ns |
| NDRV Pullup Resistance | $R_{NDRV\_P}$ | $I_{NDRV}$ = 100mA (sourcing) | | 1.6 | 2.8 | Ω |
| NDRV Pulldown Resistance | $R_{NDRV\_N}$ | $I_{NDRV}$ = 100mA (sinking) | | 0.45 | 0.9 | Ω |
| NDRV Peak Source Current | I-SOURCE | | | 2 | | A |
| NDRV Peak Sink Current | I-SINK | | | 4 | | A |
| NDRV Fall time | $T_{NDRV\_F}$ | $C_{NDRV}$ = 3.3nF | | 11 | | ns |
| NDRV Rise Time | $T_{NDRV\_R}$ | $C_{NDRV}$ = 3.3nF | | 16 | | ns |
| **SOFT-START (SS)** | | | | | | |
| Soft-Start Charging current | $I_{SS}$ | $V_{SS}$ = 1V | 4.75 | 5 | 5.25 | µA |
| Soft-Start Done Threshold | | $V_{SS}$ rising | | 0.98 | | V |
| **CURRENT SENSE (CS)** | | | | | | |
| Maximum CS Current-Limit Threshold | $V_{CS\_MAX}$ | $V_{SET}$ = 0.8V | 90 | 100 | 110 | mv |
| Minimum CS Current-Limit Threshold | $V_{CS\_MIN}$ | $V_{SET}$ = 1.2V | | 20 | | mv |
| CS Input Bias Current | $I_{CS}$ | $V_{CS}$ = 0V | 7.5 | 10 | 13.5 | µA |
| Runaway Current-Limit Threshold | $V_{CS\_RUNAWAY}$ | | 108 | 120 | 132 | mV |
| Overcurrent Hiccup Timeout | | $V_{SET}$ < 0.7V | | 16,384 | | cycles |
| **SET** | | | | | | |
| SET Regulation Voltage | $V_{SET}$ | | 0.988 | 1 | 1.012 | V |
| SET Undervoltage Trip Level to Cause Hiccup | $V_{SET\_HICF}$ | | | 0.7 | | V |
| **TC** | | | | | | |
| TC Pin Bias Voltage | $V_{TC}$ | $T_A$ = $T_J$ = +25°C | | 0.55 | | V |
| TC Current | $I_{TC}$ | $R_{TC}$ = 27.5kΩ | | 20 | | µA |
| **COMP** | | | | | | |
| Error Amplifier Transconductance | Gm | | | 1.6 | | mS |

## Electrical Characteristics (continued)

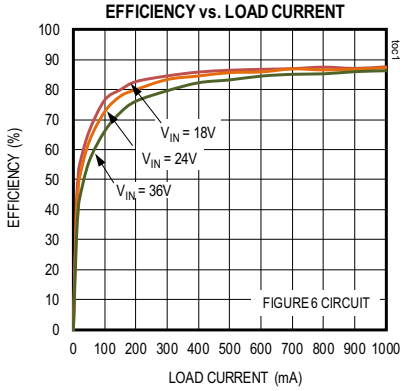
($V_{IN}$ = 24V, $V_{EN/UVLO}$ = 2V, $V_{OVI}$ = 0V, $R_{RT}$ = 49.9kΩ, $C_{INTVCC}$ = 2.2µF to PGND; $V_{PGND}$ = $V_{SGND}$ = 0V, NDRV = SS = VCM = COMP = OPEN, CS = PGND, $V_{IN}$ to FB = 0V, $R_{SET}$ = 10kΩ, $R_{TC}$ = 27.5K, $R_{RIN}$ = 60kΩ,$T_A$ = $T_J$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = $T_J$ = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

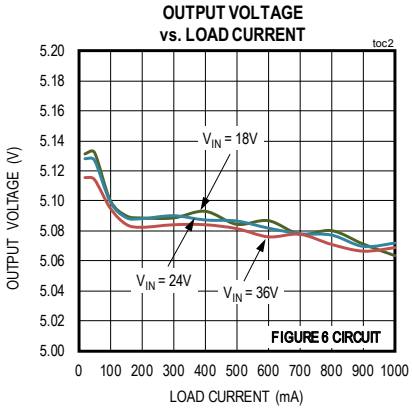
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| COMP Source Current | $I_{COMP\_SOURCE}$ | $V_{COMP}$ = 2V and $V_{SET}$ = 0.8V | 95 | 136 | 190 | µA |
| COMP Sink Current | $I_{COMP\_SINK}$ | $V_{COMP}$ = 2V and $V_{SET}$ = 1.2V | 95 | 136 | 190 | µA |
| MAX COMP Voltage | $V_{COMPH}$ | $R_{SET}$ = 8kΩ | | 2.9 | | V |
| MIN COMP Voltage | $V_{COMPL}$ | $R_{SET}$ = 12kΩ | | 1.55 | | V |
| COMP-to-CS Gain | ACS-PWM | $\Delta V_{COMP}/\Delta V_{CS}$ | 10.0 | 10.3 | 10.7 | V/V |
| **VCM** | | | | | | |
| VCM Pullup Current | | VCM = PGND | 9.4 | 10 | 10.6 | µA |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal-Shutdown Threshold | $T_{SHDNR}$ | Temperature rising | | +160 | | °C |
| Thermal-Shutdown Hysteresis | $T_{SHDNHY}$ | | | +20 | | °C |

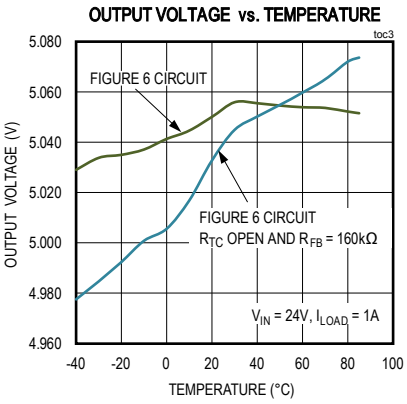
**Note 2:** Limits are 100% tested at $T_A$ = +25°C. Limits over the temperature range and relevant supply voltage range are guaranteed by design and characterization.

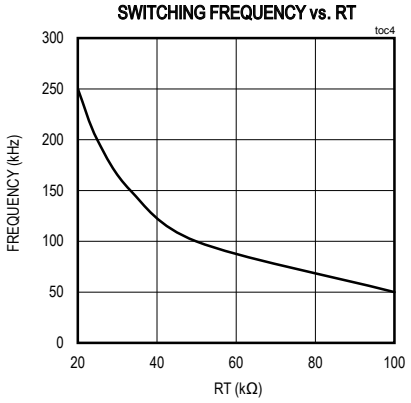
## Typical Operating Characteristics

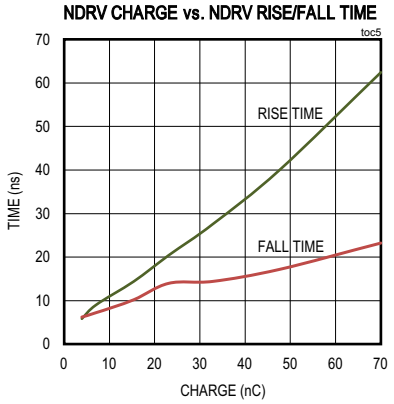
($V_{IN}$ = 24V, $V_{EN/UVLO}$ = +2V, $V_{OVI}$ = SGND, $C_{VIN}$ = 1uF, $C_{INTVCC}$ = 2.2µF, $T_A$ = +25°C, unless otherwise noted.)

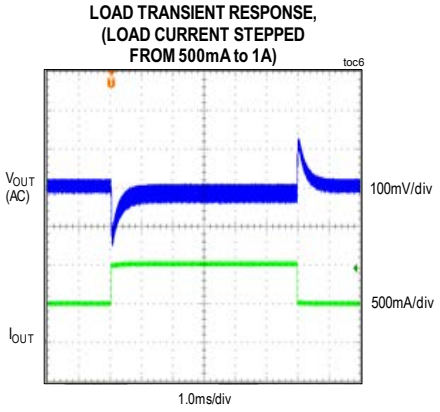


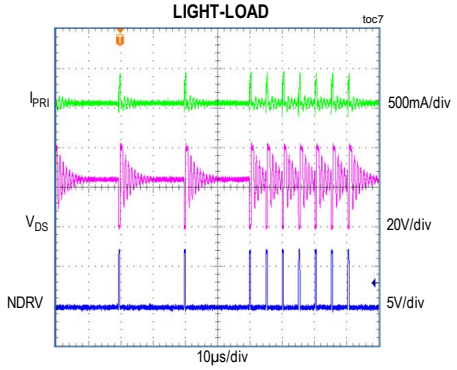



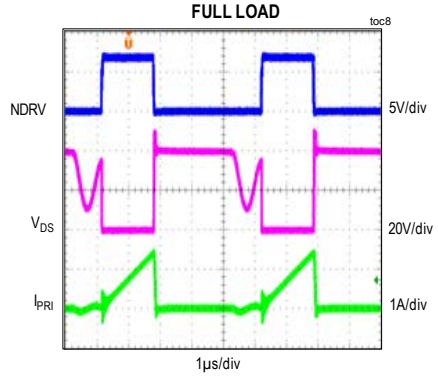
## Typical Operating Characteristics (continued)

($V_{IN}$ = 24V, $V_{EN/UVLO}$ = +2V, $V_{OVI}$ = SGND, $C_{VIN}$ = 1uF, $C_{INTVCC}$ = 2.2µF, $T_A$ = +25°C, unless otherwise noted.)

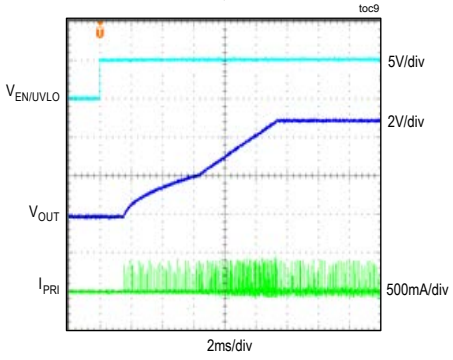
STEADY STATE WAVEFORMS
LIGHT-LOAD



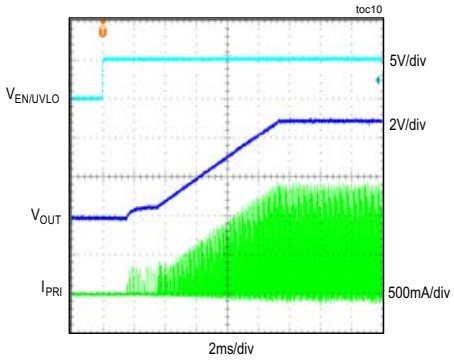

STEADY STATE WAVEFORMS
FULL LOAD



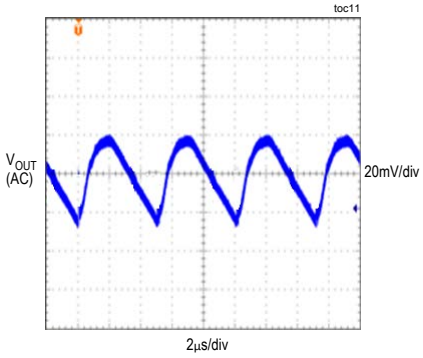

SOFT-START, LIGHT LOAD



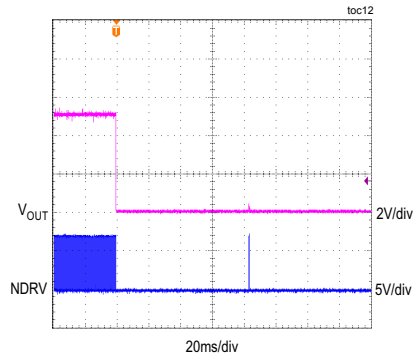

SOFT START, FULL LOAD



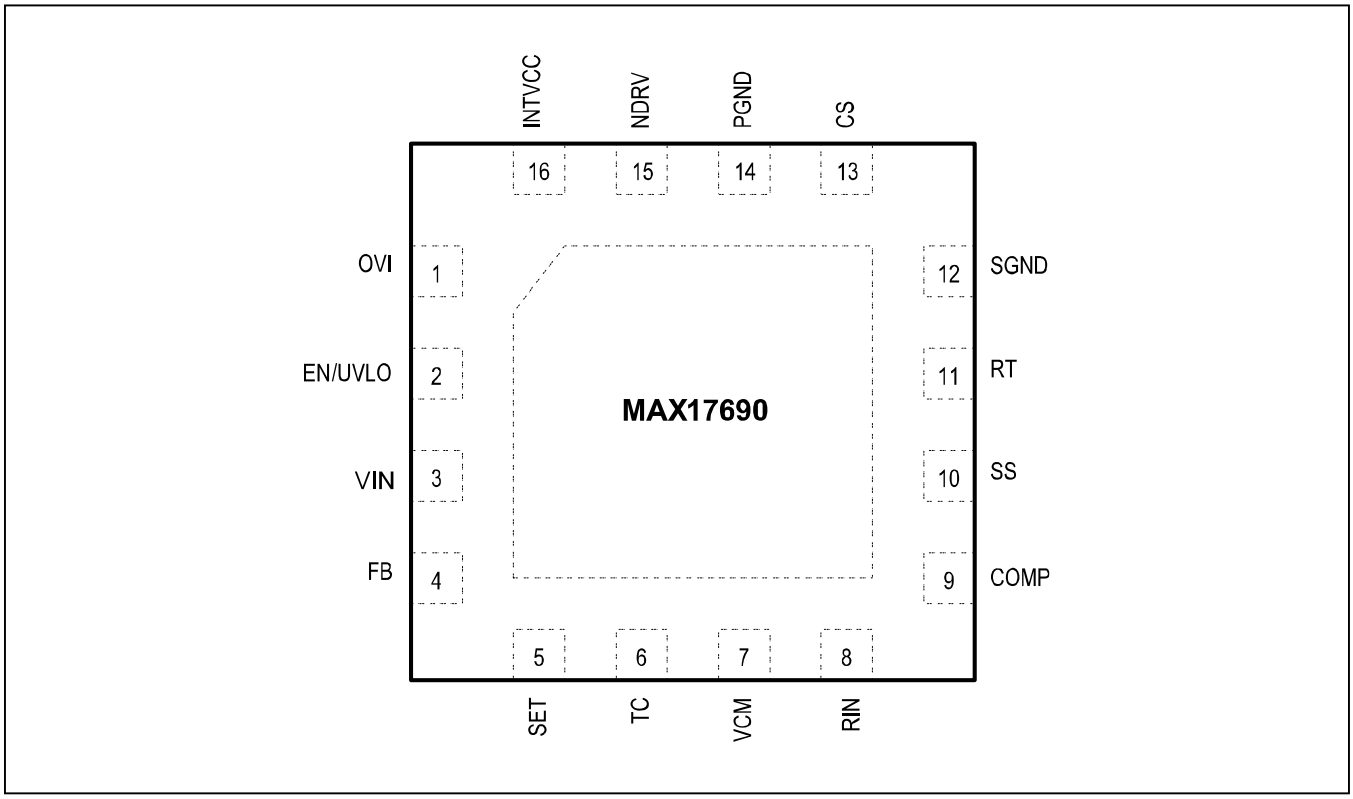

OUTPUT VOLTAGE RIPPLE
FULL LOAD




OVERLOAD PROTECTION



## Pin Configuration



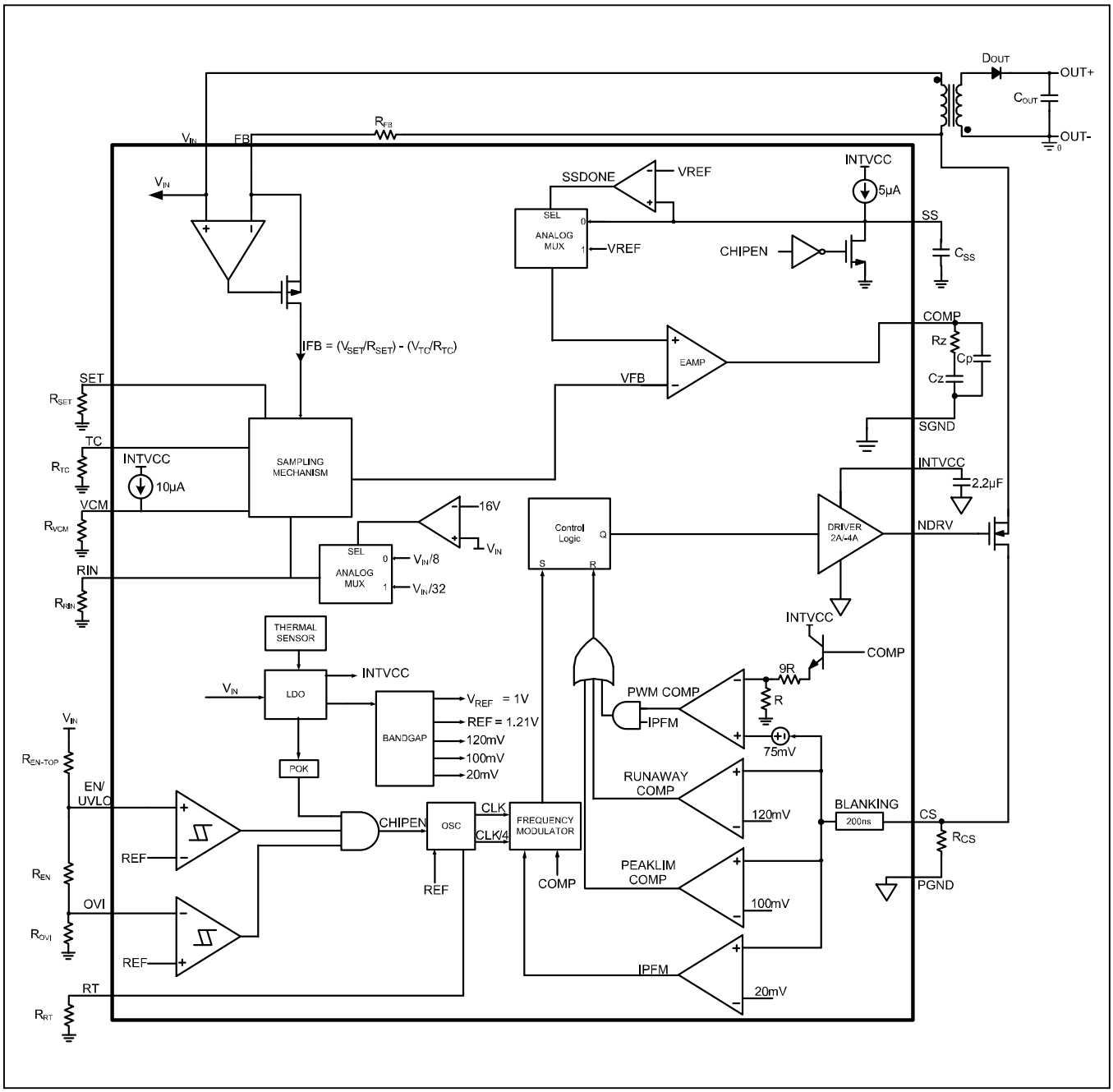

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | OVI | Input Overvoltage Detection. Connect a resistive-divider between the input supply, OVI, and SGND to set the input overvoltage threshold. The MAX17690 stops switching when the voltage at the OVI pin exceeds 1.215V and resumes switching when the voltage at the OVI pin falls below 1.1V. |
| 2 | EN/UVLO | Enable/Undervoltage Lockout Pin. Connect a resistive-divider between the input supply, EN/UVLO, and SGND to set the input turn-on threshold. The MAX17690 starts switching when the voltage at the EN/UVLO pin exceeds 1.215V and stops switching when the voltage at the EN/UVLO pin falls below 1.1V. |
| 3 | VIN | Input Supply Voltage. The input supply voltage range is 4.5V to 60V. This pin acts as a reference pin for the feedback circuitry connected to the FB pin. Connect a minimum of 1µF ceramic capacitor between the VIN pin and SGND. |
| 4 | FB | Feedback input for sensing the reflected output voltage during Flyback period. See the *Selection of $R_{IN}$, $R_{FB}$, and $R_{SET}$ Resistor* section for selecting an appropiate $R_{FB}$ resistor. |
| 5 | SET | Input for the External Ground-Referred Reference Resistor. Connect a 10kΩ resistor from the SET pin to SGND and place as close as possible to the MAX17690 IC. |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 6 | TC | Output Voltage Temperature Compensation. Connect the resistor $R_{TC}$ from the TC pin to SGND to set the temperature compensation. Current through TC pin is given by $0.55/R_{TC}$. |
| 7 | VCM | Common-Mode Voltage Selector for Internal Zero Current Detector Block. Connect a resistor $R_{VCM}$ from the VCM pin to SGND. See the *Selection of $R_{VCM}$ Resistor* section for selecting an appropriate $R_{VCM}$ resistor. |
| 8 | RIN | A current proportional to $V_{IN}$ flows through RIN resistor. Connect a resistor $R_{RIN}$ from the RIN pin to SGND. |
| 9 | COMP | Error Amplifier Output. Connect the frequency compensation network between COMP and SGND. |
| 10 | SS | Soft-Start. Connect a capacitor $C_{SS}$ from the SS pin to SGND to program the soft-start time interval. Pullup current at this pin is 5µA. |
| 11 | RT | Switching Frequency Programming Resistor. Connect a resistor $R_{RT}$ from RT to SGND to set the PWM switching frequency. This pin is regulated to 1.215V. See the *Switching Frequency* section for selecting an appropriate $R_{RT}$ resistor. |
| 12 | SGND | Signal Ground. |
| 13 | CS | Current Sense Input. See the *Setting Peak Current Limit* section for selecting an $R_{CS}$ resistor. |
| 14 | PGND | Power Ground. |
| 15 | NDRV | Driver Output. Connect this pin to the external MOSFET gate. Switches between INTVCC to PGND. |
| 16 | INTVCC | Linear Regulator Output and Driver Input. Connect a minimum of 2.2µF bypass capacitor from INTVCC pin to PGND as close as possible to the MAX17690 IC. This pin is typically regulated to 7V. |
| | EP | Exposed Pad. Connect this pin to the signal ground plane. |

## Functional Diagram



## Detailed Description

For low and medium-power applications, the flyback converter is the preferred choice due to its simplicity and low cost. However, in isolated applications, the use of optocoupler or auxiliary winding for voltage feedback across the isolation boundary increases the number of components, and design complexity. The MAX17690 eliminates the optocoupler or auxiliary winding, and achieves ±5% output voltage regulation over line, load, and temperature variations.

The MAX17690 implements an innovative algorithm to sample and regulate the output voltage by primary-side sensing. During the flyback period, the reflected voltage across the primary winding is the sum of output voltage, diode forward voltage and the drop across transformer parasitic elements, multiplied by the primary-secondary turns ratio. By sampling and regulating this reflected voltage close to the secondary zero current, the algorithm minimizes the effect of transformer parasitics and the diode forward voltage on the output voltage regulation.

### Supply Voltage

The IC supports a wide operating input voltage range from 4.5V to 60V. The MAX17690 regulates the FB pin to the voltage sensed on the VIN pin during the flyback period, thus resulting in a current in $R_{FB}$ that is proportional to the reflected voltage on the primary winding. This current is used by the MAX17690 as a feedback signal for output voltage regulation. Therefore, the VIN pin should be directly connected to the input supply with a minimum of 1µF ceramic capacitor between VIN pin and SGND, placed as close to the IC as possible for robust operation.

### EN/UVLO and OVI

This device's EN/UVLO pin serves as an enable/disable input, as well as an accurate programmable input UVLO pin. The MAX17690 do not commence startup operation until the EN/UVLO pin voltage exceeds 1.215V (typ). The MAX17690 turns-off if the EN/UVLO pin voltage falls below 1.1V (typ). A resistor-divider from $V_{IN}$ to SGND can be used to divide and apply a fraction of the input voltage ($V_{IN}$) to the EN/UVLO pin. The values of the resistor-divider can be selected so that the EN/UVLO pin voltage exceeds the 1.215V (typ) turn-on threshold at the desired input bus voltage. The same resistor-divider can be modified with an additional resistor ($R_{OVI}$) to implement input overvoltage protection in addition to the EN/UVLO functionality, as shown in Figure 1. When the voltage at the OVI pin exceeds 1.215V (typ), the device stops switching. The device resumes switching operations only if the voltage at the OVI pin falls below 1.1V (typ). For given values of startup input voltage ($V_{START}$) and input overvoltage-protection voltage ($V_{OVI}$), the resistor values for the divider can be calculated as follows, assuming a 10kΩ resistor for $R_{OVI}$:

$$R_{EN} = R_{OVI} \times \left[ \frac{V_{OVI}}{V_{START}} - 1 \right]$$

Where $R_{OVI}$ is in kΩ, while $V_{START}$ and $V_{OVI}$ are in volts

$$R_{EN-TOP} = \left[ R_{OVI} + R_{EN} \right] \times \left[ \frac{V_{START}}{1.215} - 1 \right]$$

Where $R_{EN}$ , $R_{OVI}$ is in kΩ, while $V_{START}$ is in volts.

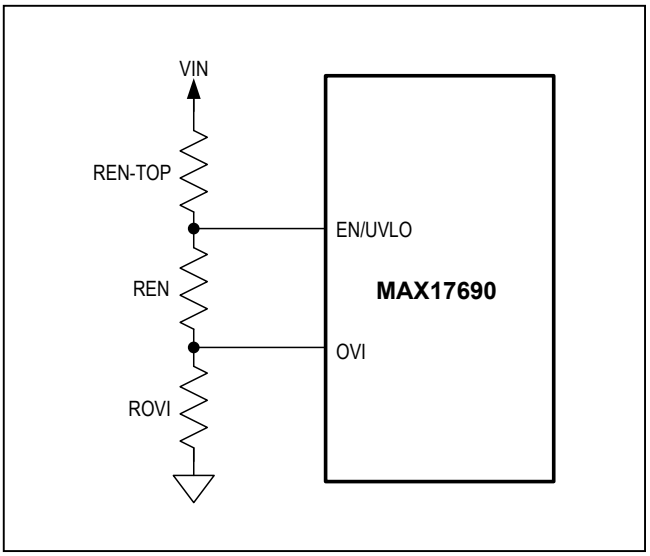



*Figure 1. Programming EN/UVLO and OVI*

## INTVCC

The $V_{IN}$ powers internal LDO of the MAX17690. The regulated output of the LDO is connected to the INTVCC pin. The LDO output voltage is 7V (typ). Connect a 2.2µF (min) ceramic capacitor between the INTVCC and PGND pins for the stable operation over the full temperature range. Place this capacitor as close as close possible to the IC. Although there is no need for an auxiliary winding for the voltage feedback, for some applications with input voltages greater than 8V, an additional winding used to overdrive the INTVCC may improve overall system efficiency. The auxiliary winding should be designed to output a voltage between 8V and 16V to ensure that the internal LDO turns off and the IC is supplied from the auxiliary winding output. The typical circuit for overdriving the INTVCC is shown in Figure 2.

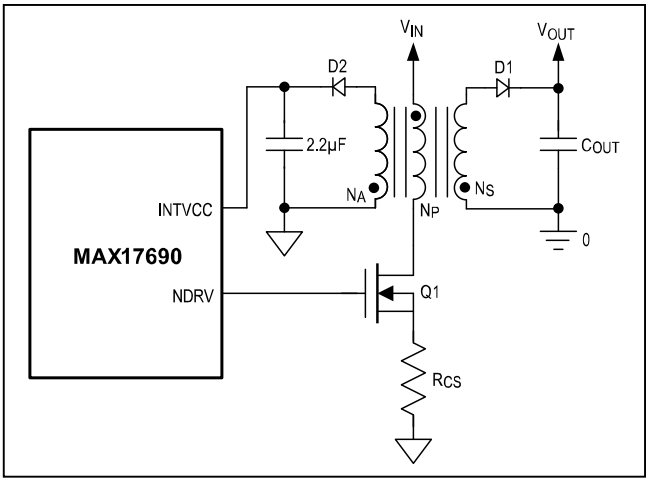



*Figure 2. INTVCC Pin Configuration.*

## Programming Soft-start time

The capacitor connected between the SS pin to SGND programs the soft-start time. Internally generated 5µA of precise current source charges the soft-start capacitor. When the EN/UVLO voltage is above 1.215V (typ), the device initiates a soft-start sequence. During the soft-start time, the SS pin voltage is used as a reference for the internal error amplifier. The soft-start feature reduces the input inrush current during startup. The reference ramp-up allows the output voltage to increase monotonically from zero to the target output value.

$$C_{SS} = 5 \times t_{SS}$$

where,

$C_{SS}$ is the soft-start capacitor in nF

$t_{SS}$ is the soft-start time in ms

## Switching Frequency

The MAX17690 switching frequency is programmable between 50kHz and 250kHz with a resistor $R_{RT}$ connected between RT and SGND. Based on the sampling algorithm requirements, for the given minimum and maximum input voltage the maximum switching frequency is determined by,

$$F_{SW} \le \left( \frac{720000 \times D_{MAX} \times V_{IN\ MIN}}{V_{IN\ MAX}} \right) \text{ where}$$

$$D_{MAX} = \left( \frac{V_{IN\ MAX}}{V_{IN\ MAX} + (2 \times V_{IN\ MIN})} \right)$$

where,

$V_{IN\ MIN}$ is the minimum Input Voltage in Volts

$V_{IN\ MAX}$ is the maximum Input Voltage in Volts

$F_{SW}$ is the switching frequency in Hz.

$D_{MAX}$ is the maximum operating duty cycle. If the calculated $D_{MAX}$ is > 0.65, then choose $D_{MAX}$ = 0.65

Use the following formula to determine the appropriate value of $R_{RT}$ to program the selected $F_{SW}$, $D_{MAX}$

$$R_{RT} = \frac{5 \times 10^6}{F_{SW}}$$

where,

$R_{RT}$ is resistor value in kohm

$F_{SW}$ is the switching frequency in Hz

## Selection of $R_{IN}$, $R_{FB}$ and $R_{SET}$ Resistor

The MAX17690 uses the current in the feedback resistor ($R_{FB}$) placed between the FB pin and the drain node of the NMOSFET to sense the reflected output voltage during the primary turn-off time. Use below equations for selecting the appropriate values of $R_{SET}$ , $R_{FB}$ and $R_{IN}$ to set the desired output voltage and for proper output voltage sampling

$$R_{SET} = 10k\Omega$$

$$R_{FB} = \left( \frac{N_P}{N_S \times 100 \times 10^{-6}} \right) \left( (V_{OUT} + V_D) + \frac{0.55 \times (\delta V_D / \delta T)}{\delta V_{TC} / \delta T} \right)$$

where,

$R_{FB}$ is the feedback resistor value in Ohm

$V_{OUT}$ is the desired output voltage in Volts

$N_P/N_S$ is the primary-to-secondary turns ratio of the transformer and its value is determined in the Transformer Magnetizing inductance and Turns Ratio section

$V_D$ is the forward voltage drop of the secondary rectifier diode in Volts

$\delta V_D/\delta T$ is the temperature coefficient of the secondary rectifier diode in mV/°C and

$\delta V_{TC}/\delta T$ =1.85mV/°C

$$R_{IN} = 0.6 \times R_{FB}$$

Where, $R_{IN}$ and $R_{FB}$ resistor values are in Ω

In practice, due to the drop across the secondary leakage inductance of the transformer and the error caused by the difference between the actual $V_D$ and the $V_D$ used to calculate the $R_{FB}$, the measured output voltage may deviate from the target output voltage. Use below equations to readjust the output voltage to the desired value,

$$R_{FB(NEW)} = \frac{V_{0(TARGET)}}{V_{0(MEASURED)}} \times R_{FB}$$

$$R_{RIN(NEW)} = 0.6 \times R_{FB(NEW)}$$

## Selection of $R_{VCM}$ Resistor

The device generates an internal voltage proportional to the on-time Volt-seconds, to determine the correct sampling instant for the reflected output voltage on primary winding during the off-time. The $R_{VCM}$ resistor is used to scale this internal voltage to the acceptable internal voltage limits. Follow the steps below to select the $R_{VCM}$ resistor,

1) Using the below formula, calculate the scaling constant ($K_C$)

$$K_C = \frac{(100\mu \times (1 - D_{MAX}))}{(F_{SW} \times 3 \times 10^{-12})}$$

where $F_{SW}$ is in Hz.

2) From Table 1, choose the row that has the equal or higher value for $K_C$ with regard to the calculated $K_C$ in step 1. Select the $R_{VCM}$ resistor value from the corresponding row.

## Table 1. $R_{VCM}$ Resistor Selection

| S.NO | $K_C$ | $R_{VCM}$ (Ω) |
|---|---|---|
| 1 | 640 | 0 |
| 2 | 320 | 75k |
| 3 | 160 | 121k |
| 4 | 80 | 220k |
| 5 | 40 | Open |

For example, if the calculated $K_C$ is 100 then choose the row with $K_C$ equal to 160. Select the corresponding 121kΩ for the $R_{VCM}$ value.

## Temperature Compensation

The secondary diode forward voltage drop ($V_D$), has a significant negative temperature coefficient. To compensate for this, a positive temperature coefficient current source is internally connected to the SET pin. The voltage at the TC pin is regulated to 0.55V at room temperature. This voltage has a 1.85mV/°C positive temperature coefficient. The $R_{TC}$, a resistor connected between the TC pin and SGND sets the current $V_{TC}$ / $R_{TC}$ into the SET pin. The following equation is used to calculate the $R_{TC}$

$$R_{TC} = \left(\frac{1}{100\mu}\right)\left(0.55 + \frac{(V_{OUT} + V_D) \times (\delta V_{TC}/\delta T)}{(\delta V_D/\delta T)}\right)$$

where,

$\delta V_D/\delta T$ is the secondary diode's forward voltage temperature coefficient in mV/°C (this value should be taken from the diode data sheet or from the manufacturer of the diode)

$$\delta V_{TC}/\delta T = 1.85mV/°C$$

## Short-Circuit Protection/Hiccup

The device offers a hiccup scheme that protects and reduces power dissipation in the design under output short-circuit conditions. One occurrence of the runaway current limit or output voltage less than 70% of regulated voltage would trigger a hiccup mode that protects the converter by immediately suspending the switching for the period of 16,384 clock cycles. The runaway current limit is set at a $V_{CS-PEAK}$ of 120mV (typ).

## Applications Information

### Transformer Magnetizing inductance and Turns Ratio

Since the DCM is the recommended mode of operation for the MAX17690 based flyback converter, use the below equation to determine the appropriate value for the $L_{MAG}$,

$$L_{MAG} = \frac{0.4 \times (V_{IN\,MIN} \times D_{MAX})^2}{V_{OUT} \times I_{OUT} \times F_{SW}}$$

where,

$V_{OUT}$ is the desired output voltage in Volts

$I_{OUT}$ is the desired output current in Amps

$L_{MAG}$ is the transformer magnetizing inductance in Henry

$D_{MAX}$ is the maximum duty cycle, use the value calculated in Switching frequency section

$F_{SW}$ is the switching frequency in Hz, select the frequency equal to or less than the value calculated for the $F_{SW}$ in the switching frequency section.

For the selected $L_{MAG}$ and the $F_{SW}$, recalculate the operating duty cycle using the below formula

$$D = \frac{\sqrt{2.5 \times L_{MAG} \times V_{OUT} \times I_{OUT} \times F_{SW}}}{V_{IN\,MIN}}$$

The following equation is used to determine the value of K,

$$K = \frac{N_S}{N_P} = \frac{0.8 \times (V_{OUT}) \times (1 - D)}{V_{IN\,MIN} \times D}$$

To achieve ±5% voltage regulation over line, load and temperature, the leakage inductance should be limited to 1.5% to 2% of the transformer magnetizing inductance. Refer Table 2 for the list of standard transformers developed for different applications using the MAX17690.

### Setting Peak Current Limit

A current-sense resistor, connected between the source of the NMOSFET and PGND, sets the peak current limit. Use the following equation to calculate the value of $R_{CS}$

$$I_{LIM} = \sqrt{\frac{2.5 \times V_{OUT} \times I_{OUT}}{L_{MAG} \times F_{SW}}}$$

$$R_{CS} = \frac{0.08}{I_{LIM}}$$

where $I_{LIM}$ is the peak current through the NMOSFET

For the stable operation, the recommended minimum on-time ($T_{ON\,MIN}$) and the minimum off-time ($T_{OFF\,MIN}$) are 230ns(max) and 490ns(max) respectively. Use the below equations to check these values for the selected transformer magnetizing inductance, turns ratio and current sense resistor.

$$T_{ON\,MIN} = \frac{L_{MAG} \times 0.02}{R_{CS} \times V_{IN\,MAX}} \geq 230n$$

$$T_{OFF\,MIN} = \frac{K \times L_{MAG} \times 0.02}{R_{CS} \times V_{OUT}} \geq 490n$$

If the above conditions are not met, reduce the $F_{SW}$ and recalculate the $L_{MAG}$, K and $R_{CS}$. Repeat this step till the conditions given above for the $T_{ON\,MIN}$ and the $T_{OFF\,MIN}$ are satisfied.

## Table 2. Predesigned Transformers—Typical Specifications Unless Otherwise Noted

| TRANSFORMER PART NUMBER | SIZE (W x L x H) (mm) | $L_{PRI}$ (µH) | $L_{LEAK}$ (nH) | NPS (NP:NS) | $I_{SAT}$ (A) | $R_{PRI}$ (mΩ) | $R_{SEC}$ (mΩ) | MANUFACTURER | TARGET APPLICATION | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | INPUT (V) | OUTPUT |
| 750343122 | 13.3 x 15.2 x 11.4 | 27 | 300 | 3:1 | 1.8 | 0.075 | 0.02 | Wurth | 18–36 | 5V/1A |
| 750343077 | 13.4 x 17.7 x 12.7 | 6 | 150 | 1:2.4 | 6.5 | 0.021 | 0.22 | Wurth | 4.5–5.5 | +15V/250mA<br>-15V/150mA |
| 750342975 | 13.3 x 15.2 x 11.4 | 27 | 300 | 3:1 | 1.8 | 0.075 | 0.02 | Wurth | 18–36 | 5V/1A |
| 750343078 | 12.04 x 12.7 x 6.1 | 60 | 1500 | 1:1 | 1 | 0.25 | 0.32 | Wurth | 15–35 | 15V/0.17A |

### Minimum Load Requirement

The MAX17690 samples the reflected output voltage information on the primary winding during the time when the primary NMOSFET is turned-off, and energy stored during the on-time is being delivered to the secondary. It is therefore mandatory for the MAX17690 to switch the external NMOSFET to sample the reflected output voltage. A minimum packet of energy needs to be delivered to the output even during light load conditions, in order to sample and regulate the output voltage. This minimum deliverable energy creates a minimum load requirement on the output that depends on the minimum peak primary current. For a discontinuous Flyback converter, the load power $P_O$ is proportional to the square of the primary peak current($I_{pk\_pry}$).

$$P_O = 0.5 \times L_{MAG} \times I^2pk\_pry \times F_{SW} \times \eta$$

The minimum peak primary current directly depends on the selection of $R_{CS}$ value, since the minimum

MAX17690 primary peak current cannot go lower than

$$\frac{V_{CS\_MIN}}{R_{CS}} \quad \text{where } V_{CS\_MIN} = 20mV(typ).$$

At low output power levels that demand energy less than that corresponding to the minimum primary current, the MAX17690 modulates the switching frequency between $F_{SW}/4$ and $F_{SW}$ to adjust the energy delivered to the correct level required to regulate the output voltage. As the load current is lowered further, the MAX17690 spends more and more switching cycles at $F_{SW}/4$, until the device completely settles down at $F_{SW}/4$. At this point the MAX17690 has reached its minimum load condition, and cannot regulate the output voltage without this minimum load connected to the output. This small minimum load can easily be provided on the output by connecting a fixed resistor. In the absence of a minimum load, or a load less than the “minimum load” the output voltage will rise to higher values. To protect for this condition, a Zener diode of appropriate breakdown voltage rating may be installed on the output. Care should be taken to ensure that the Zener breakdown voltage is outside the output voltage envelope in both steady state and transient conditions.

Given that maximum load power corresponds to a $V_{CS\_MAX}$ = 100 mV, and noting that the deliverable load current is proportional to the square of the primary peak current in a discontinuous mode Flyback converter, $V_{CS\_MIN}$ = 20mV corresponds to a 4% of full load at 100% efficiency, and switching frequency of $F_{SW}$. Since the MAX17690 can drop its switching frequency to $F_{SW}/4$, the minimum load requirement reduces further to 1%. In practice, the efficiency is less than 100%, resulting in a minimum load requirement of less than 1%.

### Output Capacitor Selection

X7R ceramic output capacitors are preferred in industrial applications due to their stability over temperature. The output capacitor is usually sized to support a step load of 50% of the rated output current so that the output voltage deviation is contained to 3% of the rated output voltage. The output capacitance can be calculated as follows

$$C_{OUT} = \frac{I_{STEP} \times T_{RESPONSE}}{2 \times \Delta V_{OUT}}$$

$$T_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{F_{SW}}\right)$$

where,

$I_{STEP}$ is the load step

$T_{RESPONSE}$ is the response time of the controller

$\Delta V_{OUT}$ is the allowable output voltage dip

$f_C$ is the target closed-loop band-width, to be selected between 1/20 to 1/40 of the $F_{SW}$.

### Loop Compensation

The MAX17690 is compensated using an external resistor capacitor network on the COMP pin. The loop compensation network are connected as shown in Figure 3.

The loop compensation values are calculated as follows:

$$R_Z = 12500 \times R_{CS} \times \left[\frac{f_C}{f_P}\right] \sqrt{\frac{V_{OUT} \times I_{OUT}}{2 \times L_{PRI} \times F_{SW}}} \ \Omega$$

$$C_Z = \frac{1}{2\pi \times R_Z \times f_P} \text{ Farad}$$

$$C_P = \frac{1}{\pi \times R_Z \times F_{SW}} \text{ Farad}$$

where :

$$f_P = \frac{1}{\pi \times \frac{V_{OUT}}{I_{OUT}} \times C_{OUT}} \text{ Hz}$$

### Selection of Primary MOSFET

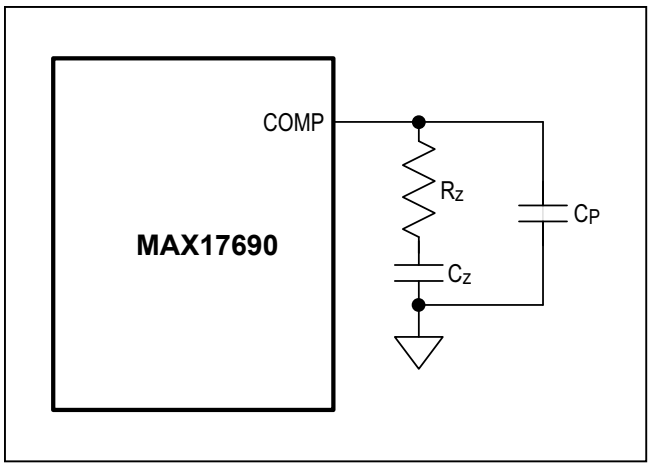



*Figure 3. Loop Compensation Arrangement*

MOSFET selection criteria includes maximum drain voltage, primary peak/RMS current, the on-state resistance ($R_{DS(ON)}$), total gate charge($Q_G$), the parasitic capacitance(Coss) and the maximum allowable power dissipation of the package without exceeding the junction temperature limits. The voltage seen by the MOSFET drain is the sum of the input voltage, the reflected secondary voltage on the transformer primary, and the leakage inductance spike. The MOSFET's absolute maximum VDS rating must be higher than the worst-case drain voltage,

$$V_{DS\,MAX} = V_{IN\,MAX} + \left(\frac{2.5 \times (V_{OUT} + V_D)}{K}\right)$$

RCD and RC snubber Circuit section covers the selection of snubber components to limit the drain-to-source voltage to $V_{DS\ MAX}$ value selected in the above equation.

The RMS current in the MOSFET can be calculated using the below formula.

$$I_{MOSFET}(RMS) = \sqrt{I_{LIM}{}^2 \times D / 3}$$

The conduction loss in the MOSFET can be calculated using the formula given below,

$$P_{CONDUCTION} = I_{MOSFET}\,2\,(RMS) \times R_{DS(ON)}$$

The designer can choose the MOSFET $R_{DS(ON)}$ based on the efficiency specification and the MOSFET package power dissipation capability. It is easy to find a MOSFET with low $R_{DS(ON)}$ that contributes to small percentage of full load power loss but it is also important to select low $Q_G$ MOSFET that require minimum losses at lighter loads. Use the below formula to calculate the driver loss,

$$P_{INTVCC} = INTVCC \times Q_G \times F_{SW}$$

## Selection of Secondary Diode

In a flyback converter, since the secondary diode is reverse biased when the primary MOSFET is conducting, the voltage stress on the diode is the sum of the output voltage and the reflected primary voltage. Choosing the diode with enough margin for the reverse blocking voltage as indicated in the below equation should preclude the use of a snubber.

$$V_{SEC,\,DIODE} = 1.5 \times (K \times V_{IN\,MAX} + V_{OUT})$$

Select a diode with low forward-voltage drop to minimize the power loss (given as the product of forward-voltage drop and the average output current) in the diode. Select fast-recovery diodes with a recovery time less than 50ns, or Schottky diodes with low junction capacitance for this purpose.

## RCD and RC Snubber Circuit

Ideally, the external MOSFET experiences a drain-source voltage stress equal to the sum of the input voltage and reflected output voltage across the primary winding during the off period of the MOSFET. In practice, parasitic inductors and capacitors in the circuit, such as leakage inductance of the flyback transformer and the MOSFET output capacitance cause voltage overshoot and ringing on the drain node of the MOSFET. Snubber circuits are used to limit the voltage overshoot to safe levels, within the voltage rating of the external MOSFET. The widely used RCD snubber circuit is shown in Figure 4 and the operating waveforms with the snubber circuit are shown in Figure 5.

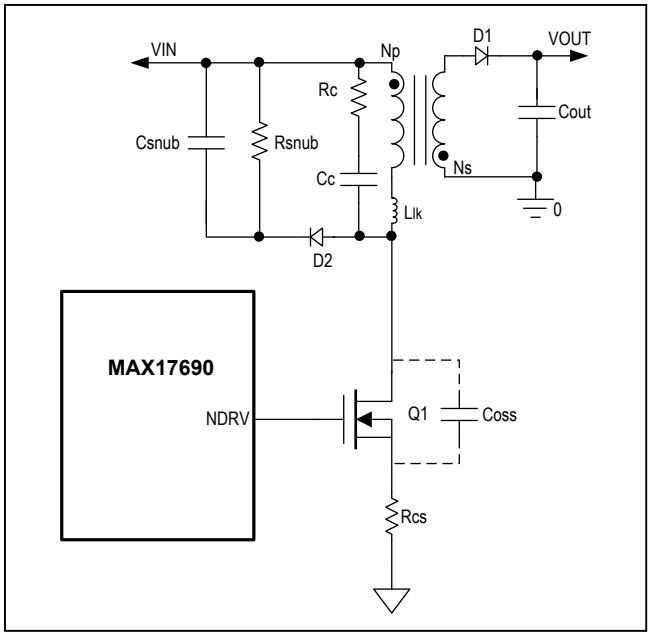



*Figure 4. RC and RCD Clamp Circuitry*

Use the following formula to calculate the snubber components,

$$P_{SNUB} = 0.833 \times L_{LK} \times (I_{LIM})^2 \times F_{SW}$$

$$R_{SNUB} = \frac{6.25 \times (V_{OUT} + V_D)2}{K^2 \times P_{SNUB}}$$

$$C_{SNUB} = \frac{2 \times L_{LK} \times I^2_{LIM} \times K^2}{(V_{OUT} + V_D)^2}$$

$$\text{where, } K = \frac{N_S}{N_P}$$

The reverse blocking voltage rating for the snubber diode (D2) is given by,

$$V_{D2} = V_{IN\,MAX} + \left(2.5 \times \frac{V_{OUT}}{K}\right)$$

The RCD clamp only limits the maximum voltage stress on the primary MOSFET during the clamping period but at the end of the clamping period due to the remaining stored energy in the leakage inductance, oscillations are observed on the drain node due to interaction between Llk and the drain node capacitance ($C_{PAR}$). The MAX17690 uses the drain voltage information to sample the output voltage and the earliest sampling instant is 350ns from the NDRV falling edge. Therefore, it is important to damp the drain node ringing within 350ns from the NDRV falling.

For designs, with dominant ringing on the drain node after 350ns from the NDRV falling, an additional RC snubber across the transformer primary winding is required. Use the following steps for designing an effective RC snubber,

1) Measure the ringing time period $t_1$ for the oscillations on the drain node immediately after the clamp period.

$$t_1 = 2\pi\sqrt{L_{LK} \times C_{PAR}}$$

2) Add a test capacitance on the drain node until the time period of this ringing is increased to 1.5 to 2 times of $t_1$. Start with a 100pF capacitor. With the added capacitance $C_D$ measure the new ringing time period ($t_2$),

$$t_2 = 2\pi\sqrt{L_{LK} \times (C_{PAR} + C_D)}$$

3) Use the following formula to calculate the drain node capacitance ($C_{PAR}$),

$$C_{PAR} = \frac{C_D}{\left(\left(\frac{t_2}{t_1}\right) - 1\right)}$$

4) Use the following formula to calculate the leakage inductance,

$$L_{LK} = \frac{t_1^2}{(4 \times \pi^2 \times C_{PAR})}$$

5) Now, use the following equations to calculate the RC snubber values,

$$C_C = 1.5 \text{ to } 2 \text{ times the } C_{PAR}$$

$$R_C = \sqrt{\frac{L_{LK}}{C_{PAR}}}$$

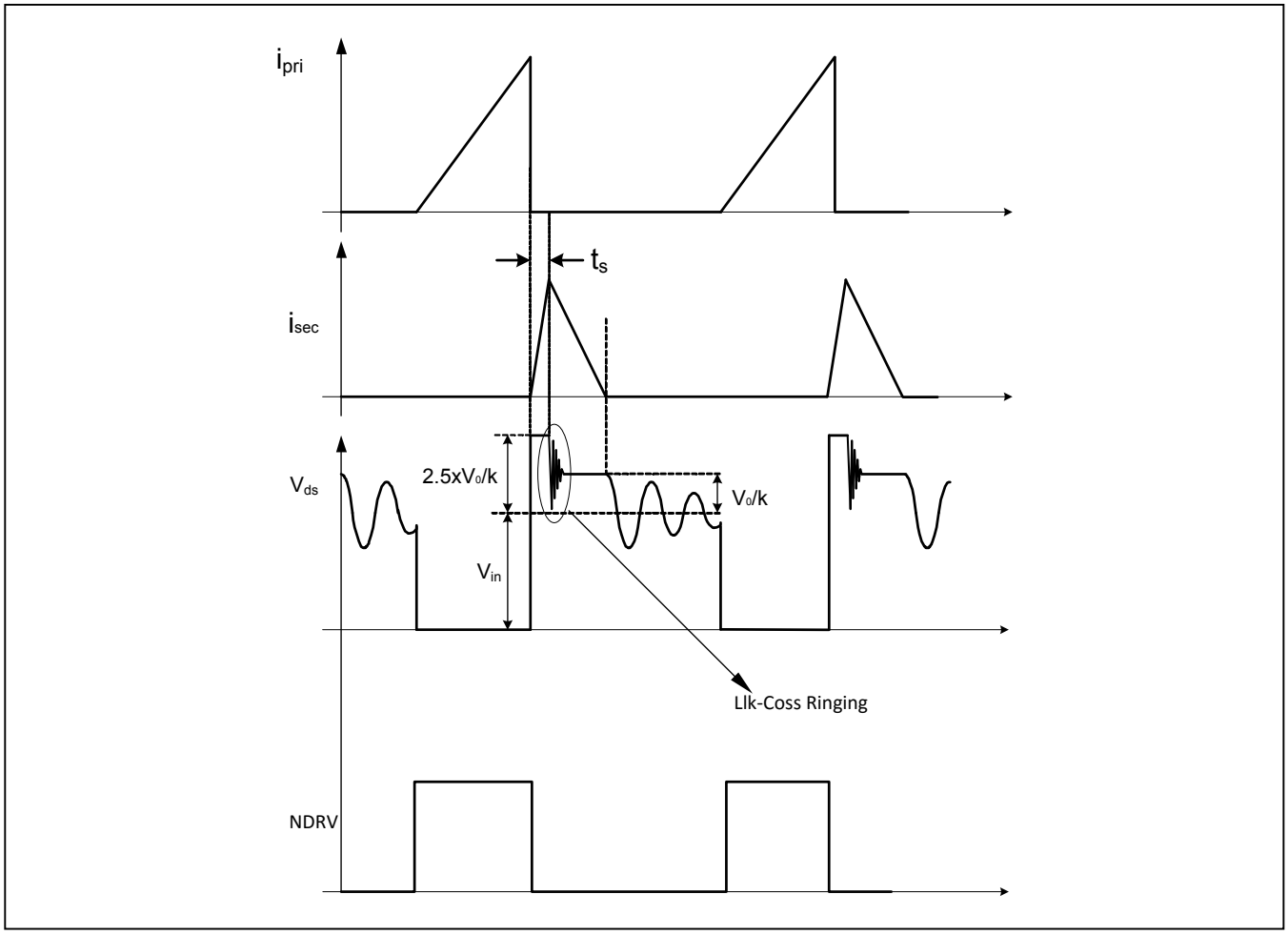



*Figure 5. Waveforms with RCD Clamp.*

## Design Example:

The following industrial specification is used to demonstrate the design calculations for the MAX17690 based flyback converter,

Input voltage range: 18V to 36V

Output voltage: 5V

Load current: 1A

### 1. Selection of Duty cycle

Plug-in the $V_{IN\ MIN}$ and $V_{IN\ MAX}$ from the above specification in the formula below to calculate the $D_{MAX}$,

$$D_{MAX} = \left( \frac{V_{IN\ MAX}}{V_{IN\ MAX} + (2 \times V_{IN\ MIN})} \right) = 0.5p.\ u$$

### 2. Switching Frequency

Use the below formula established earlier in this data sheet to calculate the maximum possible $F_{SW}$,

$$F_{SW} \leq \left( \frac{720000 \times D_{MAX} \times V_{IN\ MIN}}{V_{IN\ MAX}} \right)$$

$$F_{SW} \leq \left( \frac{720000 \times 0.5 \times 18}{36} \right)$$

$$F_{SW} \leq 180kHz$$

For the present application, the switching frequency is selected as 180kHz. The $R_{RT}$ is calculated for the selected $F_{SW}$,

$$R_{RT} = \frac{5 \times 10^6}{F_{SW}} \Omega$$

$$R_{RT} = \frac{5 \times 10^9}{180k} = 27.7k\Omega,$$

standard resistor of 27.4kΩ is selected for $R_{RT}$,

### 3. Transformer magnetizing inductance and Turns Ratio

Once the switching frequency and duty cycle are selected, the transformer magnetizing inductance($L_{MAG}$) can be calculated from the energy balance equation given in the data sheet,

$$L_{MAG} = \frac{0.4 \times (V_{IN\,MIN} \times D_{MAX})^2}{V_{OUT} \times I_{OUT} \times F_{SW}}$$

$$L_{MAG} = \frac{0.4 \times (18 \times 0.5)^2}{5 \times 1 \times 180k} = 36\mu H.$$

For the present design $L_{MAG}$ is chosen to be 36µH. Use the following equation to calculate the maximum duty cycle of the converter for the selected frequency and magnetizing inductance,

$$D = \frac{\sqrt{2.5 \times L_{MAG} \times V_{OUT} \times I_{OUT} \times F_{SW}}}{V_{IN\,MIN}}$$

$$D = \frac{\sqrt{2.5 \times 36\mu \times 5 \times 1 \times 180k}}{18} = 0.5 p.u$$

Calculate the required transformer turns ratio (K) using the below formula,

$$K = \frac{N_S}{N_P} = \frac{0.8 \times VOUT \times (1 - D)}{D \times V_{IN\,MIN}}$$

$$K = \frac{N_S}{N_P} = \frac{0.8 \times 5 \times (1 - 0.5)}{0.5 \times 18} = 0.222\ p.u$$

For the present design, K is chosen as 1:0.222

### 4. Selection of Current Sense Resistor

The transformer primary peak current value depends on the output power, $L_{MAG}$ and the $F_{SW}$. Use the below formula to calculate the peak current,

$$I_{LIM} = \sqrt{\frac{2.5 \times V_{OUT} \times I_{OUT}}{L_{MAG} \times F_{SW}}}$$

$$I_{LIM} = \sqrt{\frac{2.5 \times 5 \times 1}{36\mu \times 180k}} = 1.38A$$

The value of $R_{CS}$ decides the peak current limit and the runaway current limit. Use the below formula to select the $R_{CS}$,

$$R_{CS} = \frac{0.08}{I_{LIM}} = 57.9m\Omega$$

For the present application, a standard resistor of 56mΩ is selected.

### 5. Calculate the Min $T_{ON}$ and Min $T_{OFF}$

The MAX17690 has the minimum current sense voltage threshold limit at 20mV. For the selected current sense resistor, the minimum primary peak current allowed by the converter is,

$$I_{PY\,MIN} = \frac{0.02}{R_{CS}} = \frac{0.02}{0.056} = 0.357A$$

The minimum time required by the converter to reach the minimum primary peak current is,

$$T_{ON\,MIN} = \frac{L_{MAG} \times I_{PY\,MIN}}{V_{IN\,MAX}} = \frac{36\mu \times 0.357}{36} = 357ns$$

The calculated $T_{ON\,MIN}$ value (357ns) is higher than the MAX17690 $T_{ON\,MIN}$ (230ns). Similarly, the minimum off-time of the converter is calculated as,

$$T_{OFF\,MIN} = \frac{K \times L_{MAG} \times I_{PY\,MIN}}{V_{OUT}} = \frac{0.22 \times 36\mu \times 0.357}{5} = 565ns$$

The calculated $T_{OFF\,MIN}$ value (565ns) is higher than the MAX17690 $T_{OFF\,MIN}$ (490ns).

### 6. Selection of Secondary Diode

The maximum operating reverse-voltage rating must be higher than the sum of the output voltage and the reflected input voltage.

$$V_{SEC,\,DIODE} = 1.5 \times (K \times V_{IN\,MAX} + V_{OUT})$$

$$V_{SEC,\,DIODE} = 1.5 \times (0.22 \times 36 + 5) = 19.38V$$

The current rating of the secondary diode should be selected so that the power loss in the diode be low enough to ensure that the junction temperature is within limits. For the present design, SBR8U60P5 is selected as the secondary diode rectifier.

### 7. $R_{IN}$, $R_{FB}$, and $R_{SET}$ Resistor Selection

$$R_{SET} = 10k\Omega$$

$$R_{FB} = \left(\frac{N_P \times R_{SET}}{N_S}\right)\left((V_{OUT} + V_D) + \frac{0.55 \times (\delta V_D / \delta T)}{(\delta V_{TC} / \delta T)}\right)$$

$$R_{FB} = \left(\frac{1 \times 10k}{0.22}\right)\left((5 + 0.3) + \frac{0.55 \times 1}{1.84}\right) = 255k\Omega.$$

$R_{IN}$ = 0.6 x $R_{FB}$ = 153kΩ, a standard resistor 150kΩ is selected.

### 8. Temperature Compensation

For the selected secondary diode, from the forward characteristics of the diode data sheet note the diode temperature coefficient ( $\delta V_d/\delta T$ = 1mV/°C). To compensate the change in output voltage caused due to the diode temperature coefficient, select the $R_{TC}$ resistor to be

$$R_{TC} = \left(\frac{1}{100\mu}\right)\left(0.55 + \frac{(V_{OUT} + V_D) \times (\delta V_{TC} / \delta T)}{(\delta V_D / \delta T)}\right)$$

$$R_{TC} = \left(\frac{1}{100\mu}\right)\left(0.55 + \frac{(5 + 0.3) \times (1.84)}{1}\right) = 100k\Omega$$

### 9. Soft-Start Capacitor

For the desired soft-start time ($t_{SS}$ = 10ms), the SS capacitor is selected using

$$C_{SS} = 5 \times t_{SS} = 50nF$$

47nF is selected as the soft-start capacitor.

### 10. Selection of $R_{VCM}$ Resistor

Follow the below steps to select the $R_{VCM}$ resistor value.

1) Calculate the internal scaling factor:

$$K_C = \frac{100\mu \times (1 - D)}{3 \times F_{SW} \times 10^{-12}}$$

$$K_C = \frac{100 \times 10^{-6} \times (1 - 0.5)}{3 \times 180k \times 10^{-12}} = 92.6$$

From Table 3, choose the next higher value for the calculated $K_C$. $K_C$ = 160.

Select the resistor value corresponding to the choice of capacitor, as the $R_{VCM}$. $R_{VCM}$ = 121kΩ

### 11. MOSFET Selection

The voltage on the MOSFET drain is the sum of the input voltage, the reflected secondary voltage on the transformer primary, and the leakage inductance spike.

## Table 3. $R_{VCM}$ Resistor Selection

| $K_C$ | $R_{VCM}$ (KΩ) |
|---|---|
| 640 | 0 |
| 320 | 75 |
| 160 | 121 |
| 80 | 220 |
| 40 | Open |

The MOSFET's absolute maximum VDS rating should be selected

$$V_{DS\,MAX} = V_{IN\,MAX}\left(\frac{2.5 \times (V_{OUT} + V_D)}{K}\right)$$

$$V_{DS\,MAX} = 36 + \left(\frac{2.5 \times (5 + 0.3)}{0.22}\right) = 96.2V$$

For this application, the SIR698DP-T1-GE3 is selected as the primary MOSFET.

### 12. Output Capacitor Selection

The output capacitor is chosen to have 3% output voltage deviation for a 50% load step of the rated output current. The bandwidth is usually selected in the range of $F_{SW}$/20 to $F_{SW}$/40. For the present design, the bandwidth is chosen as 8kHz.

$$T_{RESPONSE} \cong \left(\frac{0.33}{F_C} + \frac{1}{F_{SW}}\right) = 46.8\mu s.$$

$$C_{OUT} = \frac{I_{STEP} \times T_{RESPONSE}}{2 \times \Delta V_{OUT}}$$

$$C_{OUT} = \frac{0.5 \times 46.8m}{2 \times 0.03 \times 5} = 78\mu F$$

Due to the dc-bias characteristics, the 100µF, 6.3V, 1210 capacitor offers 42.7µF at 5V. Hence two 100µF, 6.3V, 1210 capacitors are selected for the present design.

### 13. Loop Compensation

The loop compensation values are calculated as follows

$$\text{LOAD POLE } F_P = \frac{I_{OUT}}{\pi \times V_{OUT} \times C_{OUT}} = 800Hz$$

$$R_Z = 12500 \times R_{CS}\left(\frac{F_C}{F_P}\right)\sqrt{\frac{V_{OUT} \times I_{OUT}}{2 \times L_{PRI} \times F_{SW}}}$$

$$R_Z = 12500 \times 56m \times \left(\frac{8k}{800}\right)\sqrt{\frac{5 \times 1}{2 \times 36\mu \times 180k}} = 4.37k\Omega,$$

A standard 4.42kΩ is selected.

$$C_Z = \frac{1}{2\pi \times R_Z \times F_P} = 47nF$$

$$C_P = \frac{1}{\pi \times R_Z \times F_{SW}} = 470pF$$

## PCB Layout guidelines

Careful PCB layout is critical to achieve clean and stable operation. Follow the below guidelines for good PCB layout:

1) Keep the loop area of paths carrying the pulsed currents as small as possible. In flyback design, the high frequency current path from the VIN bypass capacitor through the primary-side winding, the MOSFET switch and sense resistor is a critical loop. Similarly, the high frequency current path for the MOSFET gate switching from the INTVCC capacitor through the source of the MOSFET and sense resistor is critical as well.
2) INTVCC bypass cap should be connected right across the INTVCC and PGND pins of the IC.
3) A bypass capacitor should be connected across to VIN and SGND pins, and should be placed close to the IC.
4) The exposed pad of the IC should be directly connected to SGND pin of the IC. The exposed pad should also be connected to SGND plane in other layers by means of thermal vias under the exposed pad so that the heat flows to the large “signal ground” (SGND) plane.
5) The $R_{FB}$ resistor trace length should be kept as small as possible.
6) The PGND connection from the INTVCC capacitor and the SGND plane should be star connected at the negative terminal of the current sense resistor.

To see the actual implementation of above guidelines, refer the MAX17690 evaluation kit layouts available at www.maximintegrated.com.

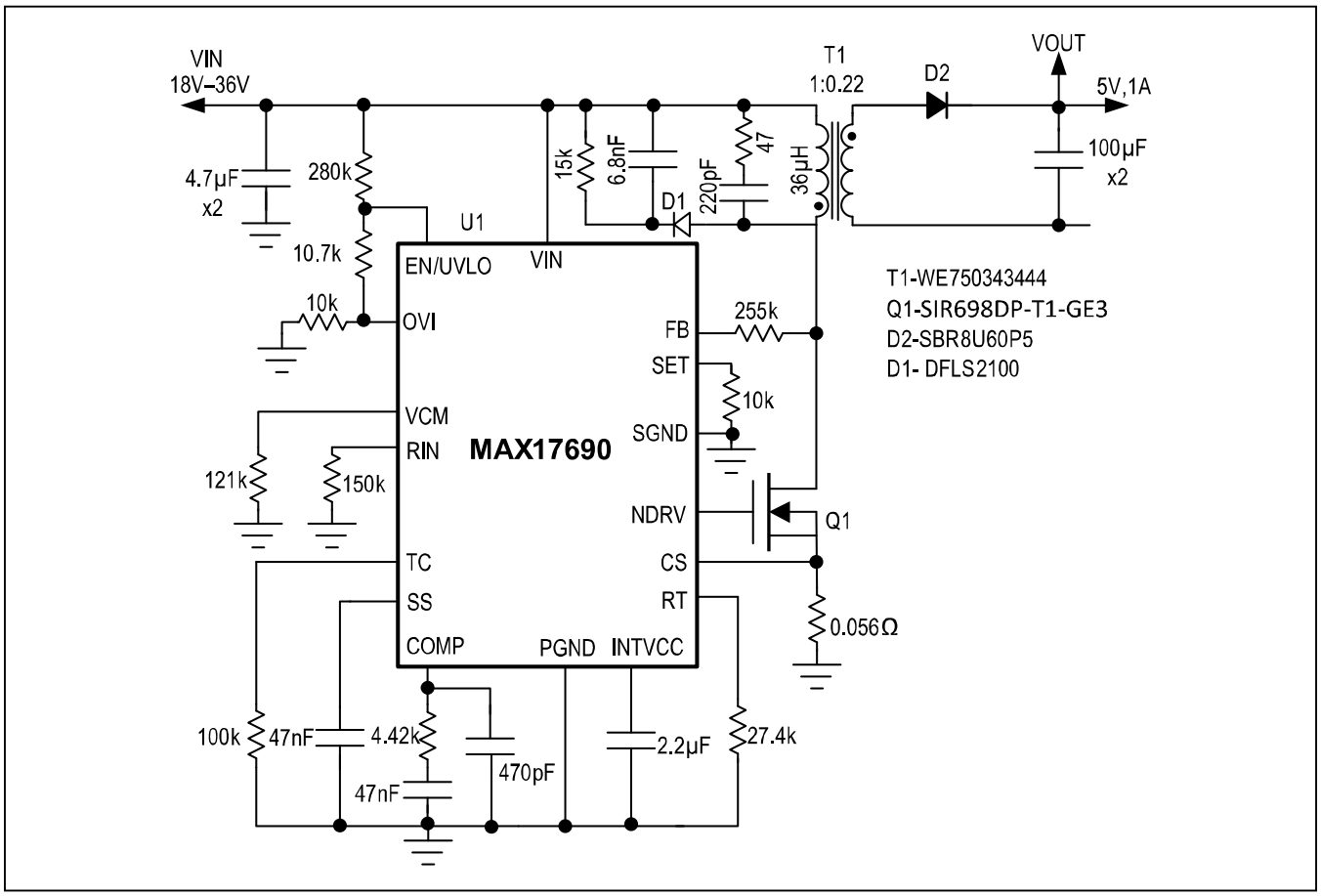



*Figure 6. 24V to 5V, 1A No-Opto Flyback Application Circuit*

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX17690ATE+ | -40°C to +125°C | 16 TQFN |

*+Denotes a lead(pB)-free/RoHS-compliant package.*

## Chip Information

PROCESS: CMOS

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 16 TQFN | T1633+4C | **21-0136** | **90-0031** |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 2/16 | Initial release | — |