CADEKA
Amplify the Human Experience

SPT5400

13-BIT, OCTAL VOLTAGE-OUTPUT DAC WITH PARALLEL INTERFACE

FEATURES

- Full 13-bit performance without external adjustments
- Eight DACs in one package
- Buffered voltage outputs
- Guaranteed monotonic to 13 bits
- Unipolar or bipolar output swing to ±4.5 V
- Output settling time of 7 µs to ±1/2 LSB
- Double-buffered digital inputs

APPLICATIONS

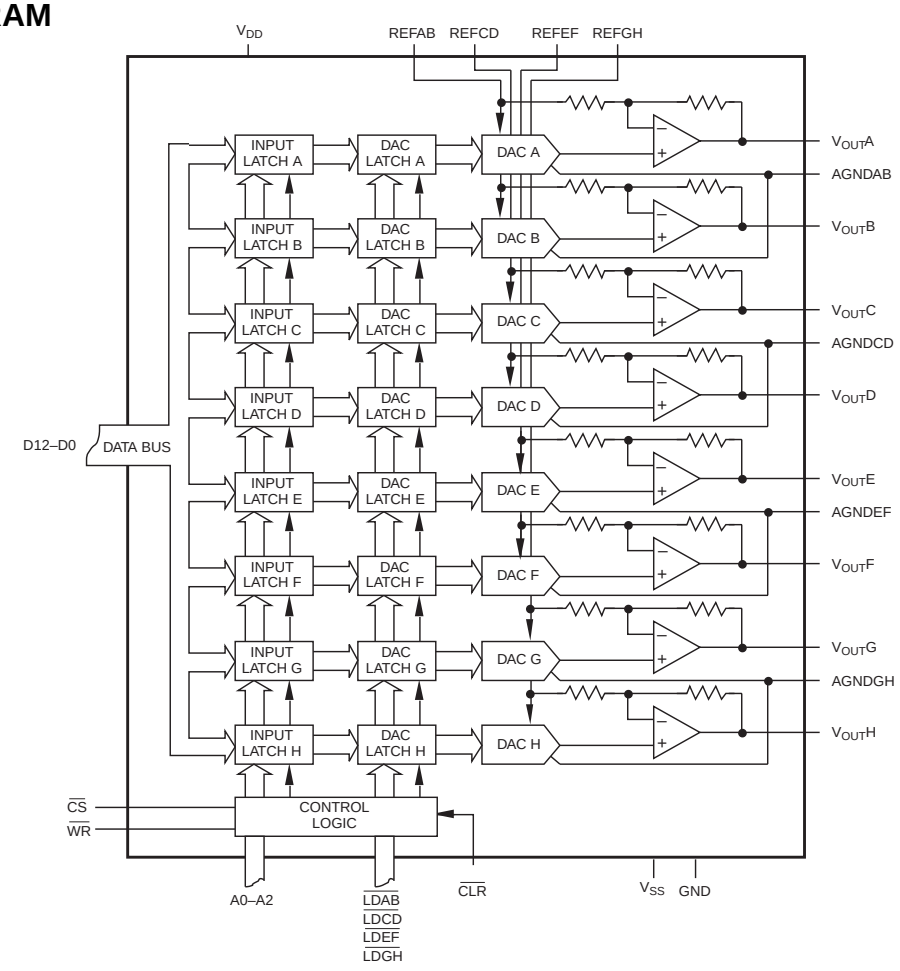
- Automatic test equipment
- Flat-panel displays
- Arbitrary function generators
- Instrumentation
- Process control

DESCRIPTION

The SPT5400 has eight 13-bit voltage output digital-to-analog converters on one chip. It operates from ±5 V power supplies and has maximum voltage output swings of up to ±4.5 V without the addition of external components. Novel circuit topology allows for a guaranteed monotonicity of 13 bits without the need for additional circuitry. The SPT5400 has four separate reference voltage inputs, one for each pair of DACs. Four separate analog ground pins allow for separate offset voltages for each DAC pair. Each DAC can be asynchronously loaded through a common 13-bit bus into a double-buffered set of latches. All logic inputs are TTL/CMOS compatible.

The SPT5400 is available in a 44-lead PLCC package over the commercial temperature range of 0 °C to +70 °C.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{DD} to GND ..... –0.3 to +6 V
V_{SS} to GND ..... –6 to +0.3 V
AGNDxx ..... (GND – 0.3 V) to (V_{DD} + 0.3 V)

Input Voltages

Digital Input Voltage to GND .. –0.3 V to (V_{DD} + 0.3 V)
REFxx ..... (AGNDxx – 0.3 V) to (V_{DD} + 0.3 V)
Maximum Current into REFxx Pin ..... ±10 mA

Output

V_{OUT}xx ..... V_{DD} to V_{SS}

Temperature

Operating Temperature, Ambient ..... 0 to +70 °C
Junction Temperature ..... +165 °C
Lead Temperature, (soldering 10 seconds) ... +300 °C
Storage Temperature ..... –65 to +150 °C
Power Dissipation ..... 1000 mW

Note 1: Operation at any Absolute Maximum Rating is not implied. Operation beyond the ratings may cause damage to the device. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

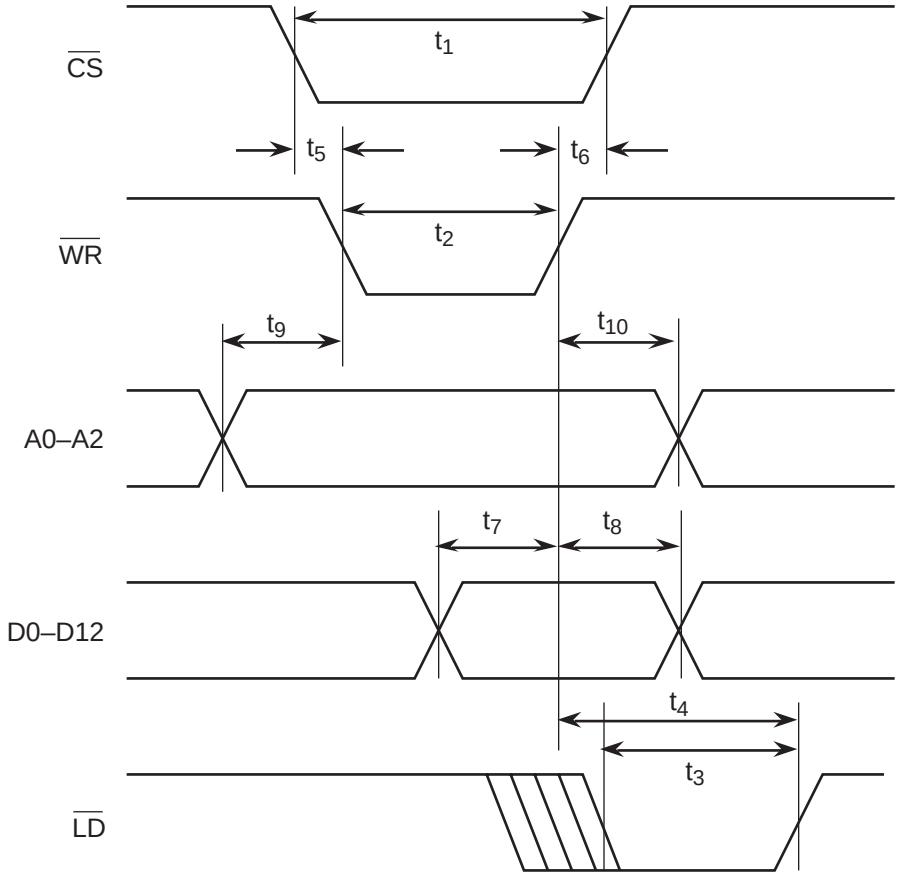
V_{DD} = +5 V, V_{SS} = –5 V, REFxx = 4.096 V, AGNDxx = GND = 0 V, R_L = 10 kΩ, C_L = 50 pF, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25 °C.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT5400 MIN	SPT5400 TYP	SPT5400 MAX	UNITS
DC Performance						
Resolution			13			Bits
Integral Linearity		VI		±0.5	±4.0	LSB
Differential Linearity	Guaranteed Monotonic	VI			±1.0	LSB
Zero Code Error[1]		VI		±10.0	±20	LSB
Gain Error[2]		VI		±1.0	±15	LSB
Power Supply Rejection Ratio[3]						
$\Delta Gain/\Delta V_{DD}$		VI			±0.0025	%/%
$\Delta Gain/\Delta V_{SS}$		VI			±0.0025	%/%
Load Regulation	R_L = ∞ to 10 kΩ	V		±0.4		LSB
Reference Input						
Ref Input Range[4,5]		IV	AGND		V_{DD}	V
Ref Input Resistance[5]		VI	5			kΩ
Analog Output						
Maximum Output Voltage		V		V_{DD} – 0.5		V
Minimum Output Voltage		V		V_{SS} + 0.5		V
Output Slew Rate		V		2.4		V/µs
Output Settling Time[6]	To ±1/2 LSB of Full Scale	V		7.0		µs
Digital Feedthrough		V		5		nV-s
Digital Crosstalk		V		50		nV-s
Digital Inputs (V_{DD} = 5 V ±5%)						
Input Voltage High		VI	2.4			V
Input Voltage Low		VI			0.8	V
Input Current (V_{IN} = 0 V or V_{DD})		VI			10.0	µA
Input Capacitance		IV			10	pF
Power Supplies						
Positive Supply Range (V_{DD})		VI	4.75		5.25	V
Negative Supply Range (V_{SS})		VI	–5.25		–4.75	V
Positive Supply Current		VI		15	25	mA
Negative Supply Current		VI		16	25	mA
Power Dissipation[7]		VI		155	250	mW

[1]Deviation of actual DAC output when all 0s are loaded to the DAC from the ideal output of –4.096 V.
[2]Deviation of actual DAC output span from the ideal span of 8.191 V.
[3]PSSR is tested by changing the respective supply voltage by ±5%.
[4]For best performance, REF should be greater than AGND + 2 V and less than V_{DD} – 0.6 V. The device operates with reference inputs outside this range, but performance may degrade.
[5]Reference input resistance is code dependent.
[6]Typical settling time with 1000 pF capacitive load is 8 µs.
[7]Does not include reference power.

TEST LEVEL CODES	TEST LEVEL	TEST PROCEDURE
All electrical characteristics are subject to the following conditions:	I	100% production tested at the specified temperature.
All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.	II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
	III	QA sample tested only at the specified temperatures.
	IV	Parameter is guaranteed (but not tested) by design and characterization data.
	V	Parameter is a typical value for information purposes only.
	VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 – Timing Diagram



NOTES:
1. All input rise and fall times are measured from 10% to 90% of +5 V. $t_R = t_F = 5$ ns.
2. If $\overline{LD}$ is activated while $\overline{WR}$ is low, $\overline{LD}$ must stay low for t_3 or longer after $\overline{WR}$ goes high.

Table I – Timing Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
$\overline{CS}$ Pulse Width Low	t_1	50			ns
$\overline{WR}$ Pulse Width Low	t_2	50			ns
$\overline{LD}$ Pulse Width Low	t_3	50			ns
$\overline{CLR}$ Pulse Width Low	t_4	100			ns
$\overline{CS}$ to $\overline{WR}$ Low	t_5	0			ns
$\overline{CS}$ High to $\overline{WR}$ High	t_6	0			ns
Data Valid to $\overline{WR}$ Setup	t_7	20			ns
Data Valid to $\overline{WR}$ Hold	t_8	0			ns
Address Valid to $\overline{WR}$ Setup	t_9	10			ns
Address Valid to $\overline{WR}$ Hold	t_{10}	0			ns

GENERAL CIRCUIT DESCRIPTION

The SPT5400 contains eight 13-bit, voltage-output DACs. It uses a novel circuit topology to convert the 13-bit digital inputs into equivalent output voltages that are proportionate to the applied reference voltages. The SPT5400 has four separate reference voltage (REFxx) and analog ground (AGNDxx) inputs for each DAC pair. The REFxx inputs allow for separate full-scale output voltages for each DAC pair. The AGNDxx inputs allow for separate offset voltages for each DAC pair.

VOLTAGE REFERENCE AND ANALOG GROUND INPUTS

The REFxx and AGNDxx inputs set the output range of the corresponding DAC pair. For a detailed description of the relationship between the DAC output range and the REFxx and AGNDxx input voltages, see the Analog Outputs section of this datasheet.

The reference input impedance is code dependent. It is at its highest value when the input code of the corresponding DAC pair is all 1s. It is at its lowest value when the input code is all 0s. Because the input impedance is code dependent, load regulation of the reference is critical.

MULTIPLYING OPERATION

Because the reference of the SPT5400 accepts both AC and DC signals, it can be used for multiplying applications. The REFxx inputs (which set the full-scale output voltage for the respective DACs) only accept positive voltages, so the multiplying operation is limited to two quadrants. Note that when applying AC signals to the reference, do not bypass the inputs.

DIGITAL INPUTS AND MICROPROCESSOR INTERFACE

All digital inputs are TTL/CMOS compatible. The SPT5400 is compatible with microprocessors having a minimum 13-bit-wide data bus. The microprocessor interface is double-buffered to allow all the DACs to be simultaneously updated.

DAC ADDRESSING AND LATCHING

Each DAC has an input latch that receives data from the data bus, and a DAC latch that receives data from the input latch. The address lines (A0–A2) for each DAC input latch are shown in table II. Data is transferred from the input latch to the DAC latch when $\overline{\text{LDXX}}$ is asserted. The analog output of each DAC reflects the data held in its corresponding DAC latch. In addition to being latched, data can be transferred to the DAC directly through transparent latches.

Table II – DAC Addressing

A2	A1	A0	Function
0	0	0	DAC A input latch
0	0	1	DAC B input latch
0	1	0	DAC C input latch
0	1	1	DAC D input latch
1	0	0	DAC E input latch
1	0	1	DAC F input latch
1	1	0	DAC G input latch
1	1	1	DAC H input latch

The control inputs of the SPT5400 are level triggered, and are shown in table III. The input latch is controlled by $\overline{\text{CS}}$ and $\overline{\text{WR}}$, and the transfer of data to the DAC latch is controlled by $\overline{\text{LDXX}}$. When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are low, the input latch is transparent. When $\overline{\text{LDXX}}$ is low the DAC latch is transparent. To avoid transferring data to the wrong DAC, the address lines (A0–A2) must be valid through the time $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are low. See the timing diagram for specific timing values. When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are high, the data is latched into the input latch. When $\overline{\text{LDXX}}$ is high, the data is latched into the DAC latch. If $\overline{\text{LDXX}}$ is low when $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are low, then it must be held low for t_3 or longer after $\overline{\text{CS}}$ or $\overline{\text{WR}}$ goes high.

When $\overline{\text{CLR}}$ is low, all DAC outputs are set to their corresponding AGNDxx. When $\overline{\text{CLR}}$ toggles from low to high, 1000hex is latched into all input and DAC latches.

Table III – Interface Truth Table

$\overline{\text{CLR}}$	$\overline{\text{LDXX}}$	$\overline{\text{WR}}$	$\overline{\text{CS}}$	Function
1	0	0	0	Both latches transparent
1	1	1	x	Both latches latched
1	1	x	1	Both latches latched
1	x	0	0	Input latch transparent
1	x	1	x	Input latch latched
1	x	x	1	Input latch latched
1	0	x	x	DAC latch transparent
0	x	x	x	All input and DAC latches at 1000hex, outputs at AGNDxx

DIGITAL CODE

The SPT5400 uses offset binary coding. Conversion to a 13-bit offset binary code from a 13-bit twos-complement code can be achieved by adding $2^{12} = 4096$.

POWER SUPPLY SEQUENCING

The required power-up sequence is as follows: V_{SS} (or V_{DD}) first, V_{DD} (or V_{SS}) second, and then REF_. The sequence in which V_{DD} and V_{SS} come up is not critical. However, REF_ must come up after V_{DD} and V_{SS} are established.

CADEKA strongly recommends that the digital input pins be driven only after V_{DD} and V_{SS} are established. Driving a digital input prior to establishing supplies will violate a condition outlined in the Input Voltages section (see the Absolute Maximum Ratings on page 2 of this data sheet) and cause damage to the part. If either REF_ or the digital inputs must come up before V_{DD} and V_{SS}, due to system constraints, limit the current to the REF_ or digital input pins to less than 1 mA.

This recommended power-up sequence must be executed in reversed order for power-down. It should be noted that none of the Absolute Maximum Rating conditions are violated during power-up and power-down.

ANALOG OUTPUTS

The voltage outputs to the SPT5400 are buffered internally by precision amplifiers with a 2.4 V/µs typical slew rate. The typical settling time to ±1/2 LSB, with a full-scale transition at the outputs, is 7 µs. Each DAC output is protected against a short to GND or AGNDxx. The typical short-circuit currents are 25 mA when the DAC is at positive full scale, and 2.5 mA when the DAC is at negative full scale.

BIPOLAR OUTPUT VOLTAGE RANGE (AGNDxx = 0 V)

For symmetrical bipolar operation, AGNDxx should be tied to the system ground. The relationship between the output voltage and the digital code is shown in table IV. The output voltage of the DAC ladder (VDAC) is multiplied by 2 and level-shifted by the reference voltage. The output voltage of the amplifier is given by the following equation:

$$V_{OUT} = 2(VDAC) - REFxx$$

Where VDAC is the voltage at the noninverting input of the amplifier and REFxx is the voltage at the reference input of the DAC.

With AGNDxx connected to the system ground, the output voltage of the DAC ladder is:

$$VDAC = (D/2^{13})REFxx$$

Where D is the numeric value of the DAC's binary input code.

Replacing VDAC in the equation gives the output voltage.

$$V_{OUT}xx = 2\left(\frac{D}{2^{13}}\right)(REFxx) - REFxx = REFxx\left(\frac{D}{2^{12}} - 1\right) = REFxx\left(\frac{D}{4096} - 1\right)$$

$$1\,LSB = REFxx\left(\frac{1}{4096}\right)$$

D ranges from 0 to 8191 (2^{13} –1).

Table IV – Input Code/Output Tables

Bipolar (AGNDxx = 0 V)

Input	Output
1 1111 1111 1111	+REFxx (4095/4096)
1 0000 0000 0001	+REFxx (1/4096)
1 0000 0000 0000	0 V
0 1111 1111 1111	–REFxx (1/4096)
0 0000 0000 0001	–REFxx (4095/4096)
0 0000 0000 0000	–REFxx

Positive Unipolar (AGNDxx = REFxx/2)

Input	Output
1 1111 1111 1111	+REFxx (8191/8192)
1 0000 0000 0000	+REFxx/2
0 0000 0000 0000	0 V

POSITIVE UNIPOLAR OUTPUT VOLTAGE RANGE (AGNDxx = REFxx/2)

For positive unipolar operation, AGNDxx should be set to REFxx/2. The relationship between the output voltage and the digital code is shown in table IV. For example, if a 4.096 V reference is used, AGNDxx should be offset by 2.048 V. This results in a unipolar output voltage of 0 to 4.0955 V, where 1 LSB = 500 µV. the maximum current out of any AGNDxx pin is:

$$I_{AGNDXX} = \left(\frac{REFxx - AGNDxx}{5\ k\Omega}\right)$$

CUSTOM OUTPUT VOLTAGE RANGE

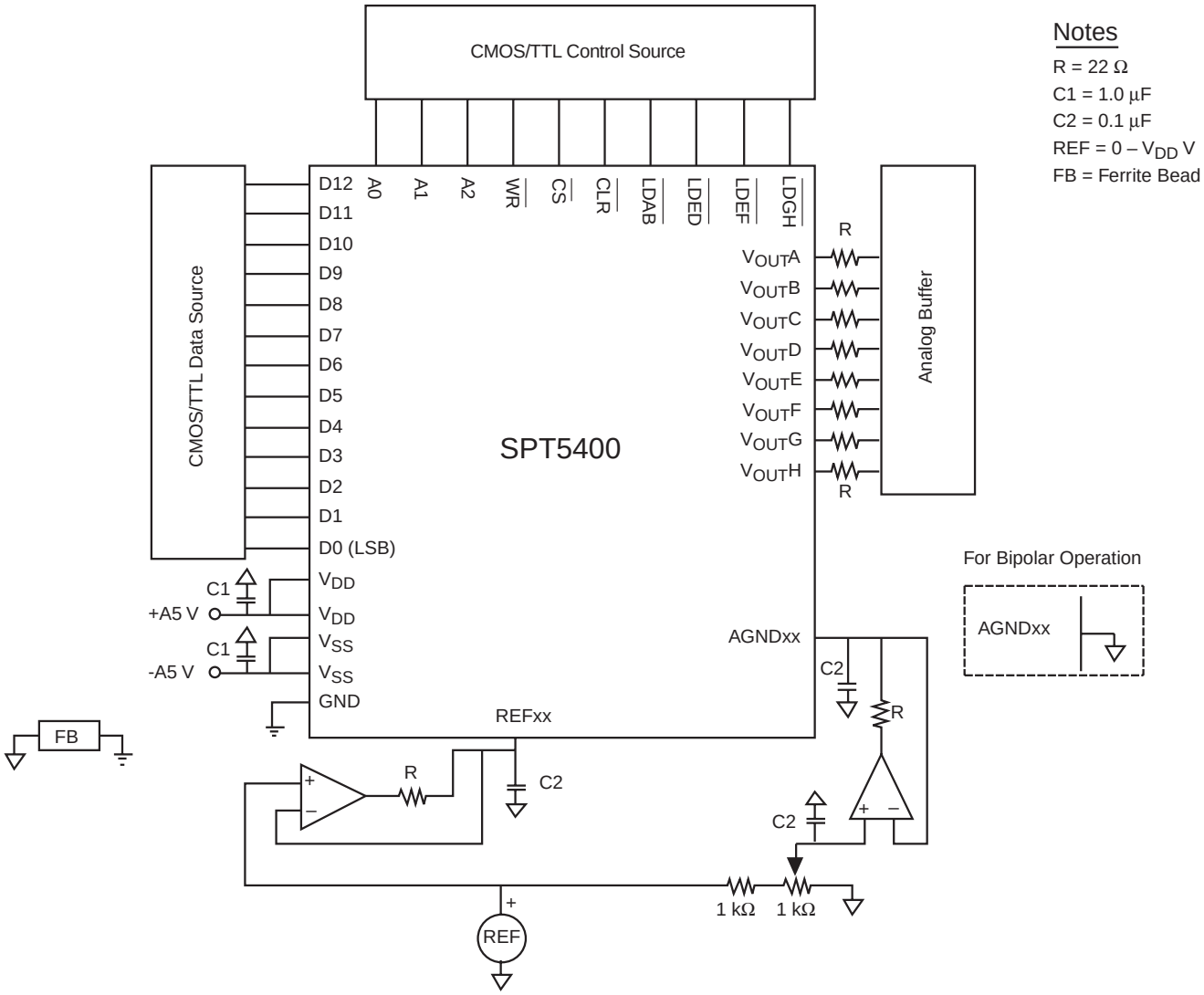
If the voltage at the REFxx input is higher than the voltage at the AGNDxx input, the AGNDxx inputs can be offset by any voltage within the supply rails. One way to achieve this is to add positive offset to AGNDxx by selecting the reference voltage and the voltage at AGNDxx such that the resulting output voltages do not come within ±0.5 V of the supply rails. Another way is to digitally offset AGNDxx by connecting one DAC output to one or more AGNDxx inputs. Note that a DAC output should not be connected to its own AGNDxx input.

The relationship between the reference, AGNDxx and output voltage is shown in table V.

Table V – Relationship between Reference, AGNDxx and Output

PARAMETER	BIPOLAR OPERATION (AGNDxx = 0 V)	POSITIVE UNIPOLAR OPERATION (AGND = REFxx/2)	CUSTOM OPERATION
Bipolar Zero Level or Unipolar Mid-Scale (Code = 1000000000000)	AGNDxx = 0 V	AGNDxx = REFxx/2	AGNDxx
Differential Reference Voltage (VDR)	REFxx	REFxx/2	REF – AGNDxx
Negative Full-Scale Output (Code = All 0s)	–REFxx	0 V	AGNDxx – VDR
Positive Full-Scale Output (Code = All 1s)	(4095/4096)(REFxx)	(8191/8192)(REFxx)	AGNDxx + (4095/4096)(VDR)
LSB Weight	(REFxx/4096)	(REFxx/8192)	(VDR/4096)
V_{OUT}xx as a Function of Digital Code (D, 0 to 8191)	((D/4096)–1)(REFxx)	(D/8192)(REFxx)	AGNDxx + ((D/4096)–1)(VDR)

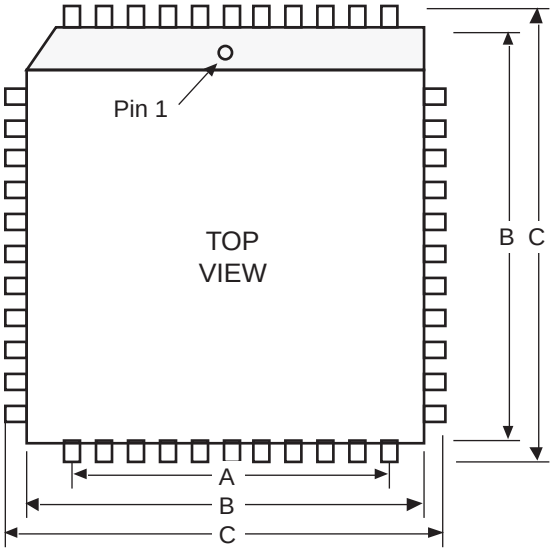
Figure 2 – Typical Interface Circuit (shown for unipolar operation)

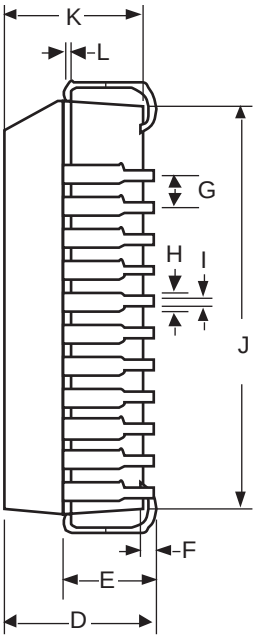


PACKAGE OUTLINE

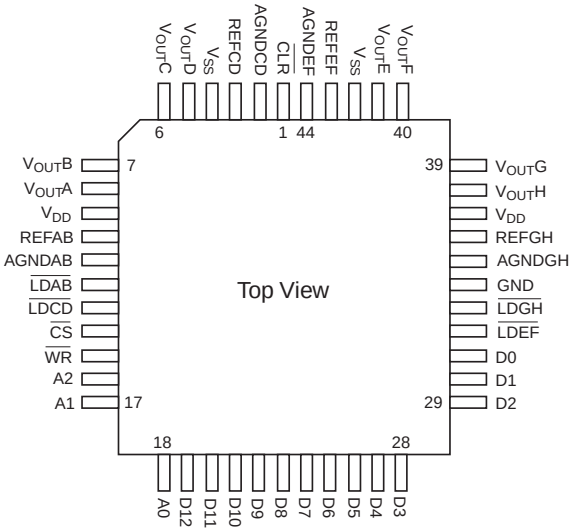
44L PLCC

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.5 typ		12.70 typ	
B	0.650	0.655	16.51	16.64
C	0.685	0.695	17.40	17.65
D	0.165	0.180	4.19	4.57
E	0.100	0.110	2.54	2.79
F	0.020		0.51	
G	0.05 typ		1.27 typ	
H	0.026	0.032	0.66	0.81
I	0.013	0.021	0.33	0.53
J	0.590	0.630	14.99	16.00
K	0.145	0.156	3.68	3.96
L	0.009	0.011	0.23	0.28





PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
$\overline{CLR}$	Clear input (active low). Driving this asynchronous input low sets the content of all latches to 1000hex. All DAC outputs are reset to AGNDxx.
AGNDCD	Analog ground for DAC C and DAC D.
REFCD	Reference voltage input for DAC C and DAC C. Bypass to AGNDCD with a 0.1 to 1 µF capacitor.
V_{SS}	Negative power supply, –5 V (two pins). Connect both pins to the supply voltage. Bypass each pin to the system analog ground with a 0.1 µF capacitor.
$V_{OUT}D$	DAC D output voltage.
$V_{OUT}C$	DAC C output voltage.
$V_{OUT}B$	DAC B output voltage.
$V_{OUT}A$	DAC A output voltage.
V_{DD}	Positive power supply, +5 V (two pins). Connect both pins to the supply voltage. Bypass each pin to the system analog ground with a 0.1 µF capacitor.
REFAB	Reference voltage input for DAC A and DAC B. Bypass to AGNDAB with a 0.1 to 1 µF capacitor.
AGNDAB	Analog ground for DAC A and DAC B.
$\overline{LDAB}$	Load input (active low). Driving this asynchronous input low transfers the contents of the input latches A and B to the respective DAC latches.
$\overline{LDCD}$	Load input (active low). Driving this asynchronous input low transfers the contents of the input latches C and D to the respective DAC latches.
$\overline{CS}$	Chip select (active low).
$\overline{WR}$	Write input (active low). $\overline{WR}$ along with $\overline{CS}$ load data into the DAC input latch selected by A0–A2.
A2	Address bit 2.
A1	Address bit 1.
A0	Address bit 0.
D12–D0	Data bits 12–0. (D0 = LSB)
$\overline{LDEF}$	Load input (active low). Driving this asynchronous input low transfers the contents of the input latches E and F to the respective DAC latches.
$\overline{LDGH}$	Load input (active low). Driving this asynchronous input low transfers the contents of the input latches G and H to the respective DAC latches.
GND	Digital ground.
AGNDGH	Analog ground for DAC G and DAC H.
REFGH	Reference voltage input for DAC G and DAC H. Bypass to AGNDGH with a 0.1 to 1 µF capacitor.
$V_{OUT}H$	DAC H output voltage.
$V_{OUT}G$	DAC G output voltage.
$V_{OUT}F$	DAC F output voltage.
$V_{OUT}E$	DAC E output voltage.
REFEF	Reference voltage input for DAC E and DAC F. Bypass to AGNDEF with a 0.1 to 1 µF capacitor.
AGNDEF	Analog ground for DAC E and DAC F.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT5400SCP	0 to +70 °C	44L PLCC

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CADEKA Headquarters Loveland, Colorado
T: 970.663.5452
T: 877.663.5452 (toll free)

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