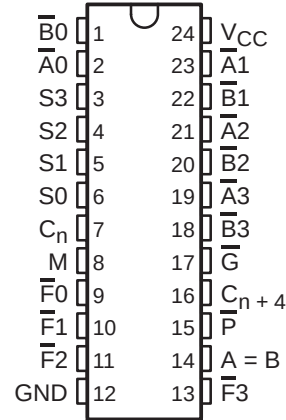


SN54AS181B, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

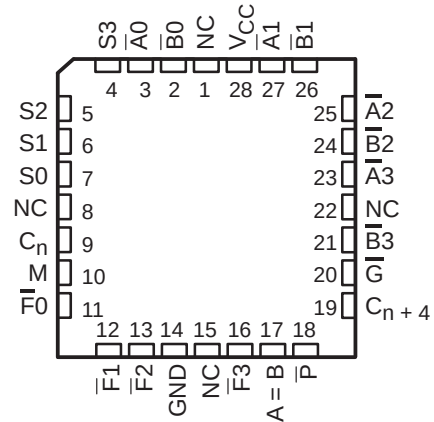
SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

- Full Look Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
 - Addition
 - Subtraction
 - Shift Operand A One Position
 - Magnitude Comparison
 - Twelve Other Arithmetic Operations
- Logic Function Modes:
 - Exclusive-OR
 - Comparator
 - AND, NAND, OR, NOR
- Package Options Include Plastic Small-Outline (N) Packages, Ceramic (FK) Chip Carriers, Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs, and Ceramic (JW) 600-mil DIPs

SN54AS181B . . . JT OR JW PACKAGE
SN74AS181A . . . N OR NT PACKAGE
(TOP VIEW)



SN54AS181B . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN54AS181B and SN74AS181A arithmetic logic units (ALUs)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select (S0, S1, S2, and S3) lines and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries are enabled by applying a low-level voltage to the mode-control (M) input. A full carry look-ahead scheme is used to generate fast, simultaneous carry by means of two cascade ($\bar{G}$ and $\bar{P}$) outputs for the four bits in the package.

If high speed is not important, a ripple-carry (C_n) input and a ripple-carry ($C_n + 4$) output are available. The ripple-carry delay is minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The SN54AS181B and SN74AS181A accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\bar{A}0$	$\bar{B}0$	$\bar{A}1$	$\bar{B}1$	$\bar{A}2$	$\bar{B}2$	$\bar{A}3$	$\bar{B}3$	$\bar{F}0$	$\bar{F}1$	$\bar{F}2$	$\bar{F}3$	C_n	$C_n + 4$	$\bar{P}$	$\bar{G}$
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\bar{C}_n$	$\bar{C}_n + 4$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

SN54AS181B, SN74AS181A

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

description (continued)

The SN54AS181B and SN74AS181A also can be used as comparators. The $A = B$ output is internally decoded from the function (F0, F1, F2, F3) outputs so that when two words of equal magnitude are applied at the A and B inputs, the output assumes a high level to indicate equality ($A = B$). The ALU must be in the subtract mode with $C_n = H$ when performing this comparison. The $A = B$ output is open collector so that it can be wire-AND connected to give a comparison for more than four bits. C_{n+4} also can be used to supply relative magnitude information. The ALU must be placed in the subtract mode by placing the function-select inputs S3, S2, S1, and S0 at L, H, H, and L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (Figure 1)	ACTIVE-HIGH DATA (Figure 2)
H	H	$A \geq B$	$A \leq B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leq B$	$A \geq B$

These circuits not only incorporate all of the designer's requirements for arithmetic operations, but also provide 16 possible functions of two Boolean variables without using external circuitry. These logic functions are selected by the four function-select inputs with M at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

TYPICAL ADDITION TIME
($C_L = 15 \text{ pF}$, $R_L = 280 \Omega$, $T_A = 25^\circ\text{C}$)

NUMBER OF BITS	ADDITION TIME USING 'S181 AND 'S182	PACKAGE COUNT		CARRY METHOD BETWEEN ALUs
		ALUs	LOOK-AHEAD CARRY GENERATORS	
1 to 4	11 ns	1		None
5 to 8	18 ns	2		Ripple
9 to 16	19 ns	3 or 4	1	Full look ahead
17 to 64	28 ns	5 to 16	2 to 5	Full look ahead

The SN54AS181B is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS181A is characterized for operation from 0°C to 70°C .

application note

An application-specific problem has been identified in the SN54AS181B device. The F0–F4 outputs exhibit voltage transients when one or more B-data inputs transition from a high to a low state. The resultant voltage transients can have an amplitude of 2 V relative to V_{OL} with a width of 5 ns at an input threshold of 1.5 V. The transient pulse occurs coincidentally with the high-to-low transition of the B-data input(s) and appears to be caused by internal coupling.

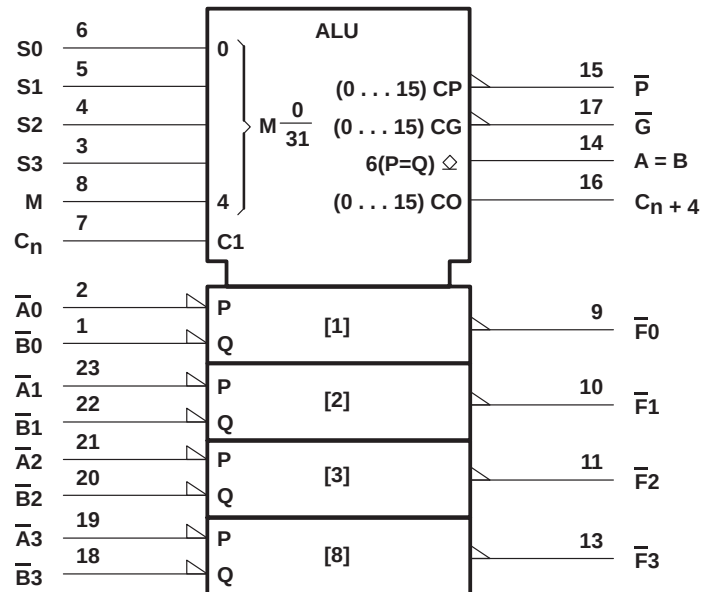
In system operations in which this device is used, it is likely that transmission-line effects minimize this anomaly. Narrow width of the voltage transient makes the pulse transparent to most circuitry; however, in certain applications, the transients can cause system errors.

SN54AS181B, SN74AS181A

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

logic symbol[†]



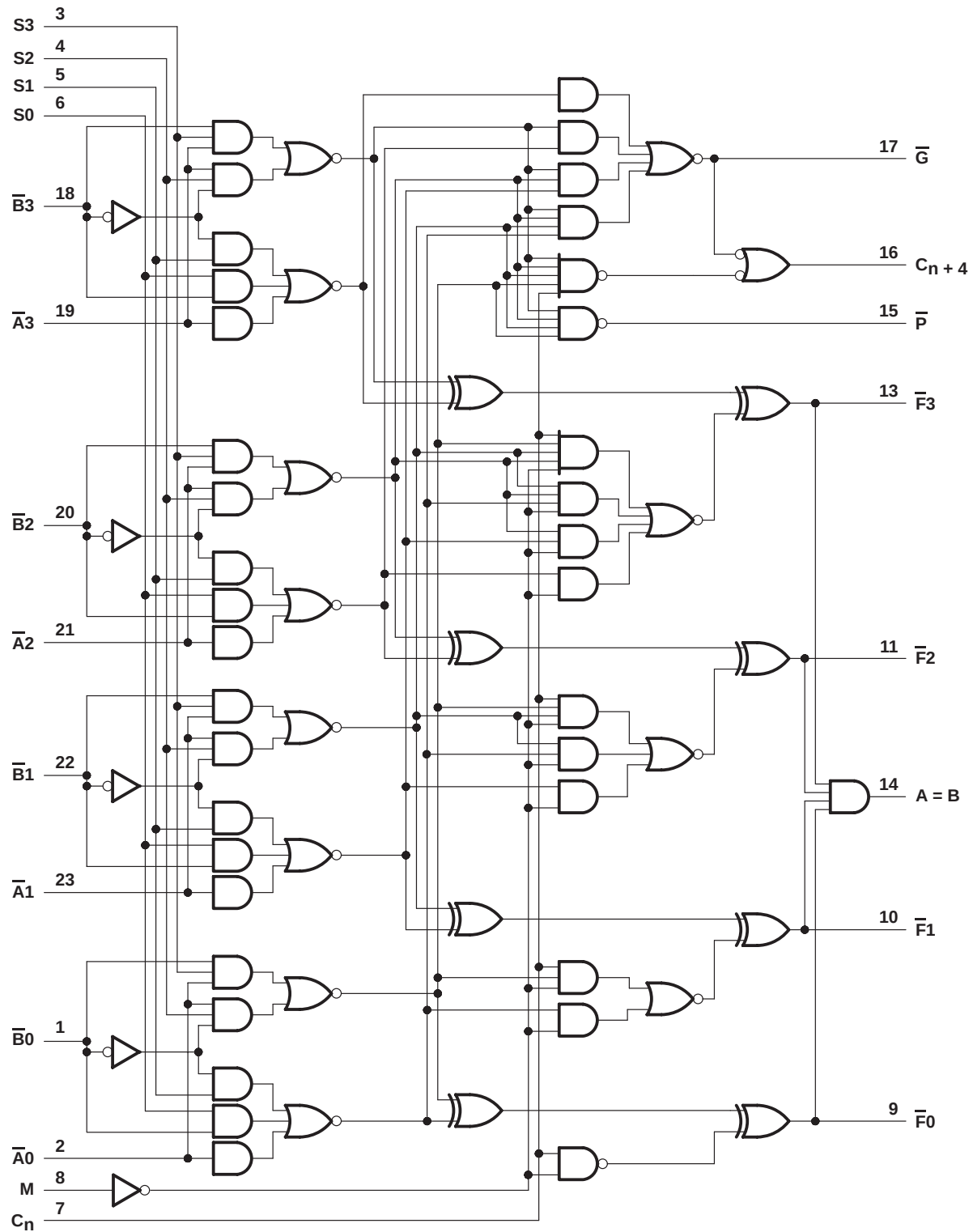
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JT, JW, N, and NT packages.

SN54AS181B, SN74AS181A

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

logic diagram



Pin numbers shown are for the JT, JW, N, and NT packages.

SN54AS181B, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

signal designations

In Figures 1 and 2, the polarity indicators ($\triangle$) indicate that the associated input or output is active low with respect to the function shown inside the symbol. The symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The SN54AS181B and SN74AS181A together with the 'S182 can be used with the signal designation of either Figure 1 or Figure 2.

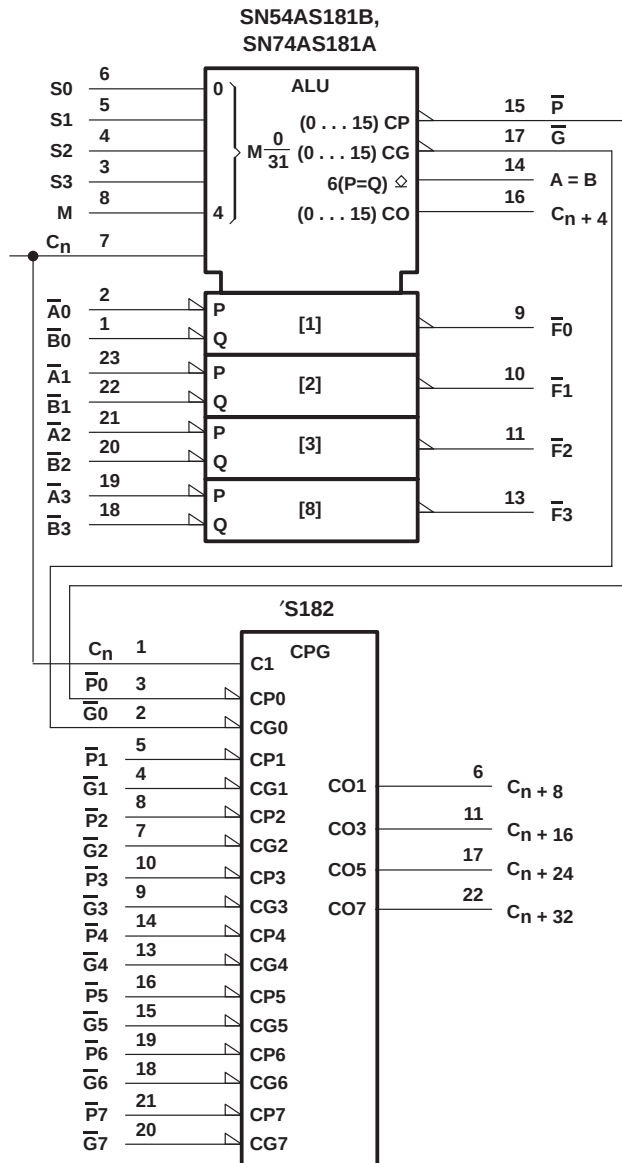


Figure 1
(use with Table 1)

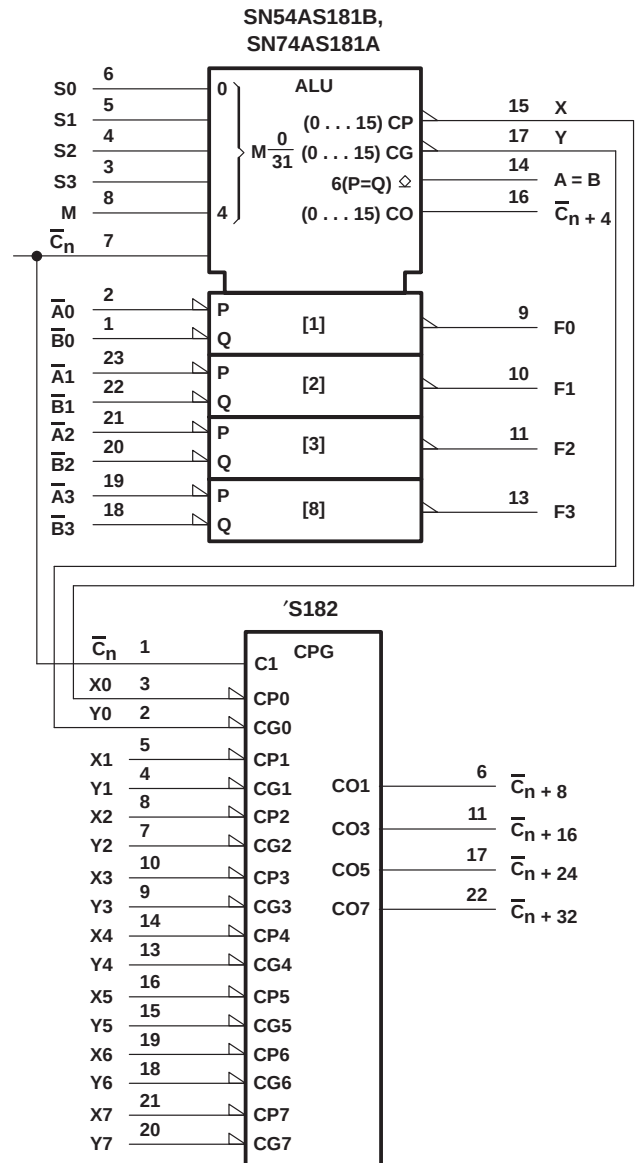


Figure 2
(use with Table 2)

SN54AS181B, SN74AS181A

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

Table 1

SELECTION				ACTIVE-LOW DATA		
				M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0		C _n = L (no carry)	C _n = H (with carry)
L	L	L	L	$F = \bar{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \bar{A}\bar{B}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \bar{A} + B$	F = $\bar{A}\bar{B}$ MINUS 1	F = $\bar{A}\bar{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{A + B}$	F = A PLUS (A + $\bar{B}$)	F = A PLUS (A + $\bar{B}$) PLUS 1
L	H	L	H	$F = \bar{B}$	F = AB PLUS (A + $\bar{B}$)	F = AB PLUS (A + $\bar{B}$) PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \bar{B}$	F = A + $\bar{B}$	F = (A + $\bar{B}$) PLUS 1
H	L	L	L	$F = \bar{A}B$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = $\bar{A}\bar{B}$ PLUS (A + B)	F = $\bar{A}\bar{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A [†]	F = A PLUS A PLUS 1
H	H	L	H	$F = \bar{A}\bar{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = $\bar{A}\bar{B}$ PLUS A	F = $\bar{A}\bar{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A PLUS 1	F = A PLUS 1

[†] Each bit is shifted to the next more significant position.

Table 2

SELECTION				ACTIVE-HIGH DATA		
				M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0		C _n = H (no carry)	C _n = L (with carry)
L	L	L	L	$F = \bar{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	$F = \bar{A}B$	F = A + $\bar{B}$	F = (A + $\bar{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	$F = \bar{A}\bar{B}$	F = A PLUS $\bar{A}\bar{B}$	F = A PLUS $\bar{A}\bar{B}$ PLUS 1
L	H	L	H	$F = \bar{B}$	F = (A + B) PLUS $\bar{A}\bar{B}$	F = (A + B) PLUS $\bar{A}\bar{B}$ PLUS 1
L	H	H	L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = \bar{A}\bar{B}$	F = $\bar{A}\bar{B}$ MINUS 1	F = A $\bar{B}$
H	L	L	L	$F = \bar{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\bar{B}$) PLUS AB	F = (A + $\bar{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A [†]	F = A PLUS A PLUS 1
H	H	L	H	$F = A + \bar{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\bar{B}$) PLUS A	F = (A + $\bar{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

[†] Each bit is shifted to the next more significant position.

SN54AS181B, SN74AS181A

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Off-state output voltage (A = B output only)	7 V
Operating free-air temperature range, T_A : SN54AS181B	–55°C to 125°C
SN74AS181A	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS181B			SN74AS181A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.8			0.8			V
V _{OH}	High-level output voltage	A = B output only	5.5			5.5			V
I _{OH}	High-level output current	All outputs except A = B and $\overline{G}$	−2			−2			mA
		$\overline{G}$	−3			−3			
I _{OL}	Low-level output current	All outputs except $\overline{G}$	20			20			mA
		$\overline{G}$	48			48			
T _A	Operating free-air temperature		−55	125		0	70		°C



SN54AS181B, SN74AS181A

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS181B			SN74AS181A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA		−1.2			−1.2			V
V _{OH}	Any output except A = B	V _{CC} = 4.5 V to 5.5 V, I _{OH} = −2 mA		V _{CC} − 2			V _{CC} − 2			V
	$\overline{\text{G}}$	V _{CC} = 4.5 V, I _{OH} = −3 mA		2.4	3.4		2.4	3.4		
V _{OL}	Any output except $\overline{\text{G}}$	V _{CC} = 4.5 V	I _{OL} = 20 mA	0.3 0.5		0.3 0.5				V
	$\overline{\text{G}}$		I _{OL} = 48 mA	0.4 0.5		0.4 0.5				
I _{OH}	A = B	V _{CC} = 4.5 V, V _{OH} = 5.5 V		0.1			0.1			mA
I _I	M	V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1			mA
	Any $\overline{\text{A}}$ or $\overline{\text{B}}$			0.3			0.3			
	Any S			0.4			0.4			
	C _N			0.6			0.6			
I _{IH}	M	V _{CC} = 5.5 V, V _I = 2.7 V		20			20			μA
	Any $\overline{\text{A}}$ or $\overline{\text{B}}$			60			60			
	Any S			80			80			
	C _N			120			120			
I _{IL}	M	V _{CC} = 5.5 V, V _I = 0.4 V		−0.5			−2			mA
	Any $\overline{\text{A}}$ or $\overline{\text{B}}$			−1.5			−6			
	Any S			−2			−8			
	C _N			−3			−12			
I _O [‡]	All outputs except A = B and $\overline{\text{G}}$	V _{CC} = 5.5 V, V _O = 2.25 V		−30	−45	−112	−30	−45	−112	mA
	$\overline{\text{G}}$			−30		−125	−30		−125	
I _{CC}		V _{CC} = 5.5 V		74 117			135 200			mA

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54AS181B, SN74AS181A

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

switching characteristics (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX‡				UNIT
				SN54AS181B		SN74AS181A		
				MIN	MAX	MIN	MAX	
t _{PLH}	C _N	C _N + 4		3	9	2	9	ns
t _{PHL}				2	7	2	9	
t _{PLH}	Any $\bar{A}$ or $\bar{B}$	C _N + 4	M = 0, S1 = S2 = 0, S0 = S3 = 4.5 V (SUM mode)	2	16	2	12	ns
t _{PHL}				2	14	2	12	
t _{PLH}	Any $\bar{A}$ or $\bar{B}$	C _N + 4	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	3	18	4	16	ns
t _{PHL}				3	14.5	2	16	
t _{PLH}	C _N	Any $\bar{F}$	M = 0 (SUM or DIFF mode)	3	10.5	3	9	ns
t _{PHL}				3	10	3	9	
t _{PLH}	Any $\bar{A}$ or $\bar{B}$	$\bar{G}$	M = 0, S1 = S2 = 0, S0 = S3 = 4.5 V (SUM mode)	3	9.5	2	8	ns
t _{PHL}				2	7	2	7	
t _{PLH}	Any $\bar{A}$ or $\bar{B}$	$\bar{G}$	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	3	12	2	9.5	ns
t _{PHL}				2	9	2	9	
t _{PLH}	Any $\bar{A}$ or $\bar{B}$	$\bar{P}$	M = 0, S1 = S2 = 0, S0 = S3 = 4.5 V (SUM mode)	3	9.5	2	8	ns
t _{PHL}				2	7.5	2	8	
t _{PLH}	Any $\bar{A}$ or $\bar{B}$	$\bar{P}$	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	3	12	2	10	ns
t _{PHL}				3	8.5	2	10	
t _{PLH}	$\bar{A}_i$ or $\bar{B}_i$	$\bar{F}_i$	M = 0, S1 = S2 = 0, S0 = S3 = 4.5 V (SUM mode)	3	11	2	9.5	ns
t _{PHL}				3	9	2	8	
t _{PLH}	$\bar{A}_i$ or $\bar{B}_i$	$\bar{F}_i$	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	3	13.5	2	10.5	ns
t _{PHL}				3	11	2	10	
t _{PLH}	$\bar{A}_i$ or $\bar{B}_i$	$\bar{F}_i$	M = 4.5 V (LOGIC mode)	3	16	2	11	ns
t _{PHL}				3	10	2	11	
t _{PLH}	Any $\bar{A}$ or $\bar{B}$	A = B	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	2	19	4	21	ns
t _{PHL}				3	22	4	21	

† Refer to the parameter measurement information tables for the SUM-, DIFF-, and LOGIC-mode test tables.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54AS181B, SN74AS181A

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

PARAMETER MEASUREMENT INFORMATION

SUM-MODE TEST TABLE
(Function Inputs: S0 = S3 = 4.5 V, S1 = S2 = M = 0)

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t _{PLH}	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ and $\bar{B}$	C_n	$\bar{F}_i$	In phase
t _{PHL}							
t _{PLH}	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$ and $\bar{B}$	C_n	$\bar{F}_i$	In phase
t _{PHL}							
t _{PLH}	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$, C_n	$\bar{P}$	In phase
t _{PHL}							
t _{PLH}	$\bar{B}_i$	$\bar{A}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$, C_n	$\bar{P}$	In phase
t _{PHL}							
t _{PLH}	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$, C_n	$\bar{G}$	In phase
t _{PHL}							
t _{PLH}	$\bar{B}_i$	None	$\bar{A}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$, C_n	$\bar{G}$	In phase
t _{PHL}							
t _{PLH}	C_n	None	None	All $\bar{A}$	All $\bar{B}$	Any $\bar{F}$ or $C_n + 4$	In phase
t _{PHL}							
t _{PLH}	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$, C_n	$C_n + 4$	Out of phase
t _{PHL}							
t _{PLH}	$\bar{B}_i$	None	$\bar{A}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$, C_n	$C_n + 4$	Out of phase
t _{PHL}							



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54AS181B, SN74AS181A

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

PARAMETER MEASUREMENT INFORMATION

DIFF-MODE TEST TABLE
(Function Inputs: S1 = S2 = 4.5 V, S0 = S3 = M = 0)

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t _{PLH}	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{A}$	Remaining $\bar{B}$, C _n	$\bar{F}_i$	In phase
t _{PHL}							
t _{PLH}	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$	Remaining $\bar{B}$, C _n	$\bar{F}_i$	Out of phase
t _{PHL}							
t _{PLH}	$\bar{A}_i$	None	$\bar{B}_i$	None	Remaining $\bar{A}$ and $\bar{B}$, C _n	$\bar{P}$	In phase
t _{PHL}							
t _{PLH}	$\bar{B}_i$	$\bar{A}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$, C _n	$\bar{P}$	Out of phase
t _{PHL}							
t _{PLH}	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$, C _n	$\bar{G}$	In phase
t _{PHL}							
t _{PLH}	$\bar{B}_i$	None	$\bar{A}_i$	None	Remaining $\bar{A}$ and $\bar{B}$, C _n	$\bar{G}$	Out of phase
t _{PHL}							
t _{PLH}	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{A}$	Remaining $\bar{B}$, C _n	A = B	In phase
t _{PHL}							
t _{PLH}	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$	Remaining $\bar{B}$, C _n	A = B	Out of phase
t _{PHL}							
t _{PLH}	C _n	None	None	$\bar{A}$ All $\bar{A}$ and $\bar{B}$	None	C _n + 4 or any F	In phase
t _{PHL}							
t _{PLH}	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}$, $\bar{B}$, C _n	C _n + 4	Out of phase
t _{PHL}							
t _{PLH}	$\bar{B}_i$	None	$\bar{A}_i$	None	Remaining $\bar{A}$, $\bar{B}$, C _n	C _n + 4	In phase
t _{PHL}							

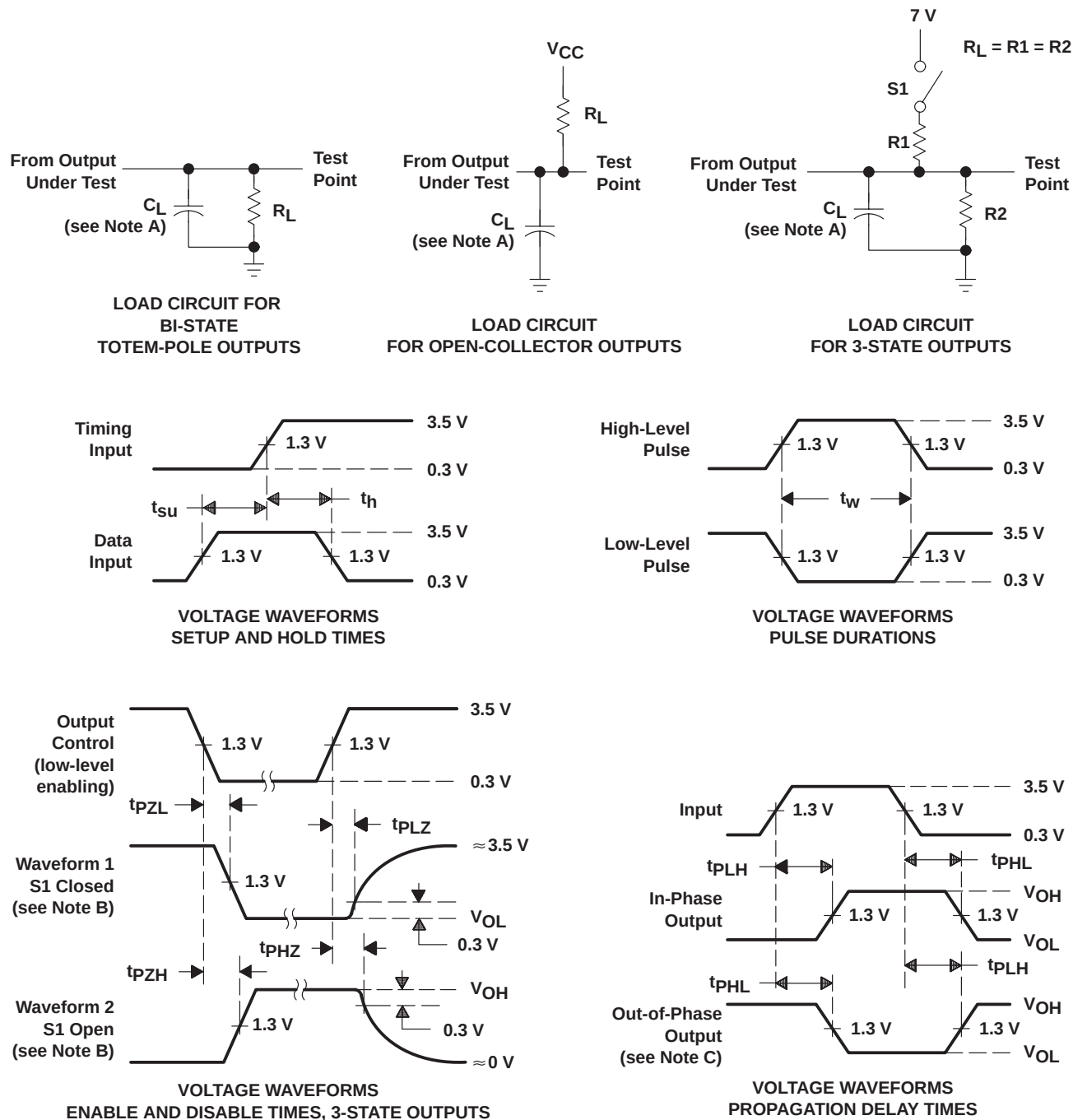
LOGIC-MODE TEST TABLE
(Function Inputs: S1 = S2 = M = 4.5 V, S0 = S3 = 0)

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 1)
		APPLY 4.5 V	APPLY GND	APPLY GND	APPLY 4.5 V		
t _{PLH}	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$, C _n	$\bar{F}_i$	Out of phase
t _{PHL}							
t _{PLH}	$\bar{B}_i$	$\bar{A}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$, C _n	$\bar{F}_i$	Out of phase
t _{PHL}							

SN54AS181B, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.