Future Technology Devices International Ltd.

UM232R USB- Serial UART Development Module

Incorporating Clock Generator Output and FTDIChip-ID™ Security Dongle

The **UM232R** *is a development module which uses FTDI's FT232RL, the latest device to be added to FTDI's range of USB UART interface Integrated Circuit Devices.*

The FT232RL is a USB to serial UART interface with optional clock generator output, and the new FTDIChip-ID™ security dongle feature. In addition, asynchronous and synchronous bit bang interface modes are available. USB to serial interface designs using the FT232RL have been further simplified by fully integrating the external EEPROM, clock circuit and USB resistors onto the device.

The FT232RL adds two new functions compared with its predecessors, effectively making it a "3-in-1" chip for some application areas. The internally generated clock (6MHz, 12MHz, 24MHz, and 48MHz) can be brought out of the device and used to drive a microcontroller or external logic. A unique number (the FTDIChip-ID™) is burnt into the device during manufacture and is readable over USB, thus forming the basis of a security dongle which can be used to protect customer application software from being copied.

The UM232R is supplied on a PCB which is designed to plug into a standard 15.0mm (0.6") wide 24 pin DIP socket. All components used, including the FT232RL are Pb-free (RoHS compliant).

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1. Features

1.1 Hardware Features

- Single chip USB to asynchronous serial data transfer interface.
- Entire USB protocol handled on the chip - No USB-specific firmware programming required.
- UART interface support for 7 or 8 data bits, 1 or 2 stop bits and odd / even / mark / space / no parity.
- Fully assisted hardware or X-On / X-Off software handshaking.
- Data transfer rates from 300 baud to 3 Megabaud (RS422 / RS485 and at TTL levels) and 300 baud to 1 Megabaud (RS232).
- FTDI's royalty-free VCP and D2XX drivers eliminate the requirement for USB driver development in most cases.
- In-built support for event characters and line break condition.
- New USB FTDIChip-ID™ feature.
- New configurable CBUS I/O pins.
- Auto transmit buffer control for RS485 applications.
- Transmit and receive LED drive signals.
- New 48MHz, 24MHz,12MHz, and 6MHz clock output signal Options for driving external MCU or FPGA.
- FIFO receive and transmit buffers for high data throughput.
- Adjustable receive buffer timeout.
- Synchronous and asynchronous bit bang mode interface options with RD# and WR# strobes.
- New CBUS bit bang mode option.
- Integrated 1024 bit internal EEPROM for storing USB VID, PID, serial number and product description strings, and CBUS I/O configuration.
- Device supplied preprogrammed with unique USB serial number.
- Support for USB suspend and resume.
- Support for bus powered, self powered, and high-power bus powered USB configurations.
- On board jumper allows for selection of USB bus powered supply or self powered supply.
- Integrated 3.3V level converter for USB I/O.
- Integrated level converter on UART and CBUS for interfacing to 5V - 1.8V Logic.
- On board jumper allows for selection of UART and CBUS interface IO voltage.
- True 5V / 3.3V / 2.8V / 1.8V CMOS drive output and TTL input.
- High I/O pin output drive option.
- Integrated USB resistors.
- Integrated power-on-reset circuit.
- Fully integrated clock - no external crystal, oscillator, or resonator required.
- Fully integrated AVCC supply filtering - No separate AVCC pin and no external R-C filter required.
- UART signal inversion option.
- USB bulk transfer mode.
- 3.3V to 5.25V Single Supply Operation.
- Low operating and USB suspend current.
- Low USB bandwidth consumption.
- UHCI / OHCI / EHCI host controller compatible
- USB 2.0 Full Speed compatible.
- -40°C to 85°C extended operating temperature range.
- Supplied in PCB designed to fit a standard 15.0mm (0.6") wide 24 pin DIP socket. Pins are on a 2.60mm (0.1") pitch.
- On board USB 'B' socket allows module to be connected to a PC via a standard A to B USB cable.

1.2 Driver Support

Royalty-Free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 98, 98SE, ME, 2000, Server 2003, XP.
- Windows Vista / Longhorn*
- Windows XP 64-bit.*
- Windows XP Embedded.
- Windows CE.NET 4.2 & 5.0
- MAC OS 8 / 9, OS-X
- Linux 2.4 and greater

Royalty-Free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 98, 98SE, ME, 2000, Server 2003, XP.
- Windows Vista / Longhorn*
- Windows XP 64-bit.*
- Windows XP Embedded.
- Windows CE.NET 4.2 & 5.0
- Linux 2.4 and greater

The drivers listed above are all available to download for free from the FTDI website. Various 3rd Party Drivers are also available for various other operating systems - see the FTDI website for details.

* Currently Under Development. Contact FTDI for availability.

1.3 Typical Applications

- USB to RS232 / RS422 / RS485 Converters
- Upgrading Legacy Peripherals to USB
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU / PLD / FPGA based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Hardware Modems
- USB Wireless Modems
- USB Bar Code Readers
- USB Software / Hardware Encryption Dongles

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2. FT232RL Features and Enhancements

2.1 Key Features

This section summarises the key features and enhancements of the FT232RL IC device which is used on the UM232R Module. For further details, consult the FT232R datasheet, which is available from the FTDI website.

Integrated Clock Circuit - Previous generations of FTDI's USB UART devices required an external crystal or ceramic resonator. The clock circuit has now been integrated onto the device meaning that no crystal or ceramic resonator is required. However, if required, an external 12MHz crystal can be used as the clock source.

Integrated EEPROM - Previous generations of FTDI's USB UART devices required an external EEPROM if the device were to use USB Vendor ID (VID), Product ID (PID), serial number and product description strings other than the default values in the device itself. This external EEPROM has now been integrated onto the FT232R chip meaning that all designs have the option to change the product description strings. A user area of the internal EEPROM is available for storing additional data. The internal EEPROM is programmable in circuit, over USB without any additional voltage requirement.

Preprogrammed EEPROM - The FT232R is supplied with its internal EEPROM preprogrammed with a serial number which is unique to each individual device. This, in most cases, will remove the need to program the device EEPROM.

Integrated USB Resistors - Previous generations of FTDI's USB UART devices required two external series resistors on the USBDP and USBDM lines, and a 1.5 kΩ pull up resistor on USBDP. These three resistors have now been integrated onto the device.

Integrated AVCC Filtering - Previous generations of FTDI's USB UART devices had a separate AVCC pin - the supply to the internal PLL. This pin required an external R-C filter. The separate AVCC pin is now connected internally to VCC, and the filter has now been integrated onto the chip.

Less External Components - Integration of the crystal, EEPROM, USB resistors, and AVCC filter will substantially reduce the bill of materials cost for USB interface designs using the FT232R compared to its FT232BM predecessor.

Configurable CBUS I/O Pin Options - There are now 5 configurable Control Bus (CBUS) lines. Options are **TXDEN** - transmit enable for RS485 designs, **PWREN#** - Power control for high power, bus powered designs, **TXLED#** - for pulsing an LED upon transmission of data, **RXLED#** - for pulsing an LED upon receiving data, **TX&RXLED#** - which will pulse an LED upon transmission OR reception of data, **SLEEP#** - indicates that the device going into USB suspend mode, **CLK48 / CLK24 / CLK12 / CLK6** - 48MHz, 24MHz,12MHz, and 6MHz clock output signal options. There is also the option to bring out bit bang mode read and write strobes (see below). The CBUS lines can be configured with any one of these output options by setting bits in the internal EEPROM. The device is supplied with the most commonly used pin definitions preprogrammed - see Section 8 for details.

Enhanced Asynchronous Bit Bang Mode with RD# and WR# Strobes - The FT232R supports FTDI's BM chip bit bang mode. In bit bang mode, the eight UART lines can be switched from the regular interface mode to an 8-bit general purpose I/O port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate prescaler). With the FT232R device this mode has been enhanced so that the internal RD# and WR# strobes are now brought out of the device which can be used to allow external logic to be clocked by accesses to the bit bang I/O bus. This option will be described more fully in a separate application note.

Synchronous Bit Bang Mode - Synchronous bit bang mode differs from asynchronous bit bang mode in that the interface pins are only read when the device is written to. Thus making it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data. The feature was previously seen in FTDI's FT2232C device. This option will be described more fully in a separate application note.

CBUS Bit Bang Mode - This mode allows four of the CBUS pins to be individually configured as GPIO pins, similar to Asynchronous bit bang mode. It is possible to use this mode while the UART interface is being used, thus providing up to four general purpose I/O pins which are available during normal operation. An application note describing this feature is available separately from the FTDI website.

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Lower Supply Voltage - Previous generations of the chip required 5V supply on the VCC pin. The FT232R will work with a Vcc supply in the range 3.3V - 5.25V. Bus powered designs would still take their supply from the 5V on the USB bus, but for self powered designs where only 3.3V is available and there is no 5V supply there is no longer any need for an additional external regulator.

Integrated Level Converter on UART Interface and Control Signals - VCCIO pin supply can be from 1.8V to 5V. Connecting the VCCIO pin to 1.8V, 2.8V, or 3.3V allows the device to directly interface to 1.8V, 2.8V or 3.3V and other logic families without the need for external level converter I.C. devices.

5V / 3.3V / 2.8V / 1.8V Logic Interface - The FT232R provides *true* CMOS Drive Outputs and TTL level Inputs.

Integrated Power-On-Reset (POR) Circuit- The device incorporates an internal POR function. A RESET# pin is available in order to allow external logic to reset the FT232R where required. However, for many applications the RESET# pin can be left unconnected, or pulled up to VCCIO.

Lower Operating and Suspend Current - The device operating supply current has been further reduced to 15mA, and the suspend current has been reduced to around 70µA. This allows greater margin for peripheral designs to meet the USB suspend current limit of 500µA.

Low USB Bandwidth Consumption - The operation of the USB interface to the FT232R has been designed to use as little as possible of the total USB bandwidth available from the USB host controller.

High Output Drive Option - The UART interface and CBUS I/O pins can be made to drive out at three times the standard signal drive level thus allowing multiple devices to be driven, or devices that require a greater signal drive strength to be interfaced to the FT232R. This option is enabled in the internal EEPROM.

Power Management Control for USB Bus Powered, High Current Designs- The PWREN# signal can be used to directly drive a transistor or P-Channel MOSFET in applications where power switching of external circuitry is required. An option in the internal EEPROM makes the device gently pull down on its UART interface lines when the power is shut off (PWREN# is high). In this mode any residual voltage on external circuitry is bled to GND when power is removed, thus ensuring that external circuitry controlled by PWREN# resets reliably when power is restored.

UART Pin Signal Inversion - The sense of each of the eight UART signals can be individually inverted by setting options in the internal EEPROM. Thus, CTS# (active low) can be changed to CTS (active high), or TXD can be changed to TXD#.

FTDIChip-ID™ - Each FT232R is assigned a unique number which is burnt into the device at manufacture. This ID number cannot be reprogrammed by product manufacturers or end-users. This allows the possibility of using FT232R based dongles for software licensing. Further to this, a renewable license scheme can be implemented based on the FTDIChip-ID™ number when encrypted with other information. This encrypted number can be stored in the user area of the FT232R internal EEPROM, and can be decrypted, then compared with the protected FTDIChip-ID™ to verify that a license is valid. Web based applications can be used to maintain product licensing this way. An application note describing this feature is available separately from the FTDI website.

Improved EMI Performance - The reduced operating current and improved on-chip VCC decoupling significantly improves the ease of PCB design requirements in order to meet FCC, CE and other EMI related specifications.

Programmable Receive Buffer Timeout - The receive buffer timeout is used to flush remaining data from the receive buffer. This time defaults to 16ms, but is programmable over USB in 1ms increments from 1ms to 255ms, thus allowing the device to be optimised for protocols that require fast response times from short data packets.

Baud Rates - The FT232R supports all standard baud rates and non-standard baud rates from 300 Baud up to 3 Megabaud. Achievable non-standard baud rates are calculated as follows -

Baud Rate = 3000000 / (n + *x*)

where n can be any integer between 2 and 16,384 (= 2^{14}) and *x* can be a sub-integer of the value 0, 0.125, 0.25, 0.375, 0.5, 0.625, 0.75, or 0.875. When n = 1, *x* = 0, i.e. baud rate divisors with values between 1 and 2 are not possible.
This gives achievable baud rates in the range 183.1 baud to 3,000,000 baud. When a non-standard baud rate is required simply pass the required baud rate value to the driver as normal, and the FTDI driver will calculate the required divisor, and set the baud rate. See FTDI application note AN232B-05 for more details.

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Extended Operating Temperature Range - The FT232R operates over an extended temperature range of -40º to +85º C thus allowing the device to be used in automotive and industrial applications.

New Package Options - The FT232R is available in two packages - a compact 28 pin SSOP (FT232RL) and an ultra-compact 5mm x 5mm pinless QFN-32 package (FT232RQ). Both packages are lead (Pb) free, and use a 'green' compound. Both packages are fully compliant with European Union directive 2002/95/EC.

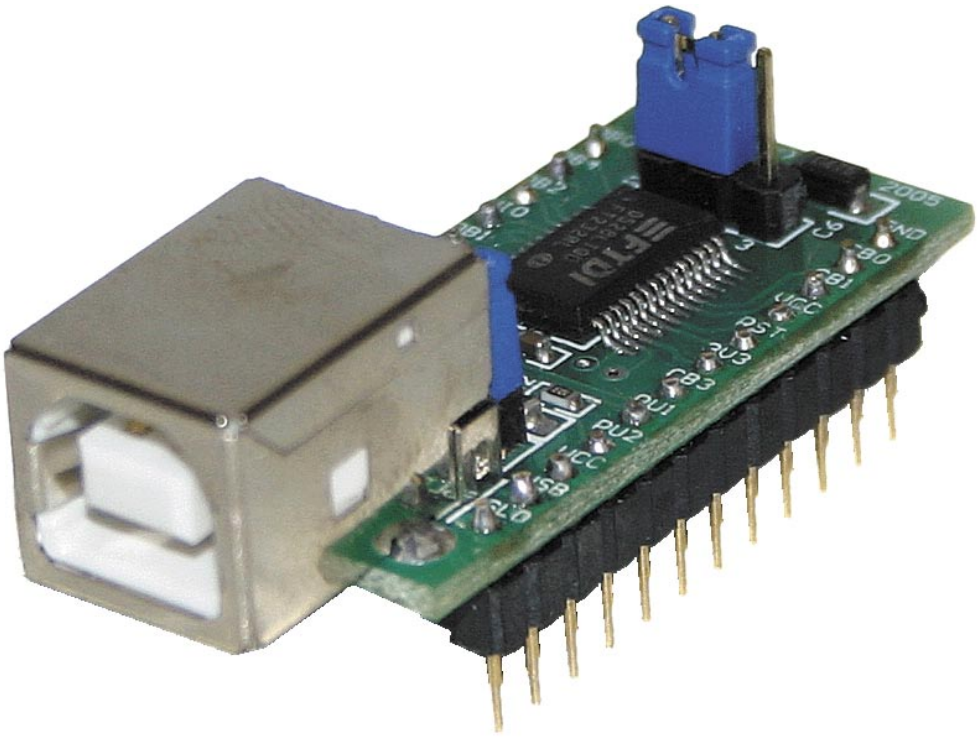


Figure 1 - The UM232R Module.

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3. UM232R Pin Out and Signal Descriptions

3.1 UM232R Pin Out

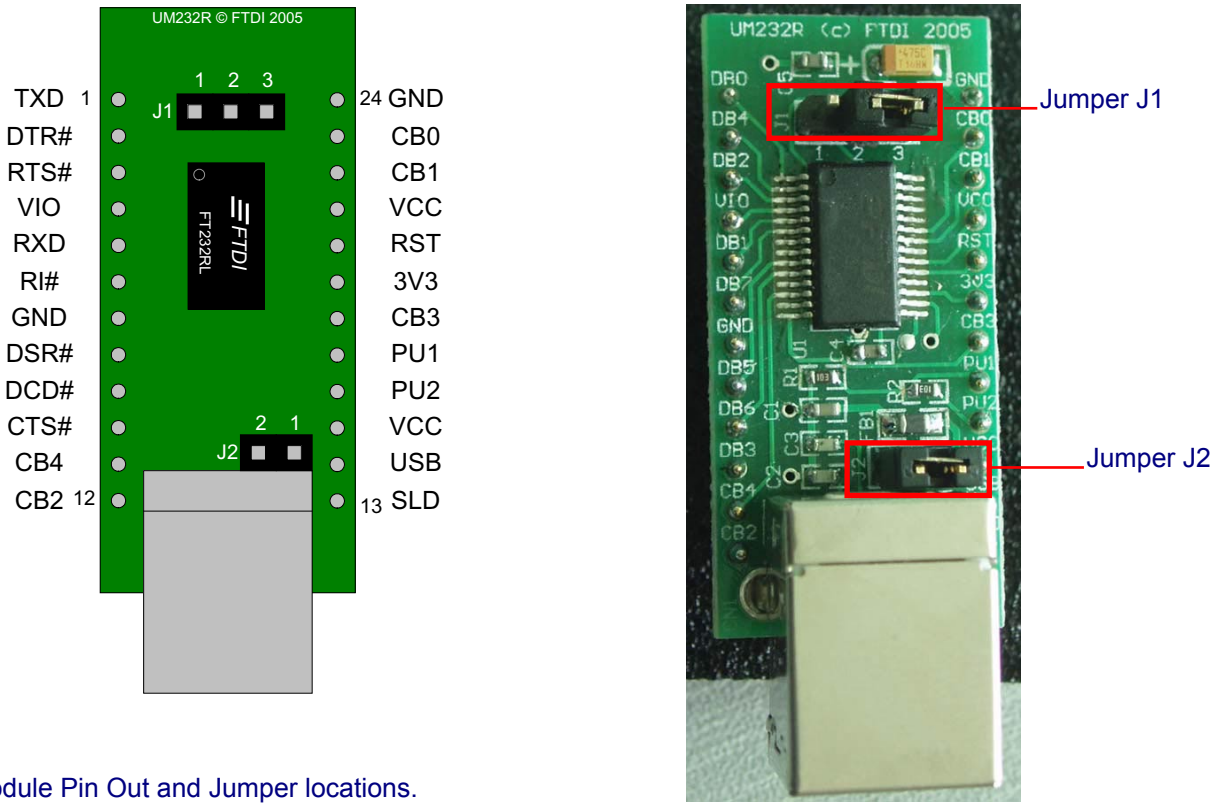


Figure 2 - Module Pin Out and Jumper locations.

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3.2 Signal Descriptions

Table 1 - Module Pin Out Description

Pin No.	Name	Type	Description
1	TXD	Output	Transmit Asynchronous Data Output.*
2	DTR#	Output	Data Terminal Ready Control Output / Handshake signal.*
3	RTS#	Output	Request To Send Control Output / Handshake signal.*
4	VIO	PWR	+1.8V to +5.25V supply to the UART Interface and CBUS I/O pins (1...3, 5, 6, 9...14, 22, 23). In USB bus powered designs connect to 3V3 to drive out at 3.3V levels (connect jumper J1 pins 1 and 2 together), or connect to VCC to drive out at 5V CMOS level (connect jumper J1 pins 2 and 3 together). This pin can also be supplied with an external 1.8V - 2.8V supply in order to drive out at lower levels. It should be noted that in this case this supply should originate from the same source as the supply to Vcc. This means that in bus powered designs a regulator which is supplied by the 5V on the USB bus should be used.
5	RXD	Input	Receive Asynchronous Data Input.*
6	RI#	Input	Ring Indicator Control Input. When remote wake up is enabled in the internal EEPROM taking RI# low can be used to resume the PC USB host controller from suspend.*
7, 24	GND	PWR	Module ground supply pins
8	DSR#	Input	Data Set Ready Control Input / Handshake signal.*
9	DCD#	Input	Data Carrier Detect Control input.*
10	CTS#	Input	Clear to Send Control input / Handshake signal.*
11	CB4	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory Default pin function is SLEEP#. See CBUS Signal Options, Table 4.*
12	CB2	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory Default pin function is TXDEN. See CBUS Signal Options, Table 4.*
13	SLD	GND	USB Cable shield.
14	USB	Output	5V Power output USB port. For a low power USB bus powered design, up to 100mA can be sourced from the 5V supply on the USB bus. A maximum of 500mA can be sourced from the USB bus in a high power USB bus powered design.
15, 21	VCC	PWR or Output	These two pins are internally connected on the module pcb. To power the module from the 5V supply on USB bus connect jumper J2 pins 1 and 2 together (this is the module default configuration). In this case these pins would have the same description as pin 14. To use the UM232R module in a self powered configuration ensure that jumper J2 pins 1 and 2 are not connected together, and apply an external 3.3V to 5.25V supply to one of these pins.
16	PU2	Control	Pull up resistor pin connection 2. Conect to pin 17 (RST#) in a self powered configuration.
17	PU1	Control	Pull up resistor pin connection 1. Connect to pin 14 (USB) in a self powered configuration
19	3V3	Output	3.3V output from integrated L.D.O. regulator. This pin is decoupled to ground on the module pcb with a 10nF capacitor. The prime purpose of this pin is to provide the internal 3.3V supply to the USB transceiver cell and the internal 1.5kΩ pull up resistor on USBDP. Up to 50mA can be drawn from this pin to power external logic if required. This pin can also be used to supply the FT232RL's VCCIO pin by connecting this pin to pin 4 (VIO), or by connecting together pins 1 and 2 on jumper J1.
20	RST#	Input	Can be used by an external device to reset the FT232R. If not required can be left unconnected, or pulled up to VCCIO.
18	CB3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory Default pin function is PWREN#. See CBUS Signal Options, Table 4.*
22	CB1	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory Default pin function is RXLED#. See CBUS Signal Options, Table 4.*
23	CB0	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory Default pin function is TXLED#. See CBUS Signal Options, Table 4.*

* When used in Input Mode, these pins are pulled to VCCIO via internal 200kΩ resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the internal EEPROM.

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3.3 Jumper Configuration Options

Table 2 - Jumper J1 Pin Description

Pin No.	Name	Type	Description
1	3V3	Output	3.3V output from integrated L.D.O. regulator. This pin is decoupled to ground on the module pcb with a 10nF capacitor. The prime purpose of this pin is to provide the internal 3.3V supply to the USB transceiver cell and the internal 1.5kΩ pull up resistor on USBDP. Up to 50mA can be drawn from this pin to power external logic if required. This pin can also be used to supply the FT232RL's VCCIO pin by connecting this pin to pin 4 (VIO), or by connecting together pins 1 and 2 on jumper J1.
2	VIO	PWR	+1.8V to +5.25V supply to the UART Interface and CBUS I/O pins (1...3, 5, 6, 9...14, 22, 23). In USB bus powered designs connect to 3V3 to drive out at 3.3V levels (connect jumper J1 pins 1 and 2 together), or connect to VCC to drive out at 5V CMOS level (connect jumper J1 pins 2 and 3 together). This pin can also be supplied with an external 1.8V - 2.8V supply in order to drive out at lower levels. It should be noted that in this case this supply should originate from the same source as the supply to Vcc. This means that in bus powered designs a regulator which is supplied by the 5V on the USB bus should be used.
3	VCC	PWR	VCC Output. This will be 5V from the USB bus if pins 1 and 2 on jumper J2 are connected. Alternativly, if the module is in a self powered configuration, the supply to the VCC module pins (15 and 21) will be brought out to this jumper pin. Connect this jumper J1 pin 2 in order to supply the device IO pins from the supply to VCCIO.

Table 3 - Jumper J2 Pin Description

Pin No.	Name	Type	Description
1	USB	PWR	5V Power output USB port. For a low power USB bus powered design, up to 100mA can be sourced from the 5V supply on the USB bus. A maximum of 500mA can be sourced from the USB bus in a high power USB bus powered design.
2	VCC	PWR or Output	Board supply input. Connect to jumper J2 pin 1 in order to supply the board from the USB bus. This pin is internally connected to the VCC DIP pins. Remove the jumper connector in a self powered design.

3.4 CBUS Signal Options

The following options can be configured on the CBUS I/O pins. These options are all configured in the internal EEPROM using the utility software MPROG, which can be downloaded from the FTDI website. The default configuration is described in Section 8.

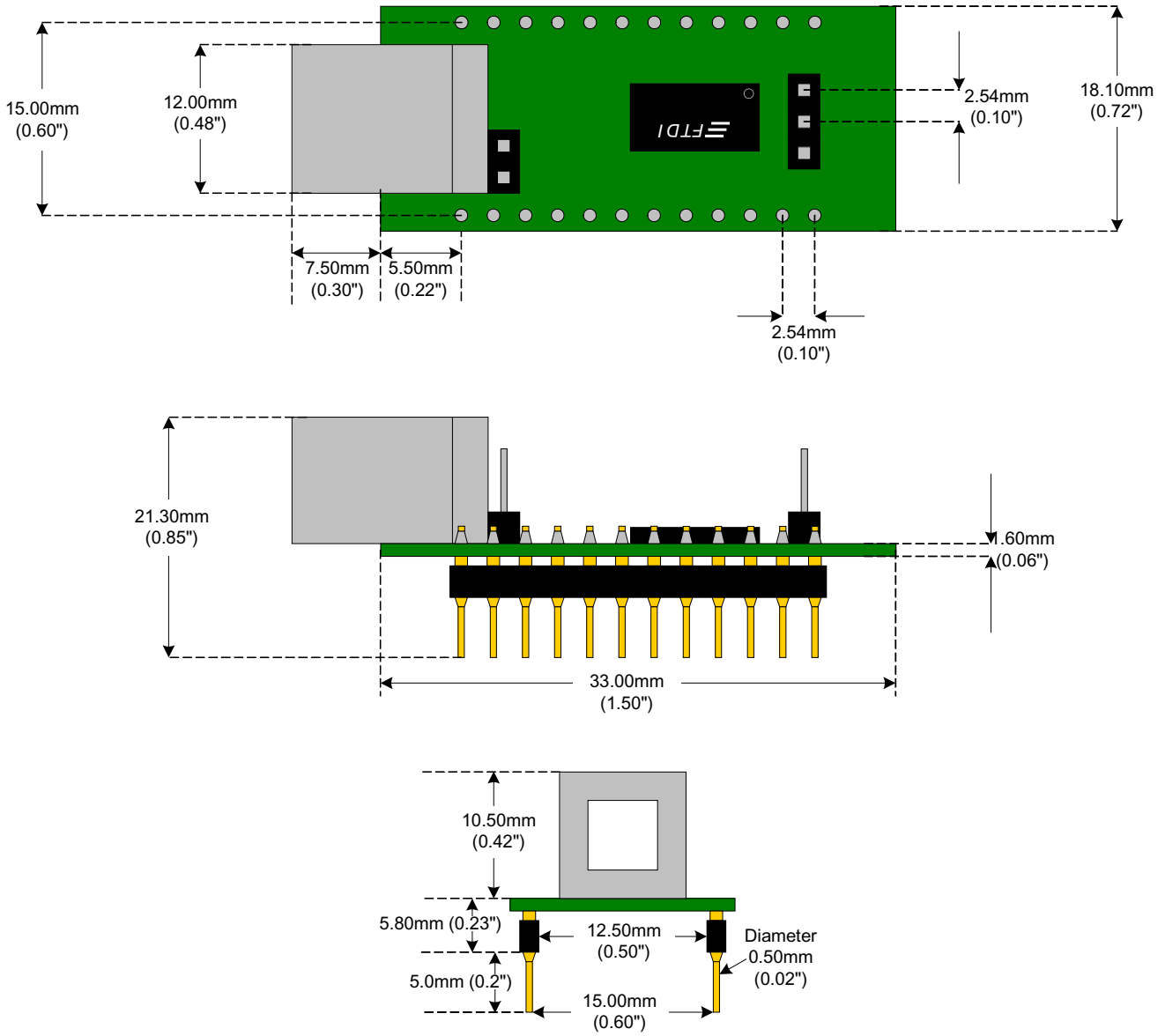
Table 4 - CBUS Signal Options

CBUS Signal Option	Available On CBUS Pin...	Description
TXDEN	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Enable transmit data for RS485
PWREN#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Goes low after the device is configured by USB, then high during USB suspend. Can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# pin in this way.
TXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Transmit data LED drive - pulses low when transmitting data via USB. See FT232R datasheet for more details.
RXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Receive data LED drive - pulses low when receiving data via USB. See FT232R datasheet for more details.
TX&RXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	LED drive - pulses low when transmitting or receiving data via USB. See FT232R datasheet for more details.
SLEEP#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Goes low during USB suspend mode. Typically used to power down an external TTL to RS232 level converter I.C. in USB to RS232 converter designs.
CLK48	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	48MHz Clock output.
CLK24	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	24MHz Clock output.
CLK12	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	12MHz Clock output.
CLK6	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	6MHz Clock output.
CBitBangI/O	CBUS0, CBUS1, CBUS2, CBUS3	CBUS bit bang mode option. Allows up to 4 of the CBUS pins to be used as general purpose I/O. Configured individually for CBUS0, CBUS1, CBUS2 and CBUS3 in the internal EEPROM. A separate application note will describe in more detail how to use CBUS bit bang mode.
BitBangWRn	CBUS0, CBUS1, CBUS2, CBUS3	Synchronous and asynchronous bit bang mode WR# strobe Output
BitBangRDn	CBUS0, CBUS1, CBUS2, CBUS3	Synchronous and asynchronous bit bang mode RD# strobe Output

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4. Module Dimensions

Figure 3 - UM232R Module Dimensions



All dimensions are in millimeters, with inches in parenthesis.

The FT232RL is supplied in a RoHS compliant 28 pin SSOP package. The package is lead (Pb) free and uses a 'green' compound. The date code format is **YYXX** where XX = 2 digit week number, YY = 2 digit year number.

The UM232R module uses exclusivly lead free components.

Both the I.C. device and the module are fully compliant with European Union directive 2002/95/EC.

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5. FT232RL Device Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT232R devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Table 5 - Absolute Maximum Ratings

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Temperature (Power Applied)	-40°C to 85°C	Degrees C.
Vcc Supply Voltage	-0.5 to +6.00	V
D.C. Input Voltage - USBDP and USBDM	-0.5 to +3.8	V
D.C. Input Voltage - High Impedance Bidirectionals	-0.5 to +(Vcc +0.5)	V
D.C. Input Voltage - All other Inputs	-0.5 to +(Vcc +0.5)	V
D.C. Output Current - Outputs	24	mA
DC Output Current - Low Impedance Bidirectionals	24	mA
Power Dissipation (Vcc = 5.25V)	500	mW

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of 125°C and baked for up to 17 hours.

5.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40 to 85°C)

Table 6 - Operating Voltage and Current

Parameter	Description	Min	Typ	Max	Units	Conditions
Vcc1	VCC Operating Supply Voltage	3.3	-	5.25	V	
Vcc2	VCCIO Operating Supply Voltage	1.8	-	5.25	V	
Icc1	Operating Supply Current	-	15	-	mA	Normal Operation
Icc2	Operating Supply Current	50	70	100	µA	USB Suspend*

Table 7 - UART and CBUS I/O Pin Characteristics (VCCIO = 5.0V, Standard Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	**
VHys	Input Switching Hysteresis	50	55	60	mV	**

Table 8 - UART and CBUS I/O Pin Characteristics (VCCIO = 3.3V, Standard Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.2	2.7	3.2	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

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Table 9 - UART and CBUS I/O Pin Characteristics (VCCIO = 2.8V, Standard Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.1	2.6	3.1	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 10 - UART and CBUS I/O Pin Characteristics (VCCIO = 5.0V, High Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 6mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 6mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	**
VHys	Input Switching Hysteresis	50	55	60	mV	**

Table 11 - UART and CBUS I/O Pin Characteristics (VCCIO = 3.3V, High Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.2	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 12 - UART and CBUS I/O Pin Characteristics (VCCIO = 2.8V, High Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.1	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

**Inputs have an internal 200kΩ pull-up resistor to VCCIO.

Table 13 - RESET# and TEST Pin Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
Vin	Input Switching Threshold	1.3	1.6	1.9	V	
VHys	Input Switching Hysteresis	50	55	60	mV	

Table 14 - USB I/O Pin (USBDP, USBDM) Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
UVoh	I/O Pins Static Output (High)	2.8		3.6	V	RI = 1.5kΩ to 3V3Out (D+) RI = 15kΩ to GND (D-)
UVol	I/O Pins Static Output (Low)	0		0.3	V	RI = 1.5kΩ to 3V3Out (D+) RI = 15kΩ to GND (D-)
UVse	Single Ended Rx Threshold	0.8		2.0	V	
UCom	Differential Common Mode	0.8		2.5	V	
UVDif	Differential Input Sensitivity	0.2			V	
UDrvZ	Driver Output Impedance	26	29	44	Ohms	***

***Driver Output Impedance includes the internal USB series resistors on USBDP and USBDM pins.

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5.3 EEPROM Reliability Characteristics

The internal 1024 bit EEPROM has the following reliability characteristics-

Table 15 - EEPROM Characteristics

Parameter Description	Value	Unit
Data Retention	15	Years
Read / Write Cycles	100,000	Cycles

5.4 Internal Clock Characteristics

The internal Clock Oscillator has the following characteristics.

Table 16 - Internal Clock Characteristics

Parameter	Value			Unit
	Min	Typical	Max	
Frequency of Operation	11.98	12.00	12.02	MHz
Clock Period	83.19	83.33	83.47	ns
Duty Cycle	45	50	55	%

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6. Module Configurations

6.1 Bus Powered Configuration

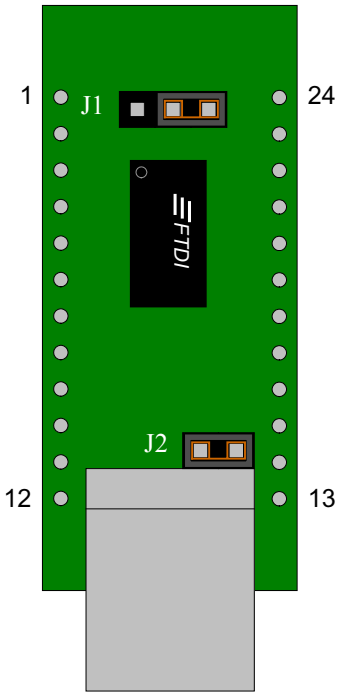


Figure 4 - Bus Powered Configuration

Figure 4 illustrates the UM232R module in a typical USB bus powered design configuration. This can easily be done by fitting the jumper link on J2, as shown above. The UM232R is supplied in this configuration by default.

A USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows –

i) On plug-in to USB, the device must draw no more than 100mA.

ii) On USB Suspend the device must draw no more than 500µA.

iii) A Bus Powered High Power USB Device (one that draws more than 100mA) should use one of the CBUS pins configured as PWREN# and use it to keep the current below 100mA on plug-in and 500µA on USB suspend.

iv) A device that consumes more than 100mA can not be plugged into a USB Bus Powered Hub.

v) No device can draw more that 500mA from the USB Bus.

Interfacing the UM232R module to a microcontroller (MCU), or other logic for a bus powered design would be done in exactly the same way as for a self powered design (see Section 6.2), except that the MCU or external logic would take its power supply from the USB bus (either the 5V on the USB pin, or 3.3V on the 3V3 pin).

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6.2 Self Powered Configuration

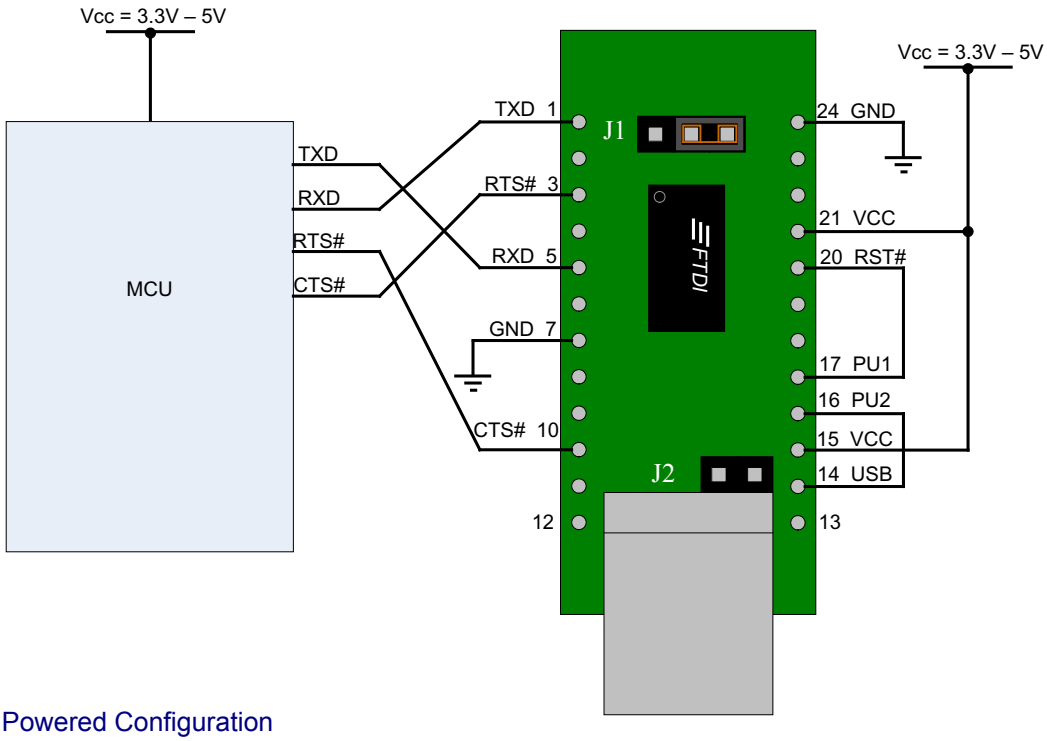


Figure 5 - Self Powered Configuration

Figure 5 illustrates the UM232R in a typical USB self powered configuration. In this case the link on jumper J2 is removed, and an external supply is connected to the module VCC pins. Figure 5 illustrates a self powered design which has a 3.3V - 5V supply.

A USB Self Powered device gets its power from its own power supply and does not draw current from the USB bus. The basic rules for USB Self powered devices are as follows –

i) A Self Powered device should not force current down the USB bus when the USB Host or Hub Controller is powered down.

ii) A Self Powered Device can use as much current as it likes during normal operation and USB suspend as it has its own power supply.

iii) A Self Powered Device can be used with any USB Host and both Bus and Self Powered USB Hubs. In this case the power descriptor in the internal EEPROM should be programmed to a value of zero (self powered).

In order to meet requirement (i) the USB Bus Power is used to control the RESET# Pin of the FT232R device. When the USB Host or Hub is powered up the internal 1.5kΩ resistor on USBDP is pulled up to 3.3V, thus identifying the device as a full speed device to USB. When the USB Host or Hub power is off, RESET# will go low and the device will be held in reset. As RESET# is low, the internal 1.5kΩ resistor will not be pulled up to 3.3V, so no current will be forced down USBDP via the 1.5kΩ pull-up resistor when the host or hub is powered down. To do this pin 14 (USB) is connected to PU2 and PU1 is connected to RST#. Failure to do this may cause some USB host or hub controllers to power up erratically.

Note : When the FT232R is in reset, the UART interface pins all go tri-state. These pins have internal 200kΩ pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.

Figure 5 is also an example of interfacing the FT232R to a Microcontroller (MCU) UART interface. This example uses TXD and RXD for transmission and reception of data, and RTS# / CTS# hardware handshaking.

Optionally, RI# can be connected to another I/O pin on the MCU and could be used to wake up the USB host controller from suspend mode. One of the CBUS pins could be configured as a 6/12/24/48 MHz clock output which can be used to clock the MCU. If the MCU is handling power management functions, then a CBUS pin can be configured as PWREN# and should also be connected to an I/O pin of the MCU.

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6.3 USB Bus Powered with Power Switching Configuration

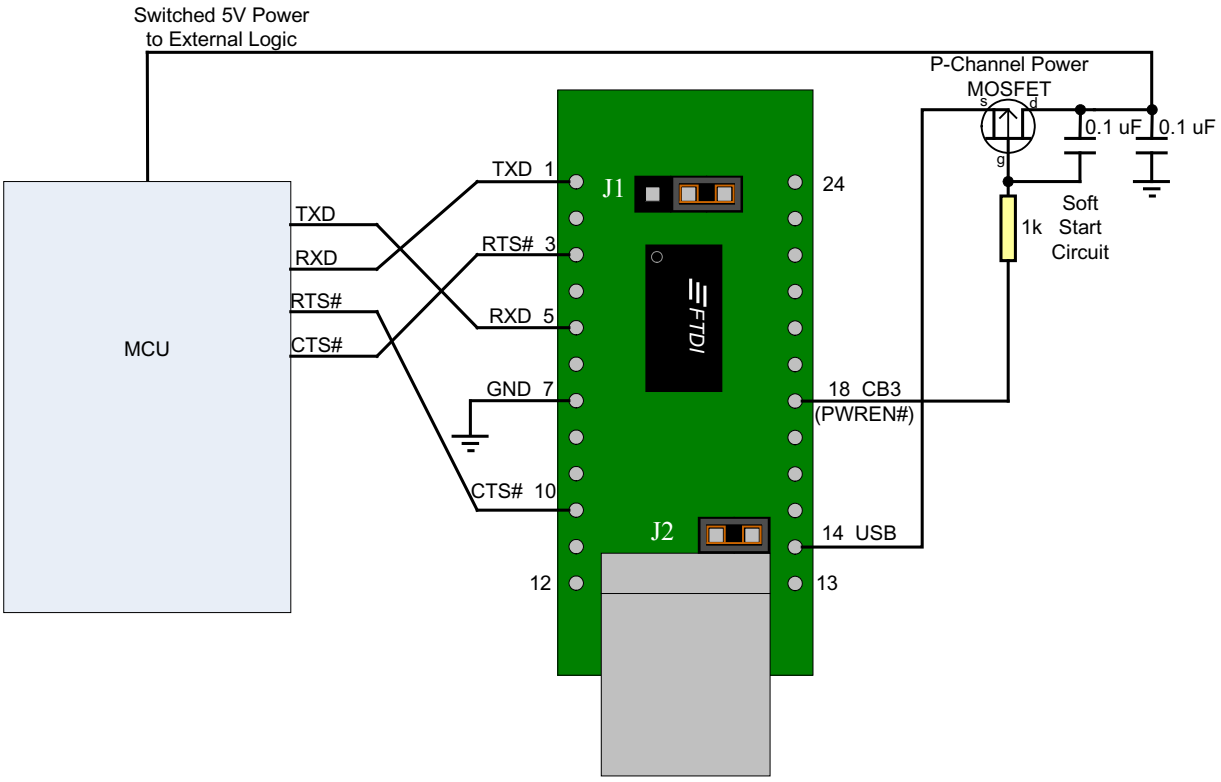


Figure 6 - Bus Powered with Power Switching Configuration

USB Bus powered circuits need to be able to power down in USB suspend mode in order to meet the <= 500µA total USB suspend current requirement (including external logic). Some external logic can power itself down into a low current state by monitoring the PWREN# signal. For external logic that cannot power itself down in this way, the FT232R provides a simple but effective way of turning off power to external circuitry during USB suspend.

Figure 6 shows how to use a discrete P-Channel Logic Level MOSFET to control the power to external logic circuits. A suitable device would be an International Rectifier (www.irf.com) IRLML6402, or equivalent. It is recommended that a “soft start” circuit consisting of a 1kΩ series resistor and a 0.1µF capacitor are used to limit the current surge when the MOSFET turns on. Without the soft start circuit there is a danger that the transient power surge of the MOSFET turning on will reset the FT232R, or the USB host / hub controller. The values used here allow attached circuitry to power up with a slew rate of ~12.5V per millisecond, in other words the output voltage will transition from GND to 5V in approximately 400 microseconds.

Alternatively, a dedicated power switch I.C. with inbuilt “soft-start” can be used instead of a MOSFET. A suitable power switch I.C. for such an application would be a Micrel (www.micrel.com) MIC2025-2BM or equivalent.

Please note the following points in connection with power controlled designs –

i) The logic to be controlled must have its own reset circuitry so that it will automatically reset itself when power is re-applied on coming out of suspend.

ii) Set the Pull-down on Suspend option in the internal EEPROM.

iii) One of the CBUS Pins should be configured as PWE# in the internal EEPROM, and should be used to switch the power supply to the external circuitry.

iv) For USB high-power bus powered device (one that consumes greater than 100mA, and up to 500mA of current from the USB bus), the power consumption of the device should be set in the max power field in the internal EEPROM. A high-power bus powered device must use this descriptor in the internal EEPROM to inform the system of its power requirements.

v) For 3.3V power controlled circuits the FT232R’s VCCIO pin must not be powered down with the external circuitry (the PWREN# signal gets its VCC supply from VCCIO). Either connect the power switch between the output of the 3.3V regulator and the external 3.3V logic or power VCCIO from the 3V3OUT pin of the FT232R.

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6.4 USB Bus Powered with 3.3V Logic Drive / IO Supply Voltage

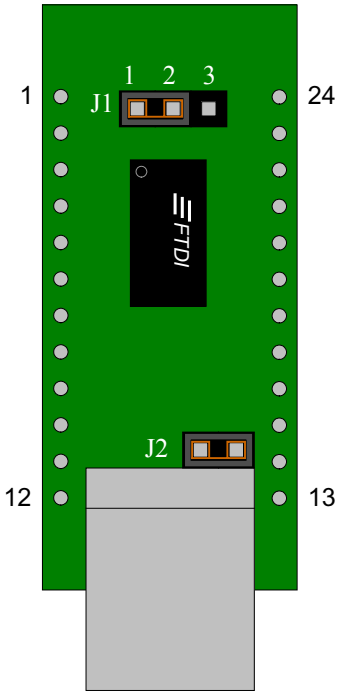


Figure 7 - USB Bus Powered 3.3V Logic Drive

Figure 7 shows a configuration where a jumper switch is used to allow the FT232R to be interfaced with a 3.3V or 5V logic devices. The FT232R's VCCIO pin is either supplied with 5V from the USB bus (connect together pins 2 and 3 on J1), or with 3.3V from the FT232R's 3V3OUT pin (connect together pins 1 and 2 on J1 as shown). The supply to UM232R's 3V3 pin can also be used to supply up to 50mA to external logic.

Please note the following in relation to bus powered designs of this type -

i) PWREN# or SLEEP# signals should be used to power down external logic during USB suspend mode, in order to comply with the limit of 500µA. If this is not possible, use the configuration shown in Section 6.3.

ii) The maximum current source from USB Bus during normal operation should not exceed 100mA, otherwise a bus powered design with power switching (Section 6.3) should be used.

Another possible configuration would be to use a discrete low dropout regulator which is supplied by the 5V on the USB bus to supply 2.8V - 1.8V to the VIO pin and to the external logic. VCC would be supplied with the 5V from the USB bus (available from the module's USB pin). With VIO connected to the output of the low dropout regulator, would in turn will cause the FT232R I/O pins to drive out at 2.8V - 1.8V logic levels.

For USB bus powered circuits some considerations have to be taken into account when selecting the regulator –

iii) The regulator must be capable of sustaining its output voltage with an input voltage of 4.35V. A Low Drop Out (L.D.O.) regulator must be selected.

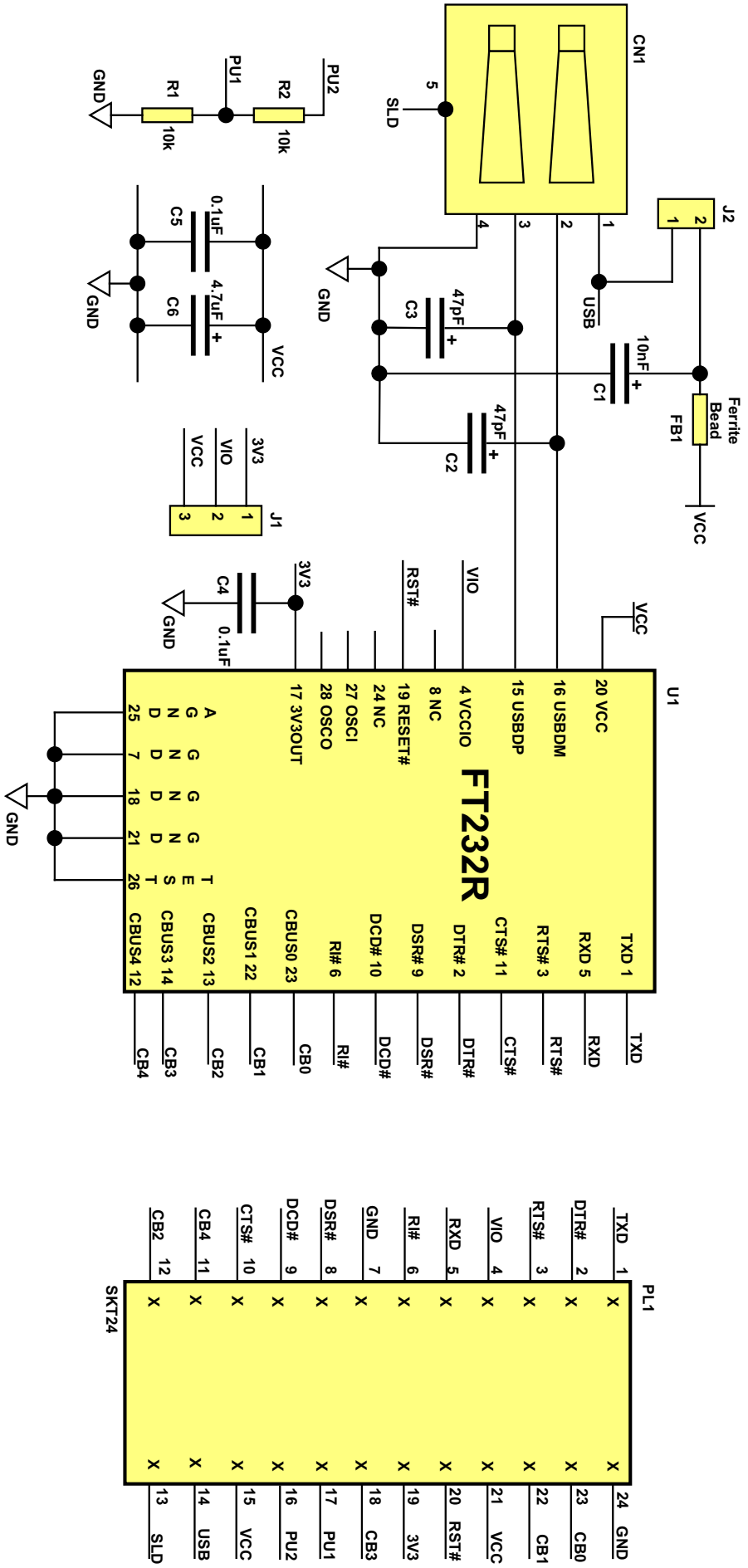
iv) The quiescent current of the regulator must be low in order to meet the USB suspend total current requirement of <= 500µA during USB suspend.

An example of a regulator family that meets these requirements is the MicroChip / Telcom TC55 Series of devices (www.microchip.com). These devices can supply up to 250mA current and have a quiescent current of under 1µA.

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7. UM232R Module Circuit Schematic

Figure 8 - Module Circuit Schematic



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8. Internal EEPROM Configuration

Following a power-on reset or a USB reset the FT232R will scan its internal EEPROM and read the USB configuration descriptors stored there. The default values programmed into the internal EEPROM in the FT232RL used on the UM232R are shown in Table 17.

Table 17 - Default Internal EEPROM Configuration

Parameter	Value	Notes
USB Vendor ID (VID)	0403h	FTDI default VID (hex)
USB Product ID (PID)	6001h	FTDI default PID (hex)
Serial Number Enabled?	Yes	
Serial Number	*See Note*	A unique serial number is generated and programmed into the EEPROM during final test of the UM232R module.
Pull Down I/O Pins in USB Suspend	Disabled	Enabling this option will make the device pull down on the UART interface lines when the power is shut off (PWREN# is high)
Manufacturer Name	FTDI	
Manufacturer ID	FT	Serial Number prefix.
Product Description	UM232R USB <-> Serial	
Max Bus Power Current	100mA	
Power Source	Bus Powered	
Device Type	FT232R	
USB Version	0200	Returns USB 2.0 device descriptor to the host. Note: The device is be a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).
Remote Wake up	Enabled	Taking RI# low will wake up the USB host controller from suspend.
High Current I/Os	Disabled	Enables the high drive level on the UART and CBUS I/O pins
Load VCP Driver	Enabled	Makes the device load the VCP driver interface for the device.
CBUS0	TXLED#	Default configuration of CBUS0 - Transmit LED drive
CBUS1	RXLED#	Default configuration of CBUS1 - Receive LED drive
CBUS2	PWREN#	Default configuration of CBUS2 - Power enable. Low after USB enumeration, high during USB suspend.
CBUS3	PWREN#	Default configuration of CBUS3 - Power enable. Low after USB enumeration, high during USB suspend.
CBUS4	SLEEP#	Default configuration of CBUS4 - Low during USB suspend.
Invert TXD	Disabled	Signal on this pin becomes TXD# if enabled.
Invert RXD	Disabled	Signal on this pin becomes RXD# if enabled.
Invert RTS#	Disabled	Signal on this pin becomes RTS if enabled.
Invert CTS#	Disabled	Signal on this pin becomes CTS if enabled.
Invert DTR#	Disabled	Signal on this pin becomes DTR if enabled.
Invert DSR#	Disabled	Signal on this pin becomes DSR if enabled.
Invert DCD#	Disabled	Signal on this pin becomes DCD if enabled.
Invert RI#	Disabled	Signal on this pin becomes RI if enabled.

The internal EEPROM in the FT232R can be programmed over USB using the utility program MPROG. MPROG can be downloaded from the FTDI website. Version 2.8a or later is required for the FT232R chip. Users who do not have their own USB Vendor ID but who would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs. Contact FTDI support for this service.

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Version 0.9 - Initial Datasheet Created August 2005
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Version 1.01 - Circuit schematic diagram updated January 2006
Version 1.02 - Module PCB length dimensions January 2006

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