DM631B

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16-CHANNEL CONSTANT CURRENT LED DRIVER

WITH 12-bit PROGRAMMABLE PWM OUTPUTS

Preliminary

新竹市科學園區展業一路 9 號 7 樓之 1
SILICON TOUCH TECHNOLOGY INC.
9-7F-1, Prosperity Road I, Science Based Industrial Park,
Hsin-Chu, Taiwan 300, R.O.C.
Tel：886-3-5645656 Fax：886-3-5645626

點晶科技股份有限公司
SILICON TOUCH TECHNOLOGY INC.
新竹市科學園區展業一路 9 號 7 樓之 1
9-7F-1, Prosperity Road I , Hsin-Chu, Taiwan, R.O.C.
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DM631B

16-CHANNEL CONSTANT CURRENT LED DRIVER WITH 12-bit PROGRAMMABLE PWM OUTPUTS

General Description

DM631B is a 16-channel constant current sink LED driver. Each channel has independent 12-bits (4096 steps) grayscale PWM control current outputs. It incorporates shift registers, data latches, constant current circuitry with current value set by an external resistor, and built-in LED open detection circuit to detect error status. It combines the selections with rising / falling edge serial out, auto-reload/one-shot PWM output, internal/external grayscale clock source. It is specifically designed for LED display or lighting applications.

Features

- Constant-current outputs: 5mA to 60mA adjustable by one external resistor
- 12-bit linear PWM control current outputs for each channel
- Maximum output voltage: 17V
- Maximum clock frequency: 25MHz
- Auto-Reload / One-Shot Mode selection.
- Serial out clock edge selection – Rising / Falling edge selection
- Internal / External PWM clock mode selection
- Built-in real-time open detection
- Package and pin assignment compatible to conventional LED drivers (DM134/5/6, DM13C)
- Power supply voltage: 3.3V to 5V
- Schmitt Trigger input
- Output channel delay

Applications

- Indoor/Outdoor LED Video Display
- LED Variable Message Signs (VMS) System
- LED Decorative Lighting

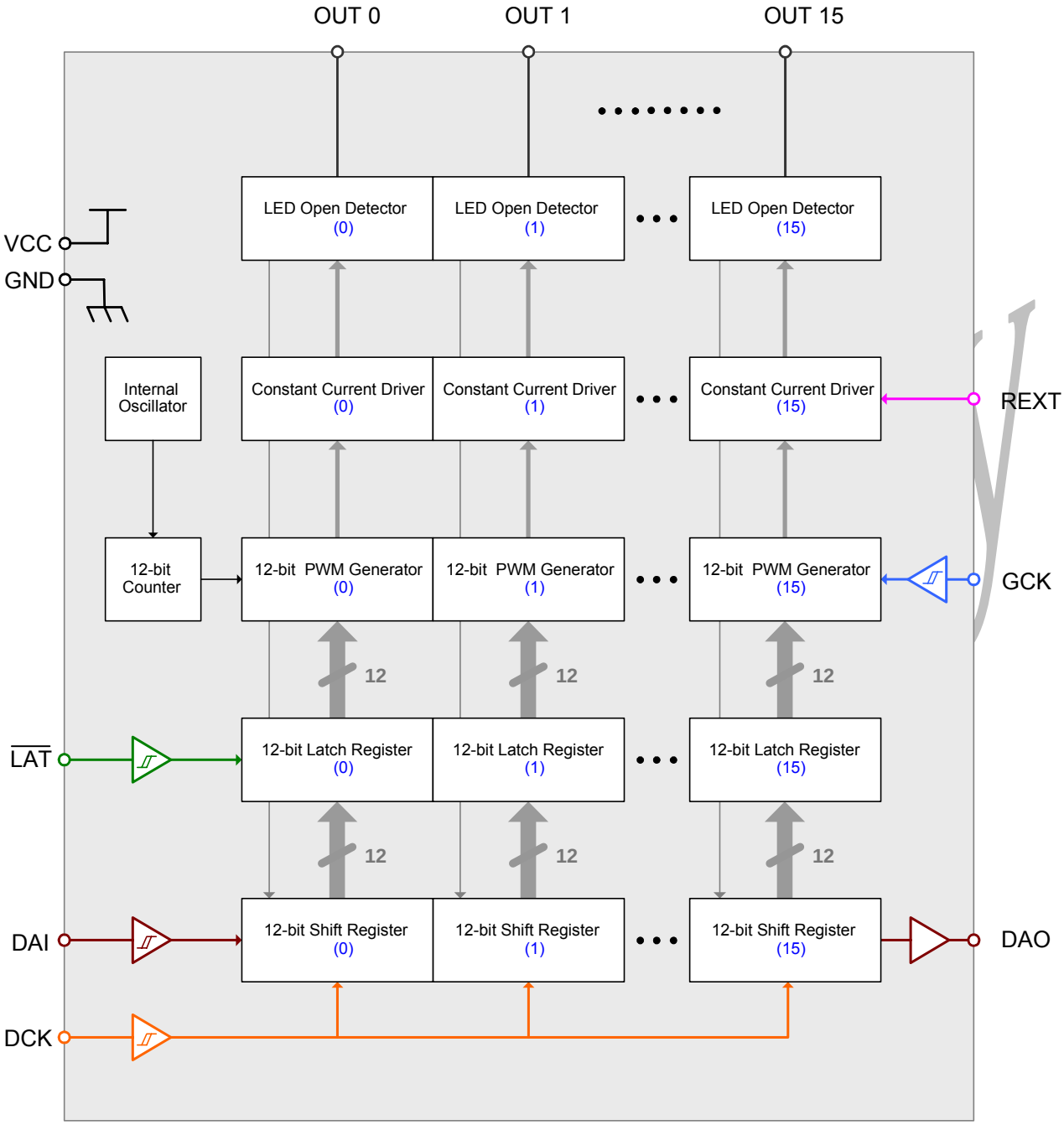
Package Types

- DIP24B, SOP24B, SSOP24, TSSOP24E (with exposed pad)

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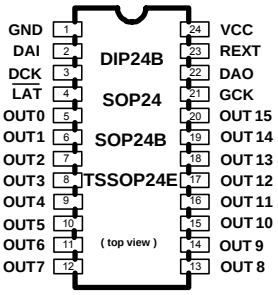
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Block Diagram



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Pin Connection



Pin Description

PIN No.	PIN NAME	FUNCTION
SOP24B/SSOP24/TSSOP24E: 1 TSSOP24E: exposed pad	GND	Ground terminal.
SOP24B/SSOP24/TSSOP24E: 2	DAI	Serial data input terminal.
SOP24B/SSOP24/TSSOP24E: 3	DCK	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of DCK.
SOP24B/SSOP24/TSSOP24E: 4	$\overline{\text{LAT}}$	Input terminal of data strobe: '**H**' means data on shift register goes through latch (level trigger), all outputs off and counter reset immediately '**L**' means data is latched.
SOP24B/SSOP24/TSSOP24E: 5~20	OUT0~15	Sink constant-current outputs (open-drain).
SOP24B/SSOP24/TSSOP24E: 21	GCK	Gray Scale Clock (GCK) : Input terminal for PWM operation.
SOP24B/SSOP24/TSSOP24E: 22	DAO	Serial data output terminal. Data shift out at the rising edge of DCK in REM[*1] (default), or data shift out at the falling edge of DCK in FEM[*2].
SOP24B/SSOP24/TSSOP24E: 23	REXT	External resistors connected between REXT and GND for output current value setting.
SOP24B/SSOP24/TSSOP24E: 24	VCC	Supply voltage terminal.

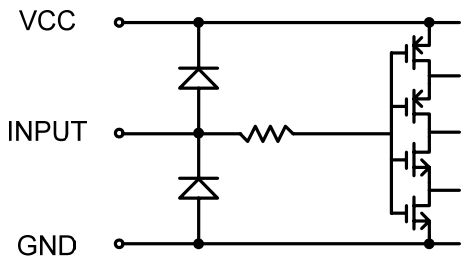
[*]1 Rising Edge Mode
[*]2 Falling Edge Mode

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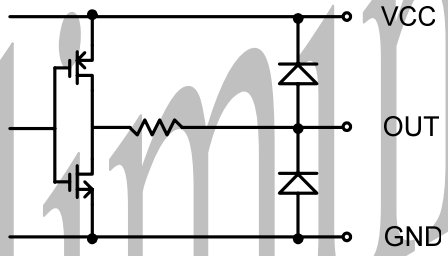
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Equivalent Circuit of Inputs and Outputs

1. DCK, DAI, $\overline{LAT}$, GCK terminals



2. DAO terminals



PCB Layout Consideration

To connect an external resistor to REXT pin and ground can determine the maximum output current. If there is any disturbance occurred to REXT pin, the constant current output may be unstable or has noise happened. Since REXT (pin23), DAO (pin22), and GCK (pin21) are next to each other, the most possible interference is caused by DAO or GCK signal. Accordingly, it is recommended that adding some shielding area within the above pins in PCB layout, or laying the signal line of above pins on different PCB layer will prevent the noise problems effectively.

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Maximum Ratings (Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VCC	-0.3 ~ 7.0	V
Input Voltage	VIN	-0.3 ~ VCC+0.3	V
Output Current	IOUT	70	mA
Output Voltage	VOUT	-0.3 ~ 17	V
Input Clock Frequency	FDCK	25	MHz
GND Terminal Current	IGND	1120	mA
Power Dissipation (4 layer PCB, at Ta=25℃)	PD	4.17 (TSSOP24E exposed pad)	W
		2.19 (SOP24B)	
		1.87 (DIP24B)	
		1.79 (SSOP24)	
Thermal Resistance (4 layer PCB, at Ta=25℃)	Rth(j-a)	30 (TSSOP24E exposed pad)	°C/W
		57 (SOP24B)	
		67 (DIP24B)	
		70 (SSOP24)	
Operating Temperature	Top	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VCC	—	3.3	5.0	5.5	V
Output Voltage	VOUT	Driver On *1	1.0	—	0.5VCC	V
Output Voltage	VOUT	Driver Off *2	—	—	17	
Output Current	IO	OUTn	5	—	60	mA
	IOH	VOH = VCC – 0.4 V	—	—	+1.5	
	IOL	VOL = 0.2 V	—	—	-1.5	
Input Voltage	VIH	VCC = 3.3 V ~ 5.5V	0.8VCC	—	VCC	V
	VIL		0.0	—	0.2VCC	
Input Clock Frequency	FDCK	Single Chip Operation	—	—	25	MHz
Input PWM Frequency	FGCK	3.3V~5.5V	—	—	25	
$\overline{LAT}$ Pulse Width	tw $\overline{LAT}$	VCC = 5.0V	15	—	—	ns
DCK Pulse Width	tw DCK		15	—	—	
Set-up Time for DAI	tsetup(D)		10	—	—	
Hold Time for DAI	thold(D)		10	—	—	
Set-up Time for $\overline{LAT}$	tsetup(L)		10	—	—	
Hold Time for $\overline{LAT}$	thold(L)		360 *3	—	—	

*1 Notice that the power dissipation is limited to its package and ambient temperature.
*2 The driver output voltage including any overshoot stress has to be compliant with the maximum voltage (17V).
*3 Due to open detection operation and output channel delay consideration.

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Electrical Characteristics (VCC = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leakage Current	IOL	VOH = 17 V	—	—	±1.0	uA
Output Voltage (S-OUT)	VOL	IOL = 1.25 mA	—	—	0.4	V
	VOH	IOH= 1.4 mA	VCC-0.2	—	—	
Output Current Skew (Channel-to-Channel) *1	IOL1	VOUT = 1.0 V Rrext = 2.2 KΩ	—	—	±3	%
Output Current Skew (Chip-to-Chip) *2	IOL2		TBD	TBD	TBD	mA
Output Voltage Regulation	% / VOUT	Rrext = 2.2 KΩ VOUT = 1 V ~ 3 V	—	±0.1	±0.5	% / V
Supply Voltage Regulation	% / VCC	Rrext = 2.2 KΩ	—	±1	±4	
LED Open Detection Threshold	V(od)	all outputs turn on	—	0.2	—	V
Supply Current *3	$I_{DD(off)}$	power on all pins are open unless VCC and GND (internal GCK mode	—	5.5	—	mA
	$I_{DD(off)}$	power on all pins are open unless VCC and GND (external GCK mode)	—	5.0	—	
	$I_{DD(on)}$	input signal is static Rrext = 12.4 KΩ all outputs turn off	—	6.0	—	
	$I_{DD(on)}$	input signal is static Rrext = 2.2 KΩ all outputs turn off	—	8.5	—	
	$I_{DD(on)}$	input signal is static Rrext = 570 Ω all outputs turn off	—	17.5	—	

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*1 Channel-to-channel skew is defined as the ratio between (any Iout – average Iout) and average Iout, where average Iout = (Imax + Imin) / 2.
*2 Chip-to-Chip skew is defined as the range into which any output current of any IC falls.
*3 IO excluded.

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Electrical Characteristics (VCC = 3.3 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leakage Current	IOL	VOH = 17 V	-1.0	—	+1.0	uA
Output Voltage (S-OUT)	VOL	IOL = 1.25 mA	—	—	0.4	V
	VOH	IOH= 1.4 mA	VCC-0.2	—	—	
Output Current Skew (Channel-to-Channel) *1	IOL1	VOUT = 1.0 V Rrext = 2.2 KΩ	—	—	±3	%
Output Current Skew (Chip-to-Chip) *2	IOL2		TBD	TBD	TBD	mA
Output Voltage Regulation	% / VOUT	Rrext = 2.2 KΩ VOUT = 1 V ~ 3 V	—	±0.1	±0.5	% / V
Supply Voltage Regulation	% / VCC	Rrext = 2.2 KΩ	—	±1	±4	
LED Open Detection Threshold	V(od)	all outputs turn on	—	0.2	—	V
Supply Current *3	$I_{DD(off)}$	power on all pins are open unless VCC and GND (internal GCK mode)	—	4.5	—	mA
	$I_{DD(off)}$	power on all pins are open unless VCC and GND (external GCK mode)	—	4.2	—	
	$I_{DD(on)}$	input signal is static Rrext = 12.4 KΩ all outputs turn off	—	5.5	—	
	$I_{DD(on)}$	input signal is static Rrext = 2.2 KΩ all outputs turn off	—	7.0	—	
	$I_{DD(on)}$	input signal is static Rrext = 570 Ω all outputs turn off	—	15.0	—	

Preliminary

*1 Channel-to-channel skew is defined as the ratio between (any Iout – average Iout) and average Iout, where average Iout = (Imax + Imin) / 2.
*2 Chip-to-Chip skew is defined as the range into which any output current of any IC falls.
*3 IO excluded.

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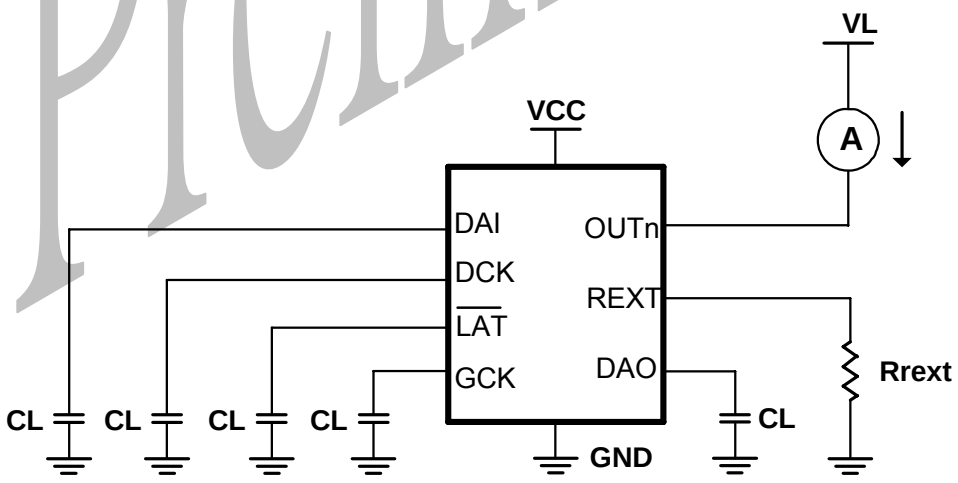
Switching Characteristics (VCC = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L' to 'H')	GCK-to-OUT	tpLH	VIH = VCC VIL = GND Rrext = 2.2 KΩ VL = 5.0 V CL = 13 pF	—	45.7	—	ns
	DCK(rising edge)-to-DAO			—	36	—	
	DCK(falling edge)-to-DAO			—	16	—	
Propagation Delay ('H' to 'L')	GCK-to-OUT	tpHL		—	23.8	—	
	DCK(rising edge)-to-DAO			—	28	—	
	DCK(falling edge)-to-DAO			—	14	—	
Output Current Rise Time		tor		—	18	—	
Output Current Fall Time		tof		—	7.0	—	
Output Delay Time Unit		Td		—	20	—	

Switching Characteristics (VCC = 3.3V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
0Propagation Delay ('L' to 'H')	GCK-to-OUT	tpLH	VIH = VCC VIL = GND Rrext = 2.2 KΩ VL = 3.3 V CL = 13 pF	—	48.8	—	ns
	DCK(rising edge)-to-DAO			—	23	—	
	DCK(falling edge)-to-DAO			—	23	—	
Propagation Delay ('H' to 'L')	GCK-to-OUT	tpHL		—	29.6	—	
	DCK(rising edge)-to-DAO			—	21	—	
	DCK(falling edge)-to-DAO			—	20	—	
Output Current Rise Time		tor		—	20	—	
Output Current Fall Time		tof		—	8.3	—	
Output Delay Time Unit		Td		—	30	—	

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Switching Characteristics Test Circuit

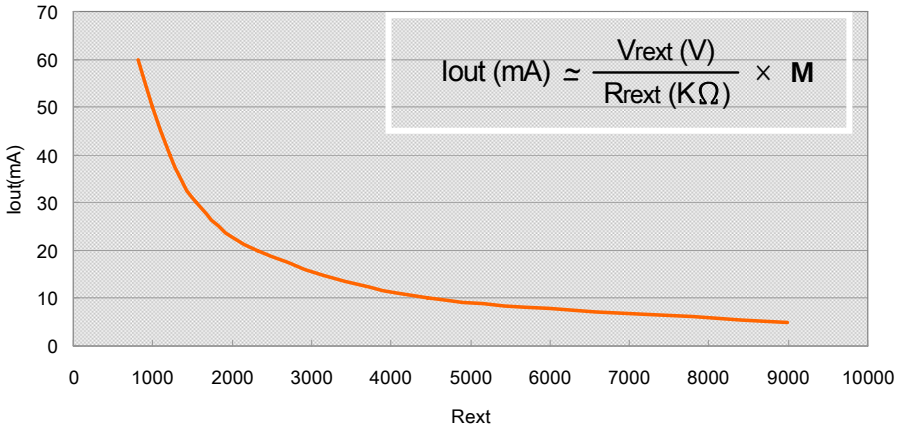
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Constant-Current Output

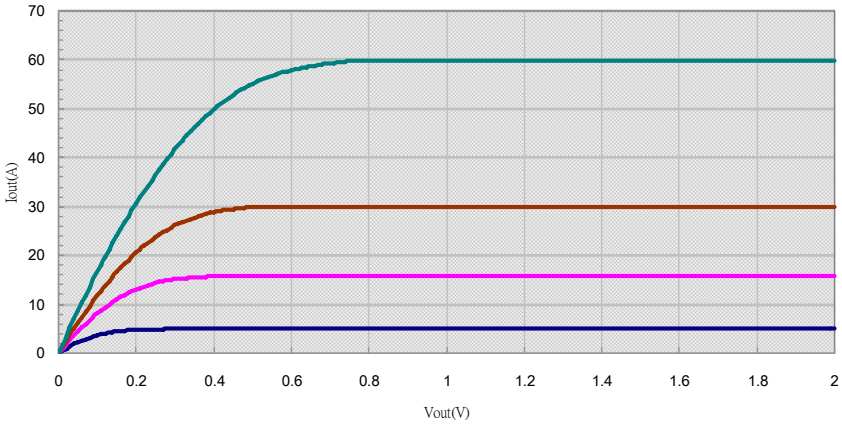
Constant-current value (Iout[*1]) of each output channel is set by an external resistor connected between the REXT pin and GND. The current scale ranging can be adjusted from 5mA to 60mA by varying the resistor value. The reference voltage of REXT terminal (Vrext) is approximately 1.23V. The output current value is calculated by the following equation:

Iout(mA)	5	10	20	30	40	50	60
M	37.11	36.29	37.55	39.03	40.36	40.4	41.28

Output current as a function of Rext value



Output Current as a function of Output Voltage



In order to obtain a good performance of constant-current output, a suitable output voltage is necessary. Users can get related information about the minimum output voltage above.

[*1] Iout is typical current value setting under 100% PWM duty cycle .

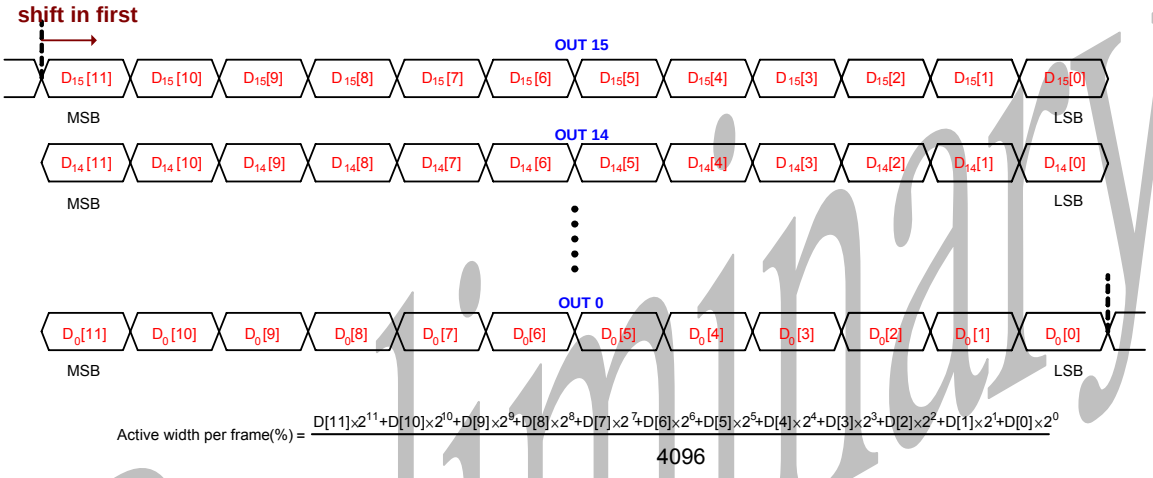
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Serial Data Interface

The serial-in data (DAI) data will be clocked into 16 × 12 bit shift registers synchronized on the rising edge of the clock (DCK). The data will be transferred into the 16 × 12 bit latch registers when the strobe signal ($\overline{LAT}$) is kept at high level (level trigger); Otherwise, the data will be held. The latch pulse should be sent after the falling edge of the last clock within one frame data. The serial-out data (DAO) will be shifted out on synchronization of the clock (DCK).

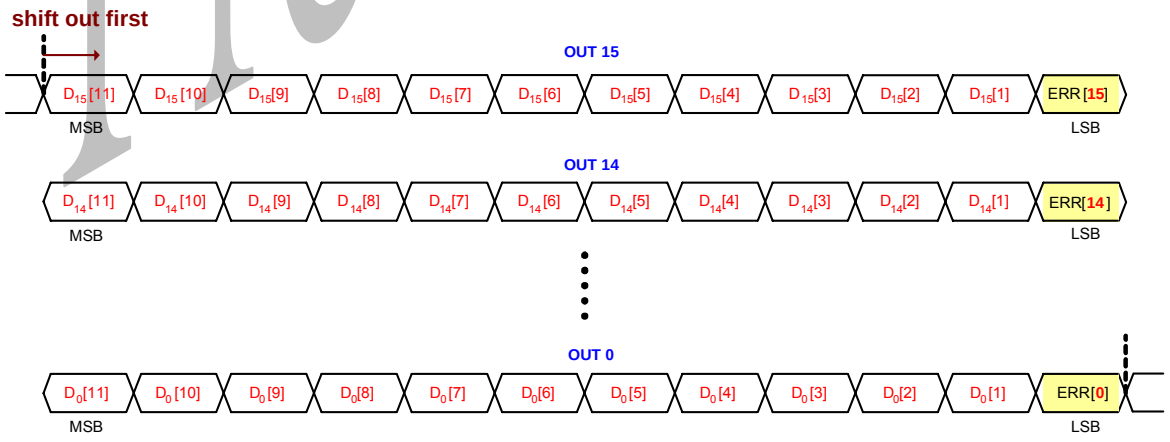
Input Data clock-in sequence

The sequence of the grayscale PWM luminous data of a driver showed as following diagram. The input data sequence of input data is from the MSB of OUT15 (D15 [11:0]) to the LSB of OUT0 (D0 [11:0]) by time passing.



Serial-out Data clock-out sequence

The data serial out from DAO include latched grayscale data and the LSB of each output data covered by detection message (ERR) after $\overline{LAT}$ pulse be active. The serial out sequence of the data is from the MSB of OUT15 (D15 [11:0]) to the LSB of OUT0 (D0 [11:0]) by time passing.



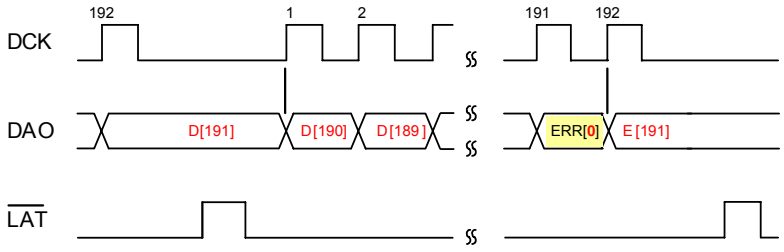
*ERR[11], ERR[10],⋯ ,ERR[0] are Error Message of LED Open Detection. ‘1’ is normal, and ‘0’ is abnormal.

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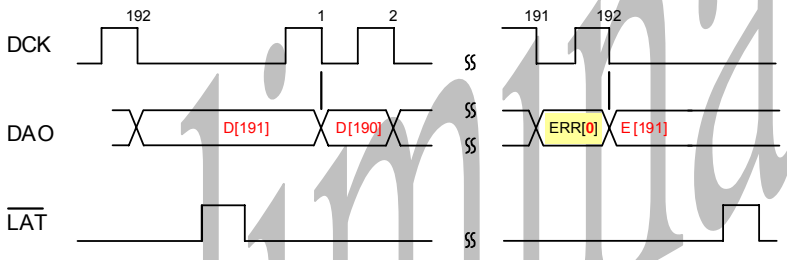
Rising/Falling Edge Mode selection

The luminous data serial out from DAO by data clock (DCK) as following waveform. In rising edge mode (REM), the data serial out by the rising edge of DCK.



Rising Edge Mode (REM)
DAO serial out by DCK rising edge.

In falling edge mode (FEM), the data serial out by the falling edge of DCK.



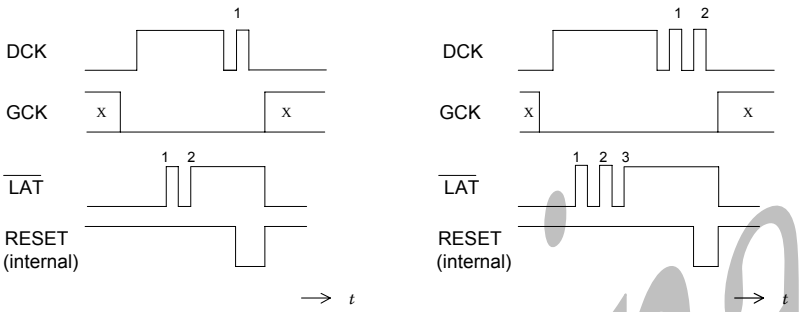
Falling Edge Mode (FEM) :
DAO serial out by DCK falling edge.

*D[191], D[190],…D[0], E[191] are clock-in data in Shift data register of driver

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The default mode is the Rising-Edge Mode (REM[*1]) after power-on. Users could do mode select between REM and FEM[*2] by following timing sequence. The option 1 shows two rising edge of latch pulses ($\overline{LAT}$) when the data-input clock (DCK) kept at high level then sending one rising edge of DCK pulses when $\overline{LAT}$ kept at high level. Then we can receive serial-out data from the data-output signal (DAO) at falling edge of DCK after the falling edge of $\overline{LAT}$. The option 2 shows three rising edge of $\overline{LAT}$ when DCK kept at high level then sending two rising edge of DCK, while $\overline{LAT}$ kept high level at the same time. After the falling edge of $\overline{LAT}$, we receive serial-out data from DAO at rising edge of DCK (REM). Notice that when internal RESET at low level, all the shift registers in DM631B will be cleared (Kept at Low level).

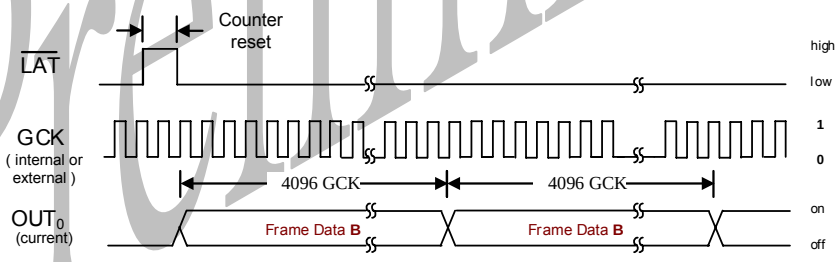


Option 1 ： Signals Combination to set up Falling-Edge Mode (FEM)

Option 2 ： Signals Combination to set up Rising-Edge Mode (REM)

Auto-Reload/One-Shot Mode selection

The Auto-Reload mode (ARM) in DM631B means outputs can repeat the grayscale PWM cycle over and over. It can decrease the data amount greatly compare to non-PWM function driver operated in grayscale PWM application.



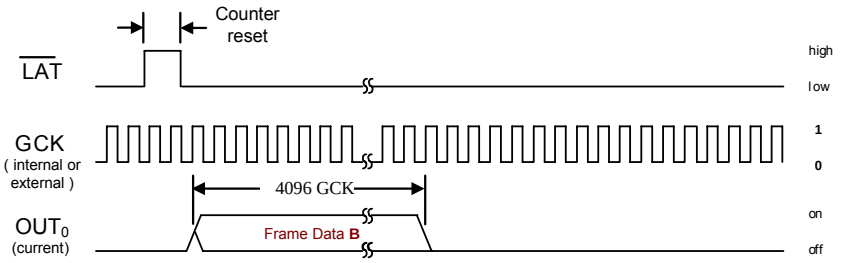
Auto-Reload Mode (ARM).

The One-Shot Mode in DM631B means each output shows one grayscale PWM cycle following one latch pulse. The grayscale PWM cycle starts with the falling edge of $\overline{LAT}$ signal. The first GCK pulse after $\overline{LAT}$ increases the grayscale counter by one and switches on all outputs with grayscale value. It makes driver synchronous control easily.

*1 REM switch to FEM timing diagram, please refer to page 16.
*2 FEM switch to REM timing diagram, please refer to page 17.

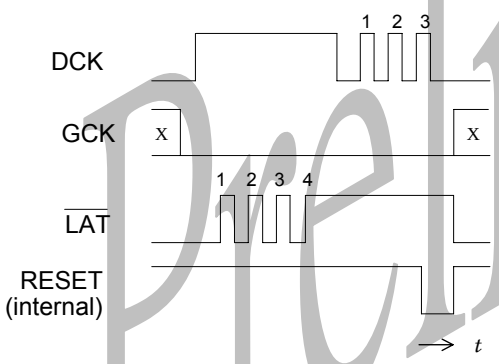
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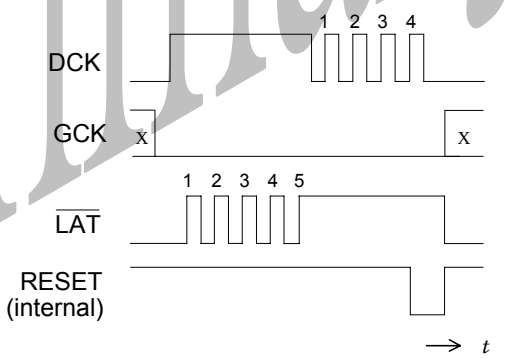


One-Shot Mode (OSM)

The default mode is the Auto-Reload Mode (ARM[*1]) after power-on. Users could do mode select between ARM and One-Shot Mode (OSM[*2]) by following timing sequence. The gray scale clock signal (GCK) should keep at low during this mode selection process. The option 1 shows four rising edges of latch pulse ($\overline{LAT}$) when the data-input clock (DCK) kept at high level then three rising edges of DCK when $\overline{LAT}$ kept at high level. Then DM631B starts OSM after the falling edge of $\overline{LAT}$. The option 2 shows five rising edges of $\overline{LAT}$ when DCK kept at high level then sending four rising edges of DCK signal, while $\overline{LAT}$ signal kept high level . After falling edge of $\overline{LAT}$, DM631B switch to ARM . Notice that when internal RESET at low level, all the shift registers in DM631B will be cleared (Kept at Low level) .



Option 1 : Signals Combination to set up One-Shot Mode (OSM)



Option 2 : Signals Combination to set up Auto-Reload Mode (ARM)

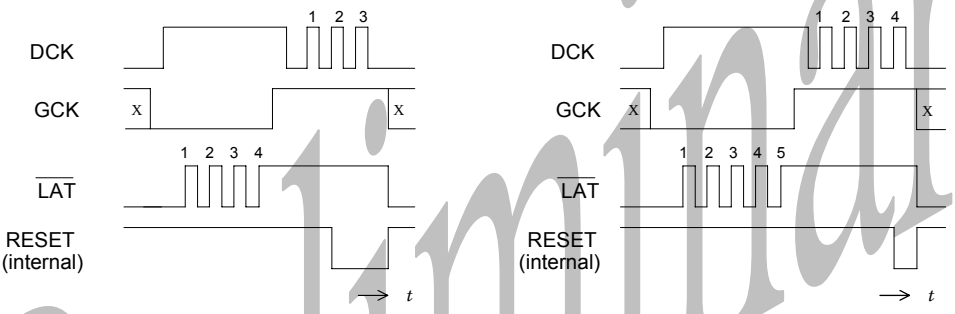
Preliminary

[*1] ARM switch to OSM timing diagram, please refer to page 18.
[*2] OSM switch to ARM timing diagram, please refer to page 19.

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Internal/External Clock Mode selection

Grayscale luminous of each channel comes from comparisons of grayscale PWM luminous data and grayscale counter value. In internal-clock mode, DM631B provides build-in oscillator for counter operation. In external-clock mode, the clock source of counter is from control system through GCK pin. The default mode is the Internal-Clock Mode(ICM*1) after power-on. Users could do mode select between ICM and External-Clock Mode (ECM*2) by following timing sequence. The option 1 shows four rising edges of latch pulses ($\overline{LAT}$) when the data clock (DCK) kept at high level and the grayscale clock (GCK) kept at low then sending three rising edges of DCK when $\overline{LAT}$ and GCK both kept at high level. Then we can input external gray scale clock from GCK pin to operate grayscale PWM function after the falling edge of $\overline{LAT}$. The option 2 shows five rising edges of $\overline{LAT}$ when DCK kept at high level and GCK at low level then sending four rising edges of DCK , while $\overline{LAT}$ and GCK kept at high level . After the falling edge of $\overline{LAT}$, grayscale PWM function operates by internal gray scale clock generator. Notice that when internal RESET at low level, all the shift registers in DM631B will be cleared (Kept at Low level).



Option1 : Signals Combination to set up External-Clock Mode (ECM)

Option 2 : Signals Combination to set up Internal-Clock Mode (ICM)

LED Open Detection

DM631B provides a real time monitor of LED open detection function without extra components or circuit design. It will be identified as a LED open failure when the output is turned on but the output voltage is below 0.2V. The test result of each channel will write to its correspondent shift register which is in LSB position (ERR[11], ERR[10], …., ERR[0]) while strobe signal is active. User can refer to timing diagram on page11. Detecting report could be retrieved from serial-out (DAO) data. If the system reads '1' back, that indicates LED is in normal status. But if '0' was retrieved then LED open failure has occurred. In order to make sure LED open detection function is in well operating condition, thold(L)*3 should larger then 360n sec(typ) due to the build-in delay between outputs. And it is recommended that all the luminance data wrote to '1' during detection.

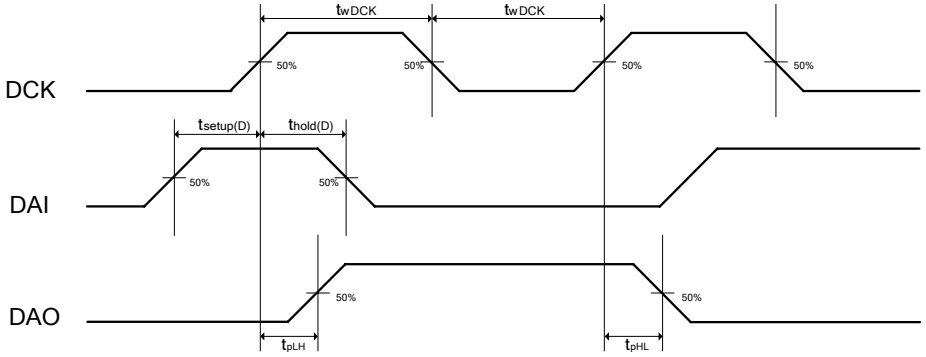
*1 ICM switch to ECM timing diagram, please refer to page 20.
*2 ECM switch to ICM timing diagram, please refer to page 21
*3 Hold time between $\overline{LAT}$ and DCK, please refer to page 15.

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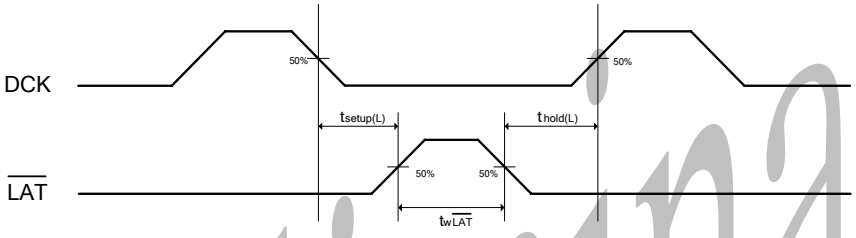
Preliminary

Timing Diagram

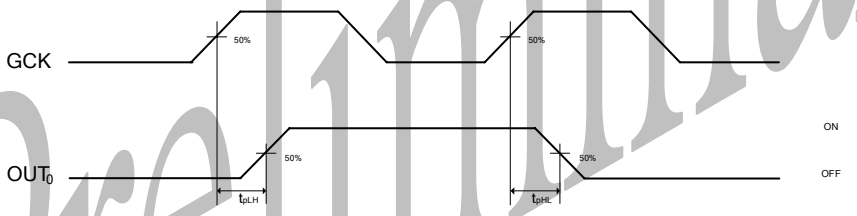
1. DCK-DAI, DAO



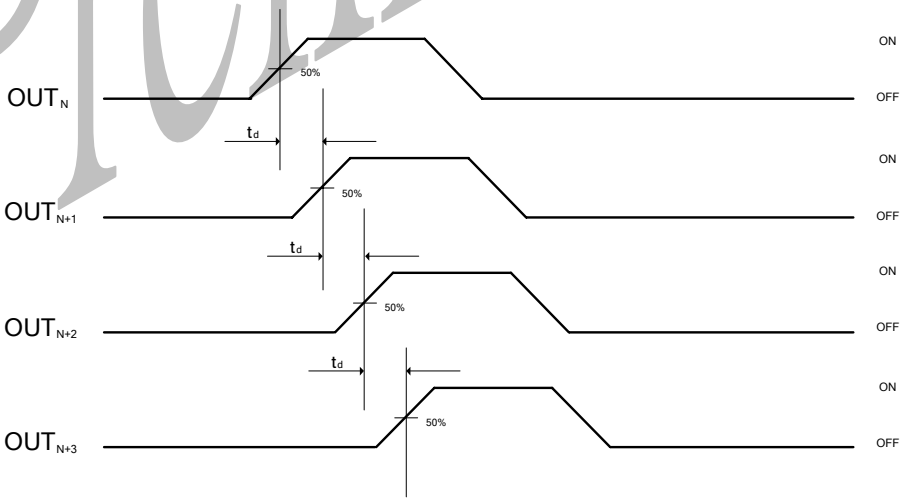
2. DCK-$\overline{LAT}$



3. GCK-OUT_0



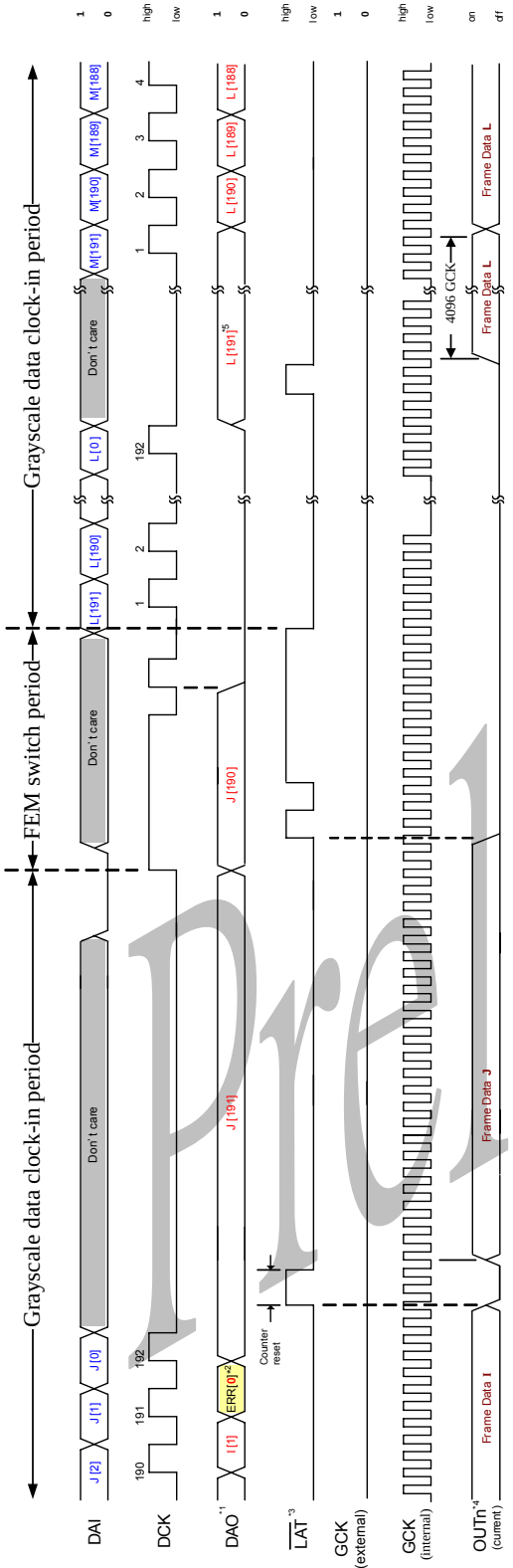
4. Output Delay Time Unit (N=0, 4, 8, 12)



Preliminary

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Timing Diagram (Rising-Edge Mode switch to Falling-Edge Mode)



*1 REM, ARM, ICM is configered by default. They can switch to FEM, OSM, ECM accordingly.
All registers in DM631B with be reset when any switch procees occur.

*2 ERR[0] is the error message of LED open detection.

*3 $\overline{LAT}$ is level trigger, not edge trigger.

*4 Iout turn off when $\overline{LAT}$ is high level ,and turn on at the first GCK rising edge when $\overline{LAT}$ is low level.

*5 J[191],J[190],J[2],J[1],J[0],I[1],L[191],L[190],… L[0],M[191],M[190],… are serial data for DM631B.

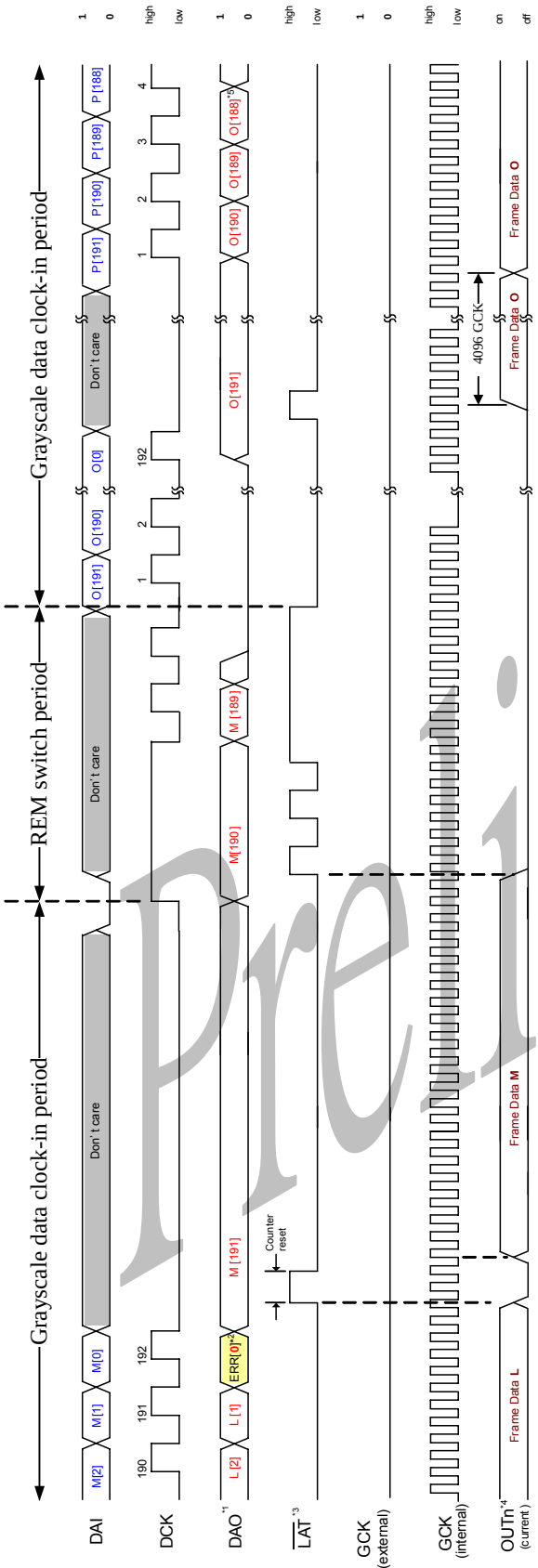
$$\text{Refresh Rate (Hz)} = \frac{\text{Input GCK Frequency (Hz)}}{\text{Total PWM resolution } (2^{12})}$$

For example, if the refresh rate in display system is higher than 60Hz, the input GCK frequency must be higher than 246kHz.

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Timing Diagram (Falling-Edge Mode switch to Rising-Edge Mode)



*1 REM, ARM, ICM is configered by default. They can switch to FEM, OSM, ECM accordingly.
All registers in DM631B with be reset when any switch procees occur.

*2 ERR[0] is the error message of LED open detection.

*3 $\overline{LAT}$ is level trigger, not edge trigger.

*4 Iout turn off when $\overline{LAT}$ is high level ,and turn on at the first GCK rising edge when $\overline{LAT}$ is low level.

*5 M[191],M[190],… M[0],L[2],L[1],O[191].O[190],… O[0],P[191],P[190],… are serial data for DM631B.

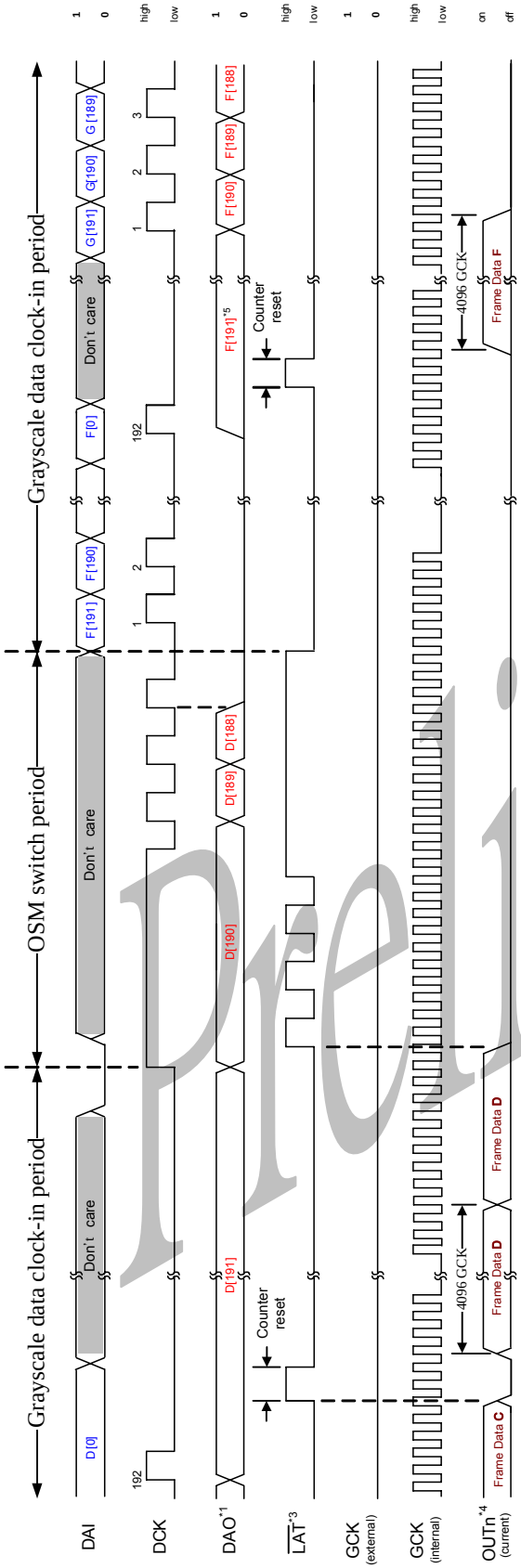
$$\text{Refresh Rate (Hz)} = \frac{\text{Input GCK Frequency (Hz)}}{\text{Total PWM resolution } (2^{12})}$$

For example, if the refresh rate in display system is higher than 60Hz, the input GCK frequency must be higher than 246kHz.

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Timing Diagram (Auto-Reload Mode switch to One-Shot Mode)



*1 REM, ARM, ICM is configed by default. They can switch to FEM, OSM, ECM accordingly.
All registers in DM631B with be reset when any switch proces occur.

*2 ERR[0] is the error message of LED open detection.

*3 $\overline{LAT}$ is level trigger, not edge trigger.

*4 Iout turn off when $\overline{LAT}$ is high level ,and turn on at the first GCK rising edge when $\overline{LAT}$ is low level.

*5 D[191],D[190],··· D[0],F[191],F[190],...F[0],G[191],G[190],··· are serial data for DM631B.

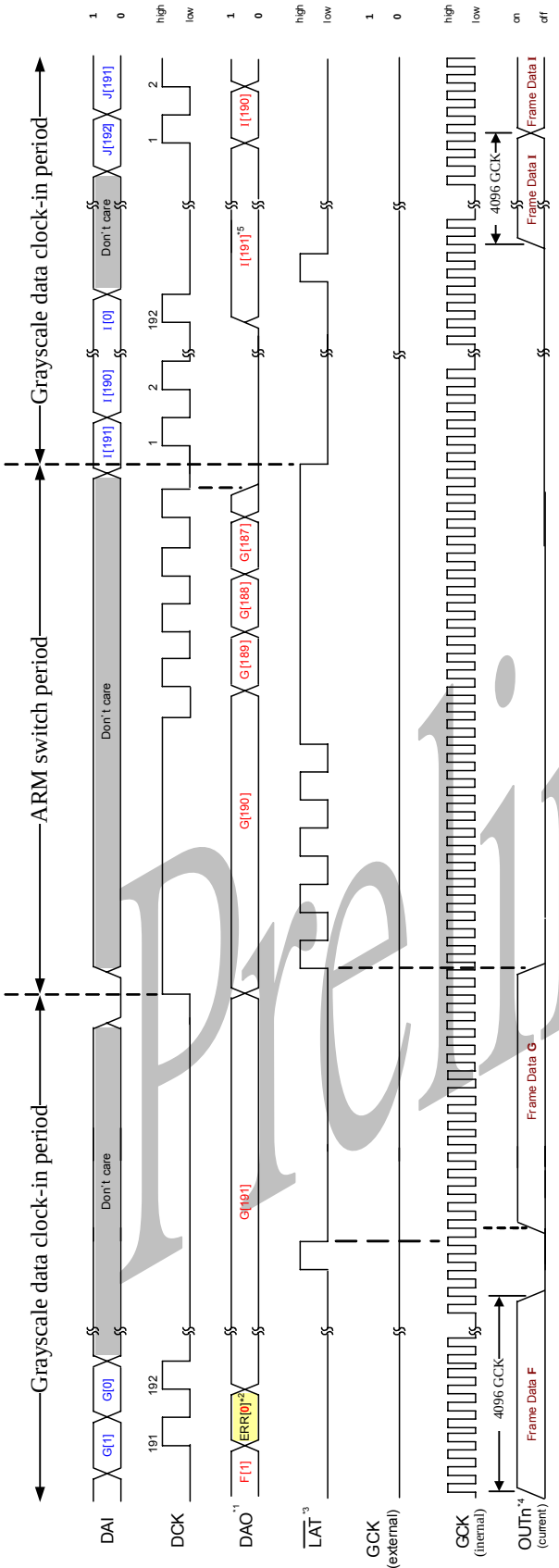
$$\text{Refresh Rate (Hz)} = \frac{\text{Input GCK Frequency (Hz)}}{\text{Total PWM resolution } (2^{12}) }$$

For example, if the refresh rate in display system is higher than 60Hz, the input GCK frequency must be higher than 256kHz.

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Timing Diagram (One-Shot Mode switch to Auto-Reload Mode)



*1 REM, ARM, ICM is configered by default. They can switch to FEM, OSM, ECM accordingly.
All registers in DM631B with be reset when any switch procees occur.

*2 ERR[0] is the error message of LED open detection.

*3 $\overline{LAT}$ is level trigger, not edge trigger.

*4 Iout turn off when $\overline{LAT}$ is high level ,and turn on at the first GCK rising edge when $\overline{LAT}$ is low level.

*5 F[1],G[191],G[190]...G[1],G[0],I[191],I[190],...I[0],J[191],J[190],… are serial data for DM631B.

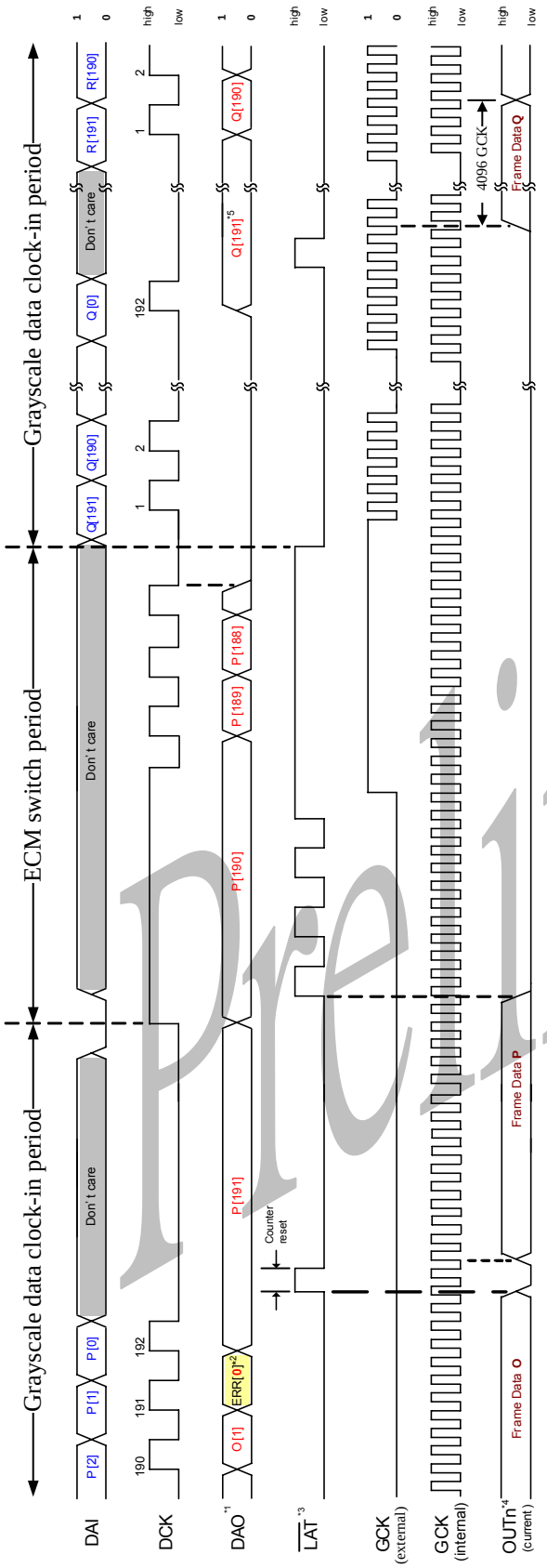
$$\text{Refresh Rate (Hz)} = \frac{\text{Input GCK Frequency (Hz)}}{\text{Total PWM resolution } (2^{12})}$$

For example, if the refresh rate in display system is higher than 60Hz, the input GCK frequency must be higher than 246kHz.

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Timing Diagram (Internal-Clock Mode switch to External-Clock Mode)



*1 REM, ARM, ICM is configered by default. They can switch to FEM, OSM, ECM accordingly.
All registers in DM631B with be reset when any switch proces occur.

*2 ERR[0] is the error message of LED open detection.

*3 $\overline{LAT}$ is level trigger, not edge trigger.

*4 Iout turn off when $\overline{LAT}$ is high level ,and turn on at the first GCK rising edge when $\overline{LAT}$ is low level.

*5 P[191],P[190],… P[0],O[1],Q[191].Q[190],… Q[0],R[191],R[190],… are serial data for DM631B.

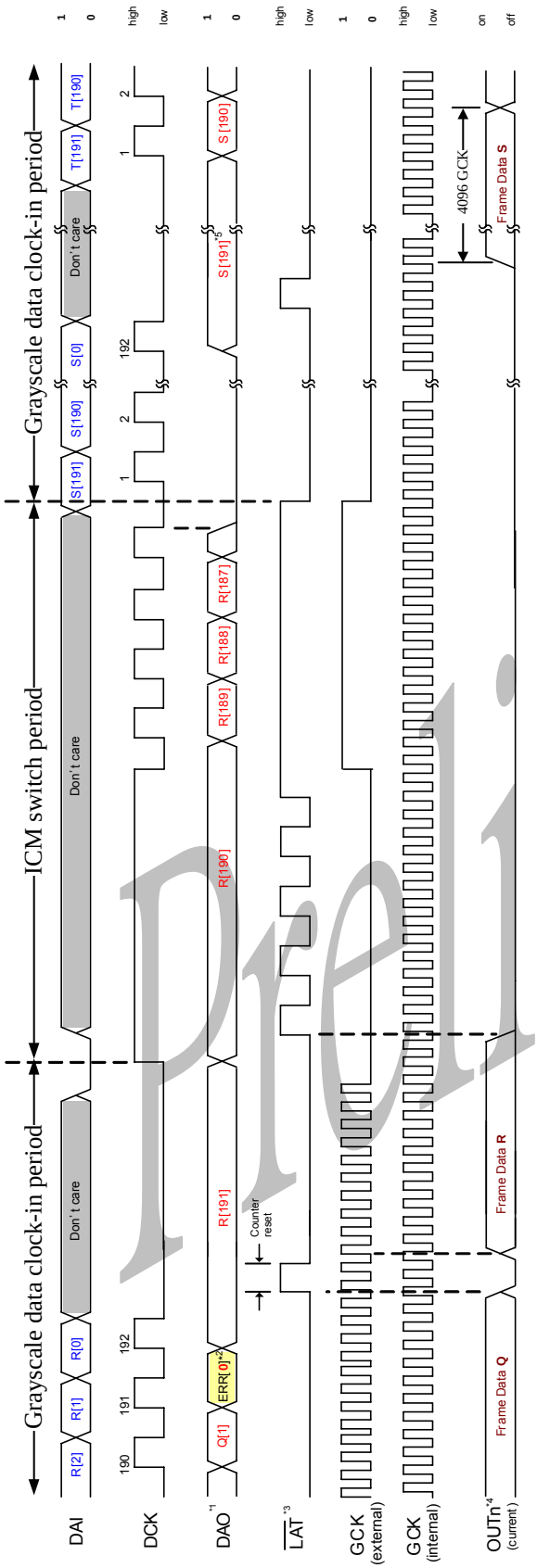
$$\text{Refresh Rate (Hz)} = \frac{\text{Input GCK Frequency (Hz)}}{\text{Total PWM resolution } (2^{12})}$$

For example, if the refresh rate in display system is higher than 60Hz, the input GCK frequency must be higher than 246kHz.

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Timing Diagram (External-Clock Mode switch to Internal-Clock Mode)



*1 REM, ARM, ICM is configered by default. They can switch to FEM, OSM, ECM accordingly.
All registers in DM631B with be reset when any switch procees occur.

*2 ERR[0] is the error message of LED open detection.

*3 $\overline{LAT}$ is level trigger, not edge trigger.

*4 Iout turn off when $\overline{LAT}$ is high level ,and turn on at the first GCK rising edge when $\overline{LAT}$ is low level.

*5 Q[1],R[191],R[190],… R[0],S[191].S[190],… S[0],T[191],T[190],… are serial data for DM631B.

$$\text{Refresh Rate (Hz)} = \frac{\text{Input GCK Frequency (Hz)}}{\text{Total PWM resolution } (2^{12})}$$

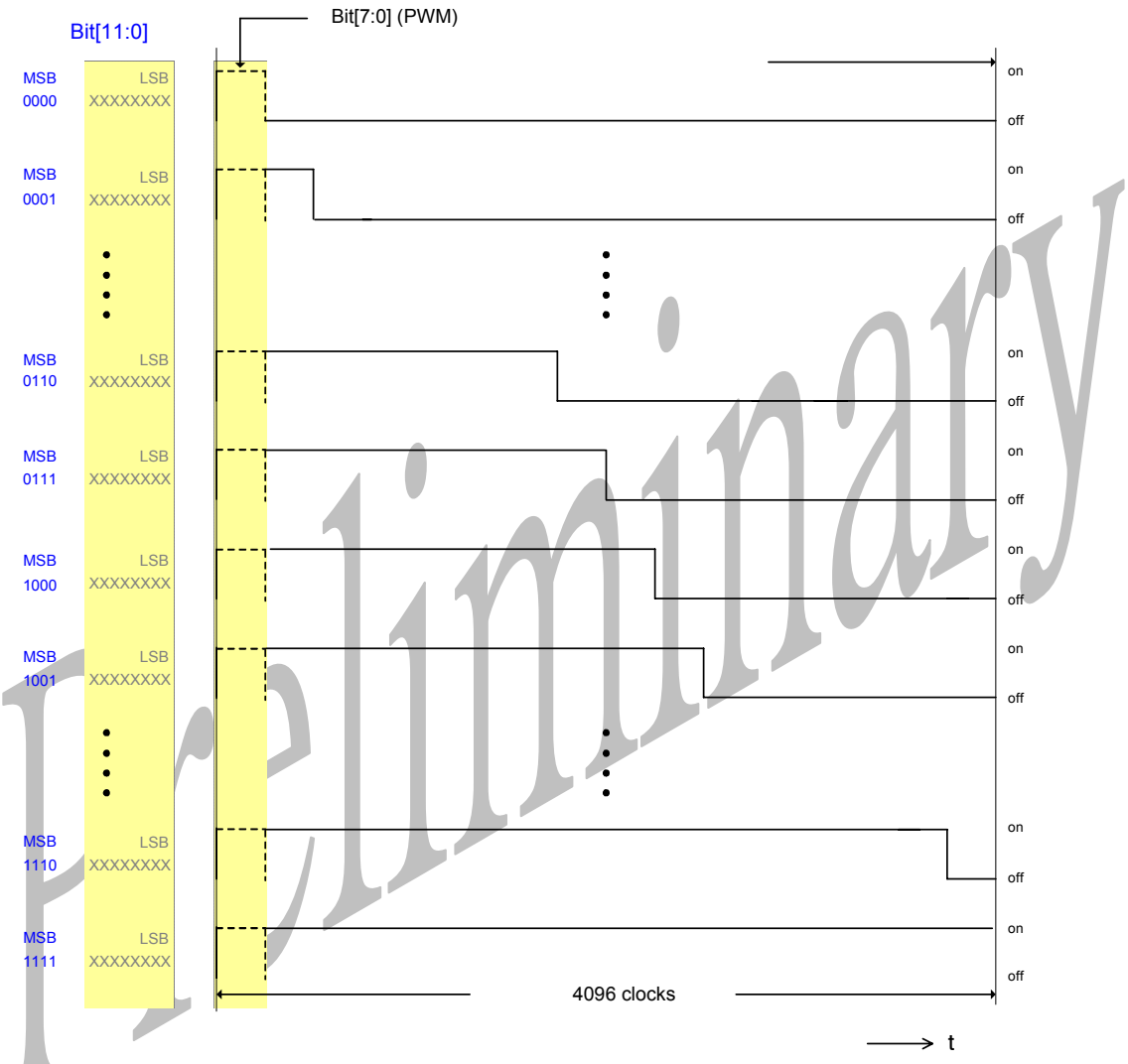
For example, if the refresh rate in display system is higher than 60Hz, the input GCK frequency must be higher than 246kHz.

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Output Modulation Technique

DM631B provides a new LED drive technique of output modulation. It improves traditional Pulse Width Modulation (PWM) by 2-section modulation. The main benefits of 2-section modulation are to drive LED with an equivalent higher refresh rate (up to 6.1MHz in DM631B when F_{GCK} = 25MHz) and change bit to next bit smoothly. The relationships between PWM and 2-section modulation in time domain can be refer to the diagram (not to scale) below:



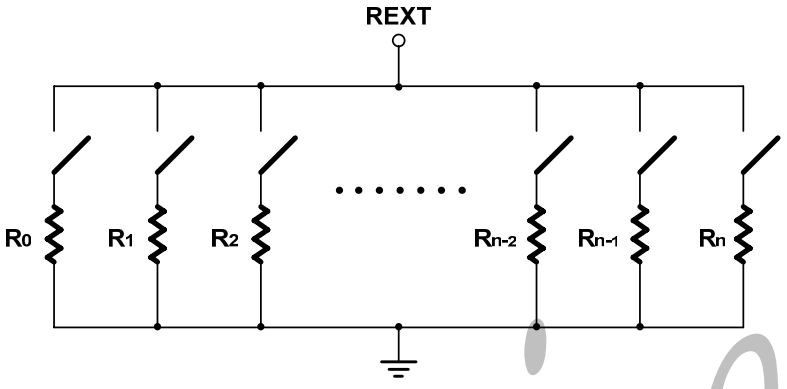
Ultra High Resolution Current Outputs

DM631B could provide 12-bit 2-section PWM control current outputs for each channel. There are two advantages for system design. One is DM631B has sufficient bit resolution (4096 steps), not only LED color information but additional data such as global brightness, dot correction, and gamma correction can be represented by the proper algorithms. The other is to reduce a lot of clock and data rate compared to conventional ON-OFF type LED drivers.

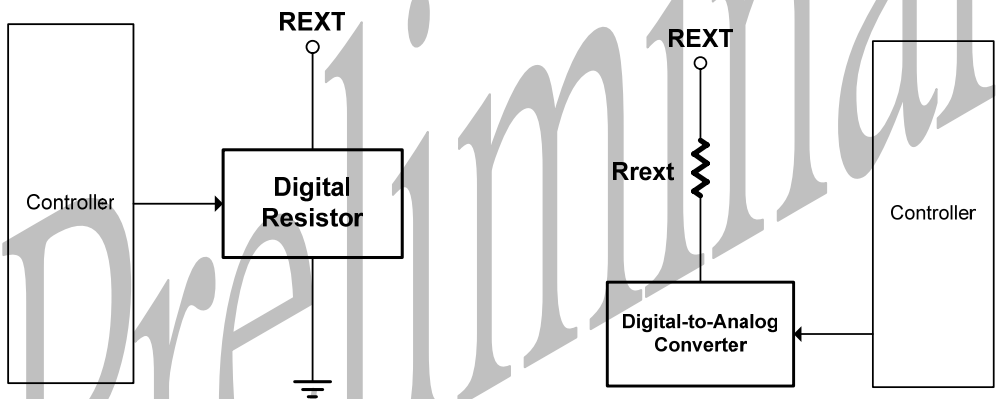
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Global Brightness Control

DM631B has no built-in global brightness control feature. In order to obtain a lower resolution of global brightness control effect, two methods could be utilized. Here show different ways to adjust the Rrext value or voltage drop across the external resistor. Please see the reference circuit below:



Global Brightness Control with Resistor Ladder



Global Brightness Control with Digital Resistor

Global Brightness Control with D/A converter

Output to Output Delay

DM631B has build-in output to output delay with a special arrangement. This arrangement help chip avoid noise cause by large current during channels switching. The arrangement details are shown as following table.

Channel	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Delay units	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3

Preliminary

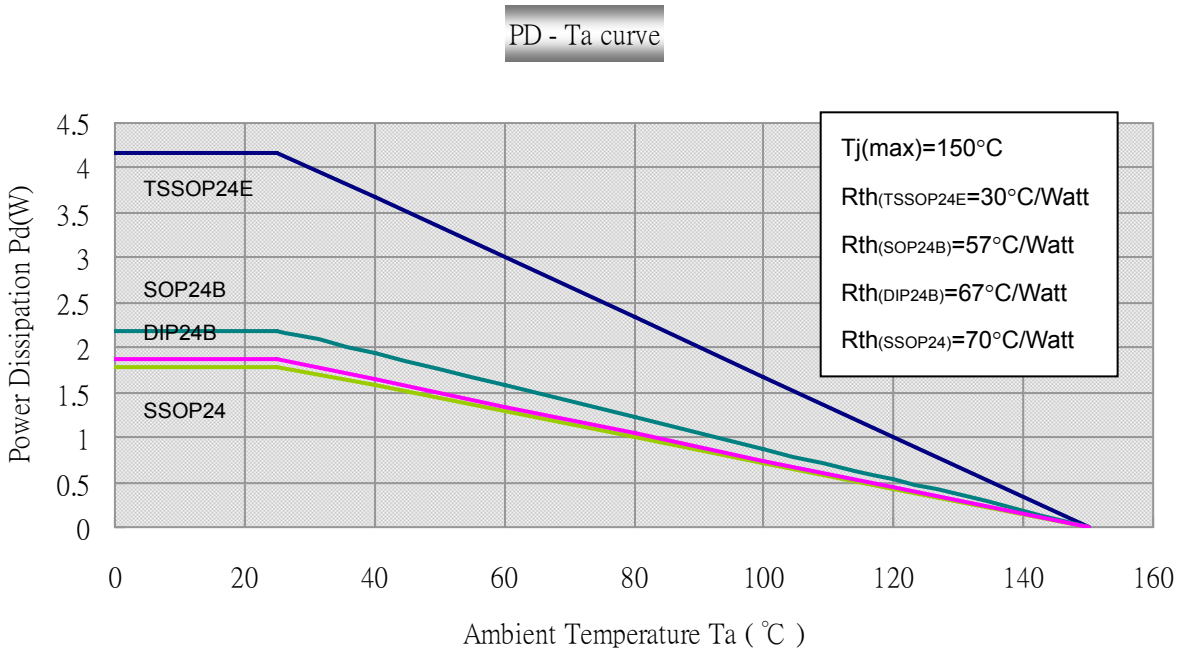
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Power Dissipation

The power dissipation of a semiconductor chip is limited to its package and ambient temperature, in which the device requires the maximum output current calculated for given operating conditions. The maximum allowable power consumption can be calculated by the following equation:

$$Pd(max)(Watt) = \frac{Tj(junction\ temperature)(max)(℃) - Ta(ambient\ temperature)(℃)}{Rth(junction\text{-}to\text{-}air\ thermal\ resistance)(℃/Watt)}$$

The relationship between power dissipation and operating temperature can be refer to the figure below:

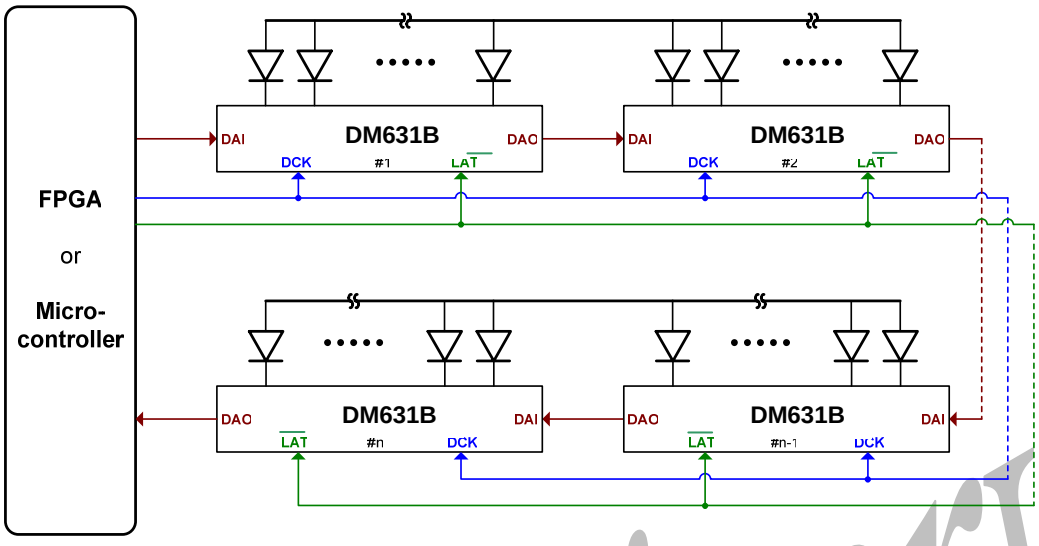


The power consumption of IC can be determined by the following equation and should be less than the maximum allowable power dissipation:

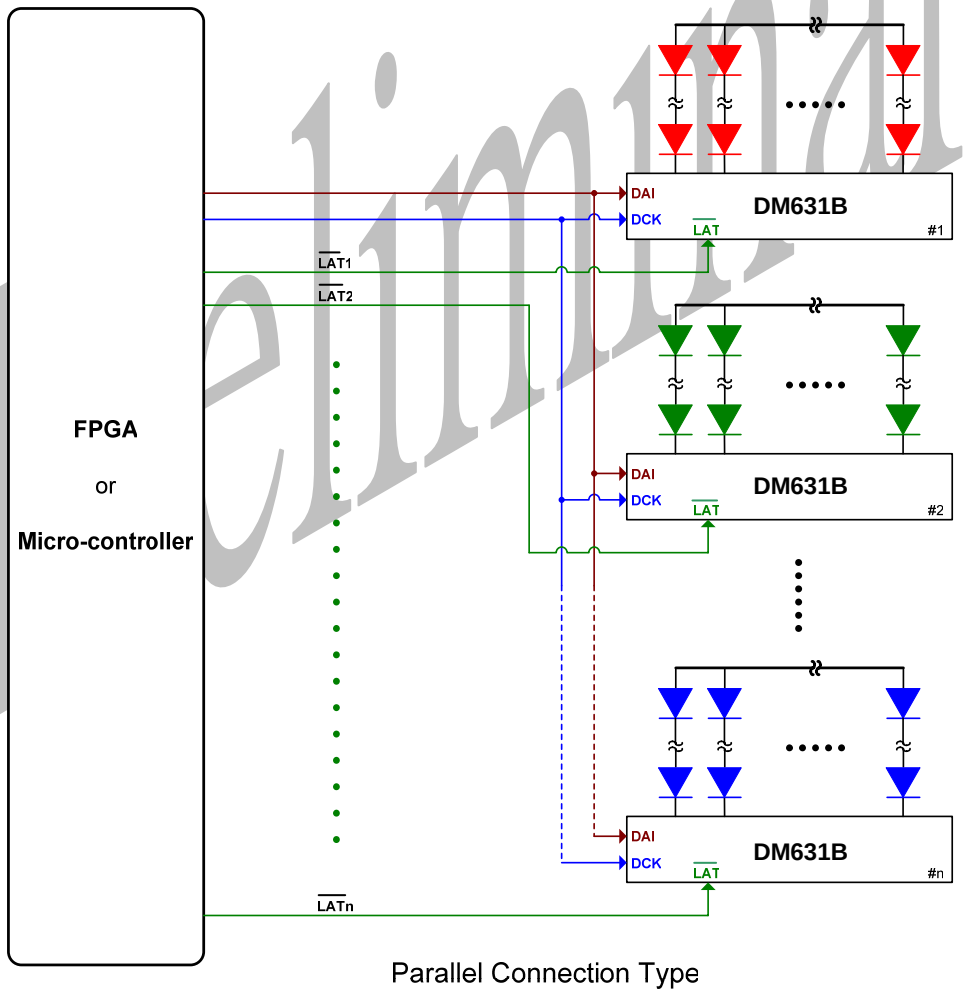
$$Pd(W) = V_{CC}(V) \times I_{DD}(A) + Vout0 \times Iout0 \times Duty0 + \cdots\cdots + Vout15 \times Iout15 \times Duty15 \leq Pd(max)(W)$$

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Typical Application



Serial Connection Type



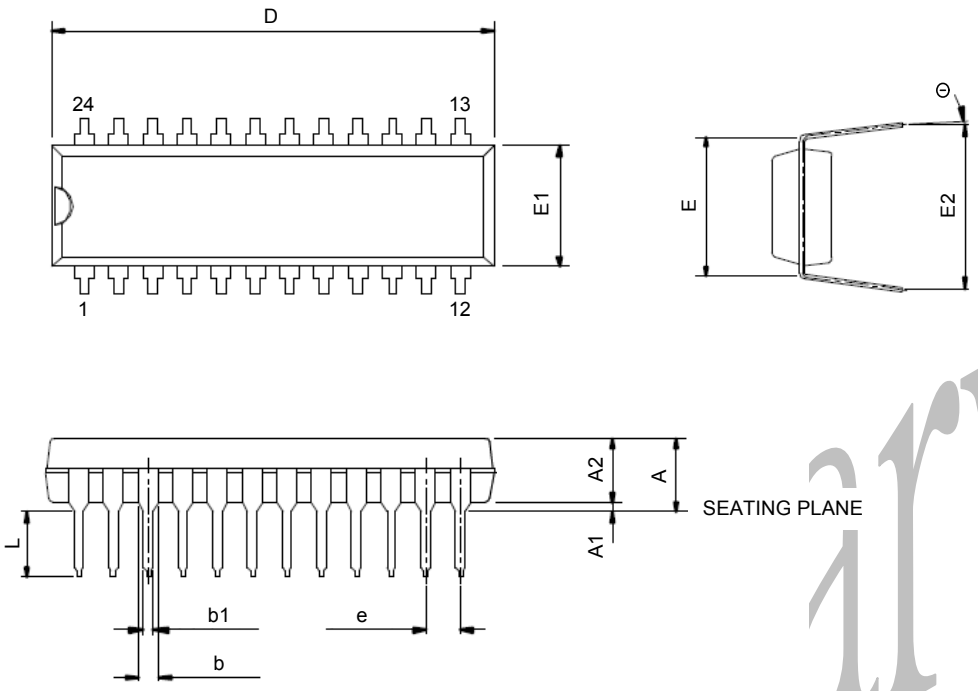
Parallel Connection Type

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Package Outline Dimension

DM631B-DIPB



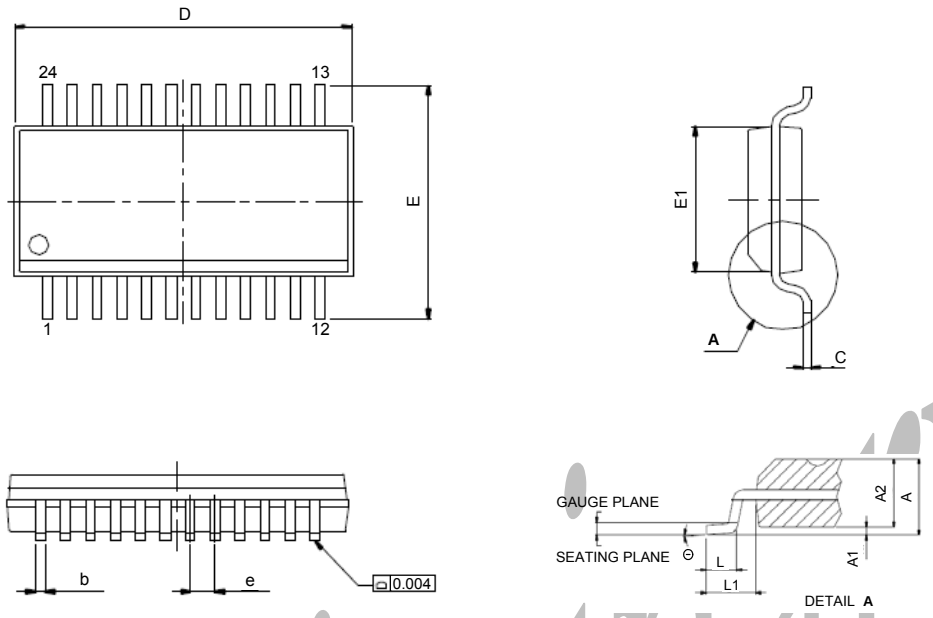
Preliminary

	DIMENSIONS IN INCH		DIMENSIONS IN MM	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	-	0.210	-	5.334
A1	0.015	-	0.381	-
A2	0.125	0.135	3.175	3.429
b	0.040		1.016	
b1	0.018		0.457	
D	0.880	0.920	22.352	23.368
E	0.300BSC		7.620BSC	
E1	0.245	0.255	6.223	6.477
E2	0.335	0.375-	8.509	9.525
e	0.070		1.778	
L	0.115	0.150	2.921	3.810
Θ	0°	15°	0°	15°

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Package Outline Dimension

DM631B-SSOP



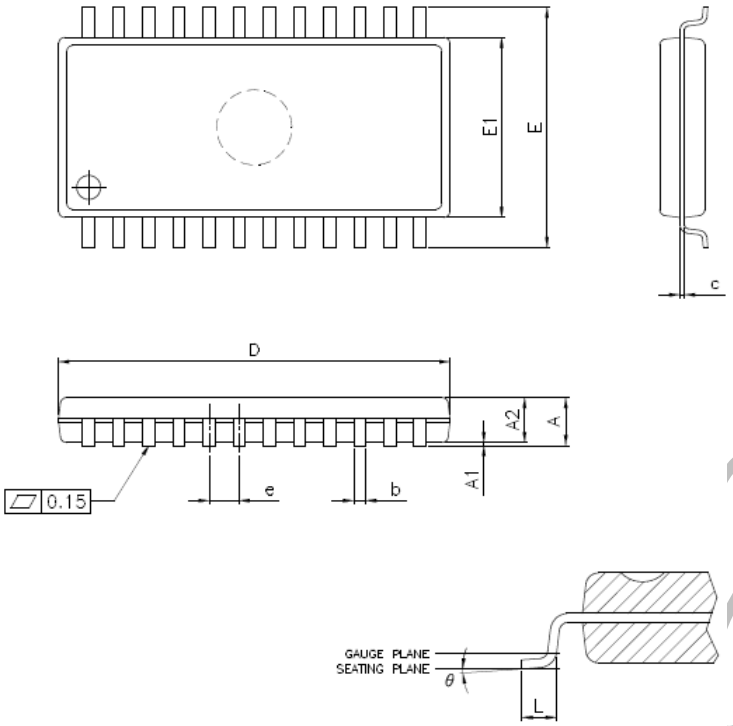
Preliminary

	DIMENSIONS IN INCH		DIMENSIONS IN MM	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.346	1.753
A1	0.004	0.010	0.102	0.254
A2	-	0.059	-	1.499
b	0.008	0.012	0.203	0.305
C	0.007	0.010	0.178	0.254
D	0.337	0.344	8.560	8.738
E	0.228	0.244	5.791	6.198
E1	0.150	0.157	3.810	3.988
e	0.025 BSC.		0.635 BSC	
L	0.016	0.050	0.406	1.270
L1	0.041 BSC		1.041 BSC	
Θ	0°	8°	0°	8°

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Package Outline Dimension

DM631B-SOPB



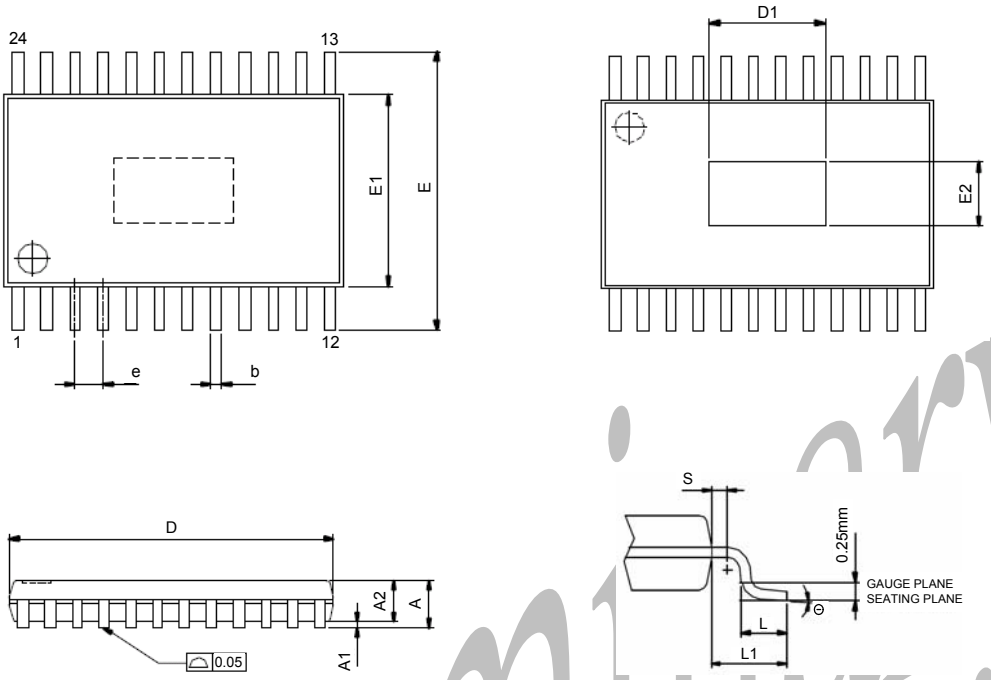
	DIMENSIONS IN INCH		DIMENSIONS IN MM	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	-	0.075	-	1.900
A1	0.002	0.008	0.050	0.200
A2	0.051	0.067	1.300	1.700
b	0.012	0.020	0.300	0.500
c	0.004	0.010	0.100	0.250
D	0.504	0.520	12.800	13.200
E	0.303	0.327	7.700	8.300
e	0.0394 BSC		1.000 BSC	
E1	0.228	0.244	5.800	6.200
L	0.010	0.026	0.250	0.650
θ	0°	10°	0°	10°

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Package Outline Dimension

DM631B-TSSOPE (exposed pad)



Preliminary

	DIMENSIONS IN INCH		DIMENSIONS IN MM	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	-	0.047	-	1.20
A1	0.000	0.006	0.00	0.15
A2	0.031	0.041	0.80	1.05
b	0.007	0.012	0.19	0.30
D	0.303	0.311	7.70	7.90
E1	0.169	0.177	4.30	4.50
E	0.252 BSC		6.400 BSC	
e	0.026 BSC		0.650 BSC	
L1	0.039 REF		1.000 REF.	
L	0.018	0.030	0.45	0.75
S	0.008	-	0.20	-
Θ	0°	8°	0°	8°
E2	0.0898	0.1122	2.280	2.850
D1	0.146	1.819	3.700	4.620

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