Automotive Audio Bus A²B Transceiver

AD2420(W)/AD2426(W)/AD2427(W)/AD2428(W)/AD2429(W)

A²B BUS FEATURES

- Line topology
  - Single master, multiple slave
  - Up to 15 m between nodes and up to 40 m overall cable length (see Table 9)
- Communication over distance
  - Synchronous data
    - Multichannel I²S/TDM to I²S/TDM
    - Synchronous clock, phase aligned in all nodes
    - Low latency slave to slave communication
  - Control and status information I²C to I²C
  - GPIO and interrupt
- Bus power or local power slave nodes
- Configurable with SigmaStudio graphical software tool
- AEC-Q100 qualified for automotive applications

A²B TRANSCEIVER FEATURES

- Configurable A²B bus master or slave operation
- I²C interface
- 8-bit to 32-bit multichannel I²S/TDM interface
  - Programmable I²S/TDM data rate
  - Up to 32 upstream and 32 downstream channels
- PDM interface
  - Programmable PDM clock rate
  - Up to 4 high dynamic range microphone inputs
- Simultaneous reception of I²S data with up to 4 PDM microphones
- Unique ID register for each transceiver
- Crossover or straight-through cabling
- Programmable settings to optimize EMC performance

APPLICATIONS

- Audio communication link
- Microphone arrays
  - Beamforming
  - Hands free and in car communication
- Active and road noise cancellation
- Audio/video conferencing systems

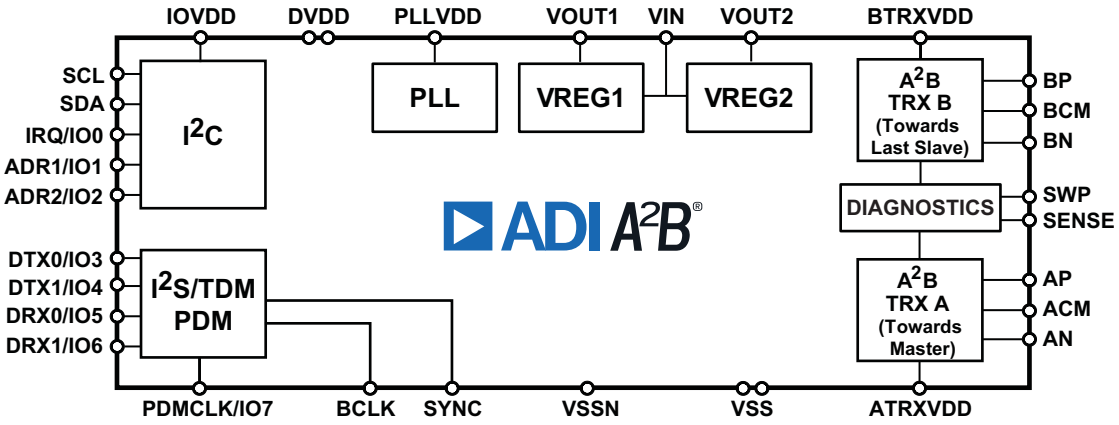


Figure 1. Functional Block Diagram

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Rev. C Document Feedback

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REVISION HISTORY

7/2021—Rev. B to Rev. C

Removed references to ambient temperature in:
- Operating Conditions 8
- Automotive Products 37
- Ordering Guide 38

Added statement on specification applicability to:
- Operating Conditions 8
- Electrical Characteristics 9
- Timing Specifications 12

Added $I_{BUSDISC}$ and $C_{BUSDISC}$ specifications to A²B Bus System Specification 17

Updated Figure 39 in Outline Dimensions 36

Changes to the Package Option column in Automotive Products 37

GENERAL DESCRIPTION

The Automotive Audio Bus ($A^2B^®$) provides a multichannel, I^2S/TDM link over distances of up to 15 m between nodes. It embeds bidirectional synchronous pulse-code modulation (PCM) data (for example, digital audio), clock, and synchronization signals onto a single differential wire pair. A^2B supports a direct point to point connection and allows multiple, daisy-chained nodes at different locations to contribute and/or consume time division multiplexed (TDM) channel content.

A^2B is a single-master, multiple-slave system where the transceiver at the host controller is the master. The master generates clock, synchronization, and framing for all slave nodes. The master A^2B transceiver is programmable over a control port (I^2C) for configuration and read back. An extension of the control port protocol is embedded in the A^2B data stream, which grants direct access of registers and status information on slave transceivers as well as I^2C to I^2C communication over distance.

The transceiver can connect directly to general-purpose digital signal processors (DSPs), field-programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), microphones, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and codecs through a multichannel I^2S/TDM interface. It also provides a pulse density modulation (PDM) interface for direct connection of up to four PDM digital microphones.

Finally, the transceiver also supports an A^2B bus powering feature, where the master node supplies voltage and current to the slave nodes over the same daisy-chained, twisted pair wire cable as used for the communication link.

Table 1. Product Comparison Guide

Feature	AD2420/ AD2420W	AD2426/ AD2426W	AD2427/ AD2427W	AD2428/ AD2428W	AD2429/ AD2429W
Master capable	No	No	No	Yes	Yes
Number of slaves discoverable[1]	N/A	N/A	N/A	Up to 10	Up to 2
Functional TRX blocks	A only	A only	A + B	A + B	B only
I^2S/TDM support	No	No	No	Yes	Yes
PDM microphone inputs	2 mics[2]	4 mics	4 mics	4 mics	4 mics
Max node to node cable length	5 m	15 m	15 m	15 m	5 m

[1] N/A means not applicable.
[2] PDM microphones must be connected to the DRX0/IO5 pin.

A²B BUS DETAILS

Figure 2 shows a single-master, multiple-slave A²B communications system with the master transceiver controlled by the host. The host generates a periodic synchronization signal on the I²S/TDM interface at a fixed frequency (typically 48 kHz) to which all A²B nodes synchronize.

Communications along the A²B bus occur in periodic superframes. The superframe frequency is the same as the synchronization signal frequency, and data is transferred at a bit rate that is 1024 times faster (typically 49.152 MHz). Each superframe is divided into periods of downstream transmission, upstream transmission, and no transmission (where the bus is not driven). Data is exchanged over the A²B bus in up to 32 equal width slots for both upstream and downstream transmissions.

The A²B bus also communicates the following control and status information between nodes:

- I²C to I²C communication
- General-purpose input/output (GPIO)
- Interrupts

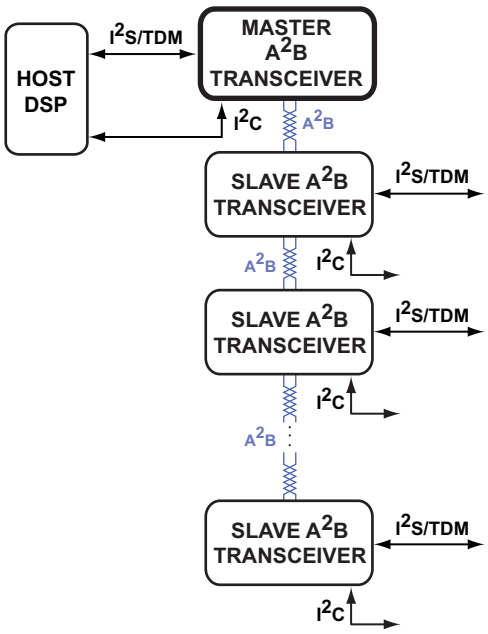


Figure 2. Communication System Block Diagram

In Figure 3, a superframe is shown with an initial period of downstream transmission and a later period of upstream transmission.

All signals on the A²B bus are line coded, and the master node forwards the synchronization signal downstream from the master transceiver to the last slave node transceiver in the form of a synchronization preamble. This preamble is followed by control data to build a synchronization control frame (SCF). Downstream, TDM synchronous data is added directly after the control frame. Every slave can use or consume some of the downstream data and add data for downstream nodes. The last slave node transceiver responds after the response time with a synchronization response frame (SRF). Upstream synchronous data is added by each node directly after the response frame. Each node can also use or consume upstream data.

The embedded control and response frames allow the host to individually address each slave transceiver in the system. The host also enables access to remote peripheral devices that are connected to the slave transceivers via the I²C or SPI ports for I²C to I²C communication over distance between multiple nodes.

All nodes in an A²B system are sampled synchronously in the same A²B superframe. Synchronous I²S/TDM downstream data from the master arrives at all slaves in the same A²B superframe, and the upstream audio data of every node arrives synchronously in the same I²S/TDM frame at the master. The remaining audio phase differences between slaves can be compensated for by register-programmable fine adjustment of the SYNC pin signal delay.

There is a sample delay incurred for data moving between the A²B bus and the I²S/TDM interfaces because data is received and transmitted over the I²S/TDM every sample period (typically 48 kHz). This timing relationship between samples over the A²B bus is shown in Figure 4.

Note in Figure 4, both downstream and upstream samples are named for the frame where they enter the A²B system as follows:

- Data transmitted by the master node transceiver in Superframe M creates Downstream Data M.
- Data transmitted by the slave node transceivers in Superframe N creates Upstream Data N.
- Data received over the I²S/TDM interface by the A²B transceiver is transmitted over the A²B bus in the next superframe.
- Data on the A²B bus is transmitted over the I²S/TDM interface of an A²B transceiver in the next superframe.
- Data transmitted across the A²B bus (master to slave or slave to master) has two frames of latency plus any internal delay that has accumulated in the transceivers as well as delays due to wire length. Therefore, overall latency is slightly over two samples (<50 µs at 48 kHz sample periods) from the I²S/TDM interface in one A²B transceiver to the I²S/TDM interface of another A²B transceiver.

To support and extend the A²B bus functions and performance, the transceivers have additional features, as described in the following sections.

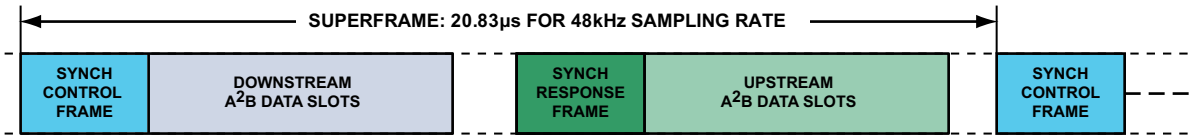


Figure 3. A²B Superframe

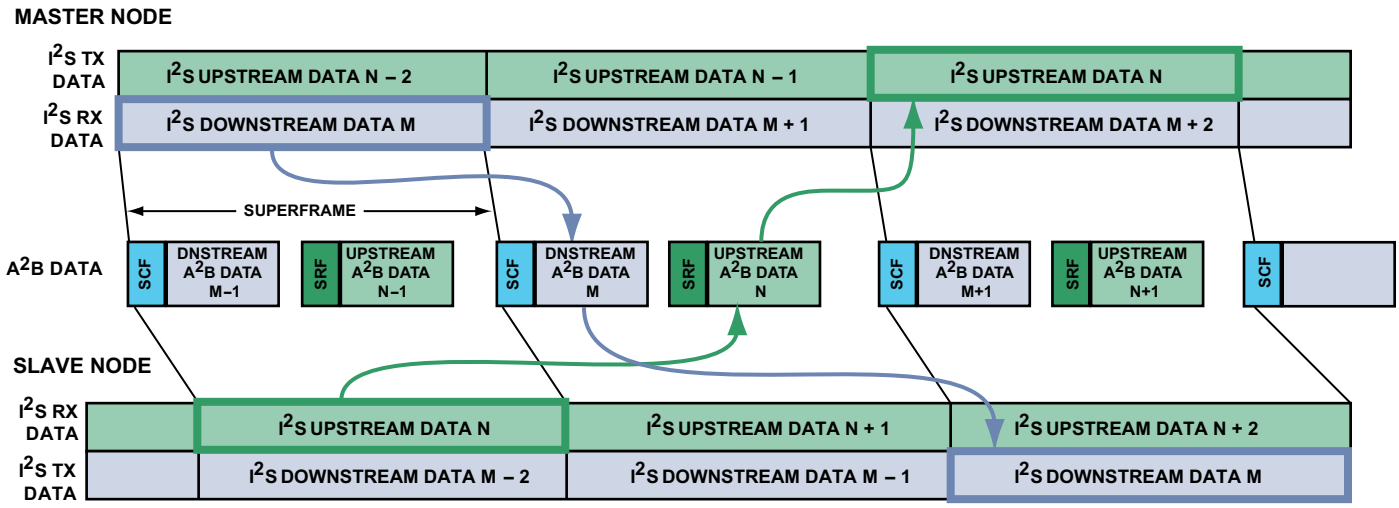


Figure 4. A²B Bus Synchronous Data Exchange

I²C INTERFACE

The I²C interface in the transceiver provides access to the internal registers. Operation is not guaranteed above the V_{I2C_VBUS} specification. The I²C interface has the following features:

- Slave functionality in the A²B master
- Master or slave functionality in the A²B slave
- Multimaster support in the A²B slave
- 100 kbps or 400 kbps rate operation
- 7-bit addressing
- Single-word and burst mode read and write operations
- Clock stretching

All transceivers can be accessed by a locally connected processor using the 7-bit I²C device address (BASE_ADDR) established by the logic levels applied to the ADR2/IO2 and ADR1/IO1 pins at power-on reset, thus providing for up to four master devices connecting to the same I²C bus. A slave configured transceiver recognizes only this I²C device address. A master configured transceiver, however, also recognizes a second I²C device address for remote access to slave nodes over the A²B bus (BUS_ADDR). The least significant bit (LSB) of the 7-bit device address determines whether an I²C data exchange uses the BASE_ADDR (Bit 1 = 0) to access the transceiver or BUS_ADDR (Bit 1 = 1) to access a bus node slave transceiver through a master configured AD2425W transceiver. See the *AD2420(W)/6(W)/7(W)/8(W)/9(W) Automotive Audio Bus A²B Transceiver Technical Reference* for details.

I²S/TDM INTERFACE

The I²S/TDM serial port operates in full-duplex mode, where both the transmitter and receiver operate simultaneously using the same critical timing bit clock (BCLK) and synchronization (SYNC) pins. A²B slave transceivers generate the timing signals on the BCLK and SYNC output pins. A²B master transceivers use the same BCLK and SYNC pins as inputs, which are driven by the host device. The I²S/TDM port includes the following features:

- Programmable clock and frame sync timing and polarity
- Numerous TDM operating modes
- 16- or 32-bit data width
- Simultaneous operation with PDM port
- Single- or dual-pin input/output (I/O)

I²S Reduced Rate

Slave transceivers can run the I²S/TDM/PDM interface at a reduced rate frequency, with respect to the superframe rate. The reduced rate frequency is derived by dividing the superframe rate from a programmable set of values. Different slave nodes can be configured to run at different reduced I²S/TDM rates.

The transceiver provides an option for a processor to track the full rate audio frame, which contains new reduced rate samples. The IO7 pin can be used as a strobe, and the direction can be configured as an input or output.

PULSE DENSITY MODULATION (PDM) INTERFACE

The PDM block on the transceiver converts a PDM input stream into pulse code modulated (PCM) data to be sent over the A²B bus and/or out to the local node through the I²S/TDM port. It supports high dynamic range microphones with high signal-to-noise ratio (SNR) and extended maximum sound pressure level. The PDM interface supports 12 kHz and 24 kHz frame rates in addition to a 48 kHz frame rate and can be used on both master and slave transceivers.

Even lower PDM sampling rates (for example, down to 375 Hz) are possible in combination with the reduced rate feature of the transceiver. The cutoff frequency of the high-pass filter in the transceiver PDM block is fixed to 1 Hz.

BCLK can be used to clock PDM microphones on a slave, but if PDMCLK/IO7 is used instead, the BCLK frequency can be set to a different frequency using the I²S/TDM registers. In this case, PDMCLK/IO7 is used as the PDM clock (PDMCLK) to capture PDM input on DRX0/DRX1. The clock rate from PDMCLK is 64× the SYNC frequency.

On a master node, BCLK is always an input, so the clock to PDM microphones that are attached to a master typically comes from PDMCLK/IO7. It is possible to use BCLK to drive the PDM clock inputs on a master node, but this restricts the possible TDM settings because BCLK is required to fall within the f_{BCLK} specification in Table 4.

BCLK and PDMCLK/IO7 can also be used concurrently to clock PDM microphones at the same frequency and phase alignment, but with opposite polarity. Additionally, a register setting selects whether rising edge data or falling edge data is sampled first.

GPIO OVER DISTANCE

The transceiver supports general-purpose input/output (GPIO) between multiple nodes without host intervention after initial programming. The host is required only for initial setup of the GPIO bus ports. I/O pins of different nodes can be logically OR or AND gate combined.

MAILBOXES

The transceiver supports interrupt driven, bidirectional message exchange between I²C master devices (microcontrollers) at different slave nodes and the host connected to the master node transceiver in two dedicated mailboxes. The mailboxes can be used to customize handshaking among numerous nodes in a system to coordinate system events, such as synchronizing audio.

DATA SLOT EXCHANGE BETWEEN SLAVES

Using the DTX0 and DTX1 pins, slave transceivers can selectively output upstream or downstream data that originates from other nodes without the need for data slots to be routed through the master node. Receive data channels can be skipped based on a programmable offset, when the data is presented as upstream or downstream slots to the A²B bus.

CLOCK SUSTAIN STATE

In the clock sustain state, audio signals of locally powered slave nodes are attenuated in the event of lost bus communication. When the bus loses communication and a reliable clock cannot be recovered by the slave node, the slave node transceiver enters the sustain state and, if enabled, signals this event to a GPIO pin.

In the clock sustain state, the phase-locked loop (PLL) of the slave node transceiver continues to run for 1024 SYNC periods, while attenuating the I²S DTX0 to DTX1 data from the current value to 0. After the 1024 SYNC periods, the slave node transceiver resets and reenters the power-up state.

PROGRAMMABLE SETTINGS TO OPTIMIZE EMC PERFORMANCE

The following programmable features can be used to improve electromagnetic compatibility (EMC) performance.

Programmable LVDS Transmit Levels

The low voltage differential signal (LVDS) transmitter can be set to transmit the signal at high, medium, or low levels. Higher transmit levels yield greater immunity to EMI, whereas lower transmit levels can reduce emissions from the twisted-pair cables that link A²B bus nodes together. The improved LVDS receiver (compared to other members of the AD242xW family) maintains robust operation when transmit levels are lowered.

Spread-Spectrum Clocking

Spread-spectrum clocking can be used to reduce narrow-band emissions on a printed circuit board (PCB). Spread-spectrum clocking is disabled on the transceiver by default, but spread-spectrum clocking for all internal clocks can be enabled during discovery by a register write.

If spread-spectrum clocking support is enabled for the internal clocks, spread-spectrum clocking can also be enabled for both the I²S interface and the programmed CLKOUTs. Enabling spread-spectrum clocking for internal clocks, CLKOUTs, and the I²S interface may reduce narrow-band emissions by several dB on a particular node. When spread-spectrum clocking is enabled on a clock output, the time interval error (TIE) jitter on that clock increases.

Unique ID

Each transceiver contains a unique ID, which can be read from registers using software. If a read of the unique ID fails, an interrupt can be generated.

Support for Crossover or Straight Through Cabling

Straight through cables can be supported by swapping the dc coupling at the B-side connector. See the Designer Reference section for details about the reference schematics.

Data Only and Power Only Bus Operation

The A^2B bus can be operated without closing the PMOS switch to send a dc bias downstream. Conversely, a dc bias can also be sent downstream without the presence of data. These features are available for debug purposes only.

SPECIFICATIONS

Specifications are subject to change without notice. For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.

Parameter		Conditions	Min	Nominal	Max	Unit
Power Supplies						
V_{DVDD}	Digital Core Logic Supply Voltage		1.70	1.90	1.98	V
V_{IOVDD}	Digital Input/Output (I/O) Supply Voltage	3.3 V I/O	3.0	3.3	3.63	V
		1.8 V I/O	1.7	1.9	1.98	V
V_{PLLVDD}	Phased-Locked Loops (PLL) Supply Voltage		1.7	1.9	1.98	V
V_{TRXVDD}	Transceiver Supply Voltage	Applies to the ATRXVDD and BTRXVDD pins	3.0	3.3	3.63	V
V_{I2C_VBUS}	External I^2C Bus Voltage	3.3 V V_{IOVDD}, 1.8 V V_{IOVDD}	1.7	1.9/3.3	3.63	V
Voltage Regulator (VREG1, VREG2)						
V_{VIN}	Regulator Input Supply Voltage	Specification must be met at the VIN pin of each A^2B bus transceiver	3.7		9.0	V
V_{RST}	V_{VIN} Chip Reset Assertion Voltage Threshold	V_{VIN} dropping	2.65		2.97	V
V_{RSTN}	V_{VIN} Chip Reset Deassertion Voltage Threshold	V_{VIN} rising	3.11		3.25	V
Digital I/O						
V_{IH}[1]	High Level Input Voltage	V_{IOVDD} = 1.98 V	0.7 × V_{IOVDD}			V
		V_{IOVDD} = 3.63 V	2.2			V
V_{IL}[1]	Low Level Input Voltage	V_{IOVDD} = 1.70 V			0.3 × V_{IOVDD}	V
		V_{IOVDD} = 3.00 V			0.8	V
V_{IH_I2C}[2]		V_{IOVDD} = 3.63 V, 1.98 V	0.7 × V_{IOVDD}			V
V_{IL_I2C}		V_{IOVDD} = 3.00 V, 1.70 V			0.3 × V_{IOVDD}	V
CONSUMER GRADE						
T_J	Junction Temperature		0		105	°C
INDUSTRIAL GRADE						
T_J	Junction Temperature		–40		+105	°C
AUTOMOTIVE GRADE[3]						
T_J	Junction Temperature		–40		+125	°C

[1] Applies to PDMCLK/IO7, BCLK, SYNC, DTX0/IO3, DTX1/IO4, DRX0/IO5, DRX1/IO6, ADR1/IO1, ADR2/IO2, IRQ/IO0 pins.
[2] Applies to SDA and SCL pins.
[3] Automotive application use profile only. Not supported for nonautomotive use. Contact Analog Devices for more information.

ELECTRICAL CHARACTERISTICS

All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Current						
I_{DVDD}	Digital Core Logic Supply Current	V_{DVDD} = 1.98 V	9.0	10.5	12.0	mA
I_{PLLVDD}	PLL Supply Current	V_{PLLVDD} = 1.98 V	0.5	1.1	1.5	mA
I_{TRXVDD}[1]	Transceiver Supply Current	TX enabled, RX disabled, 100% duty cycle (I_{TXVDD}), V_{TRXVDD} = 3.63 V	9.5	12.0	13.0	mA
		TX disabled, RX enabled, 100% duty cycle (I_{RXVDD}), V_{TRXVDD} = 3.63 V	2.2	2.8	3.5	mA
		TX disabled, RX disabled, 0% activity level, V_{TRXVDD} = 3.63 V	1.0	1.7	2.5	mA
Voltage Regulator (VREG1, VREG2)						
V_{VOUT1}	V_{REG1} Output Voltage		1.80	1.90	1.98	V
V_{VOUT2}	V_{REG2} Output Voltage		3.15	3.30	3.45	V
I_{VOUT1}[2]	V_{REG1} Output Current				40.0	mA
I_{VOUT2}[2]	V_{REG2} Output Current				50.0	mA
I_{VEXT1}[3, 4]	V_{REG1} External Device Current	$I_{VOUT1} - I_{PLLVDD} - I_{DVDD} - I_{IOVDD}$ current available to external device		20		mA
I_{VEXT2}[3, 4]	V_{REG2} External Device Current	$I_{VOUT2} - I_{TRXVDD}$ current available to external device		20		mA
$\Delta V_{OUT1}/\Delta V_{IN}$	Line Regulation	V_{VIN} = 3.7 V to VIN	0	0.017	0.055	%/V
$\Delta V_{OUT2}/\Delta V_{IN}$	Line Regulation	V_{VIN} = 3.7 V to VIN	0.013	0.030	0.060	%/V
		V_{VIN} = 5.0 V to 8 V	−0.025	+0.005	+0.055	%/V
$\Delta V_{OUT1}/\Delta I_{OUT1}$	Load Regulation	V_{VIN} = 5.0 V, I_{VOUT1} = 1 mA to 40 mA		0.009	0.017	%/mA
$\Delta V_{OUT2}/\Delta I_{OUT2}$	Load Regulation	V_{VIN} = 5.0 V, I_{VOUT2} = 1 mA to 50 mA		0.008	0.015	%/mA
I_{VINQ}	Quiescent Current	V_{VIN} =V_{IN}, I_{VOUT1} = 0 mA, I_{VOUT2} = 0 mA	530	600	750	µA
I_{VIN}	Operational Current	V_{VIN} = V_{IN}, I_{VOUT1} = 8 mA, I_{VOUT2} = 20 mA			29	mA
C_{Load1}	V_{REG1} Load Capacitance		1.0		25	µF
C_{Load2}	V_{REG2} Load Capacitance		2.2		25	µF
Digital I/O						
I_{IH}	Input Leakage, High	V_{IOVDD} = 3.63 V, V_{IN} = 3.63 V			10.0	µA
I_{IL}	Input Leakage, Low	V_{IOVDD} = 3.63 V, V_{IN} = 0 V			10.0	µA
I_{OZH_I2C}[5]	Three-State Leakage Current	V_{IOVDD} = 1.9 V, V_{IN} = 3.63 V			10.0	µA
$V_{OH1.9}$	High Level Output Voltage	V_{IOVDD} = 1.70 V, I_{OH} = 1 mA	1.35			V
$V_{OH3.3}$	High Level Output Voltage	V_{IOVDD} = 3.00 V, I_{OH} = 1 mA	2.40			V
V_{OL}[6]	Low Level Output Voltage	V_{IOVDD} = 3.00 V, I_{OL} = 1 mA			0.40	V
V_{OL}[6]	Low Level Output Voltage	V_{IOVDD} = 1.70 V, I_{OL} = 1 mA			0.40	V
V_{OL_I2C}[5, 7]	I^2C Low Level Output Voltage	V_{IOVDD} = 3.00 V, I_{OL} = 1.5 mA			0.40	V
V_{OL_I2C}[5, 7]	I^2C Low Level Output Voltage	V_{IOVDD} = 1.70 V, I_{OL} = 1.5 mA			0.40	V
C_{PD}	Pin Capacitance			4.8	5	pF
Negative Bias Switch and A²B Bus Power						
I_{VSSN}	Internal V_{SSN} Switch Current	AD2426(W)/AD2427(W)/AD2428(W)			300	mA
I_{VSSN}	Internal V_{SSN} Switch Current	AD2420(W)/AD2429W			100	mA
R_{VSSN}	Internal V_{SSN} On Resistance				1.2	Ω

[1] Master and last slave only consume half the transceiver current because only one of the two TRX blocks is used.
[2] In a bus powered system, I_{VOUT} has a direct impact on I_{VSSN} and V_{VIN} in other nodes. For more information, see the Power Analysis section.
[3] Consider the package thermal limits when dissipating current above typical limits. For more information, see the Thermal Characteristics section.
[4] Must comply with I_{VOUT1} and I_{VOUT2} maximum.
[5] Applies to SDA and SCL pins.
[6] Applies to BCLK, SYNC, DTX0/IO3, DTX1/IO4, DRX0/IO5, DRX1/IO6, ADR1/IO1, ADR2/IO2, IRQ/IO0, PDMCLK/IO7 pins.
[7] The minimum I_{OL} current is lower than the I^2C specification because the SDA and SCL pins are designed for a limited number of I^2C attached slave devices.

Table 2. Differential Input/Output

Parameter		Conditions	Min	Typ	Max	Unit
LVDS						
$\|V_{OD}\|$	Differential Output Voltage Magnitude	See Figure 19				
	High Transmit Level		425		545	mV
	Medium Transmit Level		315		415	mV
	Low Transmit Level		210		305	mV
Receiver						
V_{TH}	Differential Input Threshold Voltage		−52		+52	mV

POWER SUPPLY REJECTION RATIO (PSRR)

Typical PSRR at T_J = 40°C with load capacitance C_{LOAD} = 4.7 µF || 100 µF.

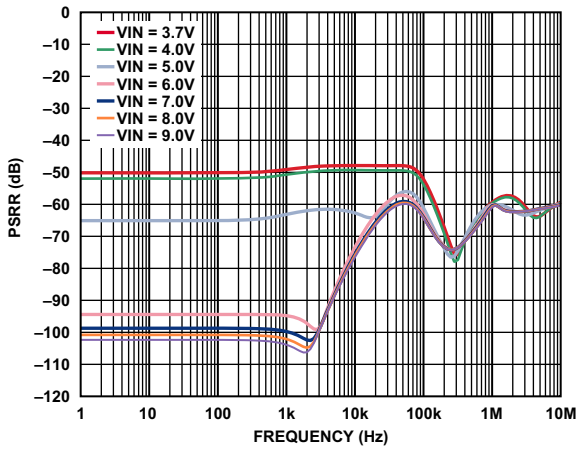


Figure 5. VOUT1 PSRR, I_{VOUT1} = 10 mA

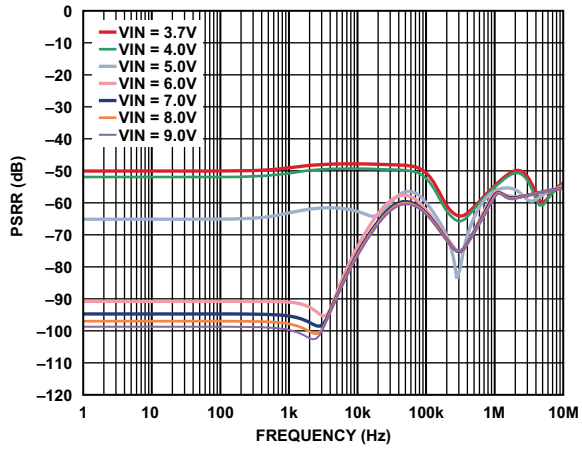


Figure 6. VOUT1 PSRR, I_{VOUT1} = 40 mA

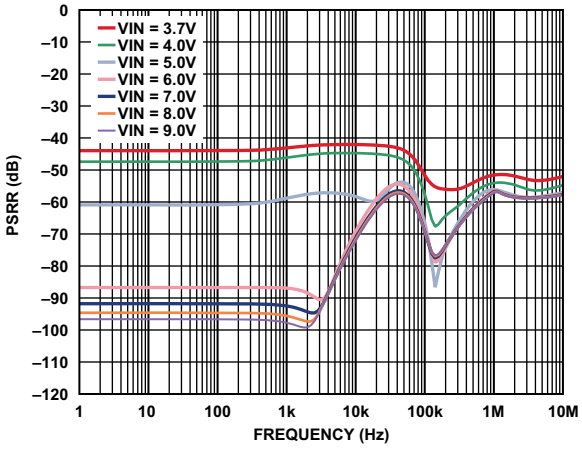


Figure 7. VOUT2 PSRR, I_{VOUT2} = 10 mA

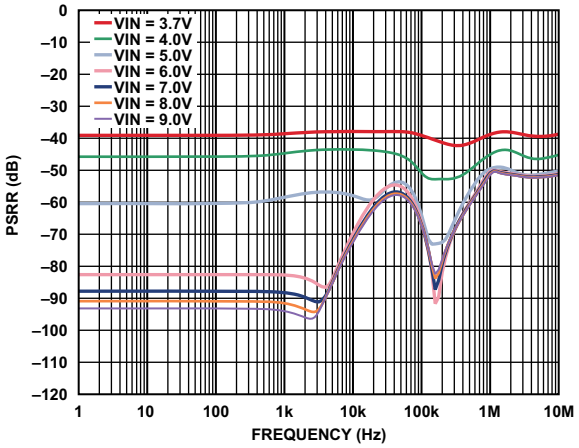


Figure 8. VOUT2 PSRR, I_{VOUT2} = 50 mA

TIMING SPECIFICATIONS

All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.

Table 3. Clock and Reset Timing (A²B Master)

Parameter		Min	Typ	Max	Unit
Timing Requirements					
f_{SYNCM}	SYNC Pin Input Frequency Continuous Clock	43.6	44.1, 48.0	48.5	kHz
t_{SYNCIJ}	SYNC Pin Input Jitter RMS TIE		0.29	1.0	ns
t_{SYNCOJ}	SYNC Pin Output Jitter RMS TIE			2.6	ns
$f_{SYSBCLK}$	Bus Clock		$1024 \times f_{SYNCM}$		kHz
$t_{DNSYNCR}$[1]	Delay from First Missed SYNC to Reset (A²B Master)	0.64		0.74	ms
t_{DNSCFR}[1]	Delay from First Missed SCF to Reset (A²B Slave)	0.64		0.74	ms
t_{PLK}	PLL Lock Time		7.5		ms

[1] Only consecutive missed SYNC or SCF transitions for the specified duration result in a reset.

Table 4. Pulse Density Modulation Microphone Input Timing

Parameter		Min	Typ	Max	Unit
Timing Requirements					
t_{RISS}	DRXn Input Setup Before BCLK	12.0			ns
t_{RIHS}	DRXn Input Hold After BCLK	0			ns
t_{RISS}	DRXn Input Setup Before PDMCLK	12.5			ns
t_{RIHS}	DRXn Input Hold After PDMCLK	0			ns
Switching Characteristics					
f_{BCLK}	BCLK/PDMCLK Output Frequency	3.05		3.18	MHz
t_{BCLKOJ}	BCLK/PDMCLK Output Jitter RMS Cycle to Cycle			175	ps
t_{SOL}	BCLK/PDMCLK Output Pulse Width Low	161.0			ns

Table 5. GPIO Timing

Parameter		Min	Typ	Max	Unit
Timing Requirement					
t_{FIPW}	Input Pulse Width	$t_{SYSBCLK} + 1$			ns
Switching Characteristic					
t_{FOPW}	Output Pulse Width	$t_{SYSBCLK} - 1$			ns

Table 6. I²C Port Timing

Parameter		Min	Typ	Max	Unit
Timing Requirements					
f_{SCL}	SCL Clock Frequency	0		400	kHz
t_{SCLH}	SCL Pulse Width High	0.6			µs
t_{SCLL}	SCL Pulse Width Low	1.3			µs
t_{SCS}	Start and Repeated Start Condition Setup Time	0.6			µs
t_{SCH}	Start Condition Hold Time	0.6			µs
t_{SPS}	Stop Condition Hold Time	0.6			µs
t_{DS}	Data Setup Time	100			ns
t_{DH}	Data Hold Time	0.0		0.9	µs
t_{SCLR}	SCL Rise Time			300	ns
t_{SCLF}	SCL Fall Time			300	ns
t_{SDR}	SDA Rise Time			300	ns
t_{SDF}	SDA Fall Time			300	ns
t_{BFT}	Bus-Free Time Between Stop and Start	1.3			µs

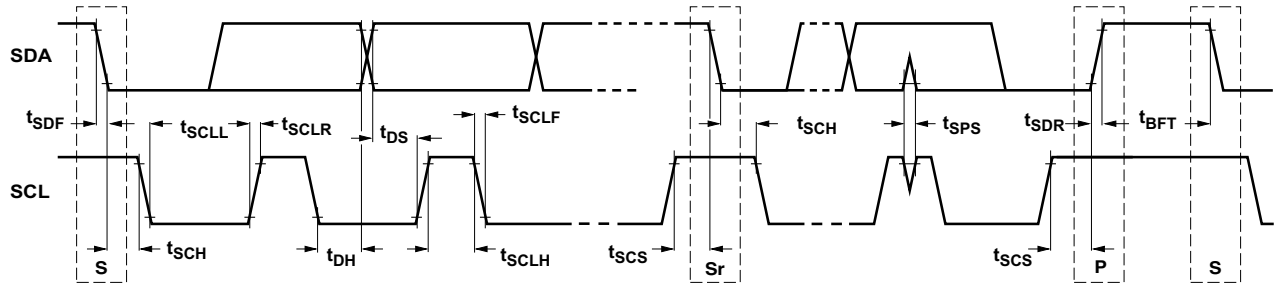


Figure 9. I²C Port Timing

Table 7. I²S Timing

Parameter		1.8 V Min	1.8 V Max	3.3 V Min	3.3 V Max	Unit
I²S Slave Timing Requirements (A²B Master)						
t_{BCLKW}	BCLK Width	19.5		9.5		ns
t_{BCLKS}	BCLK Period	39.0		19.0		ns
t_{SIS}[1]	SYNC Input Setup Before BCLK Sample Edge	2.25		2.25		ns
t_{SIH}[1]	SYNC Input Hold After BCLK Sample Edge	2.0		3.0		ns
t_{RISM}[1]	DRXn Input Setup Before BCLK Sample Edge	0.5		0.5		ns
t_{RIHM}[1]	DRXn Input Hold After BCLK Sample Edge	2.0		1.5		ns
t_{RISM}[1]	DRX1 on DTX1 Input Setup Before BCLK Sample Edge	4.0		4.5		ns
t_{RIHM}[1]	DRX1 on DTX1 Input Hold After BCLK Sample Edge	0.5		0.5		ns
I²S Slave Switching Characteristics (A²B Master)						
t_{DODM}[2]	DTXn Output Delay After BCLK Drive Edge		15.25		12.0	ns
t_{DOHM}[2]	DTXn Output Hold After BCLK Drive Edge	3.0		3.0		ns
t_{DOENM}[2]	DTXn Data Enable Delay After BCLK Drive Edge	2.0		2.0		ns
t_{DODIM}[2]	DTXn Data Disable Delay After BCLK Drive Edge		13.0		8.0	ns
I²S Master Timing Requirements (A²B Slave)						
t_{RISS}[1]	DRXn Input Setup Before BCLK Sample Edge	0.0		0.0		ns
t_{RIHS}[1]	DRXn Input Hold After BCLK Sample Edge	5.8		2.0		ns
t_{RISS}[1]	DRX1 on DTX1 Input Setup Before BCLK Sample Edge	2.5		4.5		ns
t_{RIHS}[1]	DRX1 on DTX1 Input Hold After BCLK Sample Edge	2.5		0.5		ns
I²S Master Switching Characteristics (A²B Slave)						
f_{BCLK}	BCLK Output Frequency[3]		25.0		50.0	MHz
$t_{BCLKMOJ}$	BCLK Output Jitter (RMS Cycle to Cycle, f_{BCLKS} = 12.288 MHz)		100		100	ps
t_{SOL}/t_{SOH}	Transmit or Receive BCLK Duty Cycle	0.45	0.55	0.45	0.55	t_{BCLK}
t_{SOJ}	SYNC Output Jitter (RMS Cycle to Cycle f_{SYNCM} = 48 kHz)		2.2		2.2	ns
t_{SOD}[2]	SYNC Output Delay After BCLK Drive Edge		6.5		6.5	ns
t_{SOHD}[2]	SYNC Output Hold After BCLK Drive Edge	2.8		4.5		ns
t_{DODS}[2]	DTXn Output Delay After BCLK Drive Edge		10.8		9.25	ns
t_{DOHS}[2]	DTXn Output Hold After BCLK Drive Edge	5.5		6.0		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.
[3] When V_{IOVDD} = 3.3 V, the setup and hold timing at the 50 MHz maximum bit clock rate can be violated when interfacing with other I²S devices. The timing violations are seen when the A²B slave node is receiving and A²B master node is transmitting. In these modes, the maximum BCLK frequency of 50 MHz cannot be achieved.

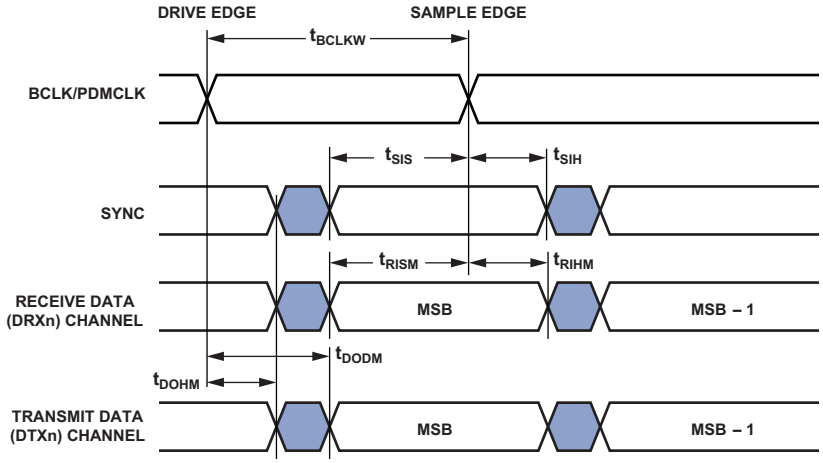


Figure 10. I²S Slave (A²B Master) Timing

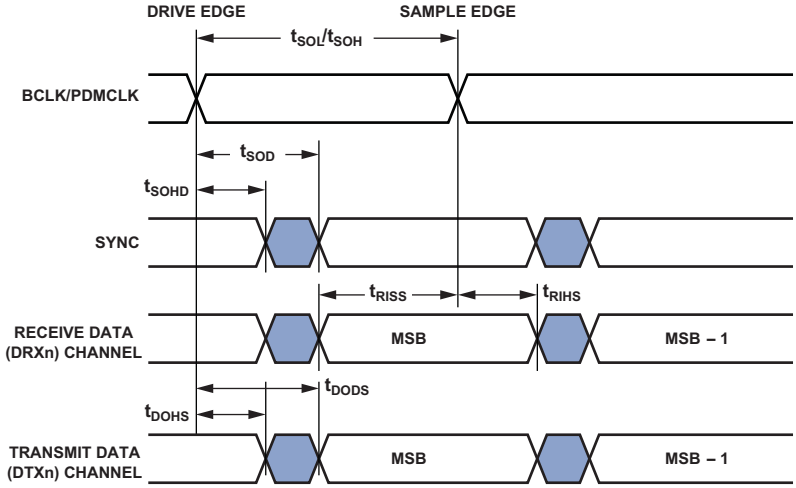


Figure 11. I²S Master (A²B Slave) Timing

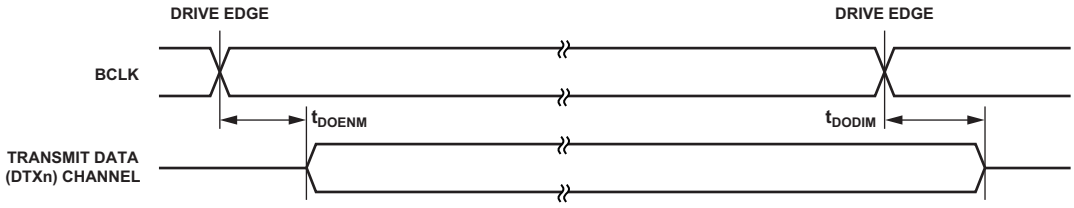


Figure 12. I²S Slave (A²B Master) Enable and Three-State Timing

POWER-UP SEQUENCING RESTRICTIONS

When externally supplied, V_{DVDD} and V_{IOVDD} must reach at least 90% of specification before V_{VIN} begins ramping. To avoid damage to input pins and to ensure correct sampling of the ADR1/ADR2 pins at start-up, V_{IOVDD} must be within specification before input signals are driven by external devices.

Table 8. Power-Up Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{VIN}	When Externally Supplied, V_{DVDD} and V_{IOVDD} Must Reach 90% of Specification Before V_{VIN} Begins Ramping	>0		ms
t_{PORST}	Minimum Time Required for V_{VIN} to be Held Below V_{RST} to Assert Power on Reset	25		ms

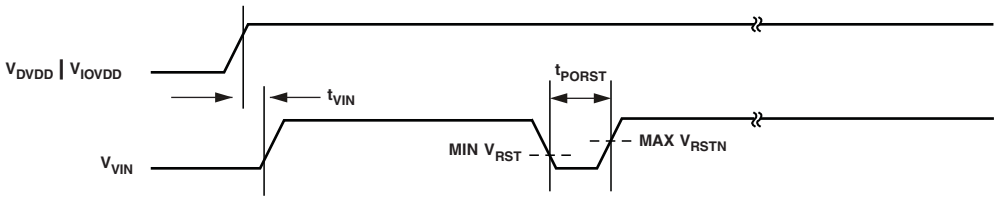


Figure 13. Power-Up Sequencing Timing with Externally Supplied V_{DVDD} and V_{IOVDD}

A²B BUS SYSTEM SPECIFICATION

Table 9. A²B System Specifications

Parameter	System Specification
Cable	Unshielded, single, twisted pair wire (UTP) with 100 Ω differential impedance. EMC performance and full functionality under worst-case environmental conditions is confirmed with Leoni Dacar 545 cable (76D00305).
Maximum Cable Length	
AD2428(W)Mastered System	40 m total, 15 m between nodes.
AD2429(W) Mastered System	10 m total, 5 m between nodes.
Maximum Number of Nodes	
AD2428(W) Mastered System	11 nodes (1 master node and 10 slave nodes).
AD2429(W) Mastered System	Three nodes (1 master node and 2 slave nodes).
Maximum Number of Audio Slots	
AD2426(W)/AD2427(W)/AD2428(W)[1]	64 total, up to 32 upstream and 32 downstream slots, depending upon system design.
AD2420(W)/AD2429(W)[1]	AD2429(W): 4 upstream and 2 downstream slots, depending upon system design. AD2420(W): 2 upstream slots, depending upon system design.
Number of Audio Channels per Slave Node	Individually programmable 0 to 32 upstream channels and 0 to 32 downstream channels.
Synchronous A²B Data Slot Size	8, 12, 16, 20, 24, 28, or 32 bits to match I²S/TDM data-word lengths. Same slot size for all nodes. Upstream and downstream can choose different slot sizes. 12-, 16-, or 20-bit slot sizes can carry compressed data over the A²B bus for 16-, 20-, or 24-bit I²S/TDM word lengths.
Audio Sampling Frequency	44.1 kHz to 48 kHz. All nodes sample synchronously. Slave node transceivers support sample rates (f_S) of 1× (48 kHz), 2× (96 kHz) or 4× (192 kHz), individually configured per slave. To support 2× and 4× sampling rates in slaves, the master uses two and four times the number of I²S/TDM data channels as the 1× sampling frequency (f_{SYNCM}) interface to the host. Transceivers also support reduced rate sampling for 24 kHz, 12 kHz, 6 kHz, 4 kHz, 3 kHz, 2.4 kHz, 2 kHz, 1.71 kHz, or 1.5 kHz at a low latency 48 kHz superframe rate.
Discovery Time	Less than 35 ms per node. Much less than 350 ms for total system startup in a system with 10 nodes. Includes register initialization.
Maximum $I_{BUSDISC}$ Bus Current per Node Prior to Discovery Completion	60 mA. Measured at the negative bias switch.
Maximum $C_{BUSDISC}$ Total Bus Capacitance	70 µF. Capacitance measured between the N and P pins in the CON1-B connector terminal.
Bit Error Detection	Robust error detection for control data and status data with 16-bit cyclic redundancy check (CRC).
Error Correction	Parity and line code error detection on synchronous data slots with audio error correction (repeat of last known good data). For 24-bit and 32-bit data channels, single error correction and double error detection (SECDED) of synchronous data slots is possible.
Failure Diagnostics[1]	Location and cause of failure can be detected for A²B wires shorted to a high voltage (for example, positive terminal of car battery), shorted to ground, wires shorted to each other, wires reversed or open connection.
System EMI/EMC	Meets or exceeds industry specifications for robustness (ISO 11452-2, ISO 11452-4, ISO 7637-3) and emissions (CISPR25).
System ESD	See IEC ESD ratings in Table 12 for terminals.

[1] See the *AD2420(W)/6(W)/7(W)/8(W)/9(W) Automotive Audio Bus A²B Transceiver Technical Reference* for more information.

RMS Time Interval Error (TIE) Jitter

Clocks in an A^{2}B system are passed from the master to Slave 0, from Slave 0 to Slave 1, and so on. Each transceiver adds self jitter to the incoming jitter, which results in jitter growth from the master to the nth slave. Table 10 illustrates typical rms TIE jitter growth.

Table 10. SYNC Output RMS TIE Jitter at Each Slave

Slave Node	Typ	Max	Unit
1	1.57		ns
2	1.79		ns
3	1.91		ns
4	2.04		ns
5	2.15		ns
6	2.27		ns
7	2.44		ns
8	2.47		ns
9	2.58		ns
10	2.70	5.50	ns

PDM TYPICAL PERFORMANCE CHARACTERISTICS

Figure 14 through Figure 18 and Table 11 describe typical PDM performance characteristics.

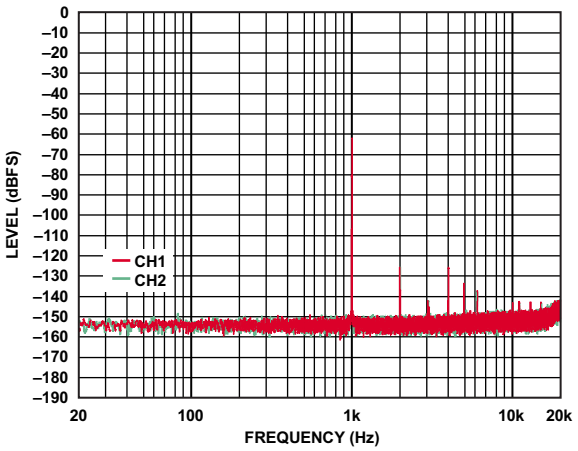


Figure 14. PDM FFT, f_{SYNCM} = 48 kHz, –60 dB Frame Sync Input

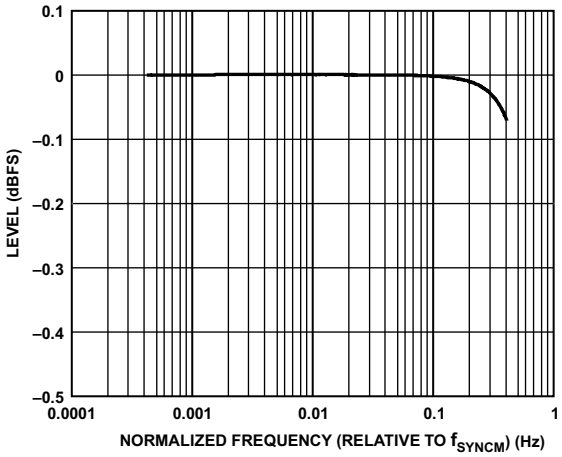


Figure 15. PDM Frequency Response

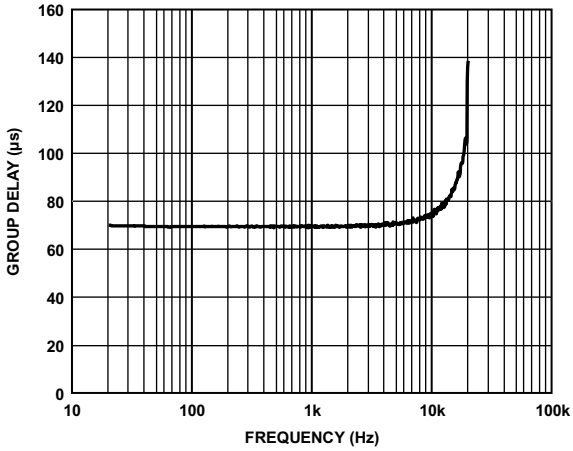


Figure 16. PDM Group Delay vs. Frequency, f_{SYNCM} = 48 kHz

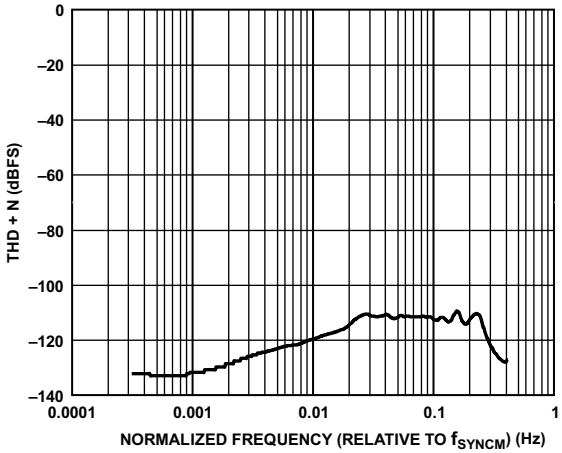


Figure 17. PDM Total Harmonic Distortion + Noise (THD + N) vs. Normalized Frequency (Relative to f_{SYNCM})

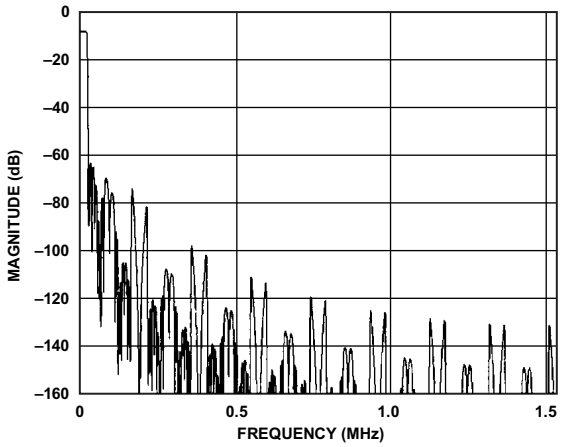


Figure 18. PDM Out of Band Frequency Response (48 kHz Output)

Table 11. PDM Interface Performance Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Dynamic Range	20 Hz to 20 kHz, –60 dB input				
With A-Weighted Filter (RMS)			120		dB
SNR	A-weighted, fourth-order input		120		dB
Decimation Ratio	Default is 64×	64×	128×	256×	
Frequency Response	DC to 0.45 f_{SYNCM}	–0.1		+0.01	dB
Stop Band			0.566		f_{SYNCM}
Attenuation		74			dB
Group Delay	0.02 f_{SYNCM} input signal		3.80		f_{SYNCM} cycles
Gain	PDM to PCM		0		dB
Start-Up Time[1]			48		f_{SYNCM} cycles
Bit Width	Internal and output		24		Bits

[1] The PDM start-up time is the time for the filters to settle after the PDM block is enabled. It is the time to wait before data is guaranteed to meet the specified performance.

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 12 can cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 12. Absolute Maximum Ratings

Parameter	Rating
VIN to VSS	–0.7 V to +30 V
Power Supply IOVDD to VSS	–0.3 V to +3.63 V
Power Supply DVDD to VSS	–0.3 V to +1.98 V
Power Supply PLLVDD to VSS	–0.3 V to +1.98 V
Power Supply TRXVDD to VSS	–0.3 V to +3.63 V
Digital Pin Output Voltage Swing[1]	–0.3 V to V_{IOVDD} + 0.5 V
Input Voltage[2, 3]	–0.33 V to +3.63 V
Input Voltage[2, 4]	–0.33 V to +2.10 V
I^2C Input Voltage[2, 5]	–0.33 V to +5.5 V
A^2B Bus Terminal Voltage	
AP, AN, BP, and BN Pins	–0.5 V to +4.1 V
SENSE, SWP, VSSN Voltage to V_{SS}	+30 V maximum
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	–40°C to +125°C
ESD Rating HBM	
VIN and SWP Pins	±2.5 kV
AP, AN, BP, and BN Pins	±2.5 kV
All Other Pins	±2.5 kV
ESD Rating FICDM	
All Pins	±1.25 kV
System ESD Rating CON1-A and CON1-B Terminals[6]	
IEC 61000-4-2, Air Discharge	±15 kV
IEC 61000-4-2, Contact Discharge	±12 kV
Digital Pin Output Current per Pin Group[7]	15 mA

[1] Applies to BCLK, SYNC, DTX0/IO3, DTX1/DRX1/IO4, DRX0/IO5, DRX1/IO6, IRQ/IO0, ADR1/IO1, ADR2/IO2, PDMCLK/IO7.
[2] Only applies when the related power supply (V_{IOVDD}) is within specification. When the power supply is below specification, the range is the voltage being applied to that power domain ± 0.2 V.
[3] Applies when nominal V_{IOVDD} is 3.3 V.
[4] Applies when nominal V_{IOVDD} is 1.8 V.
[5] Applies to SCL and SDA.
[6] CON1-A and CON1-B are connectors.
[7] For more information, see the following description and Table 13.

Permanent damage can occur if the digital pin output current per pin group value is exceeded. For example, if three pins from Group 2 in Table 13 are sourcing or sinking 2 mA each, the total current for those pins is 6 mA. Up to 9 mA can be sourced or sunk by the remaining pins in the group without damaging the device.

Table 13. Total Current Pin Groups

Group	Pins in Group
1	IRQ/IO0, ADR1/IO1, ADR2/IO2
2	BCLK, SYNC, DTX0/IO3, DTX1/DRX1/IO4, DRX0/IO5, DRX1/IO6, IO7

THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board (PCB), use the following equations:

$$T_J = T_{CASE} + \Psi_{JT} \times P_D$$

where:
T_J = junction temperature (°C).
T_{CASE} = case temperature (°C) measured by customer at top center of package.
Ψ_{JT} = values in Table 14.
P_D = power dissipation.

Values of θ_{JA} are provided for package comparison and PCB design considerations. Use θ_{JA} for a first-order approximation of T_J by the following equation:

$$T_J = T_A + \theta_{JA} \times P_D$$

where T_A = ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations.

Thermal characteristics of the LFCSP_SS package are shown in Table 14. See JESD51-13 for detailed parameter definitions. The junction to board measurement complies with JESD51-8. The junction to case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Table 14. Thermal Characteristics

Parameter	Conditions	Typical (°C/W)
θ_{JA}	Airflow = 0 m/s	31.6
θ_{JMA}	Airflow = 1 m/s	28.8
θ_{JMA}	Airflow = 2 m/s	28.1
θ_{JC}	Airflow = 0 m/s	4.6
θ_{JB}	Airflow = 0 m/s	14.7
Ψ_{JT}	Airflow = 0 m/s	0.20
Ψ_{JT}	Airflow = 1 m/s	0.27
Ψ_{JT}	Airflow = 2 m/s	0.30

The 32-lead LFCSP_SS package requires thermal trace squares and thermal vias to an embedded ground plane in the PCB. The exposed paddle must connect to ground for proper operation to data sheet specifications. Refer to JEDEC standard JESD51-5 for more information.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

Figure 19 shows a line driver voltage measurement circuit of the differential line driver and receiver AP/AN and BP/BN pins.

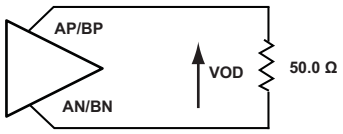


Figure 19. Differential Line Driver Voltage Measurement

OUTPUT DRIVE CURRENTS

Figure 20 through Figure 25 show typical current voltage characteristics for the output drivers of the transceiver. The curves represent the current drive capability of the output drivers as a function of output voltage. Drive Strength 0 is DS0, and Drive Strength 1 is DS1.

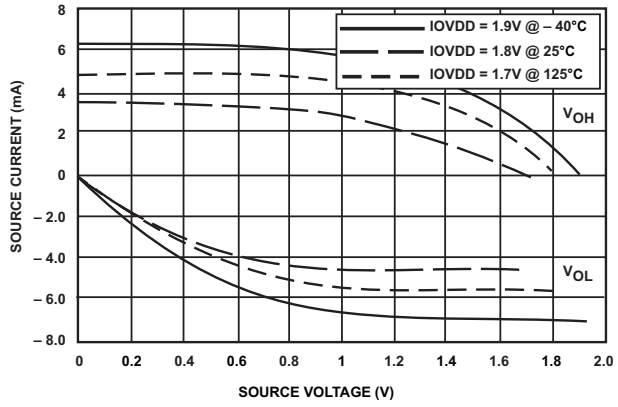


Figure 20. GPIO, BCLK, and SYNC Drivers (DS0, 1.8 V IOVDD)

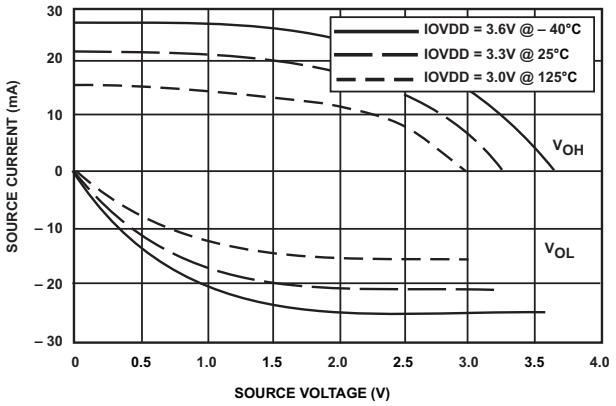


Figure 21. GPIO, BCLK, and SYNC Drivers (DS0, 3.3 V IOVDD)

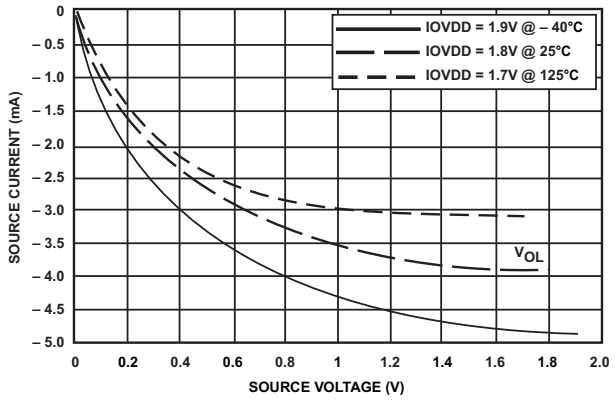


Figure 22. I²C Drivers (1.8 V IOVDD)

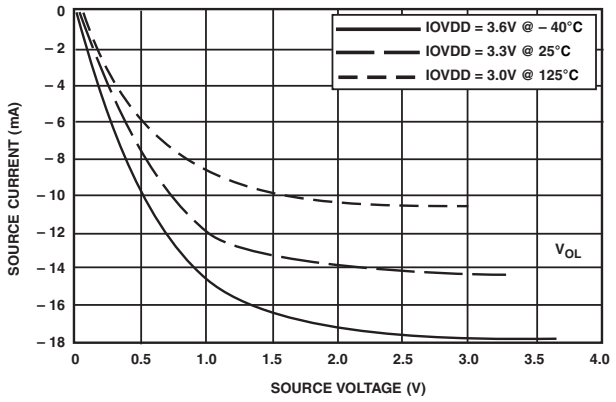


Figure 23. I²C Drivers (3.3 V IOVDD)

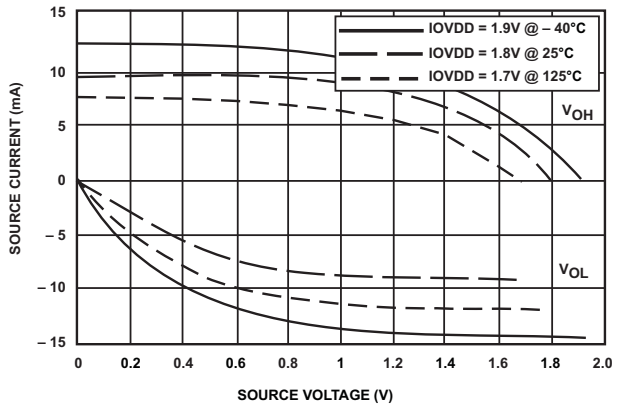


Figure 24. GPIO, BCLK, and SYNC Drivers (DS1, 1.8 V IOVDD)

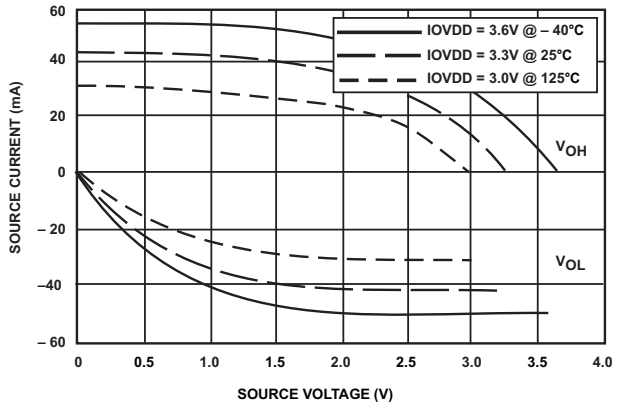


Figure 25. GPIO, BCLK, and SYNC Drivers (DS1, 3.3 V IOVDD)

TEST CONDITIONS

All timing parameters in this data sheet were measured under the conditions described in this section. Figure 26 shows the measurement point for ac measurements (except output enable/disable). The measurement point, V_{MEAS}, is $V_{IOVDD}/2$ for V_{IOVDD} (nominal) = 3.3 V.

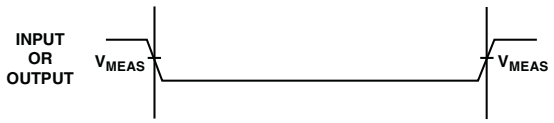


Figure 26. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered enabled when they make a transition from a high impedance state to the point when they start driving.

The output enable time, t_{ENA}, is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving, as shown on the right side of Figure 27. If multiple pins are enabled, the measurement value is that of the first pin to start driving.

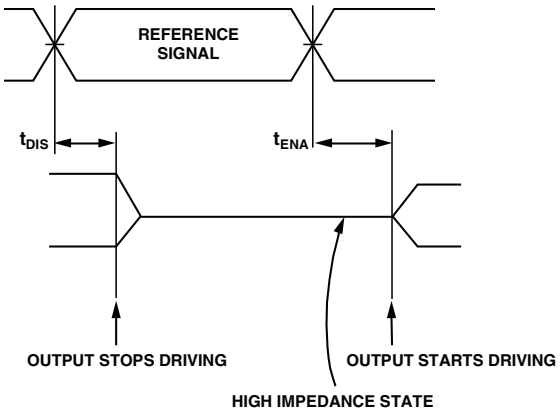


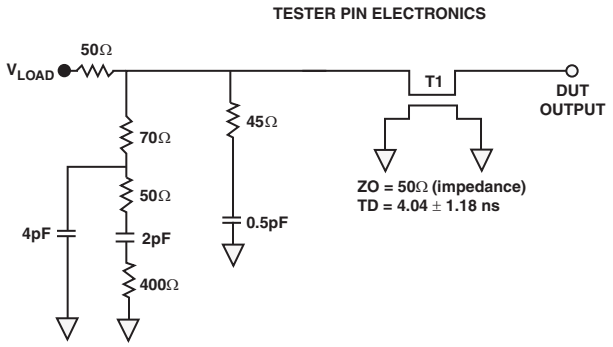
Figure 27. Output Enable/Disable

Output Disable Time Measurement

Output pins are considered disabled when they stop driving, enter a high impedance state, and start to decay from the output high or low voltage. The output disable time, t_{DIS}, is the interval from when a reference signal reaches a high or low voltage level to the point when the output stops driving, as shown on the left side of Figure 27.

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 28). V_{LOAD} is equal to $V_{IOVDD}/2$. Figure 29 through Figure 32 show how output rise time varies with capacitance. The delay and hold specifications given must be derated by a factor derived from these figures. The graphs in Figure 29 through Figure 32 cannot be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, THE SYSTEM CAN INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 28. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

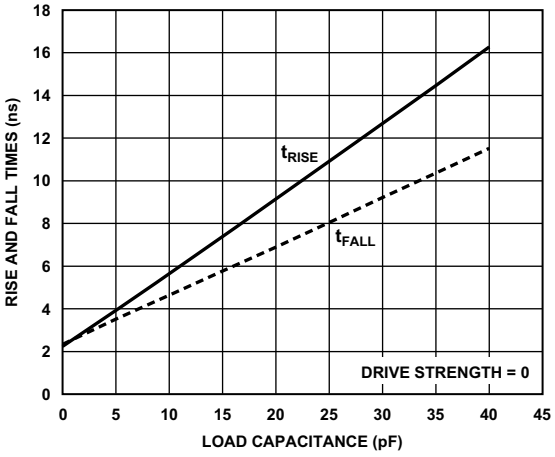


Figure 29. GPIO Driver Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{IOVDD} = 1.8 V, T_J = 25°C)

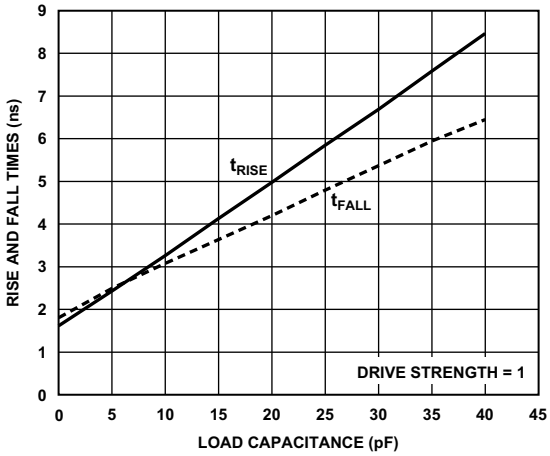


Figure 30. GPIO Driver Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{IOVDD} = 1.8 V, T_J = 25°C)

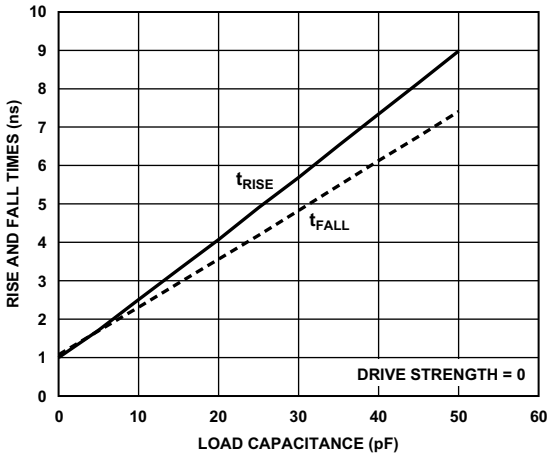


Figure 31. GPIO Driver Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{IOVDD} = 3.3 V, T_J = 25°C)

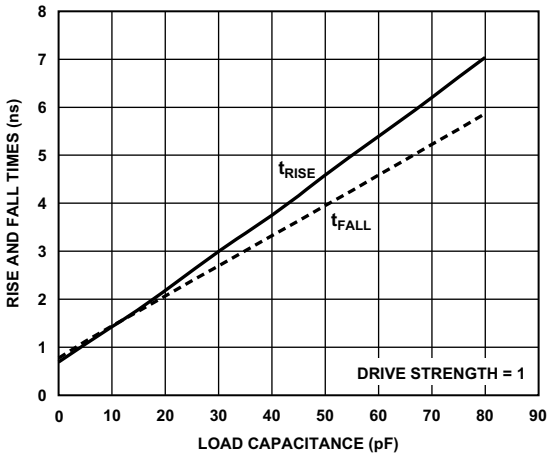


Figure 32. GPIO Driver Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{IOVDD} = 3.3 V, T_J = 25°C)

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

The 32-lead LFCSP_SS package pin configuration is shown in Figure 33. The pin function descriptions are shown in Table 15.

All digital inputs and digital outputs are three-stated with inputs disabled during reset.

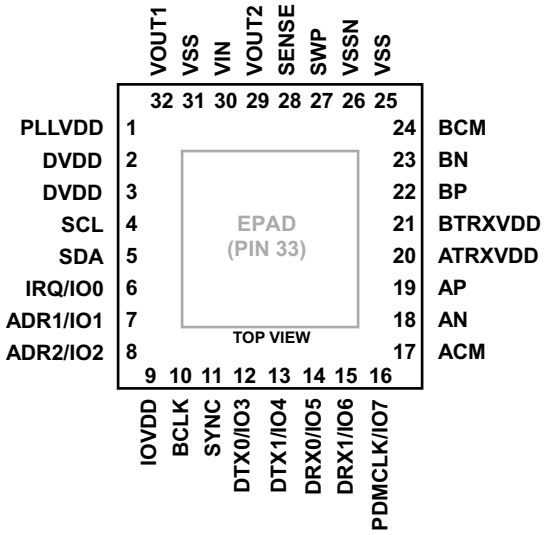


Figure 33. 32-Lead LFCSP_SS and LFCSP Package Pin Configuration

Table 15. AD2420(W)/AD2426(W)/AD2427(W)/AD2428(W)/AD2429(W) Pin Function Descriptions

Pin No.	Pin Name	Type	Alternate Functions[1]	Description
1	PLLVDD	PWR	None	Power Supply for PLL. PLLVDD can be supplied by V_{VOUT1}.
2, 3	DVDD	PWR	None	Power Supply for Digital Core Logic. DVDD can be supplied by V_{VOUT1}.
4[2]	SCL	D_IO	None	Serial Clock for I^2C Data Transfers. Digital input in A^2B master mode. Digital input (I^2C slave) or output (I^2C master) in A^2B slave mode. This pin uses open-drain I/O cells and must be pulled up to V_{I2C_VBUS} through a resistor (consult Version 2.1 of the I^2C bus specification for the proper resistor value). Connect the pin to ground when the I^2C interface is not used.
5[2]	SDA	D_IO	None	I^2C Mode Serial Data. This pin is a bidirectional open-drain input/output and must be pulled up to V_{I2C_VBUS} through a resistor (consult Version 2.1 of the I^2C bus specification for the proper resistor value). Connect the pin to ground if the I^2C interface is not used.
6[2]	IRQ/IO0	D_IO	None	Interrupt Request Output. In master mode, A^2B transceivers create event driven interrupt requests towards the host controller. In slave mode, this pin indicates mailbox empty/full status to the slave node processor when mailbox interrupts are enabled. When not serving as an interrupt output pin, this pin serves as a general-purpose I/O pin with interrupt request input capability. The IRQ/IO0 pin must be initialized to become either an input or an output. This pin is high impedance by default.
7[2]	ADR1/IO1	D_IO	CLKOUT1	The ADR1/IO1 and ADR2/IO2 pins set the I^2C slave device address during power-on reset; up to four A^2B master transceiver chips connect to the same I^2C bus. The ADR1/IO1 pin is high impedance by default. The ADR1/IO1 pin can then be initialized to become a general-purpose input/output (GPIO) pin with interrupt request capability. This pin can be programmed to become a clock output (CLKOUT1). The clock output can be used as a master clock for connected ADCs and DACs or to synchronize switching voltage regulators.

In this table, the Type is defined as follows: PWR = power/ground, A_IN = analog input, D_OUT = digital output, A_IO = analog input/output, D_IO = digital input/output, N/A = not applicable.

Table 15. AD2420(W)/AD2426(W)/AD2427(W)/AD2428(W)/AD2429(W) Pin Function Descriptions (Continued)

Pin No.	Pin Name	Type	Alternate Functions[1]	Description
8[2]	ADR2/IO2	D_IO	CLKOUT2	The ADR1/IO1 and ADR2/IO2 pins set the I²C slave device address during power-on reset; up to four A²B master transceiver chips connect to the same I²C bus. The ADR2/IO2 pin is high impedance by default. The ADR2/IO2 pin can then be initialized to become a general-purpose input/output (GPIO) pin with interrupt request capability. This pin can be programmed to become a clock output (CLKOUT2). The clock output can be used as a master clock for connected ADCs and DACs or to synchronize switching voltage regulators.
9	IOVDD	PWR	None	Power Supply for Digital Input and Output Pins. The digital output pins are supplied from IOVDD, which also sets the highest input voltage that is allowed on the digital input pins. Two I/O voltage ranges are supported (see V_{IOVDD} specifications in the Operating Conditions section). The current draw of these pins is variable and depends on the loads of the digital outputs. IOVDD can be sourced by either the VOUT1 or VOUT2 pin. However, if the signals do not originate from logic supplied by the VOUT1 pin or VOUT2 pin, source IOVDD with an external supply.
10	BCLK	D_IO	PDMCLK	Bit Clock. Digital input in master mode. Digital output in slave mode. When using the PDM interface in slave mode, this pin can operate as the clock output (PDMCLK) for PDM microphones (the PDMCLK/IO7 pin can also be used).
11	SYNC	D_IO	None	Synchronization Signal. Digital input in master mode. Digital output in slave mode. For the AD2428W and AD2429W, the SYNC signal frames a multichannel I²S/TDM data stream. An A²B master node must have a continuous signal because the A²B master transceiver derives all clocking information for itself and for the A²B bus from this input. When this pin stops toggling, the A²B bus resets after a delay. For more information, see Table 3.
12[2]	DTX0/IO3	D_IO	None	For the AD2428W and ADW2429W, serial I²S/TDM data is driven to the DTX0/IO3 pin in multichannel I²S/TDM format. This pin serves as the IO3 general-purpose I/O pin when DTX0 function is disabled. The DTX0/IO3 pin is high impedance by default until configured. The pin returns to high impedance when the chip resets due to a missing synchronization signal or low supply voltage. For the ADW2420W, AD2426W, and AD2427W, this pin is GPIO only (IO3).
13[2]	DTX1/IO4	D_IO	DRX1	For the AD2428W and AD2429W, serial I²S/TDM data is driven to the DTX1/IO4 pin in multichannel I²S/TDM format. When configured as the alternate DRX1 location, the DTX1/IO4 pin receives data presented in multichannel I²S/TDM format. This alternate location can be used when the DRX0/IO5 and DRX1/IO6 pins are used to receive PDM microphone data. This pin serves as the IO4 general-purpose I/O pin when DTX1 and DRX1 functions are disabled. The DTX1/IO4 pin is high impedance by default until configured. The pin returns to high impedance when the chip resets due to a missing synchronization signal or low supply voltage. For the AD2420W, AD2426W, and AD2427W, this pin is GPIO only (IO4).
14[2]	DRX0/IO5	D_IO	PDM0	For the AD2428W and AD2429W, serial I²S/TDM data is received on the DRX0/IO5 pin in multichannel I²S/TDM format. This pin is an input for microphone data when enabled as a PDM input (PDM0). This pin serves as the IO5 GPIO pin when DRX0 and PDM0 functions are disabled. The DRX0/IO5 pin is high impedance by default until configured. The pin returns to high impedance when the chip resets due to a missing synchronization signal or low supply voltage. For the AD2420W, AD2426W, and AD2427W, the DRX0 function is not supported.

In this table, the Type is defined as follows: PWR = power/ground, A_IN = analog input, D_OUT = digital output, A_IO = analog input/output, D_IO = digital input/output, N/A = not applicable.

Table 15. AD2420(W)/AD2426(W)/AD2427(W)/AD2428(W)/AD2429(W) Pin Function Descriptions (Continued)

Pin No.	Pin Name	Type	Alternate Functions[1]	Description
15[2]	DRX1/IO6	D_IO	PDM1	For the AD2428W and AD2429W, serial I²S/TDM data is received on the DRX1/IO6 pin in multichannel I²S/TDM format. This pin is an input for microphone data when enabled as a PDM input (PDM1). This pin serves as the IO6 GPIO pin when DRX1 and PDM1 functions are disabled. The DRX1/IO6 pin is high impedance by default until configured. The pin returns to high impedance when the chip resets due to a missing synchronization signal or low supply voltage. For the AD2420W, AD2426W, and AD2427W, the DRX1 function is not supported.
16[2]	PDMCLK/IO7	D_IO	RRSTRB	PDM Microphone Clock Output. In master mode, the PDM clock output (PDMCLK) is used to clock PDM microphones. This pin runs at 64× the SYNC frequency regardless of the BCLK rate used by the host. When using the PDM interface in slave mode, this pin can still operate as the clock output for PDM microphones (PDMCLK), but BCLK can also be used. When PDM functions are disabled, this pin serves as the IO7 GPIO pin. The PDMCLK/IO7 pin can also be used as a strobe to indicate when reduced rate data is updated (RRSTRB). The PDMCLK/IO7 pin is high impedance by default until configured. The pin returns to high impedance when the chip resets due to a missing synchronization signal or low supply voltage.
17	ACM	A_IN	None	Common-Mode Input for Bidirectional, Differential A²B Line Transceiver A.
18	AN	A_IO	None	Inverted Pin of Bidirectional, Differential A²B Line Driver and Receiver A. Pin 18 is directed towards the master. Pin 18 is self biased.
19	AP	A_IO	None	Noninverted Pin of Bidirectional, Differential A²B Line Driver and Receiver A. Pin 19 is directed towards the master. Pin 19 is self biased.
20	ATRXVDD	PWR	None	Power Supply for A²B Line Driver and Receiver Circuit. Decouple these pins to VSS with one shared 100 nF capacitor and a shared 10 nF capacitor closest to the pin. The pins can be supplied by VOUT2. Supply the ATRXVDD pin for a master, last slave, or daisy-chained slave.
21	BTRXVDD	PWR	None	Power Supply for A²B Line Driver and Receiver Circuit. Decouple these pins to VSS with one shared 100 nF capacitor and a shared 10 nF capacitor closest to the pin. The pins can be supplied by VOUT2. Supply the BTRXVDD pin for a master, last slave, or daisy-chained slave
22	BP	A_IO	None	For the AD2427W, AD2428W, and AD2429W, this is the noninverted pin of bidirectional, differential A²B line driver and Receiver B, which is directed towards the last slave. This pin is self biased.
23	BN	A_IO	None	For the AD2427W, AD2428W, and AD2429W, this is the inverted pin of bidirectional, differential A²B line driver and Receiver B, which is directed towards the last slave. This pin is self biased.
24	BCM	A_IN	None	For the AD2427W, AD2428W, and AD2429W, this is the common-mode input for bidirectional, differential A²B Line Transceiver B.
25	VSS	PWR	None	Power Supply Pin for Return Currents. Connect the VSS pin to a low impedance local VSS ground plane.
26	VSSN	PWR	None	For the AD2427W, AD2428W, and AD2429W, this is the power supply return current connection for the next slave device. Connect to the inductor that provides the negative bias for the next slave device. The AD2427W, AD2428W, and AD2429W connect VSSN to the local VSS potential to sequence power to the next slave devices in the chain. VSSN automatically disconnects under critical fault conditions.
27	SWP	D_OUT	None	For the AD2427W, AD2428W, and AD2429W, this is the active low open-drain output to drive the gate of a PMOS switch. The switch is open (SWP pin is high) by default. The switch can be closed (SWP pin goes low) to sequence power to the next slave devices in the chain. The switch automatically opens (SWP goes high) under critical fault conditions.
28	SENSE	A_IN	None	Analog input to sense the power supplied to the next slave device. For the AD2420W, AD2426W, or a last in line AD2427W/AD2428W/AD2429W, connect this pin to local ground through a 33 kΩ pull-down resistor.

In this table, the Type is defined as follows: PWR = power/ground, A_IN = analog input, D_OUT = digital output, A_IO = analog input/output, D_IO = digital input/output, N/A = not applicable.

Table 15. AD2420(W)/AD2426(W)/AD2427(W)/AD2428(W)/AD2429(W) Pin Function Descriptions (Continued)

Pin No.	Pin Name	Type	Alternate Functions[1]	Description
29	VOUT2	PWR	None	Second Output of the On-Chip low Dropout Voltage Regulator. The voltage output on this pin provides a regulated supply to the TRXVDD supply pins. External devices also can be powered by this supply if the current consumption is within the specification. Decouple VOUT2 to VSS with a 4.7 µF capacitor.
30	VIN	PWR	None	Power supply pin that accepts a wide input voltage range (see the V_{VIN} specification in the Operating Conditions section) for an on-chip low dropout voltage regulator.
31	VSS	PWR	None	Power Supply Pin for Return Currents. Connect the VSS pin to a low impedance local VSS ground plane.
32	VOUT1	PWR	None	First Output of the On-Chip Low Dropout Voltage Regulator. The voltage output on this pin provides a regulated supply to the DVDD and PLLVDD power supply pins. External devices can be powered by this supply if the current consumption is within the specification. Decouple VOUT1 to VSS with a 4.7 µF capacitor.
33	EPAD	PWR	None	Power Supply Pin for Return Currents. See other VSS pin description in this table. This pin is the exposed pad on the bottom of the package and must be connected to GND.

In this table, the Type is defined as follows: PWR = power/ground, A_IN = analog input, D_OUT = digital output, A_IO = analog input/output, D_IO = digital input/output, N/A = not applicable.

[1] See the *AD2420(W)/6(W)/7(W)/8(W)/9(W) Automotive Audio Bus A²B Transceiver Technical Reference* for more information about configuring pins for alternate functions.
[2] If the listed functions for this pin are not required, do not connect this pin.

POWER ANALYSIS

This section provides information on power consumption of the A²B system. The intent of power dissipation calculations is to assist board designers in estimating power requirements for power supply and thermal relief designs.

Power dissipation on an A²B node depends on various factors, such as the required external peripheral supply current and bus activity. An A²B system can be comprised of a mix of bus powered slaves and local powered slaves. A bus powered slave derives power from the A²B bus wires. A local powered slave derives power from separate power wires. Power estimation for a bus powered system is more complex when compared to a local powered system. For power analysis, A²B systems with both local and bus powered slaves must be divided into segments of nodes that draw from the same power supply.

CURRENT FLOW

Figure 34 describe key parameters and equations to calculate power dissipation on the transceiver. The current flow on an A²B node incorporates the described current paths.

- Constant current
  - I_{PLLVDD} — PLL supply current
  - I_{VINQ} — VIN quiescent current
  - I²C I/O current
  - I_{IOVDD} — I²S/TDM/PDM I/O current
  - I_{VEXT1} or I_{VEXT2} — peripheral supply currents
- I_{DVDD} — digital logic supply current
- I_{TRXVDD} — A²B bus TX/RX current
  - LVDS transceiver supply currents of A and B transceivers — transmit LVDS TX and receive LVDS RX

I²C activity and the resulting I/O current is considered negligible when compared to other currents. Therefore, the on-chip I²C I/O current is not considered when calculating the current consumption.

Constant Current

All currents that are not influenced directly by A²B bus activity on other nodes fall under the category of constant current.

PLL Supply Current

The PLL supply current is specified as I_{PLLVDD}, which is the static current in an active transceiver.

VIN Quiescent Current

The VIN quiescent current is specified as the static current I_{VINQ}. It is independent of the load and does not include any power drawn from the voltage regulator output pins.

IOVDD Current

The on-chip I²S/TDM/PDM I/O current I_{IOVDD} is based on dynamic switching currents on the BCLK, SYNC, DTX0, DTX1, DRX0, and DRX1 pins.

The dynamic current, due to switching activity on an output pin, is calculated using the following equation:

$$Output\ Dynamic\ Current = (C_{PDout} + C_L) \times V_{IOVDD} \times f$$

where:
C_{PDout} = dynamic, transient power dissipation capacitance internal to the transceiver output pins.
C_L = total load capacitance that an output pin sees outside the transceiver.
V_{IOVDD} = voltage on a digital pin.
f = frequency of switching on the pin.

The dynamic current, due to switching activity on an input pin, is calculated using the following equation:

$$Input\ Dynamic\ Current = C_{PDin} \times V_{IOVDD} \times f$$

where:
C_{PDin} = dynamic, transient power-dissipation capacitance internal to the input pins of the transceiver.
I_{IOVDD} = the sum of input and output dynamic currents of all pins internally supplied by the IOVDD pin.
f = frequency of switching on the pin.

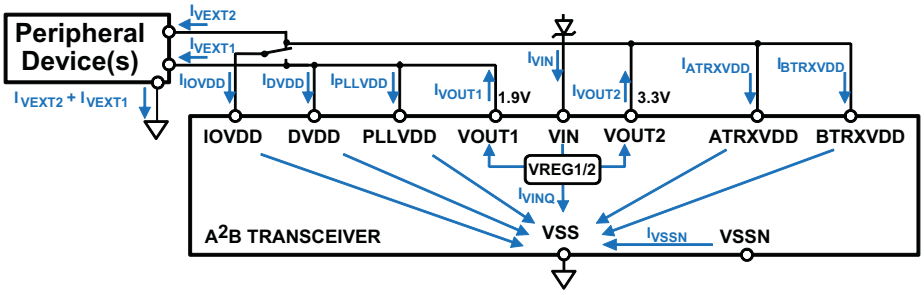


Figure 34. Current Flow Model

Peripheral Supply Current

Peripheral components that are external to the transceiver also can be supplied through the voltage regulator outputs of V_{VOUT1} and V_{VOUT2}. V_{VOUT1} can supply the current specified as I_{VEXT1} to external devices. V_{VOUT2} can supply the current specified as I_{VEXT2} to external devices.

When bus powered, peripheral supply current draw has a direct impact on other nodes in the system. It is important to stay within the thermal package limits and not exceed the specification limits of I_{VSSN} and V_{VIN} in any of the A^{2}B bus nodes.

Digital Logic Supply Current

The digital logic supply current I_{DVDD} is a combination of static current consumption and digital TX/RX current.

A^{2}B Bus TX/RX Current

The level of A^{2}B bus activity directly influences current consumption on both the LVDS transceivers related to A^{2}B transmitter and receiver processing.

LVDS Transmitter and Receiver Supply Currents

The current I_{TRXVDD} depends on I_{TXVDD} and I_{RXVDD} at 100% activity level and A^{2}B bus activity:

- Downstream LVDS transceiver current
  - B transceiver I_{BTXVDD} LVDS TX current results from downstream TX activity level of the current node.
  - A transceiver I_{ARXVDD} LVDS RX current results from downstream activity level of the previous node.
- Upstream LVDS transceiver current
  - A transceiver I_{ATXVDD} LVDS TX current results from A side upstream activity level of the current node.
  - B transceiver I_{BRXVDD} LVDS RX current results from upstream activity level of the next in line node.

Downstream/Upstream Activity Level

The activity level for downstream data of TRX B is determined by the following:

- Header bits for downstream. A^{2}B systems use 64 downstream header bits referred to as a synchronization control frame (SCF).
- The number of downstream data bits transmitted in a node = the number of downstream transmitted slots × (bits per slot + parity bit) where the parity bit = 1. The number of downstream transmitted slots does not include the locally consumed slots.
- B side downstream transmitter activity level of a node. (SCF bits + number of downstream transmitted data bits) ÷ 1024.

The activity level for upstream data of TRX A is determined by the following:

- Header bits for upstream. (SRF bits + total number of received downstream data bits) ÷ 1024.
- The number of upstream data bits transmitted in a node = number of upstream transmitted slots × (bits per slot + parity bit) where the parity bit = 1. The number of upstream transmitted slots is the sum of received upstream slots and locally contributed slots.
- A side upstream transmitter activity level of a node. (SRF bits + number of transmitted upstream data bits) ÷ 1024.

LVDS Transmitter and Receiver Idle Current

The idle current, I_{TRXVDD_IDLE}, depends on I_{TXVDD} and I_{RXVDD} at 0% activity level and A^{2}B bus idle time.

- B transceiver idle current. B Transceiver $I_{BTRXVDD_IDLE}$ LVDS current results from B transceiver idle time.
- A transceiver idle current. A Transceiver $I_{ATRXVDD_IDLE}$ LVDS current results from A transceiver idle time.
- B transceiver idle time. B transceiver idle time is the time when both the TX and RX of the B transceiver are idle.

  The idle time of the B transceiver is derived by eliminating the following activity levels from the B transceiver frame cycle:
  - B transceiver downstream activity level of the current node.
  - A transceiver upstream activity level of the next in line node.
- A transceiver idle time is the time when both the TX and RX of the A transceiver are idle.

  The idle time of the A transceiver is derived by eliminating the following activity from the A transceiver frame cycle:
  - A transceiver upstream activity level of the current node.
  - B transceiver downstream activity level of previous node.

  The sum of the LVDS transceiver currents is
  $I_{TRXVDD} = I_{BRXVDD} + I_{BTXVDD} + I_{ARXVDD} + I_{ATXVDD} + I_{BTRXVDD_IDLE} + I_{ATRXVDD_IDLE}$

VREG1 AND VREG2 OUTPUT CURRENTS

Voltage regulator output currents are governed by the following equations:

I_{VOUT2} is the current from V_{VOUT2} which is the sum of the LVDS transmitter and receiver supply currents, peripheral supply currents, and I/O current.

$$I_{VOUT2} = I_{TRXVDD} + I_{IOVDD} + I_{VEXT2}$$

I_{VOUT1} is the current from the V_{OUT1} pin which is the sum of PLL supply current, I_{PLLVDD}, digital logic supply current I_{DVDD}, peripheral supply current, I_{VEXT1}, and I^{2}S/TDM/PDM I/O current I_{IOVDD}.

$$I_{VOUT1} = I_{PLLVDD} + I_{VEXT1} + I_{DVDD} + I_{IOVDD}$$

I_{IOVDD} in a slave node can be sourced by either I_{VOUT1} or I_{VOUT2} but not both, depending on whether I_{IOVDD} is supplied from V_{VOUT1} or V_{VOUT2}.

CURRENT AT VIN (I_{VIN})

The current at the VIN pin (I_{VIN}) of the transceiver is the sum of currents I_{VOUT1} and I_{VOUT2} and the quiescent current, shown in Figure 34 and in the following equation:

$$I_{VIN} = I_{VOUT1} + I_{VOUT2} + I_{VINQ}$$

The A side node current is the line bias current from an earlier node. In a bus powered node, it is also the power supply current and a portion of this current supplies the next in line nodes.

$$I_A = I_{VIN} + I_B + I_{VREGPERI}$$

where:
I_B = B side current to the next node (= I_{VSSN} return current and I_A of the next in line node).
$I_{VREGPERI}$ = peripheral current supplied from I_A by extra voltage regulator, external to the transceiver (not illustrated in Figure 35 and Figure 36).

POWER DISSIPATION

The power dissipation of the transceiver is calculated using the following equation:

$$Power = I_{VIN} \times V_{VIN} + (I_{VSSN})^2 \times R_{VSSN} - I_{VEXT1} \times V_{VOUT1} - I_{VEXT2} \times V_{VOUT2}$$

where:
I_{VIN} = current at VIN pin.
V_{VIN} = voltage at VIN pin.
I_{VSSN} = B side current I_B to the next node and return current from the next node. The next node is the node connected to the B terminal of the current node. See Figure 35.
R_{VSSN} = internal V_{SSN} on resistance (see Table 16).
I_{VEXT1} = peripheral supply current from V_{VOUT1}.
I_{VEXT2} = peripheral supply current from V_{VOUT2}.
V_{VOUT1} = output voltage from V_{REG1}.
V_{VOUT2} = output voltage from V_{REG2}.

RESISTANCE BETWEEN NODES

Figure 35 shows the dc model of a system with a combination of local and bus powered A^2B slaves.

A voltage drop of the dc bias is observed between the A^2B nodes, due to resistance and current consumption. Table 16 lists the causes of the dc resistance between nodes ($R_{BETWEEN}$) with example resistance values.

Both bias supply and return currents are subject to resistance. Therefore, some resistance values must be doubled (for example, wire length resistance).

Table 16. Breakdown/Budget of Typical DC Resistance Between Nodes

Resistance	Each	Qty	Total	Unit
Inductor DC Resistance	0.26	4	1.04	Ω
Short Circuit Protection Resistor	1.05	1	1.05	Ω
Positive Bias PMOS Switch On-Resistance	0.11	1	0.11	Ω
Negative Bias Switch On-Resistance R_{VSSN}	1.2	1	1.2	Ω
Resistance of Connections	0.01	4	0.04	Ω
Total R_{SUM}	N/A[1]	N/A[1]	2.39	Ω
Wire Length Resistance of Cable	0.121	2	0.242	Ω/m

[1] N/A means not applicable.

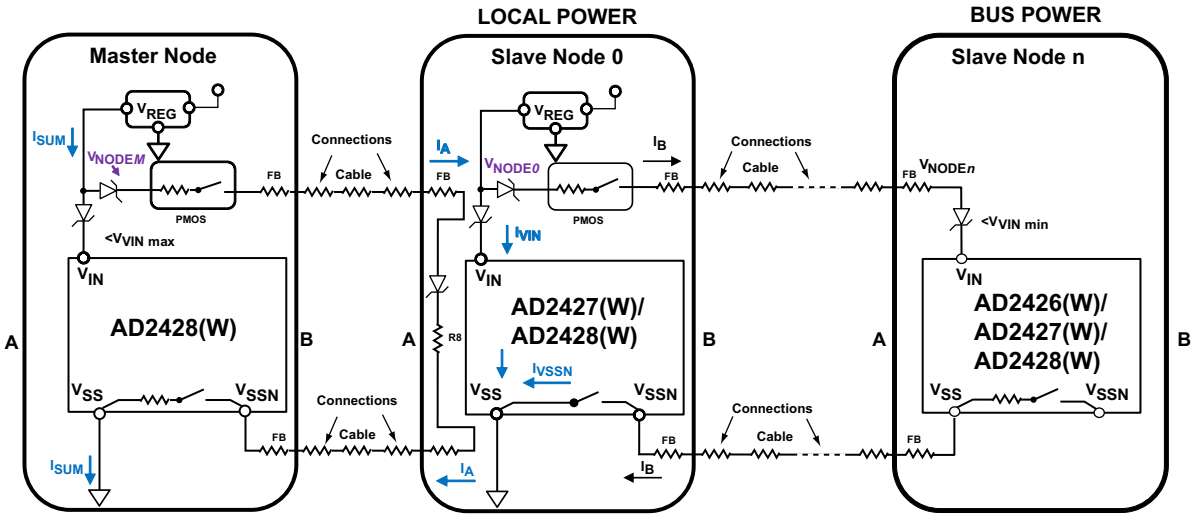


Figure 35. A^2B DC Power Model for a System with Local and Bus Powered Slaves

VOLTAGE REGULATOR CURRENT IN MASTER NODE OR LOCAL POWERED SLAVE NODE

The bus power, required from a local powered node (master node) for powering all nodes in the system, is calculated using the following equation:

$$I_{SUM} = I_{VIN} + I_{VSSN} + I_{INRUSH} + I_{VREGPERI}$$

where:
I_{VIN} is the current to V_{VIN} of the local powered mode.
I_{VSSN} is the return current from next in line slave node. It is equal to the I_A current supplied to the next in line node.

I_{INRUSH} is the inrush current required to charge capacitors on the VIN pin at power-up.
$I_{VREGPERI}$ is the input current of extra V_{REG} for peripherals (not illustrated in Figure 35 and Figure 36).

Analog Devices recommends a minimum I_{INRUSH} of 150 mA to support the components shown in the reference schematics. The selected voltage regulator must be sized to meet I_{SUM} for the application.

I_{VSSN} current is below 2 mA when the next in line node is a local powered slave with a circuit-based on the Designer Reference section. The I_{SUM} current in most applications is less than 100 mA if the next in line node is a local powered slave node.

More current, I_{VSSN}, is drawn if the next in line node uses bus power.The I_{VSSN} maximum specification limits the bus power draw of slave nodes, especially in a line of bus powered slaves.

POWER DISSIPATION OF A²B BUS

The power dissipation of an A²B system is calculated as follows:

$$Power\ Dissipation = I_{SUM} \times V_{VIN} \text{ of master.}$$

POWER ANALYSIS OF BUS POWERED SYSTEM

Figure 36 shows the dc model for a bus powered A²B system.

Power equations in this data sheet are used for power calculations in the SigmaStudio® software. The power equations are also available in an Excel spreadsheet, provided by technical support upon request.

SUPPLY VOLTAGE

The supply voltage (V_{VIN}) level on a bus powered transceiver is predictable and can be calculated using the following equations derived from Figure 36.

For the master node, the supply voltage is calculated as,

$$V_{NODEM} = V_{REGM} - V_{DIODE3}$$
$$V_{VIN} = V_{REGM} - V_{DIODE1} \text{ for master}$$

For a slave node, the supply voltage is calculated as,

$$V_{NODE} = V_{NODE}' - I_A \times R_{BETWEEN}$$
$$V_{VIN} = V_{NODE} - V_{DIODE1}$$

where:
V_{NODE}' is the V_{NODE} voltage potential of the earlier node. The earlier node is the node connected to the A side transceiver of the current node.
$R_{BETWEEN}$ is the connection resistance between the current and earlier node, described in the Resistance Between Nodes section.
V_{DIODE} is the voltage drop of the Shottkey reverse polarity protection diode.

I_A is the current that a bus powered slave node draws from an earlier node.

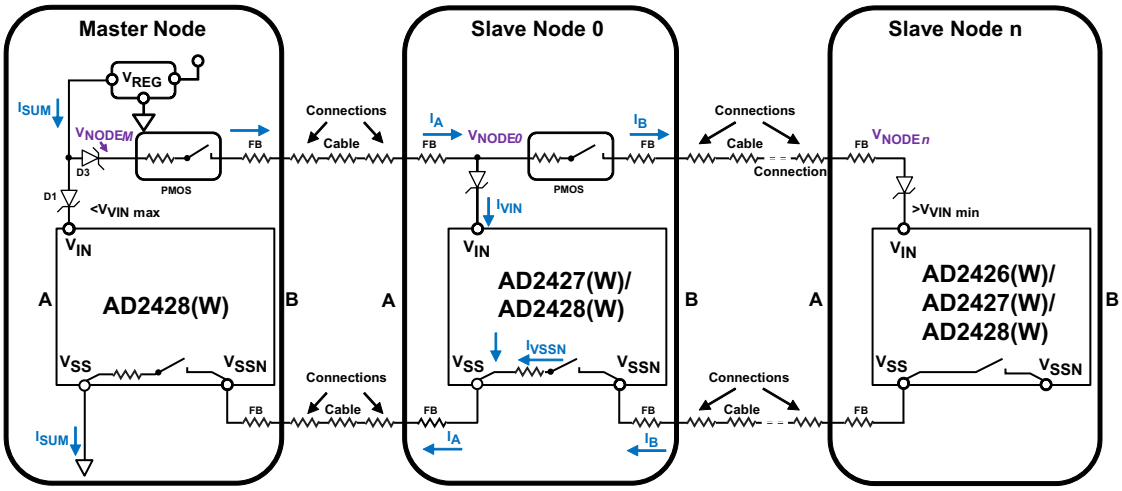


Figure 36. A²B Power Model for Bus Powered System

For a system with all in-line bus powered nodes, I_A is calculated cumulatively from the last in-line node as

$$I_A = I_{VIN} + I_B$$

where:
I_A = current that a bus powered slave node draws from an earlier node.
I_{VIN} = current at VIN pin.
I_B = B side return current from the next in line node. The next in line node is the node connected to the B terminal of the current node.

REDUCING POWER CONSUMPTION

The following sections describe three methods that reduce power consumption.

Power-Down Mode

Any node in an A^{2}B bus powered system can be shut down by disconnecting the power supply in the previous slave node (towards the master). Disconnecting a slave from the power supply also powers down all of the following slaves (towards the last slave).

Standby Mode

The A^{2}B bus enters standby mode by setting the AD242X_DATCTL.STANDBY bit of the master. The SCF in standby mode is 19 bits long, instead of 64 bits. In standby mode, there is no upstream and no downstream traffic on the A^{2}B bus, and only a minimal SCF keeps all the slave nodes synchronized. This keeps the A^{2}B bus power in the lowest power state while maintaining clock synchronization between nodes. Using the equations in the Downstream/Upstream Activity Level section, the bus activity level in standby mode is,

- Downstream activity level = 19 ÷ 1024 = 1.9%
- Upstream activity level = 0%

The digital transceiver current, including the LVDS TX and RX current, are subject to the activity levels. The LVDS TX and RX current also are subject to idle current during the bus idle time.

Control Mode

In control mode, there are no data channels in a superframe. The superframe only has the 64-bit SCF and SRF in the frame with the control data embedded in the header bits. Therefore, the A^{2}B bus power is less when compared to normal mode, which has data channels in the superframe. Using the equations in the Downstream/Upstream Activity Level section, the bus activity level in control mode is,

- Bus activity level downstream = 64 ÷ 1024 = 6.3%
- Bus activity level upstream = 64 ÷ 1024 = 6.3%

The LVDS TX and RX current also are subject to idle current during the bus idle time.

THERMAL POWER

When calculating power, system designers must consider thermal power. Thermal power calculations are based on the package thermal characteristics, shown in the following equation:

θ_{JA} = thermal resistance

$(T_J - T_A) \div power$ [°C/W] *with airflow* = 0 m/s

Table 17 provides the thermal power allowance example. These values are derived from a JEDEC standard 2S2P test board. θ_{JA} values vary significantly and depend on system design and conditions. For the example calculation in Table 17, the θ_{JA} value provided is determined using the JEDEC standard conditions.

In this example (Table 17), a slave node with 292 mW of power dissipation is used to provide the maximum estimated power. The margin is calculated by subtracting the maximum estimated power from the thermal power allowance.

Table 17. Thermal Power Allowance Example

Parameter	Example Value	Unit
T_A	105	°C
T_J	125	°C
Delta ($T_J - T_A$)	20	°C
Example θ_{JA}	31.6	°C/W
Maximum Allowed Thermal Power	633	mW
Maximum Estimated Power	292	mW
Power Margin	341	mW

DESIGNER REFERENCE

The following sections provide descriptions and layouts of some typical node configurations.

An A^{2}B-compliant master transceiver requires external components to pass EMC and ESD tests in the automotive environment and support full line diagnostics functionality. Diodes are required for correct line diagnostics and to prevent damage under line fault conditions. The master circuit must also supply bias voltage for line diagnostics and power supply to bus powered slaves.

An A^{2}B-compliant, last in the line, local powered, slave node transceiver requires external components to pass EMC and ESD tests in the automotive environment. The circuit must allow for full line diagnostics with properly terminated A^{2}B bus bias and properly terminated signals. The circuit must also electrically isolate the local powered slave node from the earlier node to prevent line faults triggered by the formation of ground loops across power and communication wires.

An A^{2}B-compliant, local powered, slave node transceiver requires external components to pass EMC and ESD tests in the automotive environment. The circuit must allow for full line diagnostics with properly terminated A^{2}B bus bias and properly terminated signals (A-side). The local powered slave node regenerates the bias voltage from its local supply and provides it to the next node (B-side) for line diagnostics and as a voltage supply for bus powered nodes. Diodes are required for correct line diagnostics and damage prevention under line fault conditions.

An A^{2}B-compliant, bus powered, slave node transceiver requires external components to pass EMC and ESD tests in the automotive environment. The circuit must use the A^{2}B bias (A-side) as its low-pass filtered supply voltage (using inductors and capacitors). A^{2}B communication signals must be separated from the dc content at the A-side transceiver by high-pass filtering with ac coupling capacitors. Capacitors must also be used on the B-side where the ac-coupled signal is merged with the recovered bias, which is supplied through ac signal blocking inductors. The bus powered slave node must include circuitry to forward the recovered bias voltage to the next node and to perform line diagnostics. A diode is required for correct line diagnostics and damage prevention under line fault conditions.

Contact your local Analog Devices representative for the latest schematic circuit recommendations and bill of materials for each of these node configurations. The recommended circuit and component selection must be followed for A^{2}B automotive-grade compliance.

V_{SENSE} AND CONSIDERATIONS FOR DIODES

The relative difference between the voltage on the VIN pin, V_{VIN}, and the A^{2}B bus bias voltage, V_{SENSE}, is monitored by the SENSE pin under steady state normal operating conditions. The range must be within the values described in Table 18 for all line diagnostics to function correctly.

Table 18. V_{VIN} to V_{SENSE} Range

Range	Min	Max	Unit
V_{VIN} to V_{SENSE}	– 0.6	+0.5	V

The difference between V_{VIN} and V_{SENSE} is primarily influenced by diode voltage drops and the on resistance of the PMOS. (Contact your local Analog Devices representative for the latest schematic circuit recommendations and bill of materials.) Table 19 identifies which diodes cause voltage drops for each node type.

Table 19. V_{VIN} to V_{SENSE}Voltage Dependencies

Node Type	V_{VIN} to V_{SENSE} Diode Dependencies
Master	D1, D3
Locally Powered Slave	D1, D3
Bus Powered Slave	D1

OPTIONAL ADD ON CIRCUITS

An earlier node in the sequence can remotely power up the next locally powered slave node over the A^{2}B bus by switching the bias voltage onto the A^{2}B bus. The local powered slave node can sense this bias voltage and use it as an enable input for power switches or voltage regulators to awake the device from a very low current sleep mode.

An optocoupler, shown in Figure 37, can differentiate input of the bias voltage and ensures that the locally powered slave node is electrically isolated. This avoids ground loops that can induce noise and also trigger line fault detection. Current during sleep is determined by the optocoupler transistor off current, the resistor to ground (R12), and the power switch enable circuit.

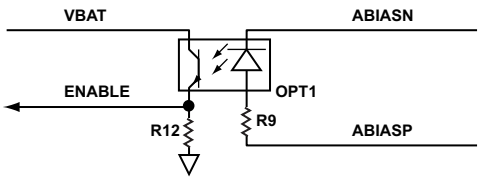


Figure 37. Optional Power Supply Enable Circuit with Optocoupler

LAYOUT GUIDELINES

The transceivers are highly integrated devices, comprising both digital sections for audio data, clocks, PLL, and analog A^2B transceiver sections. Use the following design rules to maximize performance and signal integrity:

- Solder the exposed paddle underneath the transceiver effectively to the PCB where it is locally connected to the ground plane. Figure 38 shows transceiver foot print, recommended solder mask (matching exposed paddle), paste mask (dividing exposed paddle), and stitching of the ground plane.

  The solder paste under the exposed paddle is split into four square areas, which minimizes solder wicking through uncovered thermal vias and prevents sliding or tilting of the chip during solder reflow. See *Soldering Considerations for Exposed-Pad Packages (EE-352)*, on the Analog Devices web site. The exposed paddle is used for a thermal pathway as well as for electrical connection.
- Place power supply decoupling capacitors as close as possible to the transceiver chip with the smallest value capacitor being closest to the pin.
- Route all traces as short as possible, especially the AP/AN and BP/BN signals.
- Symmetrically route the AP/AN and BP/BN signals to suppress EMC. Match routing parasitic capacitance and inductance.
- Symmetrically shield the AP/AN and BP/BN signals with ground. Use shields that are at least 0.5 mm wide and stitched generously with vias to the GND plane. Symmetry is best achieved with flooded plane areas.
- Do not route switching signals or power supply traces next to or underneath the AP/AN and BP/BN signals.
- Avoid using trace stubs, especially if they create an asymmetry on the AP/AN and BP/BN signals. Symmetrically route into and out of pads rather than branch out.
- Differential impedance trace of the AP/AN and BP/BN signals should be 100 Ω ± 10% (10 MHz to 100 MHz) on both sides of the common-mode choke.
- Avoid unnecessary layer transitions for the AP/AN and BP/BN signals. Match necessary layer transitions for differential signals.
- Use an impedance of 50 Ω ± 10% to ground on all traces.
- Magnetically separate common-mode chokes from each other by at least 2 mm.
- Do not route ground or other signals on any layer underneath the common-mode chokes. Extend this exclusion at least 2 mm from between the pads.
- For shielded wires, connect the shield to the local ground.
- Place one side of the inductors in the signal path and bridge dc signals to the power and ground nets.
- Place termination resistors symmetrically and close to the common-mode chokes.
- Where possible, flood unused PCB areas with connected ground planes on all layers.
- Stitch ground planes at least every 5 mm.
- Do not obstruct power supply and ground return paths by vias.
- Use series resistors (≥33 Ω) near the source of clock and fast data signals. Also consider footprints for small filter capacitors for such signal traces.
- Avoid using right angle bends in signal routing. Use rounded or 45 degree mitered bends instead.
- Use shortest possible signal path on connectors (inner row of multirow, right angled connectors).
- On multipin connectors, provide at least 3 mm spacing around differential A^2B pin pairs to ensure that A^2B signal pairs are closer to each other than to adjacent signals. The spacing improves EMC performance.

  Use low impedance static signals (ground) symmetrically on connector pins adjacent to the A^2B bus pairs when tight spacing is required.

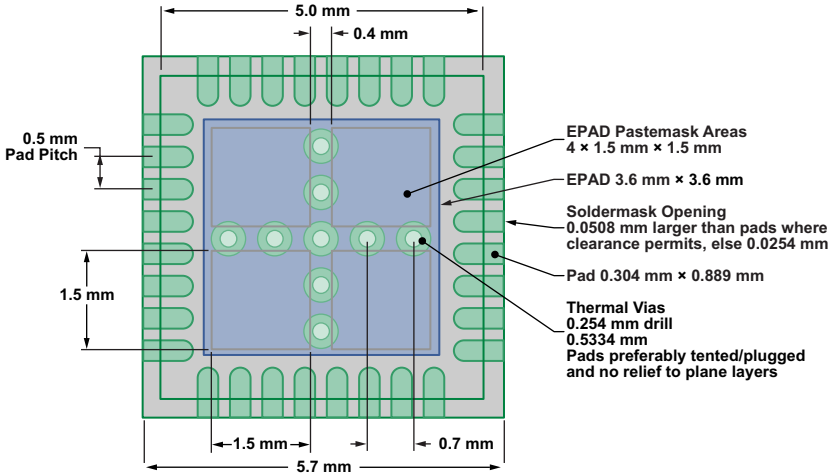


Figure 38. Transceiver Footprint

OUTLINE DIMENSIONS

Figure 39 shows the outline dimensions for the 32-Lead LFCSP_SS (CS-32-3).

Figure 40 shows the outline dimensions for the 32-Lead LFCSP (CP-32-12).

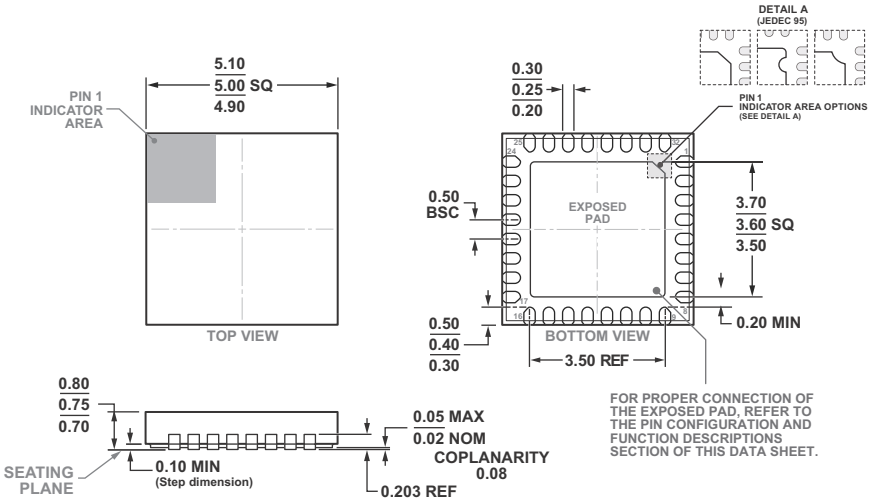
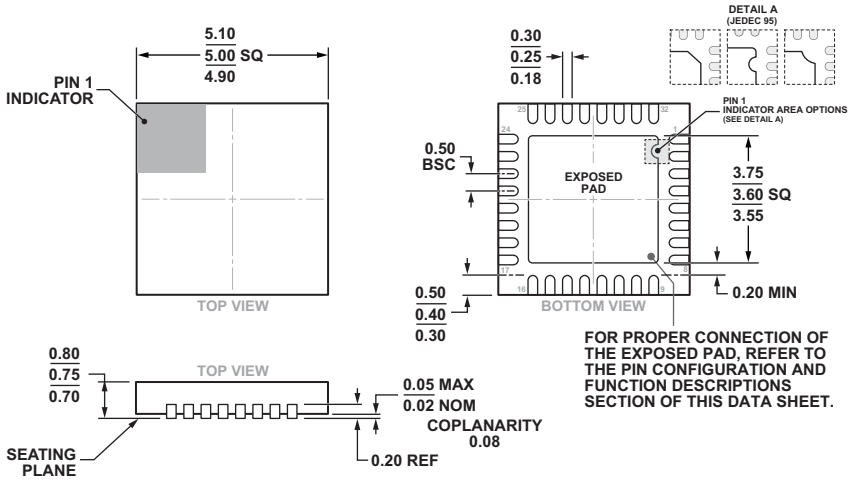


Figure 39. 32-Lead Lead Frame Chip Scale Package [LFCSP_SS]
5 mm x 5 mm Body, With Side Solderable Leads
(CS-32-3)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5

Figure 40. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm x 5 mm Body and 0.75 mm Package Height
(CP-32-12)
Dimensions shown in millimeters

AUTOMOTIVE PRODUCTS

The AD2420W/AD2426W/AD2427W/AD2428W/AD2429W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the nonautomotive models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 20 are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 20. Automotive Products

Model[1, 2, 3, 4]	Temperature Range[5]	Description	Package Option
AD2420WCCPZxx	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12
AD2420WCCPZxx-RL	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12
AD2426WCCSZ	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP_SS]	CS-32-3
AD2426WCCSZ-RL	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP_SS]	CS-32-3
AD2426WCCSZxx	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP_SS]	CS-32-3
AD2426WCCSZxx-RL	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP_SS]	CS-32-3
AD2427WCCSZ	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP_SS]	CS-32-3
AD2427WCCSZ-RL	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP_SS]	CS-32-3
AD2427WCCSZxx	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP_SS]	CS-32-3
AD2427WCCSZxx-RL	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP_SS]	CS-32-3
AD2428WCCSZ	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP_SS]	CS-32-3
AD2428WCCSZ-RL	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP_SS]	CS-32-3
AD2428WCCSZxx	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP_SS]	CS-32-3
AD2428WCCSZxx-RL	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP_SS]	CS-32-3
AD2429WCCPZxx	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12
AD2429WCCPZxx-RL	−40°C to +125°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] RL = Supplied on Tape and Reel.
[4] For model numbers ending in xx or xx-RL, xx denotes the die revision.
[5] Referenced temperature is junction temperature. See the Operating Conditions section for junction temperature (T_J) specification.

ORDERING GUIDE

Model[1]	Temperature Range[2]	Description	Package Option
AD2420KCPZ	0°C to 105°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12
AD2420BCPZ	–40°C to +105°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12
AD2426KCPZ	0°C to 105°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12
AD2426BCPZ	–40°C to +105°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12
AD2427KCPZ	0°C to 105°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12
AD2427BCPZ	–40°C to +105°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12
AD2428KCPZ	0°C to 105°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12
AD2428BCPZ	–40°C to +105°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12
AD2429KCPZ	0°C to 105°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12
AD2429BCPZ	–40°C to +105°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12

[1] Z = RoHS Compliant Part.
[2] Referenced temperature is junction temperature. See the Operating Conditions section for junction temperature (T_J) specification.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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