



Enhanced Product

AD5324-EP

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REVISION HISTORY

6/2019—Rev. 0 to Rev. A

Changes to Patent Information.....	1
Changes to Offset Error Parameter, Table 1 and Gain Error Parameter, Table 1.....	3
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Updated Outline Dimensions	11

4/2010—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 2.5\text{ V to }5.5\text{ V}$; $V_{REF} = 2\text{ V}$; $R_L = 2\text{ k}\Omega$ to GND; $C_L = 200\text{ pF}$ to GND; all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 1.

Parameter	S Version			Unit	Conditions/Comments
	Min	Typ	Max		
DC PERFORMANCE ¹					
Resolution		12		Bits	Guaranteed monotonic by design over all codes See Figure 6 and Figure 8 See Figure 6 and Figure 8 Lower dead band exists only if offset error is negative $\Delta V_{DD} = \pm 10\%$ $R_L = 2\text{ k}\Omega$ to GND or V_{DD}
Relative Accuracy		± 2	± 10	LSB	
Differential Nonlinearity ²		± 0.2	± 1	LSB	
Offset Error		± 0.4	± 3	% of FSR	
Gain Error		± 0.15	± 1	% of FSR	
Lower Dead Band		20	60	mV	
Offset Error Drift ³		-12		ppm of FSR/ $^{\circ}\text{C}$	
Gain Error Drift ³		-5		ppm of FSR/ $^{\circ}\text{C}$	
DC Power Supply Rejection Ratio ³		-60		dB	
DC Crosstalk ³		200		μV	
DAC REFERENCE INPUTS ³					
V_{REF} Input Range	0.25		V_{DD}	V	Normal operation Power-down mode Frequency = 10 kHz
V_{REF} Input Impedance	37	45		k Ω	
		>10		M Ω	
Reference Feedthrough		-90		dB	
OUTPUT CHARACTERISTICS ³					
Minimum Output Voltage ⁴		0.001		V	Measurement of the minimum and maximum V drive capability of the output amplifier
Maximum Output Voltage ⁴		$V_{DD} - 0.001$			
DC Output Impedance		0.5		Ω	$V_{DD} = 5\text{ V}$ $V_{DD} = 3\text{ V}$
Short Circuit Current		25		mA	
		16		mA	
Power-Up Time		2.5		μs	Coming out of power-down mode $V_{DD} = 5\text{ V}$
		5		μs	Coming out of power-down mode $V_{DD} = 3\text{ V}$
LOGIC INPUTS ³					
Input Current			± 1	μA	$V_{DD} = 5\text{ V} \pm 10\%$ $V_{DD} = 3\text{ V} \pm 10\%$ $V_{DD} = 2.5\text{ V}$ $V_{DD} = 5\text{ V} \pm 10\%$ $V_{DD} = 3\text{ V} \pm 10\%$ $V_{DD} = 2.5\text{ V}$
V_{IL} , Input Low Voltage			0.8	V	
			0.6	V	
			0.5	V	
V_{IH} , Input High Voltage	2.4			V	
	2.1			V	
	2.0			V	
Pin Capacitance		3		pF	
POWER REQUIREMENTS					
V_{DD}	2.5		5.5	V	$V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$ $V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$
I_{DD} (Normal Mode) ⁵					
$V_{DD} = 4.5\text{ V to }5.5\text{ V}$		600	900	μA	$V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$ $V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$
$V_{DD} = 2.5\text{ V to }3.6\text{ V}$		500	700	μA	
I_{DD} (Power-Down Mode)					$V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$ $V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$
$V_{DD} = 4.5\text{ V to }5.5\text{ V}$		0.2	1	μA	
$V_{DD} = 2.5\text{ V to }3.6\text{ V}$		0.08	1	μA	

¹ DC specifications tested with the outputs unloaded.

² Linearity is tested using a reduced code range: Code 115 to Code 3981.

³ Guaranteed by design and characterization, not production tested.

⁴ For the amplifier output to reach the minimum voltage, offset error must be negative. For the amplifier output to reach the maximum voltage, $V_{REF} = V_{DD}$ and offset plus gain error must be positive.

⁵ I_{DD} specification is valid for all DAC codes; interface inactive; all DACs active; load currents excluded.

AC CHARACTERISTICS

$V_{DD} = 2.5 \text{ V}$ to 5.5 V ; $R_L = 2 \text{ k}\Omega$ to GND; $C_L = 200 \text{ pF}$ to GND; all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 2.

Parameter ¹	S Version ²			Unit	Conditions/Comments
	Min	Typ	Max		
Output Voltage Settling Time		8	10	μs	$V_{REF} = V_{DD} = 5 \text{ V}$ $\frac{1}{4}$ scale to $\frac{3}{4}$ scale change (0x400 to 0xC00)
Slew Rate		0.7		$\text{V}/\mu\text{s}$	
Major Code Transition Glitch Energy		12		$\text{nV}\cdot\text{sec}$	1 LSB change around major carry
Digital Feedthrough		1		$\text{nV}\cdot\text{sec}$	
Digital Crosstalk		1		$\text{nV}\cdot\text{sec}$	
DAC-to-DAC Crosstalk		3		$\text{nV}\cdot\text{sec}$	
Multiplying Bandwidth		200		kHz	$V_{REF} = 2 \text{ V} \pm 0.1 \text{ V p-p}$
Total Harmonic Distortion		-70		dB	$V_{REF} = 2.5 \text{ V} \pm 0.1 \text{ V p-p}$; frequency = 10 kHz

¹ Guaranteed by design and characterization, not production tested.

² Temperature range (S Version): -55°C to $+125^\circ\text{C}$; typical at $+25^\circ\text{C}$.

TIMING CHARACTERISTICS

$V_{DD} = 2.5\text{ V to }5.5\text{ V}$; all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 3.

Parameter ^{1, 2, 3}	Limit at T_{MIN} , T_{MAX}		Unit	Conditions/Comments
	$V_{DD} = 2.5\text{ V to }3.6\text{ V}$	$V_{DD} = 3.6\text{ V to }5.5\text{ V}$		
t_1	40	33	ns min	SCLK cycle time
t_2	16	13	ns min	SCLK high time
t_3	16	13	ns min	SCLK low time
t_4	16	13	ns min	$\overline{\text{SYNC}}$ to SCLK falling edge setup time
t_5	5	5	ns min	Data setup time
t_6	4.5	4.5	ns min	Data hold time
t_7	0	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
t_8	80	33	ns min	Minimum $\overline{\text{SYNC}}$ high time

¹ Guaranteed by design and characterization, not production tested.

² All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

³ See Figure 2.

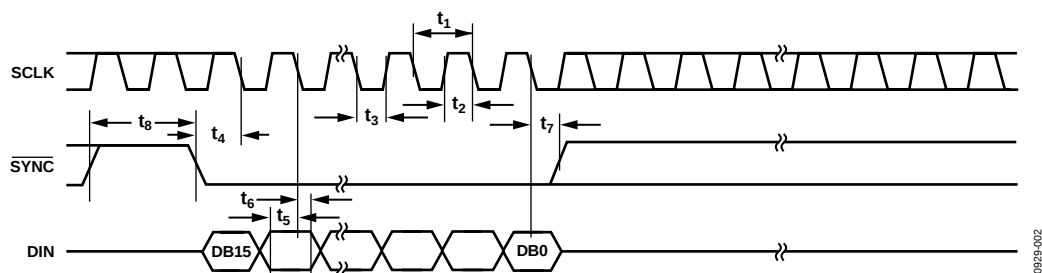


Figure 2. Serial Interface Timing Diagram

00929-002

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter ¹	Rating
V_{DD} to GND	–0.3 V to +7 V
Digital Input Voltage to GND	–0.3 V to $V_{DD} + 0.3$ V
Reference Input Voltage to GND	–0.3 V to $V_{DD} + 0.3$ V
V_{OUTA} through V_{OUTD} to GND	–0.3 V to $V_{DD} + 0.3$ V
Operating Temperature Range	
Industrial (EP Version)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature (T_J max)	150°C
10-Lead MSOP	
Power Dissipation	$(T_J \text{ max} - T_A) / \theta_{JA}$
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	10 sec to 40 sec

¹ Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

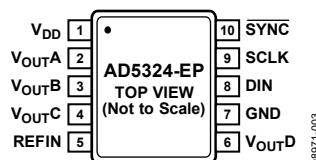


Figure 3. MSOP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD}	Power Supply Input. This part can be operated from 2.5 V to 5.5 V and the supply can be decoupled to GND.
2	V _{OUTA}	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
3	V _{OUTB}	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
4	V _{OUTC}	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
5	REFIN	Reference Input Pin for All Four DACs. It has an input range from 0.25 V to V _{DD} .
6	V _{OUTD}	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
7	GND	Ground Reference Point for All Circuitry on the Part.
8	DIN	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input. The DIN input buffer is powered down after each write cycle.
9	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at clock speeds up to 30 MHz. The SCLK input buffer is powered down after each write cycle.
10	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the input shift register and data is transferred in on the falling edges of the following 16 clocks. If $\overline{\text{SYNC}}$ is taken high before the 16 th falling edge of SCLK, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.

TYPICAL PERFORMANCE CHARACTERISTICS

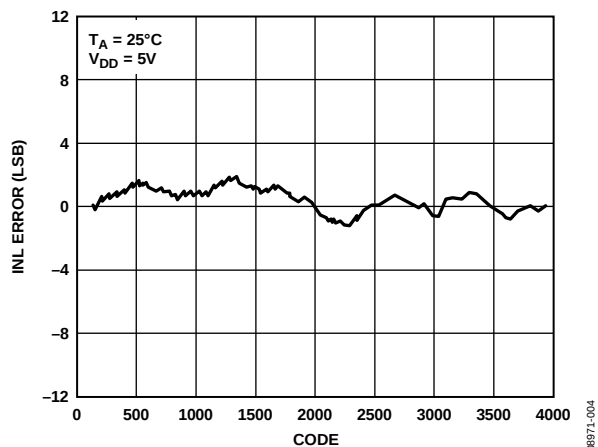


Figure 4. Typical Integral Nonlinearity (INL) Plot

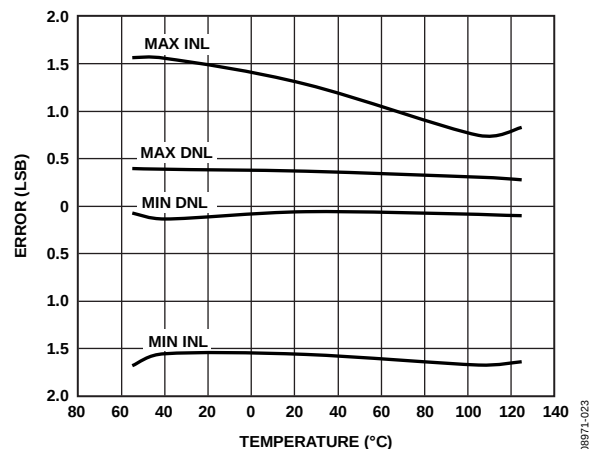


Figure 7. INL and DNL Error vs. Temperature

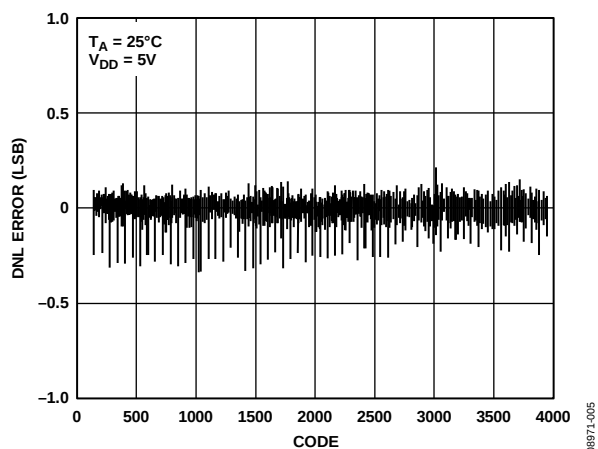


Figure 5. Typical Differential Nonlinearity (DNL) Plot

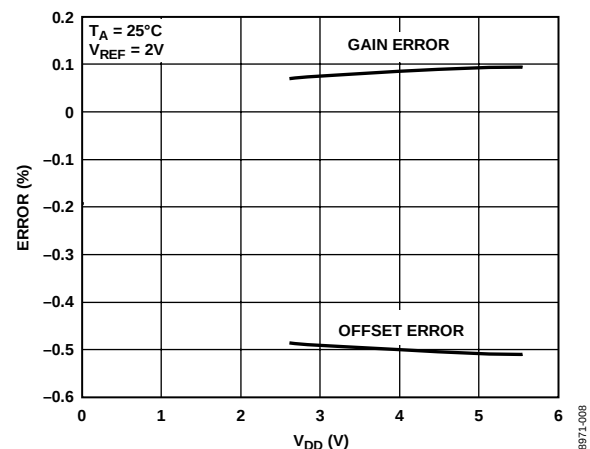
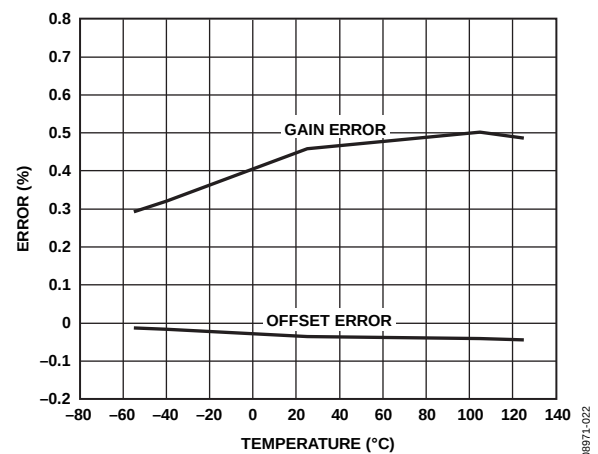
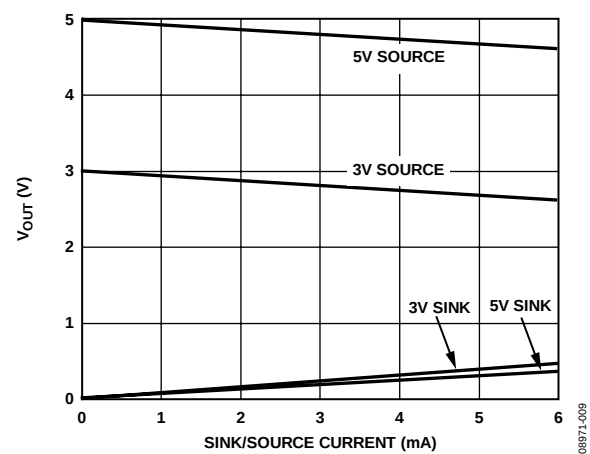
Figure 8. Offset Error and Gain Error vs. V_{DD} 

Figure 6. Offset Error and Gain Error vs. Temperature

Figure 9. V_{OUT} Source and Sink Current Capability

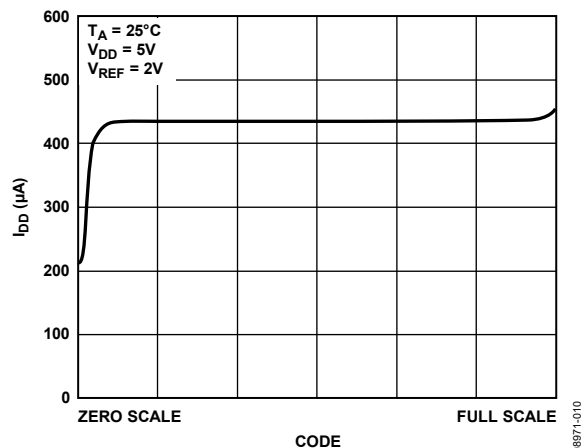


Figure 10. Supply Current vs. DAC Code

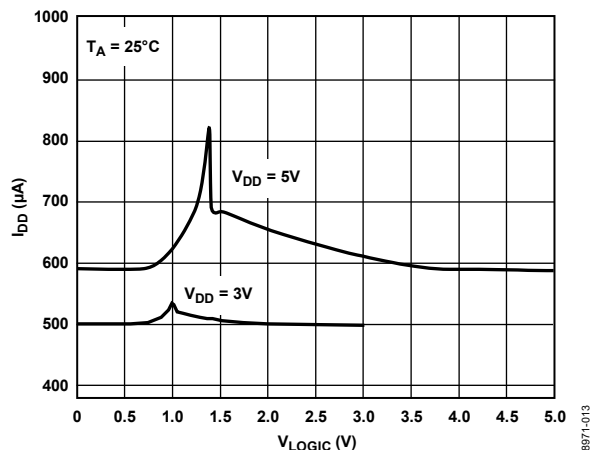


Figure 13. Supply Current vs. Logic Input Voltage

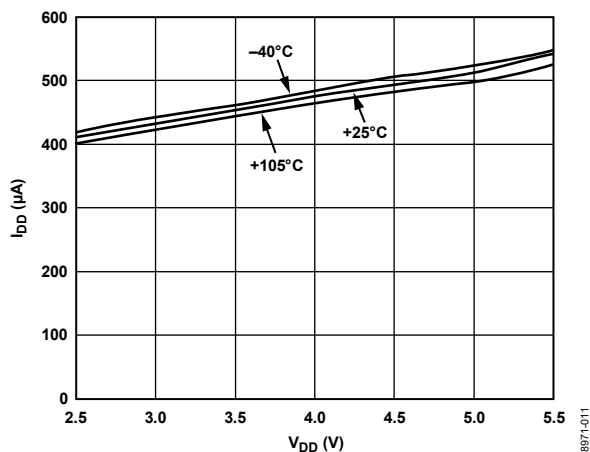


Figure 11. Supply Current vs. Supply Voltage

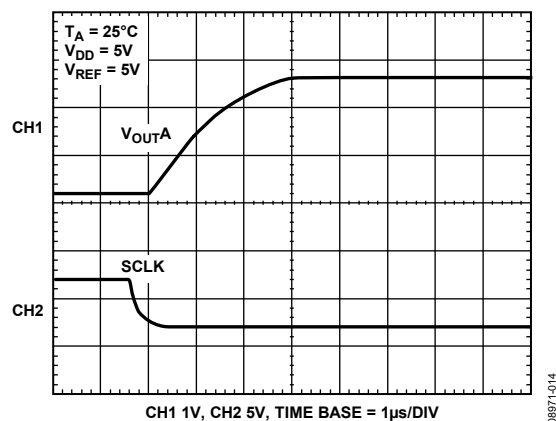


Figure 14. Half-Scale Settling (1/4 to 3/4 Scale Code Change)

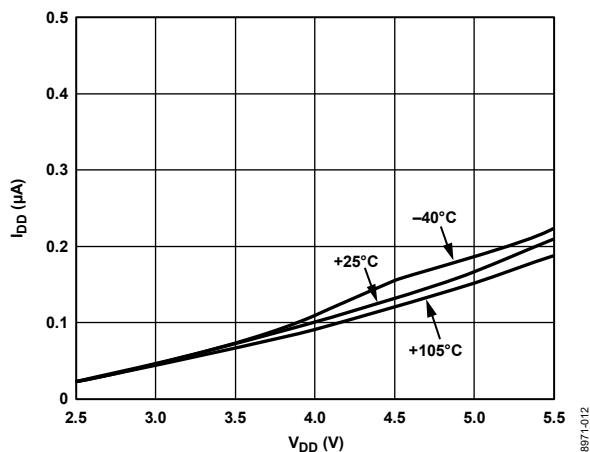


Figure 12. Power-Down Current vs. Supply Voltage

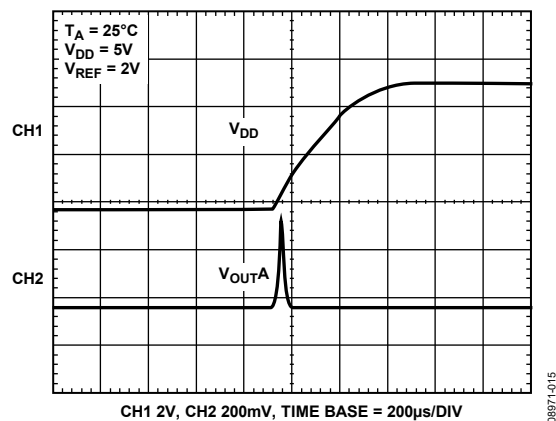


Figure 15. Power-On Reset to 0V

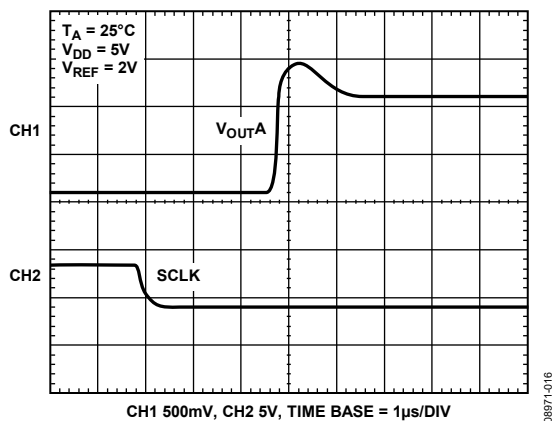


Figure 16. Exiting Power-Down to Midscale

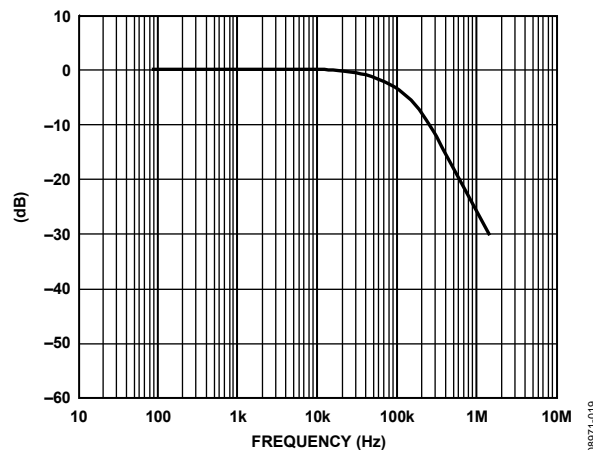


Figure 19. Multiplying Bandwidth (Small-Signal Frequency Response)

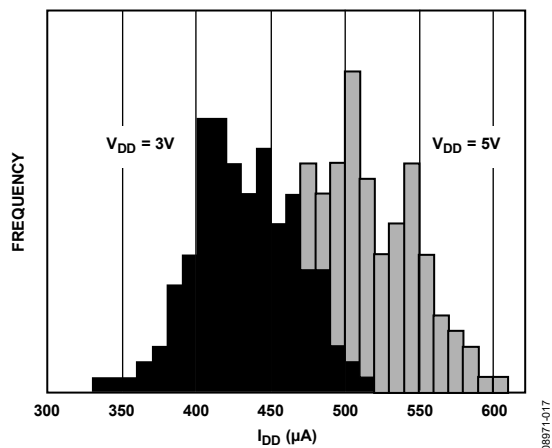
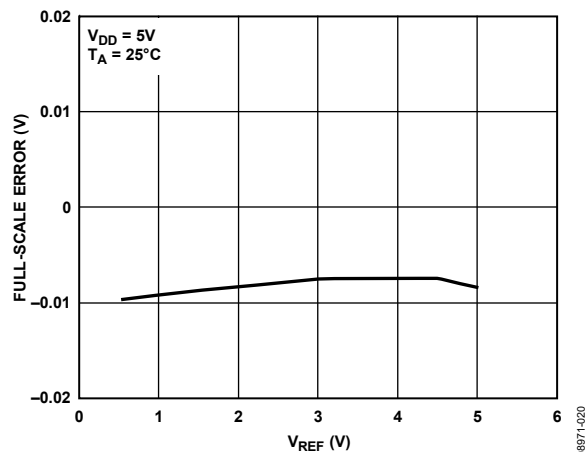
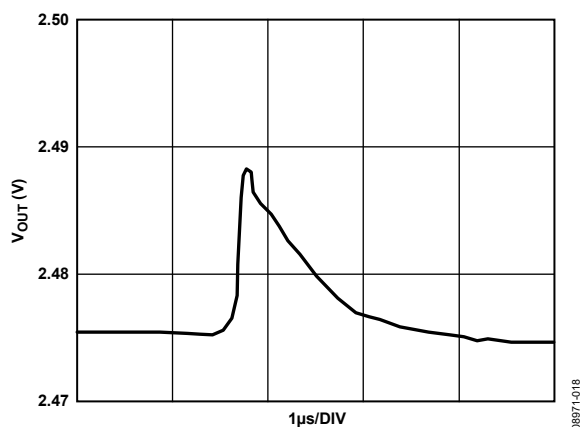
Figure 17. I_{DD} Histogram with $V_{DD} = 3V$ and $V_{DD} = 5V$ Figure 20. Full-Scale Error vs. V_{REF} 

Figure 18. Major-Code Transition Glitch Energy

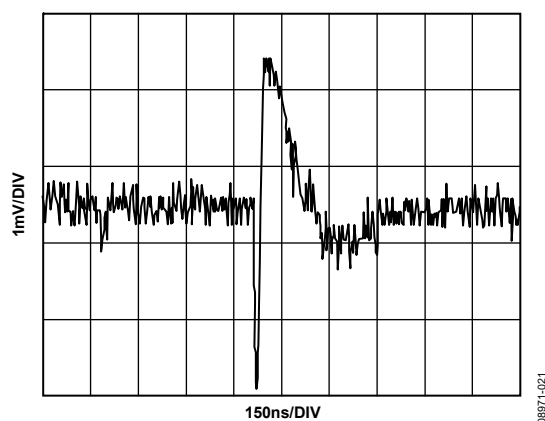
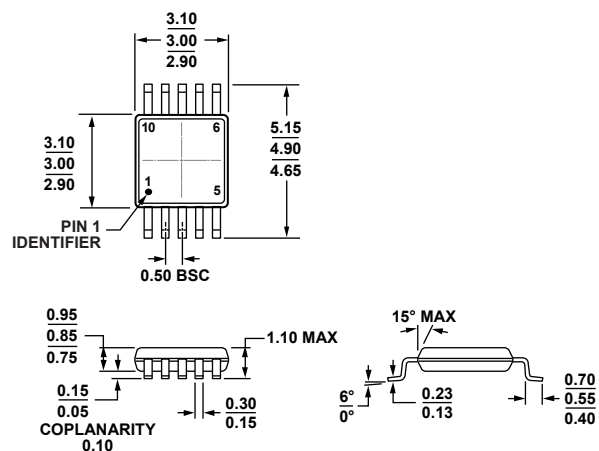


Figure 21. DAC-to-DAC Crosstalk

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA
 Figure 22. 10-Lead Mini Small Outline Package [MSOP]
 (RM-10)
 Dimensions shown in millimeters

091709-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Marking Code
AD5324SRMZ-EP-RL7	-55°C to +125°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	DFT

¹ Z = RoHS Compliant Part.