Data Sheet | May 1999 | FN2813.3

Numerically Controlled Oscillator/Modulator

The Intersil HSP45116/883 combines a high performance quadrature numerically controlled oscillator (NCO) and a high speed 16-bit Complex Multiplier/Accumulator (CMAC) on a single IC. This combination of functions allows a complex vector to be multiplied by the internally generated (cos, sin) vector for quadrature modulation and demodulation. As shown in the Block Diagram, the HSP45116/883 is divided into three main sections. The Phase/Frequency Control Section (PFCS) and the Sine/Cosine Section together form a complex NCO. The CMAC multiplies the output of the Sine/Cosine Section with an external complex vector.

The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The phase resolution of the PFCS is 32 bits, which results in frequency resolution better than 0.006Hz at 25.6MHz. The output of the PFCS is the argument of the sine and cosine. The spurious free dynamic range of the complex sinusoid is greater than 90dBc.

The output vector from the Sine/Cosine Section is one of the inputs to the Complex Multiplier/Accumulator. The CMAC multiplies this (cos, sin) vector by an external complex vector and can accumulate the result. The resulting complex vectors are available through two 20-bit output ports which maintain the 90dB spectral purity. This result can be accumulated internally to implement an accumulate and dump filter.

A quadrature down converter can be implemented by loading a center frequency into the Phase/Frequency Control Section. The signal to be downconverted is the Vector Input of the CMAC, which multiplies the data by the rotating vector from the Sine/Cosine Section. The resulting complex output is the down converted signal.

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- NCO and CMAC on One Chip
- 15MHz and 25.6MHz Versions
- 32-Bit Frequency Control
- 16-Bit Phase Modulation
- 16-Bit CMAC
- 0.006Hz Tuning Resolution at 25.6MHz
- Spurious Frequency Components < -90dBc
- Fully Static CMOS

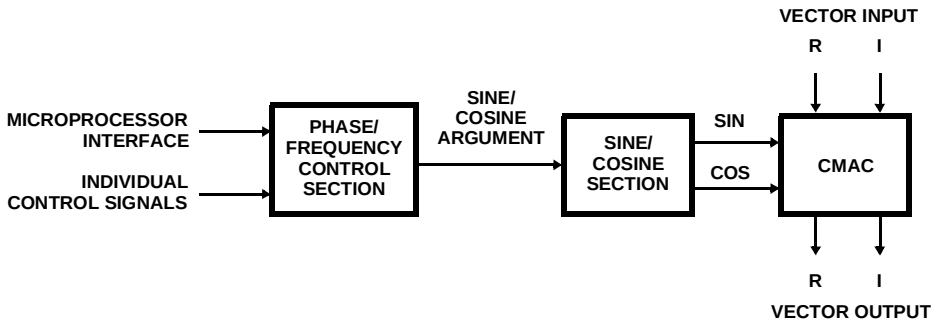
Applications

- Frequency Synthesis
- Modulation - AM, FM, PSK, FSK, QAM
- Demodulation, PLL
- Phase Shifter
- Polar to Cartesian Conversions

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP45116GM-15/883	-55 to 125	145 Ld PGA	G145.A
HS45116GM-25/883	-55 to 125	145 Ld PGA	G145.A

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input or Output Voltage Applied . . . . . GND -0.5V to V_{CC} +0.5V
ESD Rating Classification . . . . . Class 1

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC
Supply Range . . . . . +4.5V to +5.5V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PGA Package	30.0	5.0

Maximum Package Power Dissipation at 125^oC
PGA Package 2.16W
Maximum Junction Temperature . . . . . 175^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
Number of Transistors or Gates . . . . . 103,000 Transistors

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	TEST CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (^oC)	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$55 \le T_A \le 125$	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$55 \le T_A \le 125$	-	0.8	V
Logical One Input Voltage Clock	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	$55 \le T_A \le 125$	3.0	-	V
Logical Zero Input Voltage Clock	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	$55 \le T_A \le 125$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA V_{CC} = 4.5V (Note 2)	1, 2, 3	$55 \le T_A \le 125$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC} = 4.5V (Note 2)	1, 2, 3	$55 \le T_A \le 125$	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$55 \le T_A \le 125$	-10	+10	µA
Output or I/O Leakage Current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$55 \le T_A \le 125$	-10	+10	µA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, (Note 5)	1, 2, 3	$55 \le T_A \le 125$	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 15MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.5V (Notes 3, 5)	1, 2, 3	$55 \le T_A \le 125$	-	150	mA
Functional Test	FT	(Note 4)	7, 8	$55 \le T_A \le 125$	-	-	

NOTES:

2. Interchanging of force and sense conditions is permitted.
3. Operating Supply Current is proportional to frequency, typical rating is 10mA/MHz.
4. Tested as follows: f = 1MHz, V_{IH} (clock inputs) = 3.4V, V_{IH} (all other inputs) = 2.6V, V_{IL} = 0.4V, $V_{OH} \ge 1.5V$, and $V_{OL} \le 1.5V$.
5. Output per test load circuit with switch open and C_L = 40pF.

TABLE 2. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	NOTES	GROUP A SUBGROUPS	TEMPERATURE (^oC)	-15 (15MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
CLK Period	t_{CP}		9, 10, 11	$-55 \le T_A \le 125$	66	-	39	-	ns
CLK High	t_{CH}		9, 10, 11	$-55 \le T_A \le 125$	26	-	15	-	ns
CLK Low	t_{CL}		9, 10, 11	$-55 \le T_A \le 125$	26	-	-15	-	ns
$\overline{WR}$ Low	t_{WL}		9, 10, 11	$-55 \le T_A \le 125$	26	-	15	-	ns
$\overline{WR}$ High	t_{WH}		9, 10, 11	$-55 \le T_A \le 125$	26	-	15	-	ns
Setup Time; ADO-1, $\overline{CS}$ to $\overline{WR}$ Going High	t_{AWS}		9, 10, 11	$-55 \le T_A \le 125$	20	-	18	-	ns
Hold Time; AD0, AD1, $\overline{CS}$ from $\overline{WR}$ Going High	t_{AWH}		9, 10, 11	$-55 \le T_A \le 125$	0	-	0	-	ns
Setup Time CO-15 from $\overline{WR}$ Going High	t_{CWS}		9, 10, 11	$-55 \le T_A \le 125$	20	-	18	-	ns
Hold Time CO-15 from $\overline{WR}$ Going High	t_{CWA}		9, 10, 11	$-55 \le T_A \le 125$	0	-	0	-	ns
Setup Time $\overline{WR}$ to CLK High	t_{WC}	(Note 7)	9, 10, 11	$-55 \le T_A \le 125$	20	-	16	-	ns
Setup Time MODO-1 to CLK Going High	t_{MCS}		9, 10, 11	$-55 \le T_A \le 125$	20	-	18	-	ns
Hold Time MODO-1 from CLK Going High	t_{MCH}		9, 10, 11	$-55 \le T_A \le 125$	0	-	0	-	ns
Setup Time $\overline{PACI}$ to CLK Going High	t_{PCS}		9, 10, 11	$-55 \le T_A \le 125$	25	-	18	-	ns
Hold Time $\overline{PACI}$ from CLK Going High	t_{PCH}		9, 10, 11	$-55 \le T_A \le 125$	0	-	0	-	ns
Setup Time $\overline{ENPHREG}$, $\overline{ENCFRCTL}$, $\overline{ENPHAC}$, $\overline{ENTICTL}$, $\overline{CLROFR}$, $\overline{PMSEL}$, $\overline{LOAD}$, $\overline{ENI}$, ACC, $\overline{BINFMT}$, $\overline{PEAK}$, $\overline{MODPI/2PI}$, SHO-1, $\overline{RBYTILD}$ from CLK Going High	t_{ECS}		9, 10, 11	$-55 \le T_A \le 125$	20	-	15	-	ns
Hold Time $\overline{ENPHREG}$, $\overline{ENCFRCTL}$, $\overline{ENPHAC}$, $\overline{ENTICTL}$, $\overline{CLROFR}$, $\overline{PMSEL}$, $\overline{LOAD}$, $\overline{ENI}$, ACC, $\overline{BINFMT}$, $\overline{PEAK}$, $\overline{MODPI/2PI}$, SHO-1, $\overline{RBYTILD}$ from CLK Going High	t_{ECH}		9, 10, 11	$-55 \le T_A \le 125$	0	-	0	-	ns
Setup Time RINO-18, IMINO-18 to CLK Going High	t_{DS}		9, 10, 11	$-55 \le T_A \le 125$	20	-	15	-	ns
Hold Time RINO-18, IMINO-18, to CLK Going High	t_{DH}		9, 10, 11	$-55 \le T_A \le 125$	0	-	0	-	ns
CLK to Output Delay R0O-19, I0O-19	t_{DO}		9, 10, 11	$-55 \le T_A \le 125$	40	-	25	-	ns

TABLE 2. ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	NOTES	GROUP A SUBGROUPS	TEMPERATURE (^oC)	-15 (15MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
CLK to Output Delay DETO-1	t_{DEO}		9, 10, 11	$-55 \le T_A \le 125$	40	-	27	-	ns
CLK to Output Delay $\overline{PACO}$	t_{PO}		9, 10, 11	$-55 \le T_A \le 125$	-	30	-	20	ns
CLK to Output Delay $\overline{TICO}$	t_{TO}		9, 10, 11	$-55 \le T_A \le 125$	-	30	-	20	ns
Output Enable Time $\overline{OER}$, $\overline{OEI}$, $\overline{OEREXT}$, $\overline{OEIEXT}$	t_{OE}	(Note 8)	9, 10, 11	$-55 \le T_A \le 125$	-	25	-	20	ns
OUTMUXO-1 to Output Delay	t_{MD}		9, 10, 11	$-55 \le T_A \le 125$	-	40	-	28	ns

NOTES:

6. AC testing is performed as follows: V_{CC} = 4.5V and 5.5V. Input levels (CLK Input) 4.0V and 0V; input levels (all other inputs) 3.0V and 0V; timing reference levels (CLK) 2.0V; all others 1.5V. Output load per test load circuit with switch closed and C_L = 40pF. Output transition is measured at $V_{OH} \ge 1.5V$ and $V_{OL} \le 1.5V$.
7. Applicable only when outputs are being monitored and $\overline{ENCFREG}$, $\overline{ENPHREG}$, or $\overline{ENTIREG}$ is active.
8. Transition is measured at ±200mV from steady state voltage, output loading per test load circuit, with switch closed and C_L = 40pF.

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	NOTES	TEMPERATURE (^oC)	-15		-25		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz All measurements are referenced to device GND	9	T_A - +25	-	15	-	15	pF
Output Capacitance	C_{OUT}		9	T_A - +25	-	15	-	15	pF
Output Disable Time	t_{OD}		9, 10	$-55 \le T_A \le 125$	-	20	-	15	ns
Output Rise Time	t_R	From 0.8V to 2.0V	9, 10	$-55 \le T_A \le 125$	-	8	-	8	ns
Output Fall Time	t_F	From 2.0V to 0.8V	9, 10	$-55 \le T_A \le 125$	-	8	-	8	ns

NOTES:

9. The parameters in Table 3 are controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
10. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Tess	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples	1, 7, 9

Burn-In Circuit

145 PIN PGA
TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	V_{CC}	IMIN4	IMIN8	IMIN9	IMIN11	IMIN15	IMIN16	GND	V_{CC}	IO18	IO15	IO12	IO10	GND	V_{CC}	A
B	GND	IMIN 1	IMIN5	IMIN7	IMIN10	IMIN13	IMIN14	IO19	IO16	IO14	IO11	IO8	IO7	IO5	IO2	B
C	RIN15	RIN18	IMIN2	IMIN3	IMIN6	IMIN12	IMIN17	IMIN18	IO17	IO13	IO9	IO6	IO4	IO1	RO18	C
D	RIN13	RIN17	IMIN0	INDEX									IO3	RO19	RO17	D
E	RIN10	RIN14	RIN16										IO0	RO16	RO15	E
F	RIN7	RIN11	RIN12										RO14	RO13	RO11	F
G	V_{CC}	RIN9	RIN8										RO9	RO12	RO10	G
H	GND	RIN6	RIN5										RO8	RO7	GND	H
J	RIN3	RIN1	RIN4										RO5	RO4	V_{CC}	J
K	RIN2	RIN0	SH1										RO1	RO2	RO6	K
L	SH0	ACC	$\overline{\text{RBYTILD}}$										$\overline{\text{PACO}}$	DET1	RO3	L
M	$\overline{\text{ENPH}}$ $\overline{\text{REG}}$	$\overline{\text{PEAK}}$	MOD1										$\overline{\text{OEREXT}}$	$\overline{\text{OEI}}$	RO0	M
N	$\overline{\text{ENOF}}$ $\overline{\text{REG}}$	$\overline{\text{BINFMT}}$	MOD0	$\overline{\text{LOAD}}$	$\overline{\text{ENCF}}$ $\overline{\text{REG}}$	$\overline{\text{MODPI}}$ /2PI	AD0	C14	C13	C8	C2	OUT-MUX1	OUT-MUX0	$\overline{\text{OEIEXT}}$	DET0	N
P	$\overline{\text{TICO}}$	$\overline{\text{PACI}}$	PMSEL	$\overline{\text{CLROFR}}$	$\overline{\text{ENTIREG}}$	$\overline{\text{CS}}$	AD1	C15	C10	C9	C6	C3	C1	$\overline{\text{OER}}$	GND	P
Q	V_{CC}	GND	$\overline{\text{ENPHAC}}$	$\overline{\text{ENI}}$	CLK	$\overline{\text{WR}}$	V_{CC}	GND	C12	C11	C7	C5	C4	C0	V_{CC}	Q
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

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Burn-in Circuit

PGA PIN	PIN NAME	BURN-IN-SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
D3	IMIN(0)	F4	Q3	ENPHAC	F1	K14	RO(2)	$V_{CC}/2$	A10	IO(18)	$V_{CC}/2$
C2	RIN(18)	F9	P5	$\overline{\text{ENTIREG}}$	F4	L15	RO(3)	$V_{CC}/2$	B8	IO(19)	$V_{CC}/2$
D2	RIN(17)	F8	Q4	$\overline{\text{ENI}}$	F1	J14	RO(4)	$V_{CC}/2$	C8	IMIN(18)	F9
E3	RIN(16)	F7	N6	$\overline{\text{MODPI/2PI}}$	F16	J13	RO(5)	$V_{CC}/2$	C7	IMIN(17)	F8
C1	RIN(15)	F6	P6	$\overline{\text{CS}}$	F2	K15	RO(6)	$V_{CC}/2$	A7	IMIN(16)	F7
E2	RIN(14)	F5	Q5	CLK	F0	H14	RO(7)	$V_{CC}/2$	A6	IMIN(15)	F6
D1	RIN(13)	F4	P7	AD(1)	F4	H13	RO(8)	$V_{CC}/2$	B7	IMIN(14)	F5
F3	RIN(12)	F16	N7	AD(0)	F3	G13	RO(9)	$V_{CC}/2$	B6	IMIN(13)	F4
F2	RIN(11)	F15	Q6	$\overline{\text{WR}}$	F1	G15	RO(10)	$V_{CC}/2$	C6	IMIN(12	F16
E1	RIN(10)	F14	P8	C(15)	GND	F15	RO(11)	$V_{CC}/2$	A5	IMIN(11)	F15
G2	RIN(9)	F13	N8	C(14)	GND	G14	RO(12)	$V_{CC}/2$	B5	IMIN(10)	F14
G3	RIN(8)	F12	N9	C(13)	GND	F14	RO(13)	$V_{CC}/2$	A4	IMIN(9)	F13
F1	RIN(7)	F11	Q9	C(12)	GND	F13	RO(14)	$V_{CC}/2$	A3	IMIN(8)	F12
H2	RIN(6)	F10	Q10	C(11)	GND	E15	RO(15)	$V_{CC}/2$	B4	IMIN(7)	F11
H3	RIN(5)	F9	P9	C(10)	GND	E14	RO(16)	$V_{CC}/2$	C5	IMIN(6)	F10
J3	RIN(4)	F8	P10	C(9)	GND	D15	RO(17)	$V_{CC}/2$	B3	IMIN(5)	F9
J1	RIN(3)	F7	N10	C(8)	GND	C15	RO(18)	$V_{CC}/2$	A2	IMIN(4)	F8
K1	RIN(2)	F6	Q11	C(7)	GND	D14	RO(19)	$V_{CC}/2$	C4	IMIN(3)	F7
J2	RIN(1)	F5	P11	C(6)	GND	E13	IO(0)	$V_{CC}/2$	C3	IMIN(2)	F6
K2	RIN(0)	F4	Q12	C(5)	GND	C14	IO(1)	$V_{CC}/2$	B2	IMIN(1)	F5
K3	SH(1)	F3	Q13	C(4)	GND	B15	IO(2)	$V_{CC}/2$	A1	VC	None
L1	SH(0)	F2	P12	C(3)	GND	D13	IO(3)	$V_{CC}/2$	A9	V_{CC}	V_{CC}
L2	ACC	F4	N11	C(2)	GND	C13	IO(4)	$V_{CC}/2$	A15	V_{CC}	None
M1	$\overline{\text{ENPHREG}}$	F16	P13	C(1)	GND	B14	IO(5)	$V_{CC}/2$	G1	V_{CC}	V_{CC}
N1	$\overline{\text{ENOFREG}}$	F4	Q14	C(0)	V_{CC}	C12	IO(6)	$V_{CC}/2$	J15	V_{CC}	V_{CC}
M2	$\overline{\text{PEAK}}$	F8	N12	OUT-MUX(1)	F11	B13	IO(7)	$V_{CC}/2$	Q1	V_{CC}	None
L3	$\overline{\text{RBYTILD}}$	F16	N13	OUT-MUX(0)	F10	B12	IO(8)	$V_{CC}/2$	Q7	V_{CC}	V_{CC}
N2	$\overline{\text{BINFMT}}$	F4	P14	$\overline{\text{OER}}$	F0	C11	IO(9)	$V_{CC}/2$	Q15	V_{CC}	None
P1	$\overline{\text{TICO}}$	$V_{CC}/2$	M13	$\overline{\text{OEREXT}}$	F0	A13	IO(10)	$V_{CC}/2$	A8	GND	GND
M3	MOD(1)	GND	N14	$\overline{\text{OEIEXT}}$	F0	B11	IO(11)	$V_{CC}/2$	A14	GND	None
N3	MOD(0)	GND	M14	$\overline{\text{OEI}}$	F0	A12	IO(12)	$V_{CC}/2$	B1	GND	None
P2	$\overline{\text{PACI}}$	F4	L13	$\overline{\text{PACO}}$	$V_{CC}/2$	C10	IO(13)	$V_{CC}/2$	H1	GND	GND
N4	$\overline{\text{LOAD}}$	F15	N15	DET0	$V_{CC}/2$	B10	IO(14)	$V_{CC}/2$	H15	GND	GND
P3	PMSEL	F1	L14	DET1	$V_{CC}/2$	A11	IO(15)	$V_{CC}/2$	P15	GND	None
P4	$\overline{\text{CLROFR}}$	F4	M15	RO(0)	$V_{CC}/2$	B9	IO(16)	$V_{CC}/2$	Q2	GND	None
N5	$\overline{\text{ENCFREG}}$	F4	K13	RO(1)	$V_{CC}/2$	C9	IO(17)	$V_{CC}/2$	Q8	GND	GND

NOTE:

11. 47kΩ ±20%) resistor connected to all pins except V_{CC} and GND.
12. V_{CC} = 5.5V ±0.5V with 0.1µF (min) capacitor between V_{CC} and GND per position.
13. F0 = 100kHz ±10%, F1 = F0/2, F2 = F1/2 . . . . . , F11 = F10/2, 40% to 60% duty cycle.
14. Input Voltage limits: V_{IL} = 0.8V max, V_{IH} = 4.5V ±10%.

Die Characteristics

DIE DIMENSIONS:

350 mils x 353 mils x 19 ± 1mils

METALLIZATION:

Type: Si-Al, or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:

Type: Nitrox
Thickness: 10kÅ

WORST CASE DENSITY:

$1.6 \times 10^5 A/cm^2$