TMS27C210A 65536 BY 16-BIT UV ERASABLE
TMS27PC210A 65536 BY 16-BIT
PROGRAMMABLE READ-ONLY MEMORIES

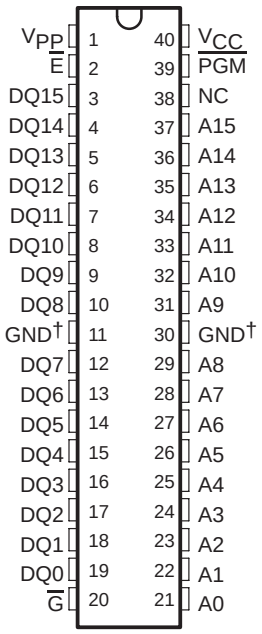
SMLS310D– NOVEMBER 1990 – REVISED SEPTEMBER 1997

- **Organization . . . 65536 by 16 Bits**
- **Single 5-V Power Supply**
- **Operationally Compatible With Existing Megabit EPROMs**
- **40-Pin Dual-In-Line Package and 44-Lead Plastic Leaded Chip Carrier**
- **All Inputs/Outputs Fully TTL Compatible**
- **±10% V_{CC} Tolerance**
- **Maximum Access/Minimum Cycle Time**

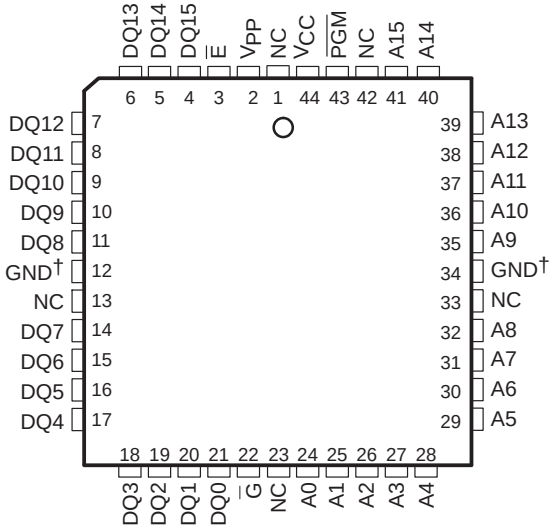
'27C/PC210A-10	**100**	**ns**
'27C/PC210A-12	**120**	**ns**
'27C/PC210A-15	**150**	**ns**
'27C/PC210A-20	**200**	**ns**
'27C/PC210A-25	**250**	**ns**

- **16-Bit Output For Use in Microprocessor-Based Systems**
- **Very High-Speed SNAP! Pulse Programming**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation**
  - **Active . . . 275 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**
- **Temperature Range Options**

J PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A15	Address Inputs
DQ0–DQ15	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
$\overline{PGM}$	Program
V_{CC}	5-V Power Supply
V_{PP}	13-V Power Supply‡

† Pins 11 and 30 (J package) and pins 12 and 34 (FN package) must be connected externally to ground.

‡ Only in program mode

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TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

description

The TMS27C210A series are 65536 by 16-bit (1048576-bit), ultraviolet-light erasable, electrically programmable read-only memories (EPROMs).

The TMS27PC210A series are 65536 by 16-bit (1048576-bit), one-time programmable (OTP) electrically programmable read-only memories (PROMs).

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27C210A EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C210A is offered with two choices of temperature ranges, 0°C to 70°C (JL suffix) and − 40°C to 85°C (JE suffix). See Table 1.

The TMS27PC210A OTP PROM is offered in a 44-pin plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FN suffix). The TMS27PC210A is offered with two choices of temperature ranges, 0°C to 70°C (FNL suffix) and −40°C to 85°C (FNE suffix). See Table 1.

Table 1. Temperature Range Suffixes

EPROM AND OTP PROM	SUFFIX FOR OPERATING FREE-AIR TEMPERATURE RANGES	
	0°C to 70°C	− 40°C to 85°C
TMS27C210A-xx	JL	JE
TMS27PC210A-xx	FNL	FNE

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor based systems. One other (13 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

The seven modes of operation for the TMS27C210A and TMS27PC210A are listed in Table 2. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V), and 12 V on A9 for signature mode.

Table 2. Operation Modes

FUNCTION	MODE†							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0−DQ15	Data Out	Hi-Z	Hi-Z	Data In	Data Out	Hi-Z	CODE	
							MFG	DEVICE
							97	AB

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C210As or TMS27PC210As are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit must have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C210A and TMS27PC210A is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, "*Design Considerations; Latchup Immunity of the HVCMOS EPROM Family*", available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 50 mA to 500 μA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C210A)

Before programming, the TMS27C210A is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W•s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. Normal ambient light contains the correct wavelength for erasure; therefore, when using the TMS27C210A the window should be covered with an opaque label.

initializing (TMS27PC210A)

The OTP TMS27PC210A PROM is provided with all bits in the logic high state then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C210A and TMS27PC210A are programmed using the TI SNAP! Pulse programming algorithm (shown in the flow chart in Figure 1), which can program in a nominal time of seven seconds. Actual programming time varies as a function of the programmer used.

The SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$. Data is presented in parallel (16 bits) on pins DQ0 through DQ15. Once addresses and data are stable, $\overline{PGM}$ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 5\ V \pm 10\%$.

program inhibit

Programming can be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pins.

program verify

Programmed bits can be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V. Two identifier bytes are accessed by toggling A0. DQ0−DQ7 contain the valid codes. All other addresses must be held low. The signature code for these devices is 97AB. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code AB (Hex), as shown in Table 3.

Table 3. Signature Mode

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Manufacturer Code	V_{IL}	1	0	0	1	0	1	1	1	97
Device Code	V_{IH}	1	0	1	0	1	0	1	1	AB

† $\overline{E} = \overline{G} = V_{IL}$, A9 = V_H, A1−A8 = V_{IL}, A10−A15 = V_{IL}, $V_{PP} = V_{CC}$, $\overline{PGM} = V_{IH}$ or V_{IL}.

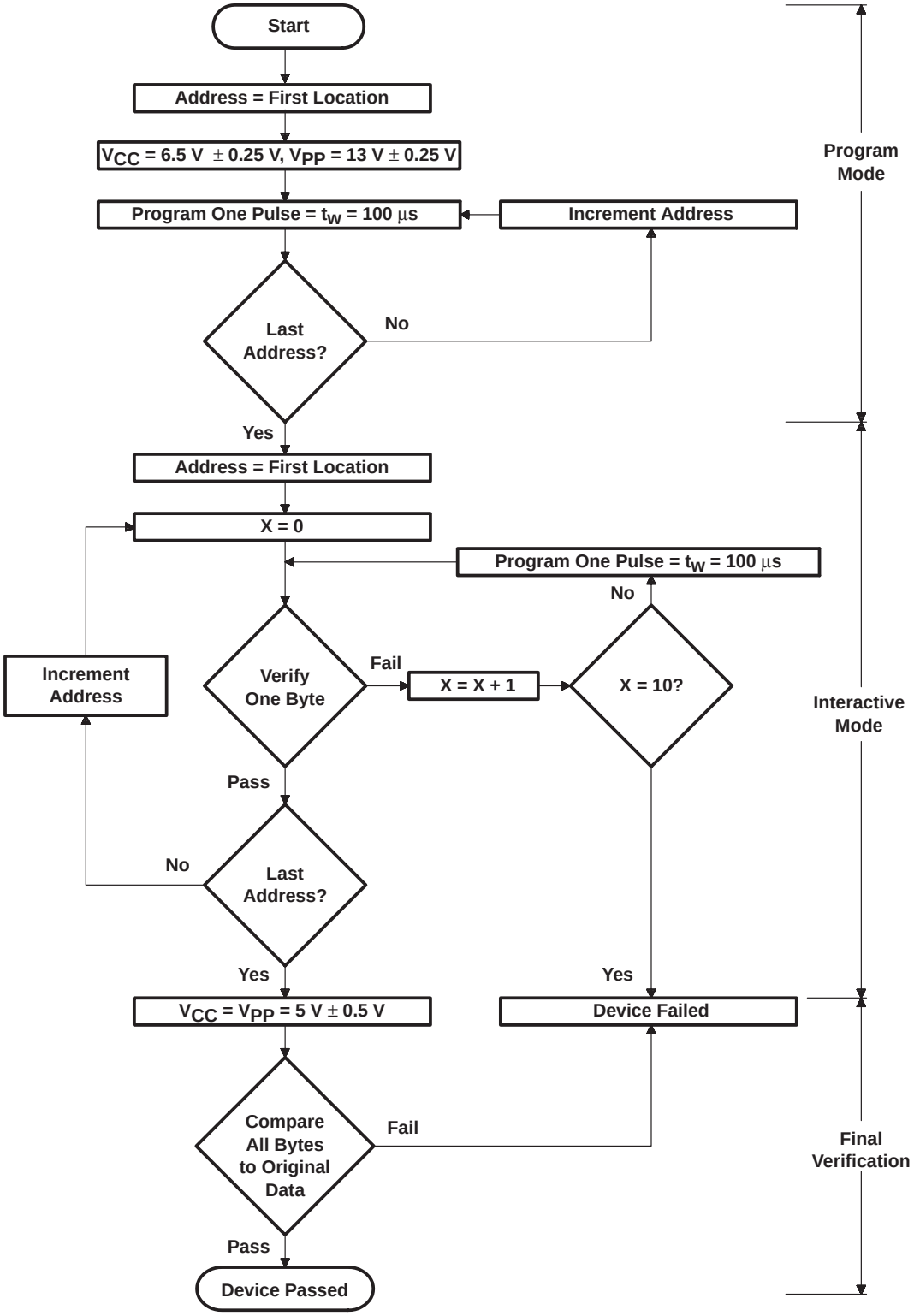
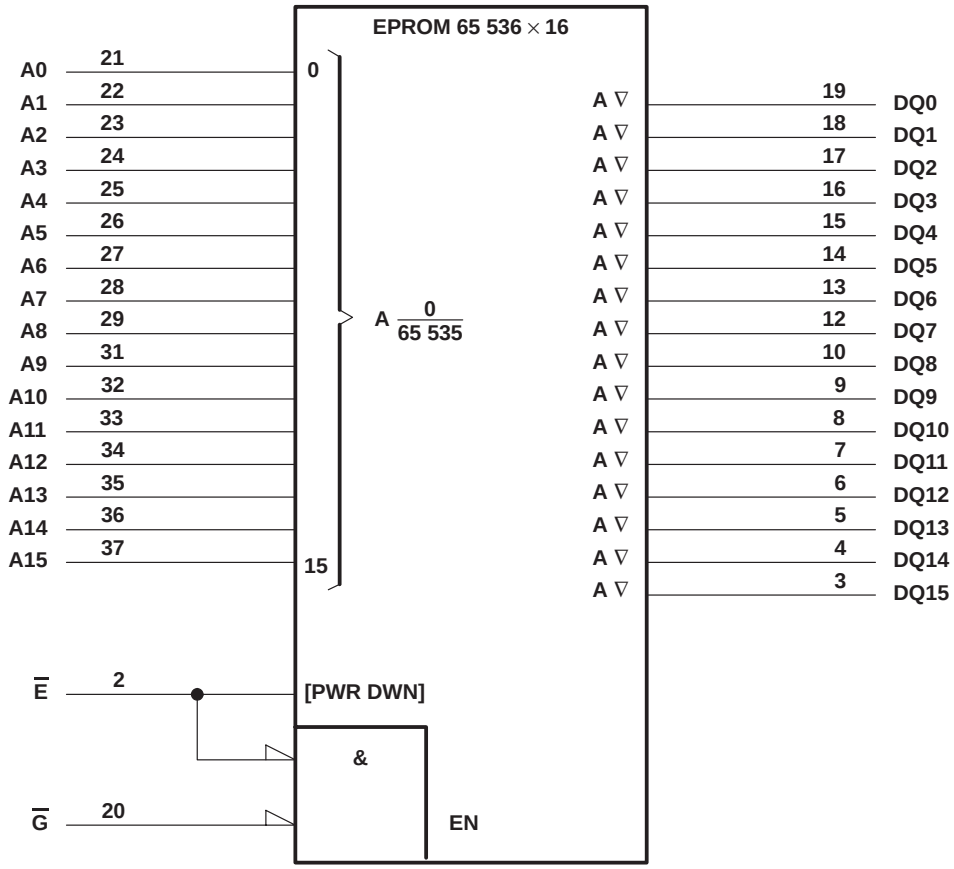


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91−1984 and IEC Publication 617−12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 . . . . . −0.6 V to V_{CC} + 1 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C210A-_ _JL, '27PC210A-_ _FNL) . . . . . 0° C to 70°C
Operating free-air temperature range ('27C210A-_ _JE, '27PC210A-_ _FNE) . . . . . − 40° C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			TMS27C/PC210A-10 TMS27C/PC210A-12 TMS27C/PC210A-15 TMS27C/PC210A-20 TMS27C/PC210A-25			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode	V_{CC}−0.6	V_{CC}	V_{CC}+0.6	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	
V_{IH}	High-level dc input voltage	TTL	2		V_{CC}+0.5	V
		CMOS	V_{CC} − 0.2		V_{CC}+0.5	
V_{IL}	Low-level dc input voltage	TTL	− 0.5		0.8	V
		CMOS	− 0.5		GND+0.2	
T_A	Operating free-air temperature	'27C210A-_ _JL '27PC210A-_ _FNL	0		70	°C
T_A	Operating free-air temperature	'27C210A-_ _JE, '27PC210A-_ _FNE	− 40		85	°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over recommended ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level dc output voltage		I_{OH} = – 20 μA	V_{CC} – 0.2		V
			I_{OH} = – 2 mA	2.4		
V_{OL}	Low-level dc output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 μA		0.1	
I_I	Input current (leakage)		V_I = 0 V to 5.5 V		±1	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}		±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open†		50	mA

† Minimum cycle time = maximum address access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
C_I	Input capacitance	V_I = 0 V, f = 1 MHz		8	12	pF
C_O	Output capacitance	V_O = 0 V, f = 1 MHz		12	15	pF

‡ Capacitance measurements are made on a sample basis only.
§ Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS	'27C210A-10 '27PC210A-10		'27C210A-12 '27PC210A-12		'27C210A-15 '27PC210A-15		'27C210A-20 '27PC210A-20		'27C210A-25 '27PC210A-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	CL = 100 pF, 1 Series 74 TTL load, Input t_r ≤ 20 ns, Input t_f ≤ 20 ns		100		120		150		200		250	ns
$t_{a(E)}$	Access time from chip enable			100		120		150		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		55		75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first¶		0	50	0	50	0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first¶		0		0		0		0		0		ns

¶ Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

NOTES: 3. For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (see Figure 2).
4. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0	100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		150	ns

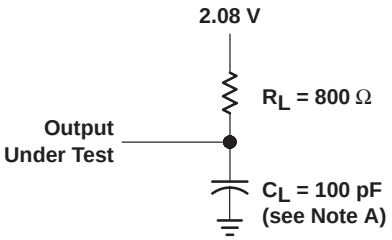
NOTE 3: For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (See Figure 2).

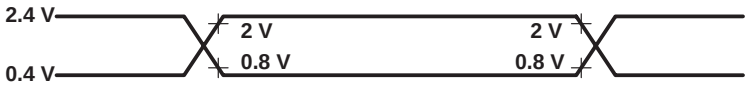
timing requirements for programming

			MIN	NOM	MAX	UNIT
$t_{w(PGM)}$	Pulse duration, program	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Setup time, address		2			µs
$t_{su(E)}$	Setup time, $\overline{E}$		2			µs
$t_{su(G)}$	Setup time, $\overline{G}$		2			µs
$t_{su(D)}$	Setup time, data		2			µs
$t_{su(VPP)}$	Setup time, V_{PP}		2			µs
$t_{su(VCC)}$	Setup time, V_{CC}		2			µs
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs

NOTE 3: For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (See Figure 2).

PARAMETER MEASUREMENT INFORMATION





NOTES: A. C_L includes probe and fixture capacitance.
B. The ac testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

Figure 2. The ac Testing Output Load Circuit and ac Waveform

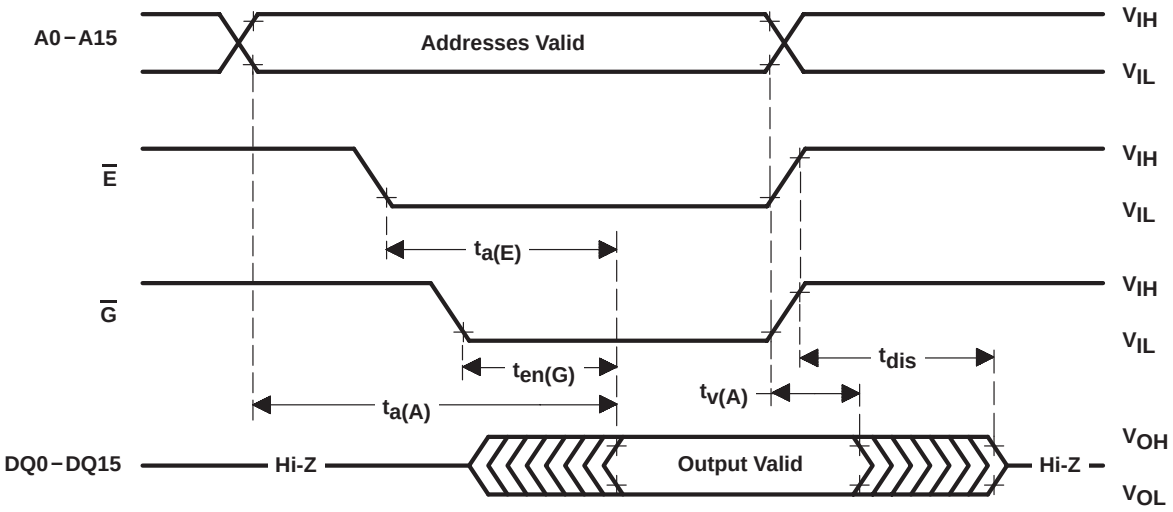
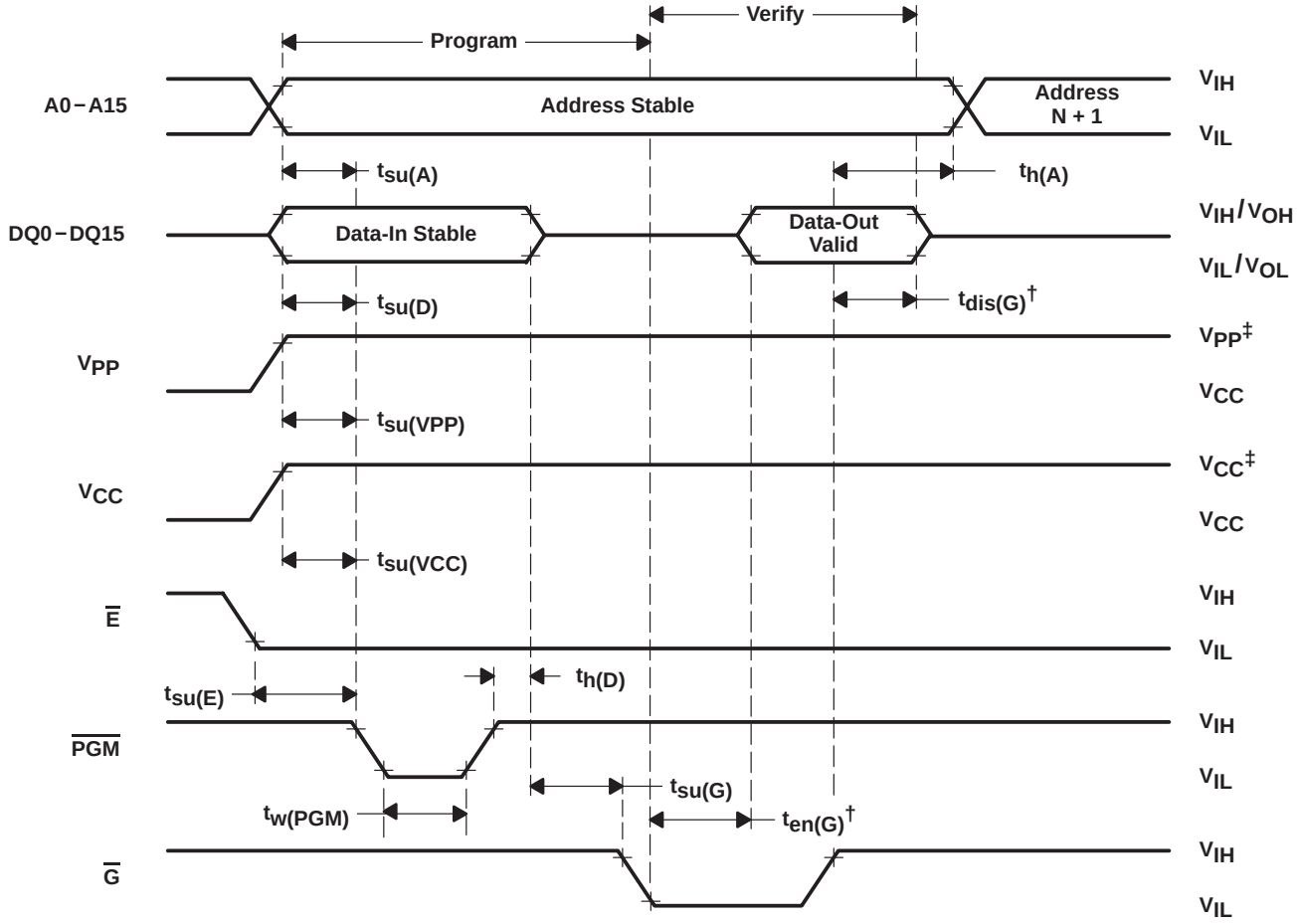


Figure 3. Read-Cycle Timing

PROGRAMMING INFORMATION

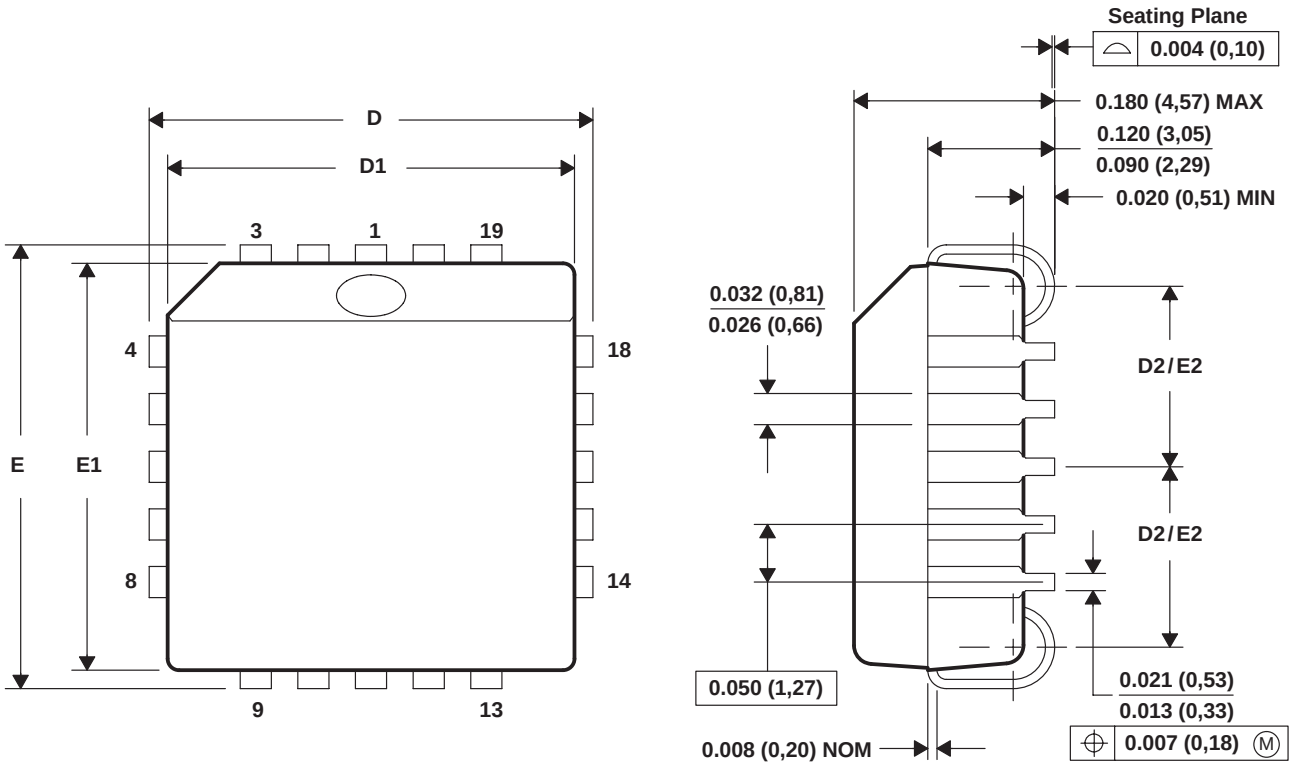


† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program-Cycle Timing (SNAP! Pulse Programming)

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



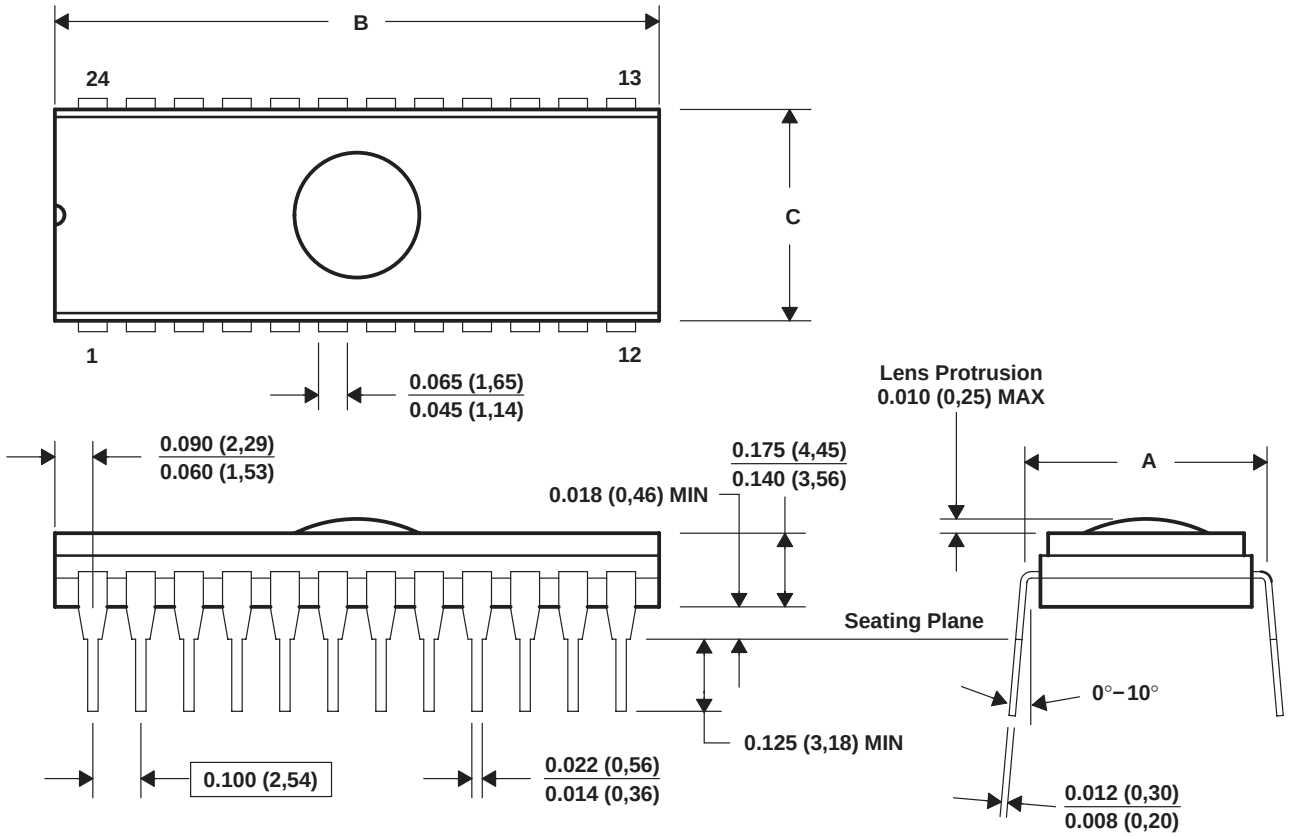
NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

J (R-CDIP-T**) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

24 PIN SHOWN



DIM	PINS**	24 NARR	24 WIDE	28 NARR	28 WIDE	32 NARR	32 WIDE	40 NARR	40 WIDE
A	MAX	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)
	MIN	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)
B	MAX	1.265(32,13)	1.265(32,13)	1.465(37,21)	1.465(37,21)	1.668(42,37)	1.668(42,37)	2.068(52,53)	2.068(52,53)
	MIN	1.235(31,37)	1.235(31,37)	1.435(36,45)	1.435(36,45)	1.632(41,45)	1.632(41,45)	2.032(51,61)	2.032(51,61)
C	MAX	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)
	MIN	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)

4040084/B 04/95

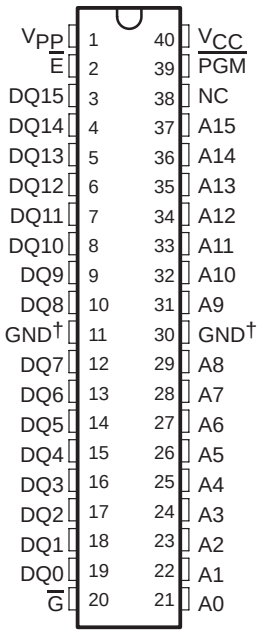
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.

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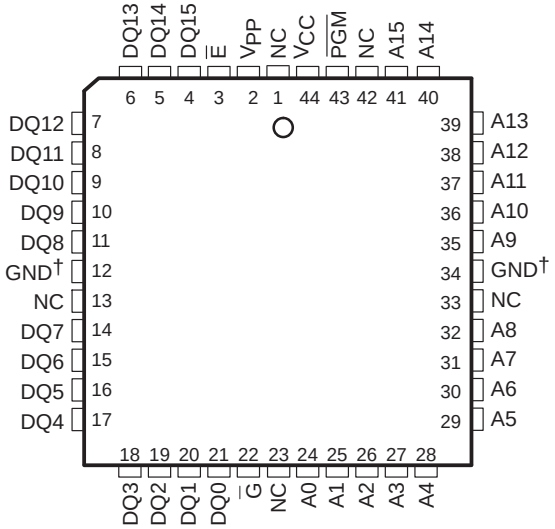
'27C/PC210A-10	**100**	**ns**
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- **Very High-Speed SNAP! Pulse Programming**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation**
  - **Active . . . 275 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**
- **Temperature Range Options**

J PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A15	Address Inputs
DQ0–DQ15	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
$\overline{PGM}$	Program
V_{CC}	5-V Power Supply
V_{PP}	13-V Power Supply‡

† Pins 11 and 30 (J package) and pins 12 and 34 (FN package) must be connected externally to ground.

‡ Only in program mode

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description

The TMS27C210A series are 65536 by 16-bit (1048576-bit), ultraviolet-light erasable, electrically programmable read-only memories (EPROMs).

The TMS27PC210A series are 65536 by 16-bit (1048576-bit), one-time programmable (OTP) electrically programmable read-only memories (PROMs).

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27C210A EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C210A is offered with two choices of temperature ranges, 0°C to 70°C (JL suffix) and − 40°C to 85°C (JE suffix). See Table 1.

The TMS27PC210A OTP PROM is offered in a 44-pin plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FN suffix). The TMS27PC210A is offered with two choices of temperature ranges, 0°C to 70°C (FNL suffix) and −40°C to 85°C (FNE suffix). See Table 1.

Table 1. Temperature Range Suffixes

EPROM AND OTP PROM	SUFFIX FOR OPERATING FREE-AIR TEMPERATURE RANGES	
	0°C to 70°C	− 40°C to 85°C
TMS27C210A-xx	JL	JE
TMS27PC210A-xx	FNL	FNE

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor based systems. One other (13 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

The seven modes of operation for the TMS27C210A and TMS27PC210A are listed in Table 2. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V), and 12 V on A9 for signature mode.

Table 2. Operation Modes

FUNCTION	MODE†							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0−DQ15	Data Out	Hi-Z	Hi-Z	Data In	Data Out	Hi-Z	CODE	
							MFG	DEVICE
							97	AB

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C210As or TMS27PC210As are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit must have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C210A and TMS27PC210A is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, "*Design Considerations; Latchup Immunity of the HVCMOS EPROM Family*", available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 50 mA to 500 μA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C210A)

Before programming, the TMS27C210A is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W•s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. Normal ambient light contains the correct wavelength for erasure; therefore, when using the TMS27C210A the window should be covered with an opaque label.

initializing (TMS27PC210A)

The OTP TMS27PC210A PROM is provided with all bits in the logic high state then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C210A and TMS27PC210A are programmed using the TI SNAP! Pulse programming algorithm (shown in the flow chart in Figure 1), which can program in a nominal time of seven seconds. Actual programming time varies as a function of the programmer used.

The SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$. Data is presented in parallel (16 bits) on pins DQ0 through DQ15. Once addresses and data are stable, $\overline{PGM}$ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 5\ V \pm 10\%$.

program inhibit

Programming can be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pins.

program verify

Programmed bits can be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V. Two identifier bytes are accessed by toggling A0. DQ0−DQ7 contain the valid codes. All other addresses must be held low. The signature code for these devices is 97AB. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code AB (Hex), as shown in Table 3.

Table 3. Signature Mode

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Manufacturer Code	V_{IL}	1	0	0	1	0	1	1	1	97
Device Code	V_{IH}	1	0	1	0	1	0	1	1	AB

† $\overline{E} = \overline{G} = V_{IL}$, A9 = V_H, A1−A8 = V_{IL}, A10−A15 = V_{IL}, $V_{PP} = V_{CC}$, $\overline{PGM} = V_{IH}$ or V_{IL}.

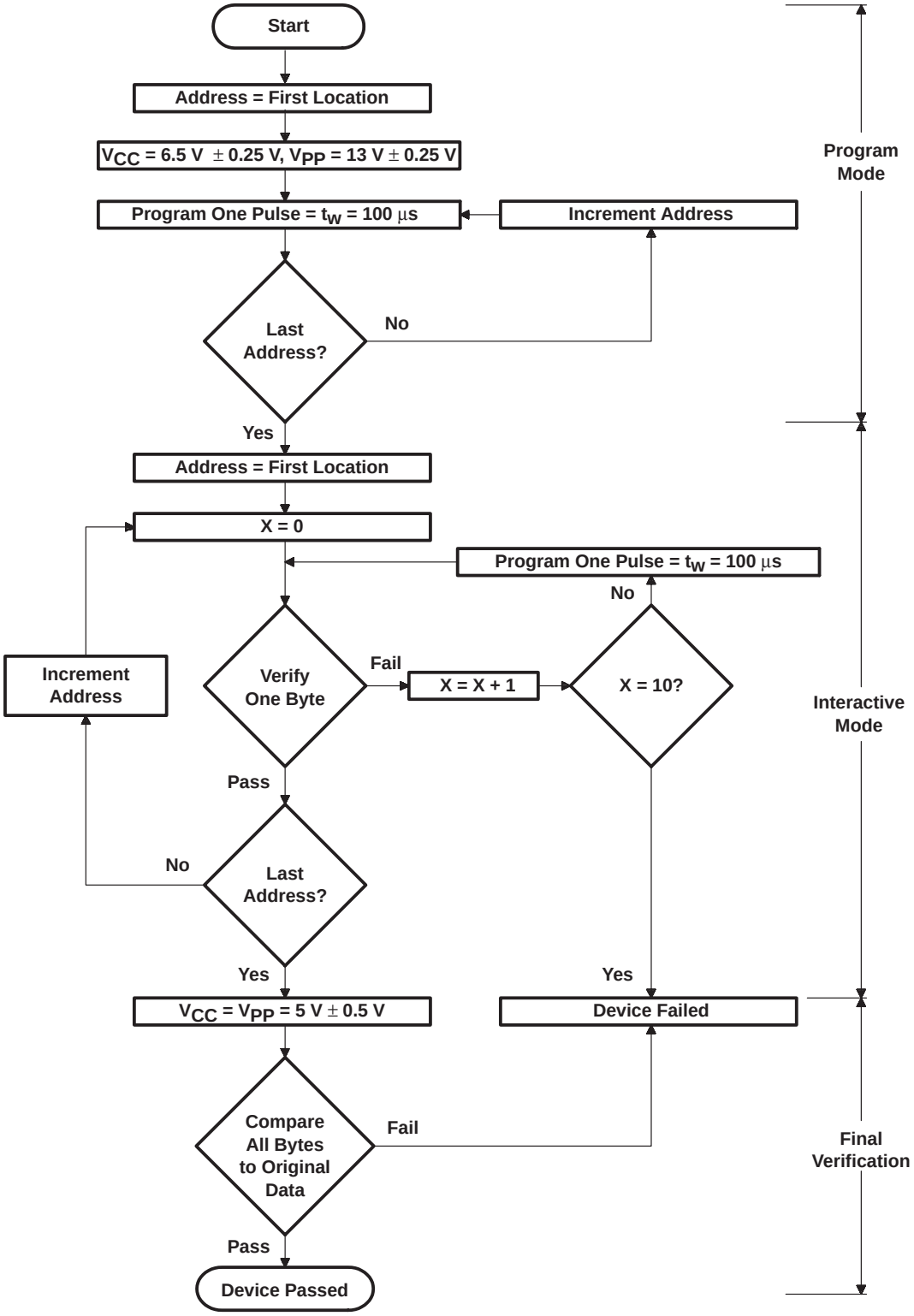
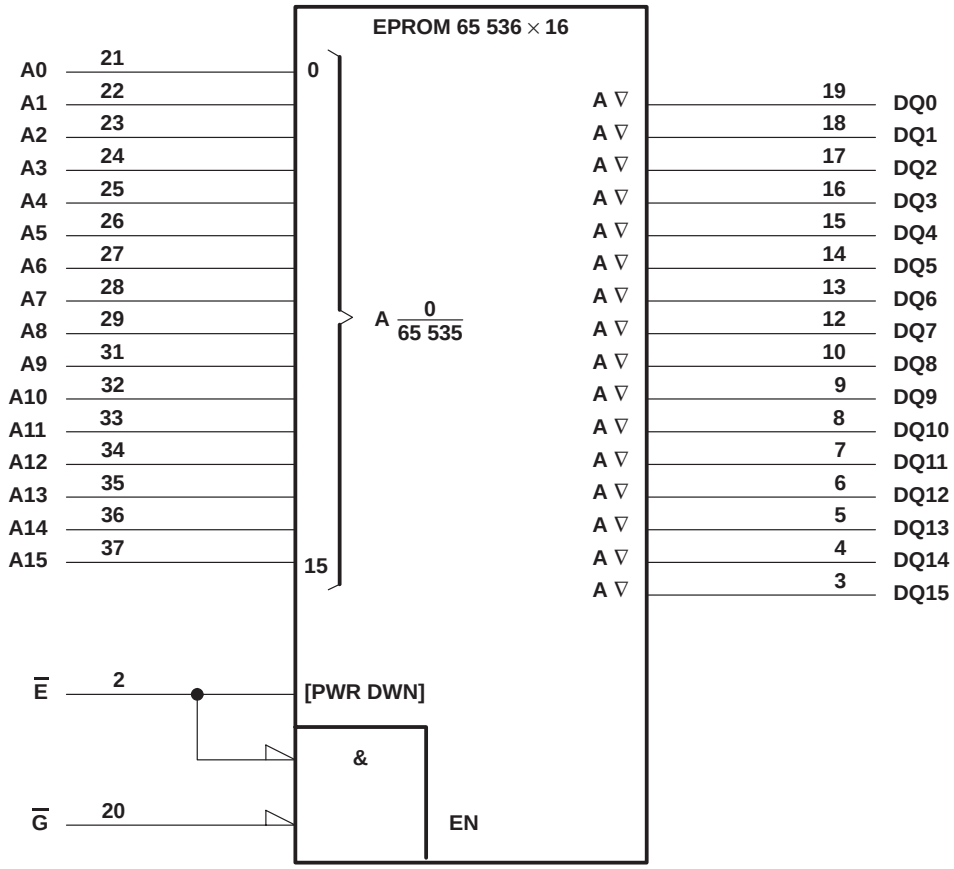


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91−1984 and IEC Publication 617−12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 . . . . . −0.6 V to V_{CC} + 1 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C210A-_ _JL, '27PC210A-_ _FNL) . . . . . 0° C to 70°C
Operating free-air temperature range ('27C210A-_ _JE, '27PC210A-_ _FNE) . . . . . − 40° C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			TMS27C/PC210A-10 TMS27C/PC210A-12 TMS27C/PC210A-15 TMS27C/PC210A-20 TMS27C/PC210A-25			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode	V_{CC}−0.6	V_{CC}	V_{CC}+0.6	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	
V_{IH}	High-level dc input voltage	TTL	2		V_{CC}+0.5	V
		CMOS	V_{CC} − 0.2		V_{CC}+0.5	
V_{IL}	Low-level dc input voltage	TTL	− 0.5		0.8	V
		CMOS	− 0.5		GND+0.2	
T_A	Operating free-air temperature	'27C210A-_ _JL '27PC210A-_ _FNL	0		70	°C
T_A	Operating free-air temperature	'27C210A-_ _JE, '27PC210A-_ _FNE	− 40		85	°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over recommended ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level dc output voltage		I_{OH} = – 20 μA	V_{CC} – 0.2		V
			I_{OH} = – 2 mA	2.4		
V_{OL}	Low-level dc output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 μA		0.1	
I_I	Input current (leakage)		V_I = 0 V to 5.5 V		±1	μA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}		±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open†		50	mA

† Minimum cycle time = maximum address access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
C_I	Input capacitance	V_I = 0 V, f = 1 MHz		8	12	pF
C_O	Output capacitance	V_O = 0 V, f = 1 MHz		12	15	pF

‡ Capacitance measurements are made on a sample basis only.
§ Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS	'27C210A-10 '27PC210A-10		'27C210A-12 '27PC210A-12		'27C210A-15 '27PC210A-15		'27C210A-20 '27PC210A-20		'27C210A-25 '27PC210A-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	CL = 100 pF, 1 Series 74 TTL load, Input t_r ≤ 20 ns, Input t_f ≤ 20 ns		100		120		150		200		250	ns
$t_{a(E)}$	Access time from chip enable			100		120		150		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		55		75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first¶		0	50	0	50	0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first¶		0		0		0		0		0		ns

¶ Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

NOTES: 3. For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (see Figure 2).
4. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0	100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		150	ns

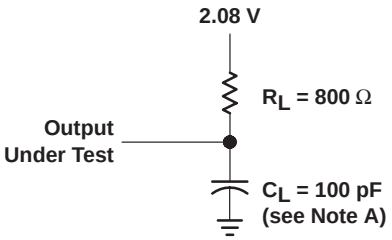
NOTE 3: For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (See Figure 2).

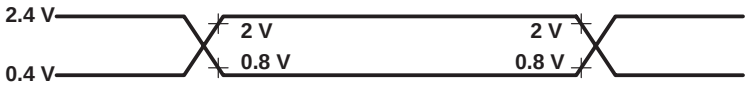
timing requirements for programming

			MIN	NOM	MAX	UNIT
$t_{w(PGM)}$	Pulse duration, program	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Setup time, address		2			µs
$t_{su(E)}$	Setup time, $\overline{E}$		2			µs
$t_{su(G)}$	Setup time, $\overline{G}$		2			µs
$t_{su(D)}$	Setup time, data		2			µs
$t_{su(VPP)}$	Setup time, V_{PP}		2			µs
$t_{su(VCC)}$	Setup time, V_{CC}		2			µs
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs

NOTE 3: For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (See Figure 2).

PARAMETER MEASUREMENT INFORMATION





NOTES: A. C_L includes probe and fixture capacitance.
B. The ac testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

Figure 2. The ac Testing Output Load Circuit and ac Waveform

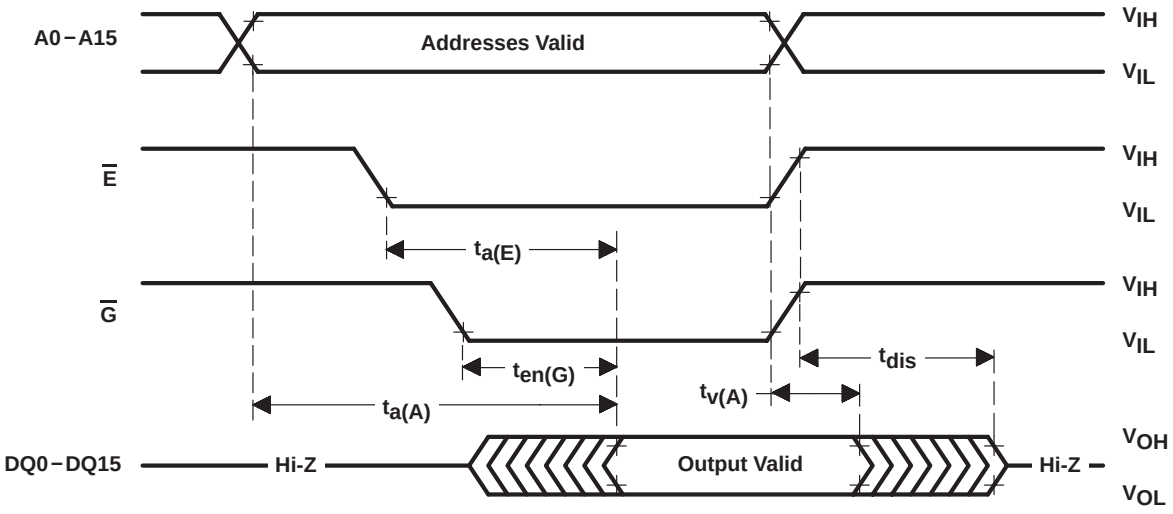
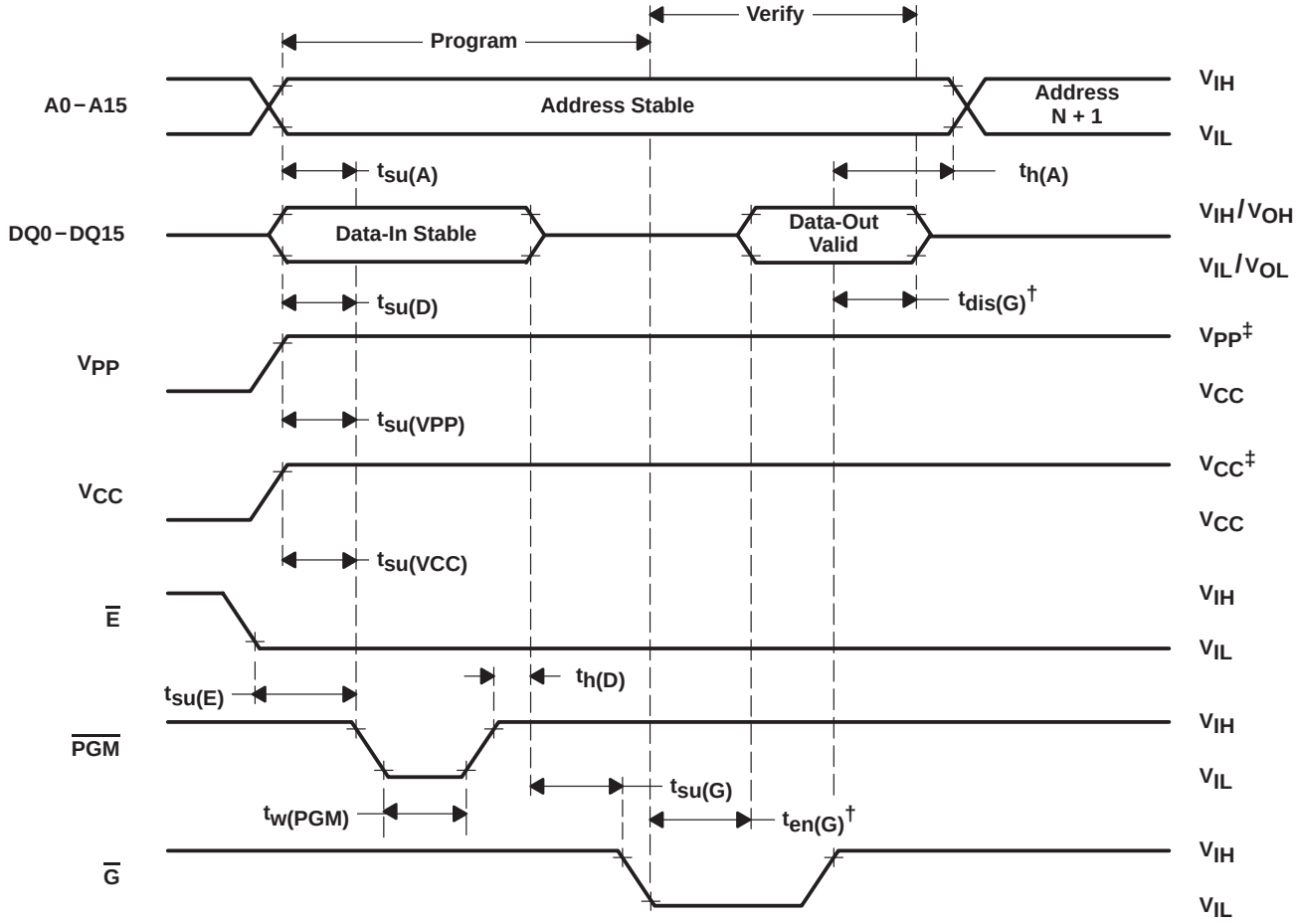


Figure 3. Read-Cycle Timing

PROGRAMMING INFORMATION

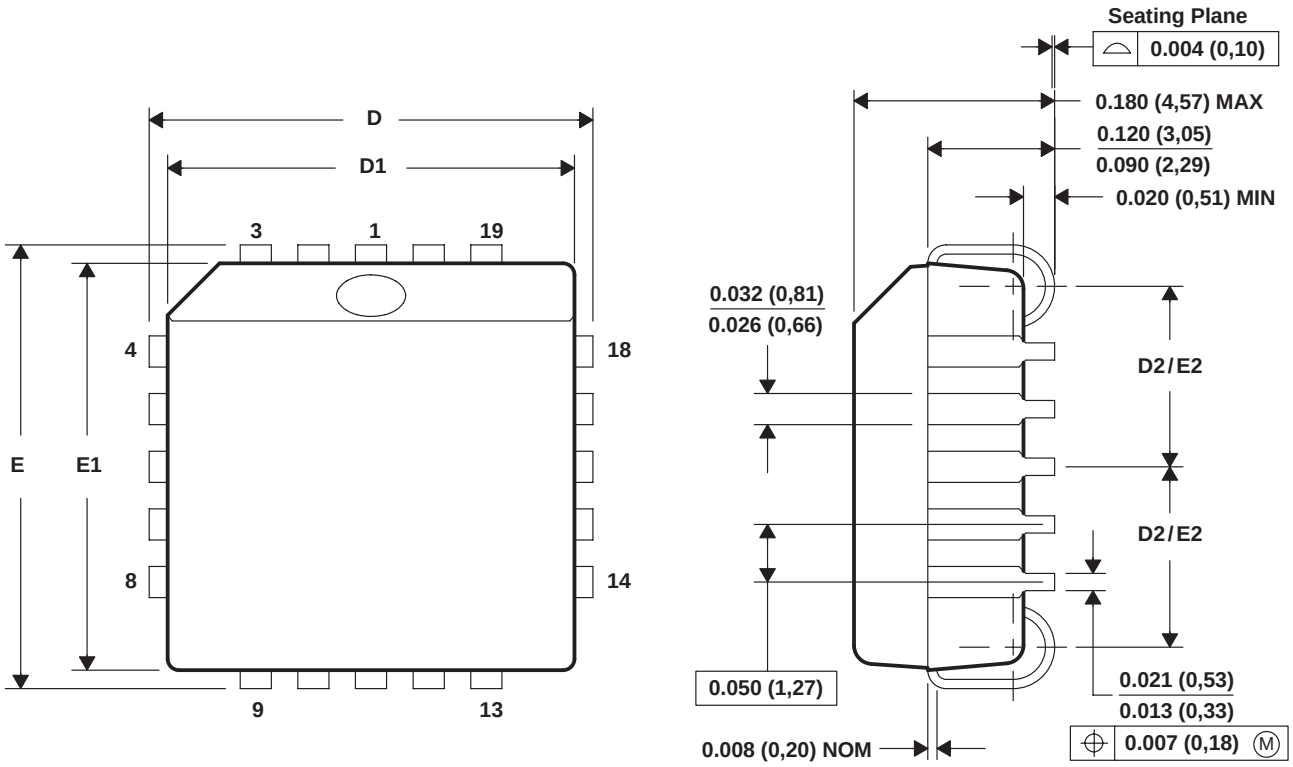


† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program-Cycle Timing (SNAP! Pulse Programming)

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



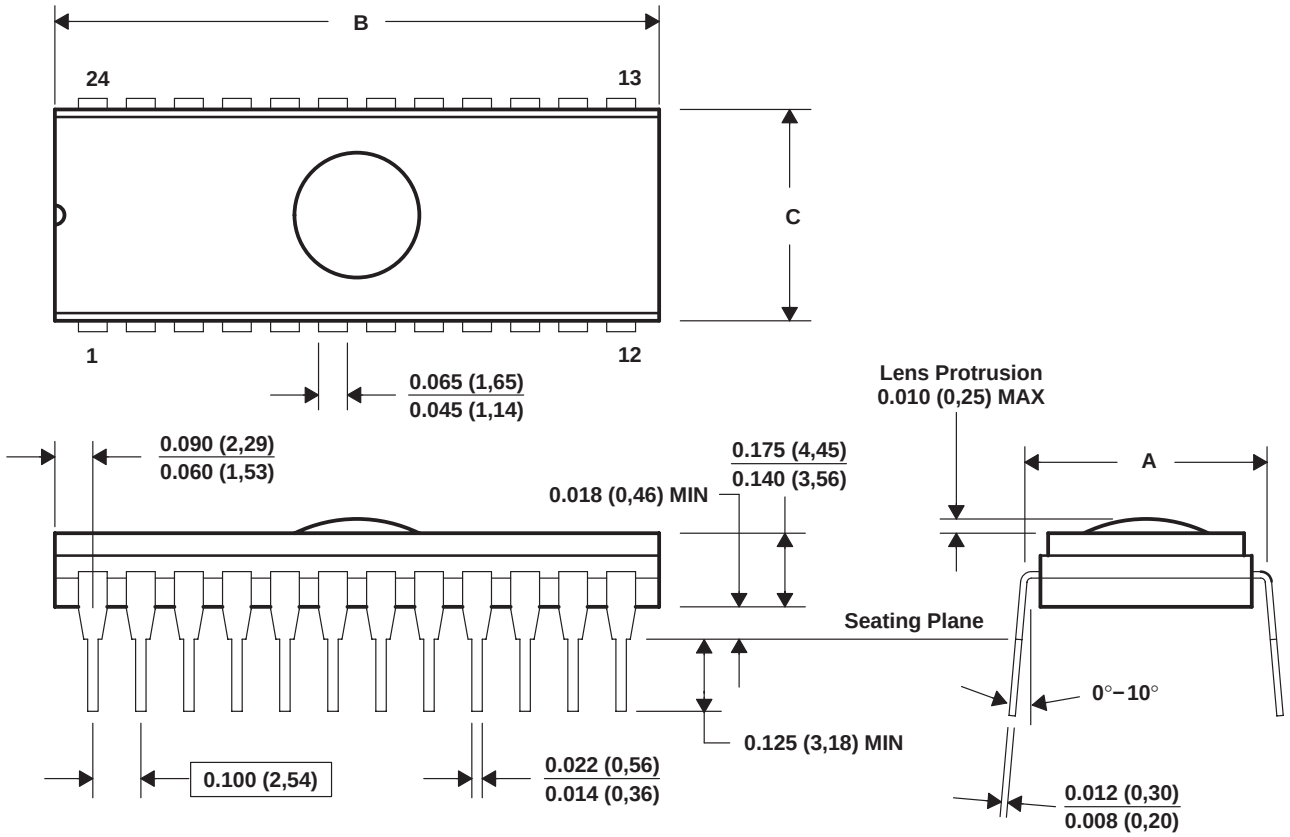
NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

J (R-CDIP-T**) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

24 PIN SHOWN



DIM	PINS**	24 NARR	24 WIDE	28 NARR	28 WIDE	32 NARR	32 WIDE	40 NARR	40 WIDE
A	MAX	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)
	MIN	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)
B	MAX	1.265(32,13)	1.265(32,13)	1.465(37,21)	1.465(37,21)	1.668(42,37)	1.668(42,37)	2.068(52,53)	2.068(52,53)
	MIN	1.235(31,37)	1.235(31,37)	1.435(36,45)	1.435(36,45)	1.632(41,45)	1.632(41,45)	2.032(51,61)	2.032(51,61)
C	MAX	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)
	MIN	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)

4040084/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.

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