LM386 低电压音频功率放大器

1 特性

- 电池供电
- 外部元件超少
- 宽电源电压范围：4V 至 12V 或 5V 至 18V
- 低静态电流消耗：4mA
- 电压增益范围：20 至 200
- 以地为基准的输入
- 自动居中的输出静态电压
- 低失真：0.2%（A_V = 20，V_S = 6V，R_L = 8Ω，P_O = 125mW，f = 1kHz）
- 采用 8 引脚 MSOP 封装

2 应用

- AM-FM 无线电放大器
- 便携式磁带播放器放大器
- 对讲机
- 电视音响系统
- 线路驱动器
- 超声波驱动器
- 小型伺服驱动器
- 电源转换器

3 说明

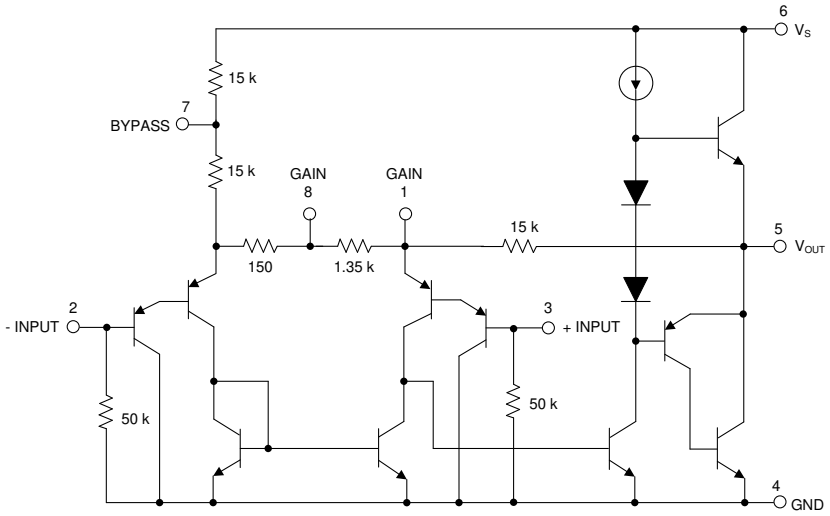
LM386M-1 和 LM386MX-1 是旨在用于低电压消费类应用的功率放大器。增益在内部设置为 20，用于减少外部元件数量，但在引脚 1 和 8 之间添加外部电阻器和电容器后，可将增益设置为 20 到 200 之间的任意值。

输入以地为基准，而输出自动偏置到电源电压的一半。LM386M-1 和 LM386MX-1 采用 6V 电源供电时，静态功耗仅为 24mW，因此非常适合采用电池供电。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LM386N-1	PDIP (8)	9.60mm × 6.35mm
LM386N-3	PDIP (8)	9.60mm × 6.35mm
LM386N-4	PDIP (8)	9.60mm × 6.35mm
LM386M-1	SOIC (8)	4.90mm × 3.90mm
LM386MX-1	SOIC (8)	4.90mm × 3.90mm
LM386MMX-1	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



原理图

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (May 2017) to Revision D (August 2023) — **Page**

- Updated Typical Output Power Spec 5

Changes from Revision B (March 2017) to Revision C (May 2017) — **Page**

- 将数据表标题中的器件 LM386M-1/LM386MX-1 更改为 LM386 1
- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- Changed From: LM386N-4 To: Speaker Impedance in the *Recommended Operating Conditions* table 4
- Changed From: 5 Ω to 12 Ω To: 5 V to 12 V for Supply Voltage in 表 9-1 10
- Changed kW To: kΩ in the *Gain Control* section 10
- Changed kW To: kΩ in the *Input Biasing* section 11
- Changed 图 9-2 11
- Changed From: 5 Ω to 12 Ω To: 5 V to 12 V for Supply Voltage in 表 9-2 12
- Changed 图 9-4 12
- Changed From: 5 Ω to 12 Ω To: 5 V to 12 V for Supply Voltage in 表 9-3 13
- Changed 图 9-6 13
- Changed From: 5 Ω to 12 Ω To: 5 V to 12 V for Supply Voltage in 表 9-4 14
- Changed 图 9-8 14
- Changed From: 5 Ω to 12 Ω To: 5 V to 12 V for Supply Voltage in 表 9-5 15
- Changed From: 5 Ω to 12 Ω To: 5 V to 12 V for Supply Voltage in 表 9-6 16
- Changed 图 9-12 16
- Changed From: 5 Ω to 12 Ω To: 5 V to 12 V for Supply Voltage in 表 9-7 17
- Changed 图 9-14 17

Changes from Revision A (May 2004) to Revision B (March 2017) — **Page**

- 向数据表添加了 LM386MX-1 器件 1
- 添加了“器件信息”、“应用和实施”、“电源相关建议”、“布局”以及“器件和文档支持”部分 1
- Inserted Functional Block Diagram 9

5 Pin Configuration and Functions

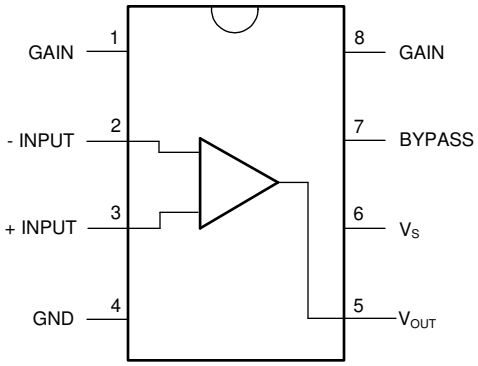


图 5-1. D Package 8-Pin MSOP Top View

表 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
GAIN	1	–	Gain setting pin
– INPUT	2	I	Inverting input
+INPUT	3	I	Noninverting input
GND	4	P	Ground reference
V_{OUT}	5	O	Output
V_S	6	P	Power supply voltage
BYPASS	7	O	Bypass decoupling path
GAIN	8	–	Gain setting pin

(1) I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage, V_{CC}	LM386N-1/-3, LM386M-1		15	V
	LM386N-4		22	
Package Dissipation	LM386N		1.25	W
	LM386M		0.73	
	LM386MM-1		0.595	
Input Voltage, V_I		– 0.4	0.4	V
Storage temperature, T_{stg}		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	4		12	V
	LM386N-4	5		18	V
	Speaker Impedance	4			Ω
VI	Analog input voltage	– 0.4		0.4	V
TA	Operating free-air temperature	0		70	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM386 D (SOIC) 8	LM386 DGK (VSSOP) 8	LM386 P (PDIP) 8	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.7	169.3	53.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.7	73.1	42.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.2	100.2	30.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.4	9.2	19.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.6	99.1	50.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_S	Operating Supply Voltage	LM386N-1, -3, LM386M-1, LM386MM-1	4		12	V
		LM386N-4	5		18	
I_Q	Quiescent Current	V_S = 6 V, V_{IN} = 0		4	8	mA
P_{OUT}	Output Power	V_S = 6 V, R_L = 8 Ω, THD = 10% (LM386N-1, LM386M-1, LM386MM-1)	250	325		mW
		V_S = 9 V, R_L = 8 Ω, THD = 10% (LM386N-3)	500	700		
		V_S = 16 V, R_L = 32 Ω, THD = 10% (LM386N-4)	700	1000		
A_V	Voltage Gain	V_S = 6 V, f = 1 kHz		26		dB
		10 µF from Pin 1 to 8		46		
BW	Bandwidth	V_S = 6 V, Pins 1 and 8 Open		300		kHz
THD	Total Harmonic Distortion	V_S = 6 V, R_L = 8 Ω, POUT = 125 mW f = 1 kHz, Pins 1 and 8 Open		0.2%		
PSRR	Power Supply Rejection Ratio	V_S = 6 V, f = 1 kHz, CBYPASS = 10 µF Pins 1 and 8 Open, Referred to Output		50		dB
R_{IN}	Input Resistance			50		kΩ
I_{BIAS}	Input Bias Current	V_S = 6 V, Pins 2 and 3 Open		250		nA

6.6 Typical Characteristics

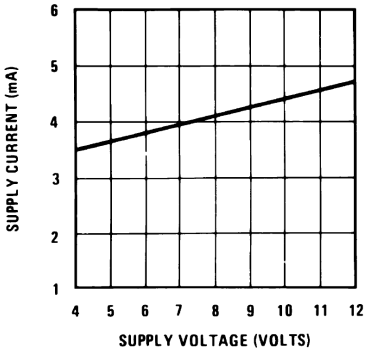


图 6-1. Supply Current vs Supply Voltage

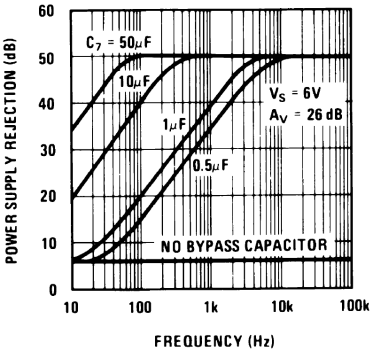


图 6-2. Power Supply Rejection vs Frequency

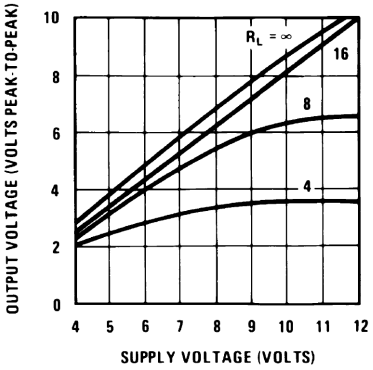


图 6-3. Output Voltage vs Supply Voltage

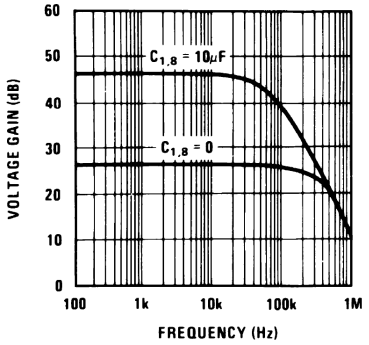


图 6-4. Voltage Gain vs Frequency

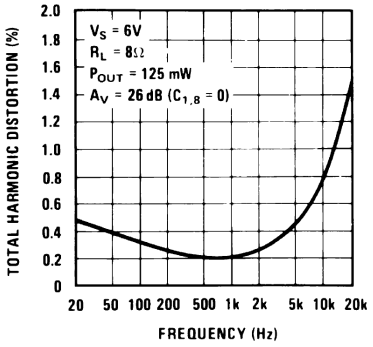


图 6-5. Total Harmonic Distortion vs Frequency

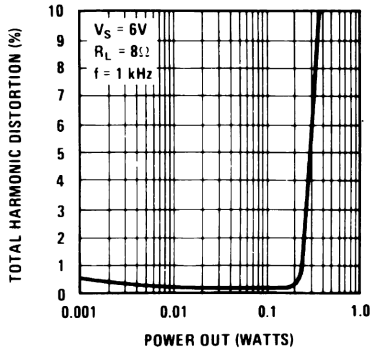


图 6-6. Total Harmonic Distortion vs Power Out

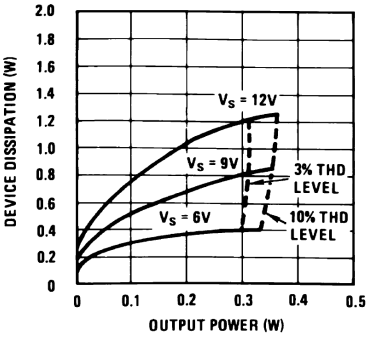


图 6-7. Device Dissipation vs Output Power

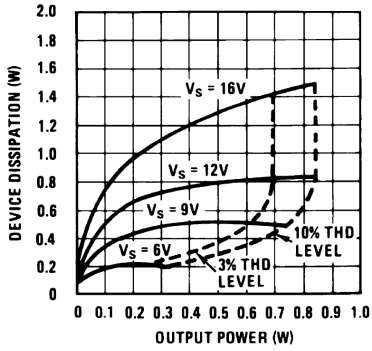


图 6-8. Device Dissipation vs Output Power

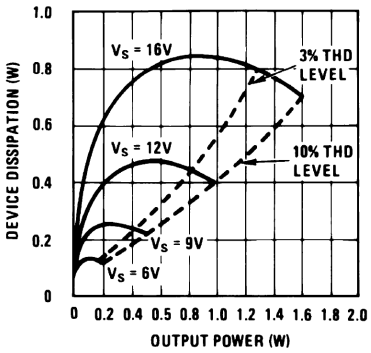


图 6-9. Device Dissipation vs Output Power

7 Parameter Measurement Information

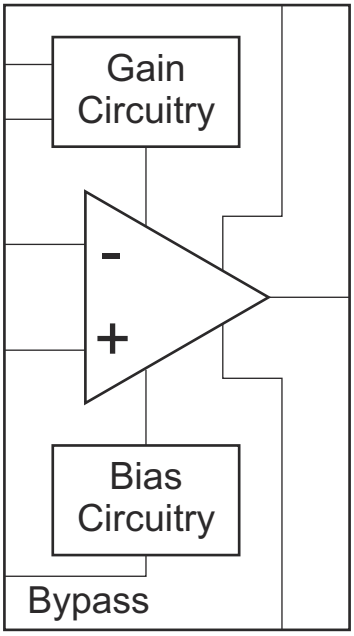
All parameters are measured according to the conditions described in the 节 6 section.

8 Detailed Description

8.1 Overview

The LM386 is a mono low voltage amplifier that can be used in a variety of applications. It can drive loads from 4 Ω to 32 Ω. The gain is internally set to 20 but it can be modified from 20 to 200 by placing a resistor and capacitor between pins 1 and 8. This device comes in three different 8-pin packages as PDIP, SOIC and VSSOP to fit in different applications.

8.2 Functional Block Diagram



8.3 Feature Description

There is an internal 1.35-KΩ resistor that sets the gain of this device to 20. The gain can be modified from 20 to 200. Detailed information about gain setting can be found in the 节 9.2.2.2 section.

8.4 Device Functional Modes

As this is an Op Amp it can be used in different configurations to fit in several applications. The internal gain setting resistor allows the LM386 to be used in a very low part count system. In addition a series resistor can be placed between pins 1 and 5 to modify the gain and frequency response for specific applications.

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Below are shown different setups that show how the LM386 can be implemented in a variety of applications.

9.2 Typical Application

9.2.1 LM386 with Gain = 20

图 9-1 shows the minimum part count application that can be implemented using LM386. Its gain is internally set to 20.

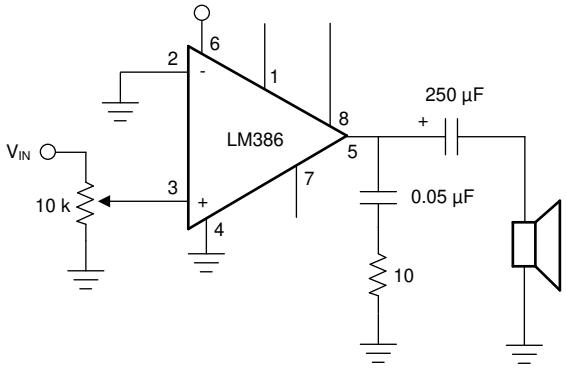


图 9-1. LM386 with Gain = 20

9.2.1.1 Design Requirements

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Load Impedance	4 Ω to 32 Ω
Supply Voltage	5 V to 12 V

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Gain Control

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35-kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35-kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal

15-kΩ resistor). For 6 dB effective bass boost: R ~= 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

9.2.1.2.2 Input Biasing

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance on the driven input.

9.2.1.3 Application Curve

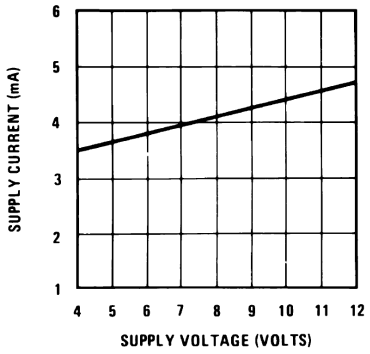


图 9-2. Supply Current vs Supply Voltage

9.2.2 LM386 with Gain = 200

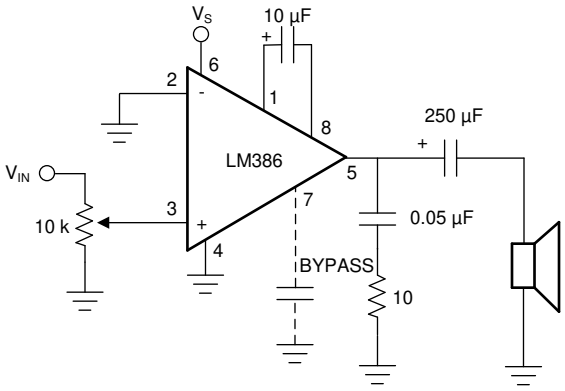


图 9-3. LM386 with Gain = 200

9.2.2.1 Design Requirements

表 9-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Load Impedance	4 Ω to 32 Ω
Supply Voltage	5 V to 12 V

9.2.2.2 Detailed Design Procedure

The Detailed Design Procedure can be found in the 节 *9.2.1.2* section.

9.2.2.3 Application Curve

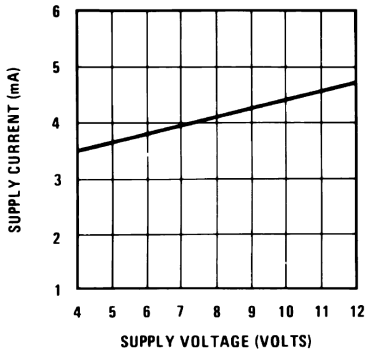


图 9-4. Supply Current vs Supply Voltage

9.2.3 LM386 with Gain = 50

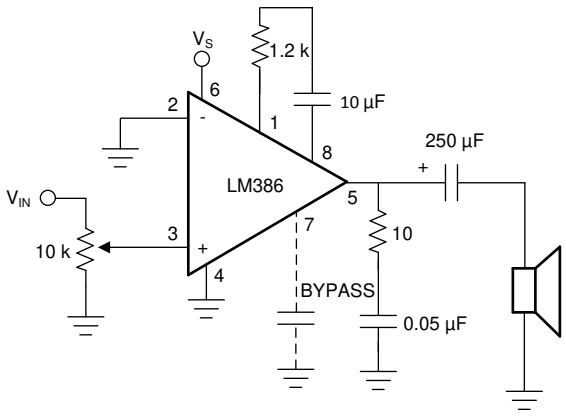


图 9-5. LM386 with Gain = 50

9.2.3.1 Design Requirements

表 9-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Load Impedance	4 Ω to 32 Ω
Supply Voltage	5 V to 12 V

9.2.3.2 Detailed Design Procedure

The Detailed Design Procedure can be found in the 节 *9.2.1.2* section.

9.2.3.3 Application Curve

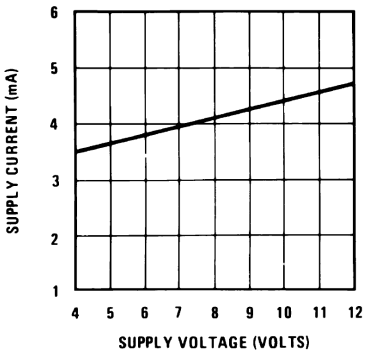


图 9-6. Supply Current vs Supply Voltage

9.2.4 Low Distortion Power Wienbridge Oscillator

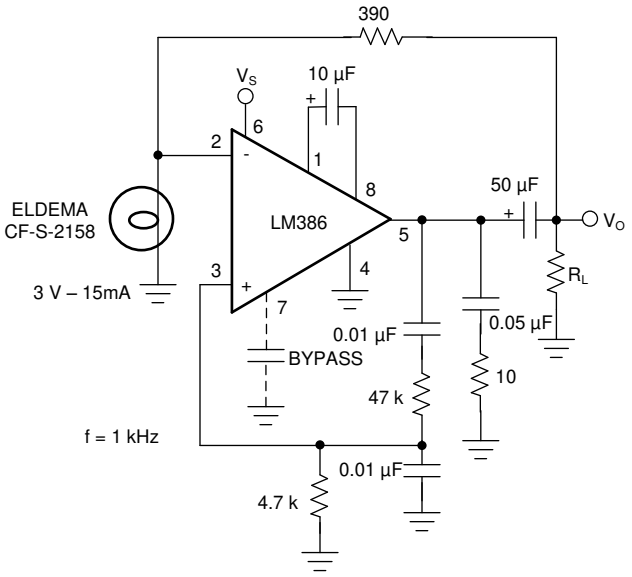


图 9-7. Low Distortion Power Wienbridge Oscillator

9.2.4.1 Design Requirements

表 9-4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Load Impedance	4 Ω to 32 Ω
Supply Voltage	5 V to 12 V

9.2.4.2 Detailed Design Procedure

The Detailed Design Procedure can be found in the 节 *9.2.1.2* section.

9.2.4.3 Application Curve

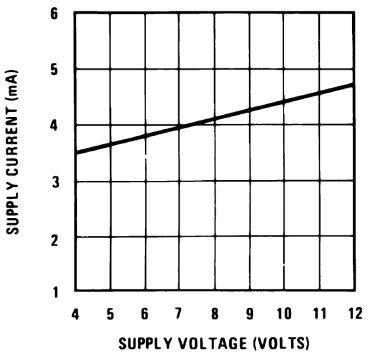


图 9-8. Supply Current vs Supply Voltage

9.2.5 LM386 with Bass Boost

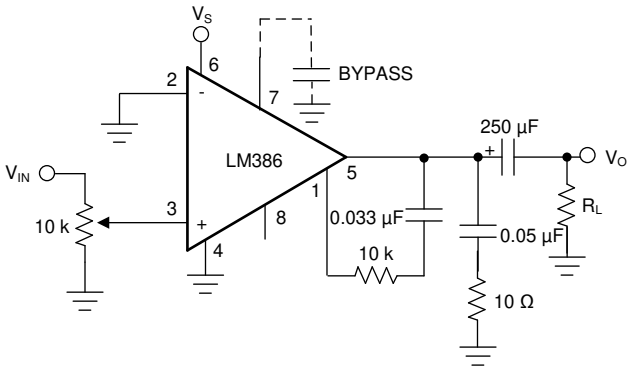


图 9-9. LM386 with Bass Boost

9.2.5.1 Design Requirements

表 9-5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Load Impedance	4 Ω to 32 Ω
Supply Voltage	5 V to 12 V

9.2.5.2 Detailed Design Procedure

The Detailed Design Procedure can be found in the 节 *9.2.1.2* section.

9.2.5.3 Application Curve

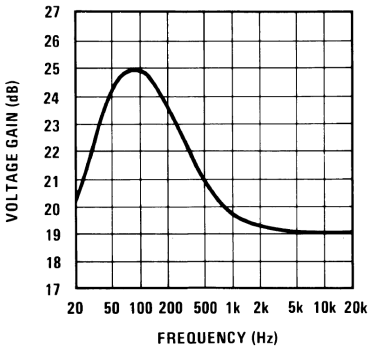


图 9-10. Voltage Gain vs Frequency

9.2.6 Square Wave Oscillator

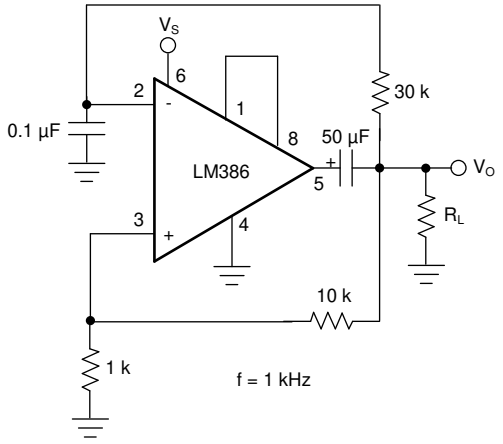


图 9-11. Square Wave Oscillator

表 9-6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Load Impedance	4 Ω to 32 Ω
Supply Voltage	5 V to 12 V

9.2.6.1 Detailed Design Procedure

The Detailed Design Procedure can be found in the 节 *9.2.1.2* section.

9.2.6.2 Application Curve

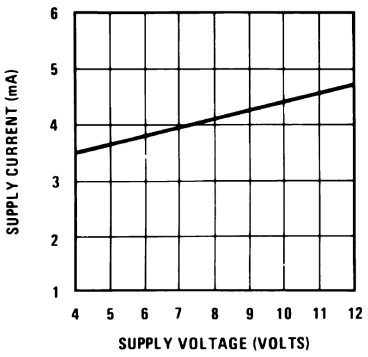


图 9-12. Supply Current vs Supply Voltage

9.2.7 AM Radio Power Amplifier

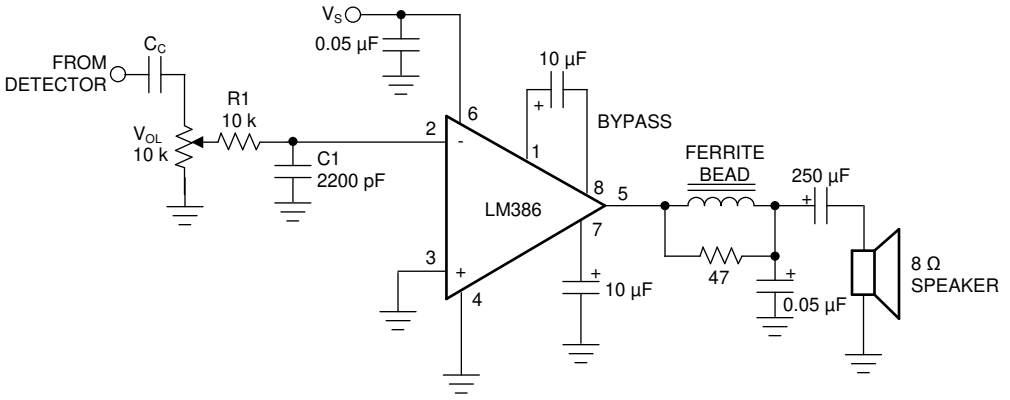


图 9-13. AM Radio Power Amplifier

9.2.7.1 Design Requirements

表 9-7. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Load Impedance	4 Ω to 32 Ω
Supply Voltage	5 V to 12 V

9.2.7.2 Detailed Design Procedure

The Detailed Design Procedure can be found in the 节 *9.2.1.2* section.

9.2.7.3 Application Curve

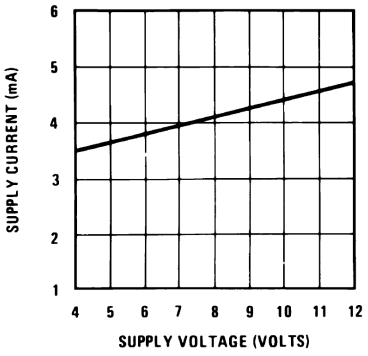


图 9-14. Supply Current vs Supply Voltage

10 Power Supply Recommendations

The LM386 is specified for operation up to 12 V or 18 V. The power supply should be well regulated and the voltage must be within the specified values. It is recommended to place a capacitor to GND close to the LM386 power supply pin.

11 Layout

11.1 Layout Guidelines

Place all required components as close as possible to the device. Use short traces for the output to the speaker connection. Route the analog traces far from the digital signal traces and avoid crossing them.

11.2 Layout Examples

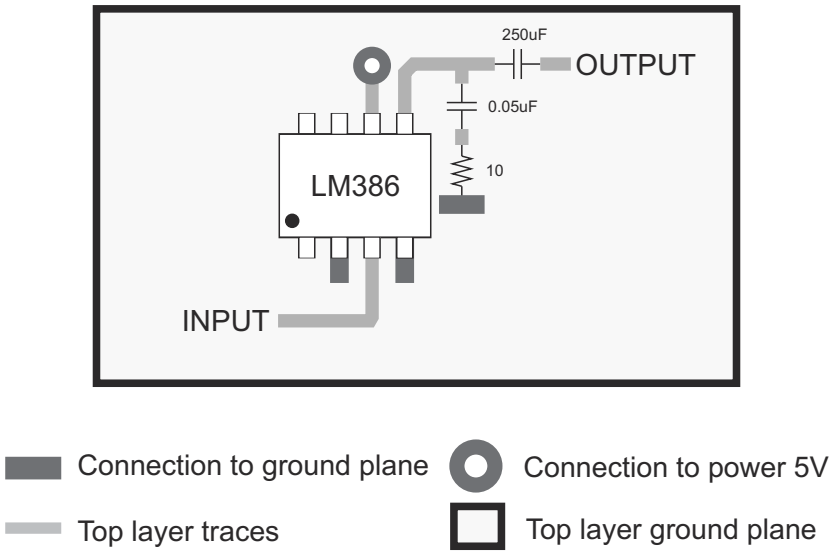


图 11-1. Layout Example for Minimum Parts Gain = 20 dB on PDIP package

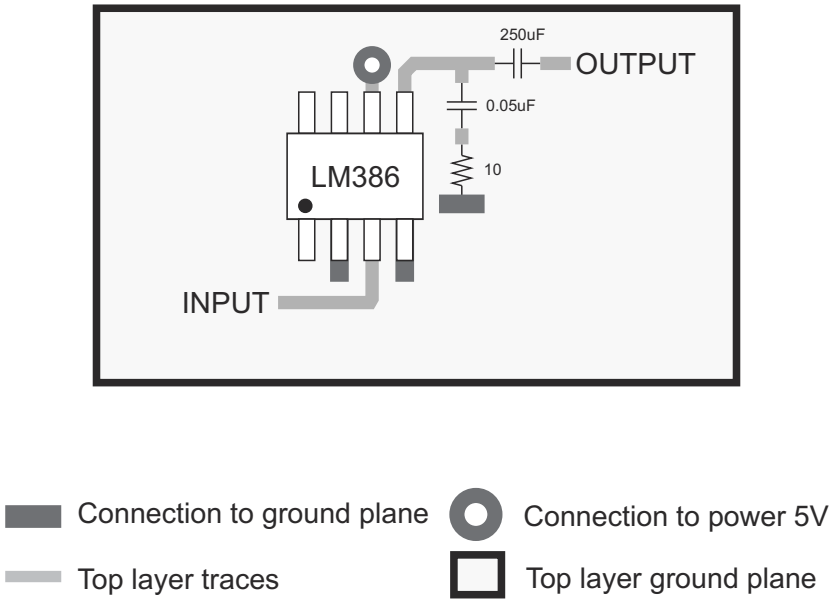


图 11-2. Layout Example for Minimum Parts Gain = 20 dB on SOIC package

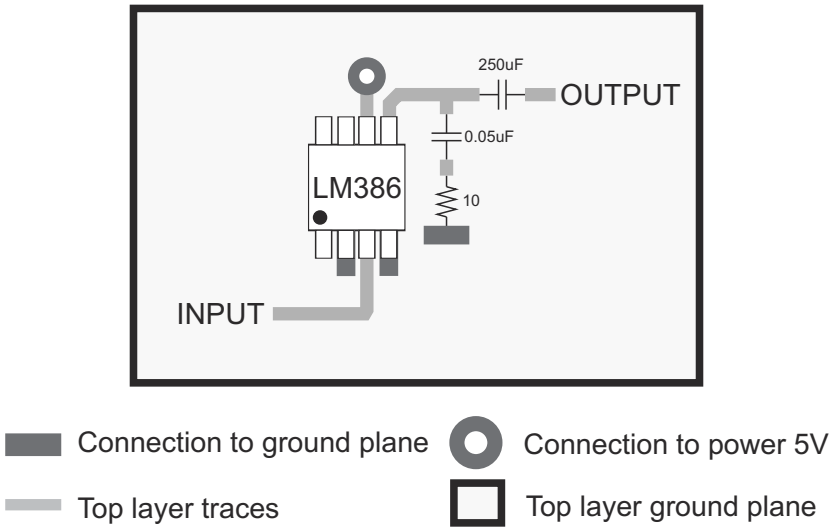


图 11-3. Layout Example for Minimum Parts Gain = 20 dB on VSSOP package

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.2 Documentation Support

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

12.4 Community Resources

12.5 Trademarks

所有商标均为其各自所有者的财产。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM386M-1/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LM386 M-1	Samples
LM386MMX-1/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	Z86	Samples
LM386MX-1/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LM386 M-1	Samples
LM386N-1/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM 386N-1	Samples
LM386N-3/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM 386N-3	Samples
LM386N-4/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM 386N-4	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

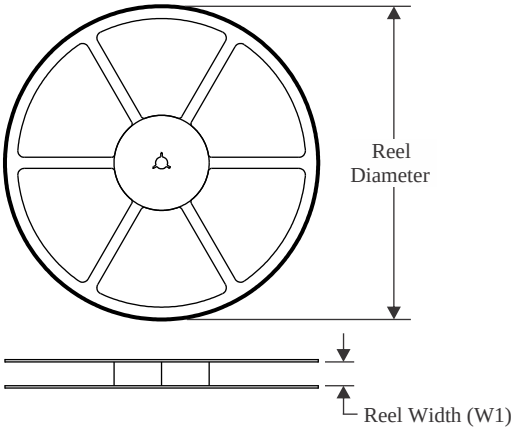
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

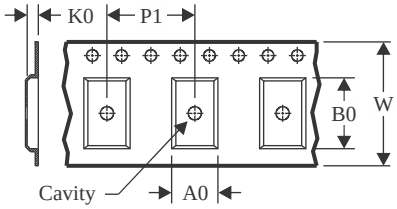
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

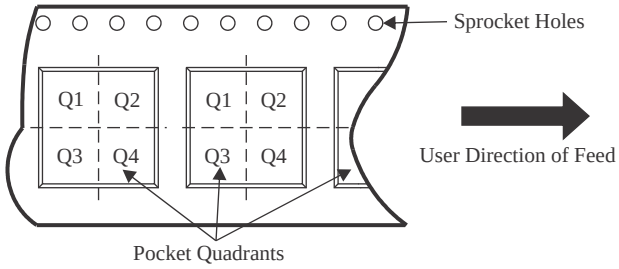


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

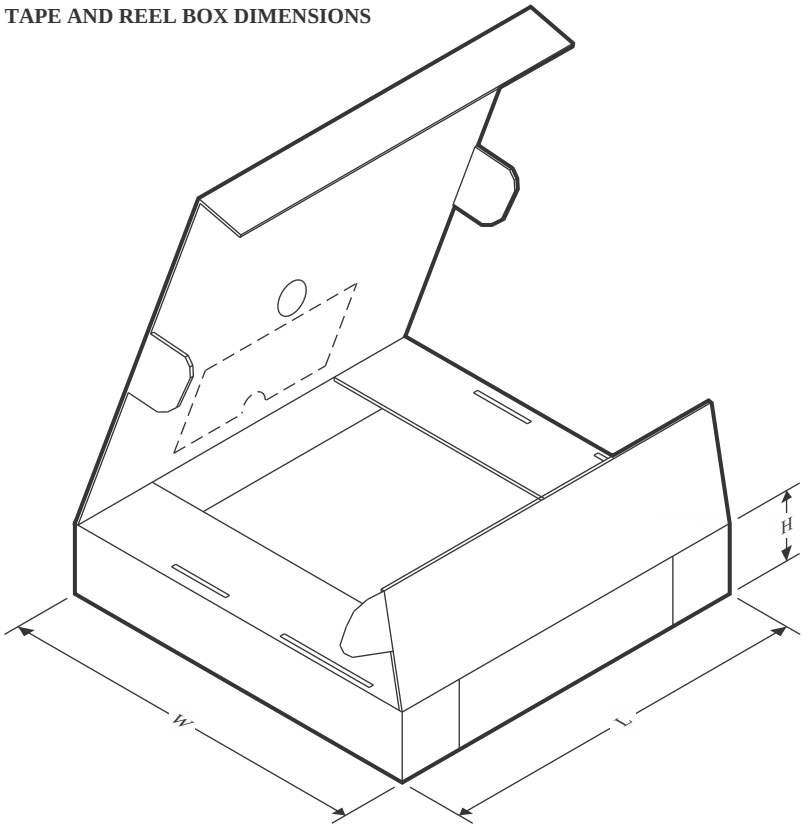
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM386MMX-1/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM386MX-1/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

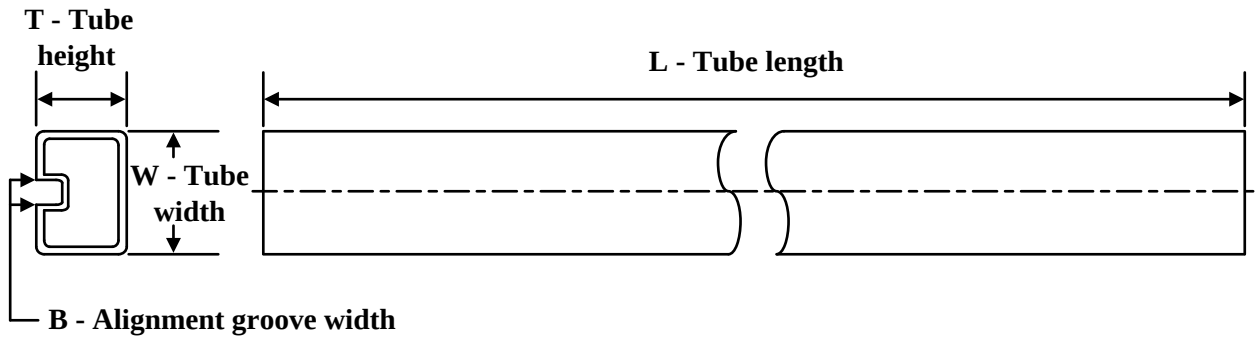
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

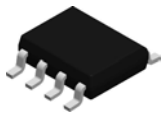
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM386MMX-1/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM386MX-1/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM386M-1/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM386N-1/NOPB	P	PDIP	8	40	502	14	11938	4.32
LM386N-3/NOPB	P	PDIP	8	40	502	14	11938	4.32
LM386N-4/NOPB	P	PDIP	8	40	502	14	11938	4.32

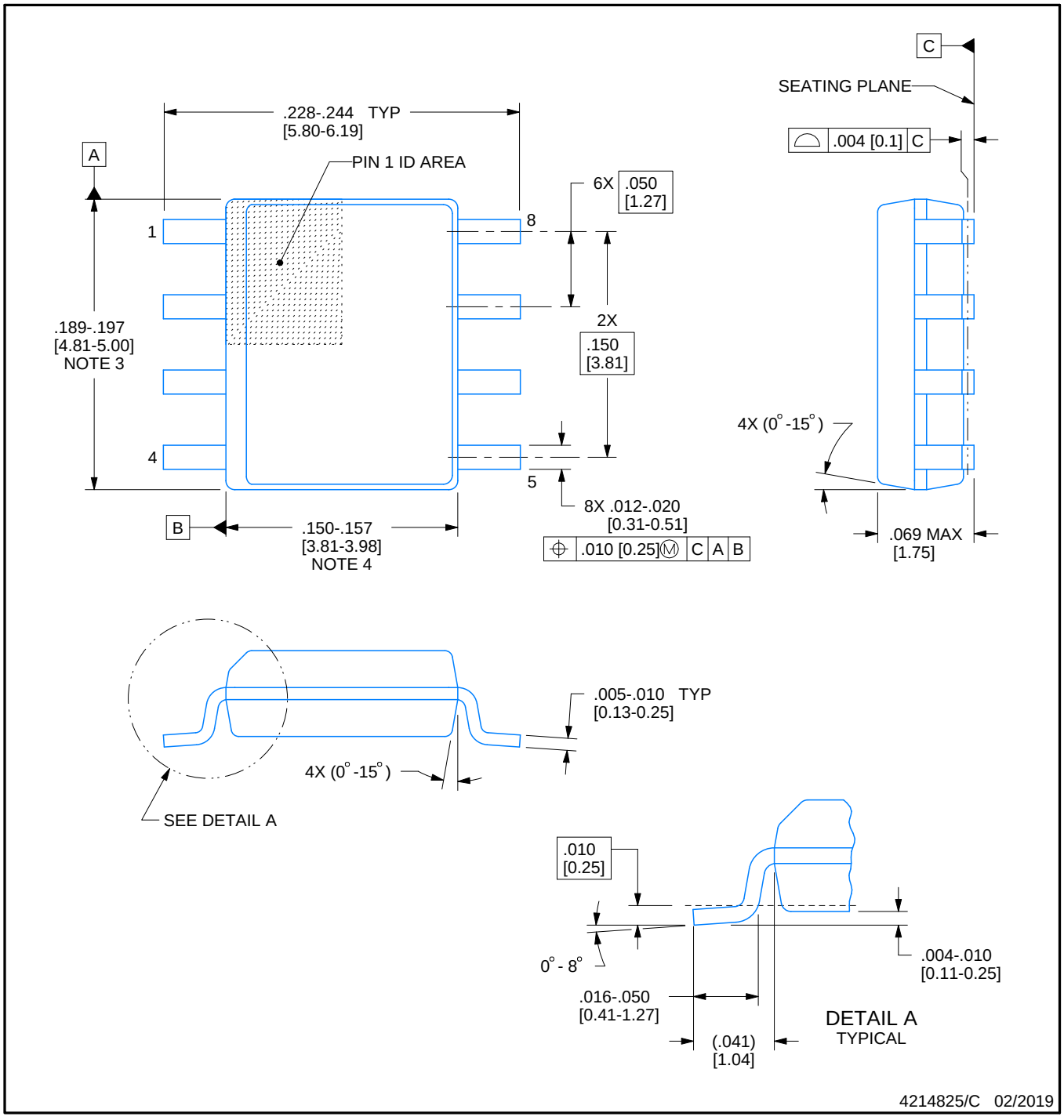


PACKAGE OUTLINE

D0008A

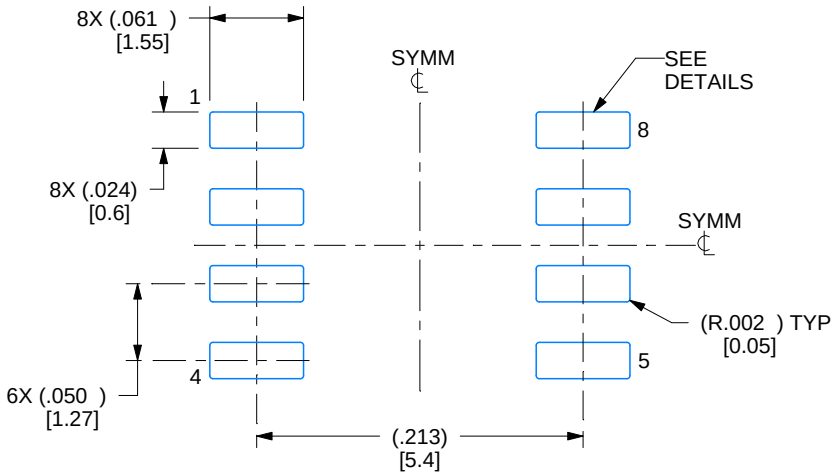
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

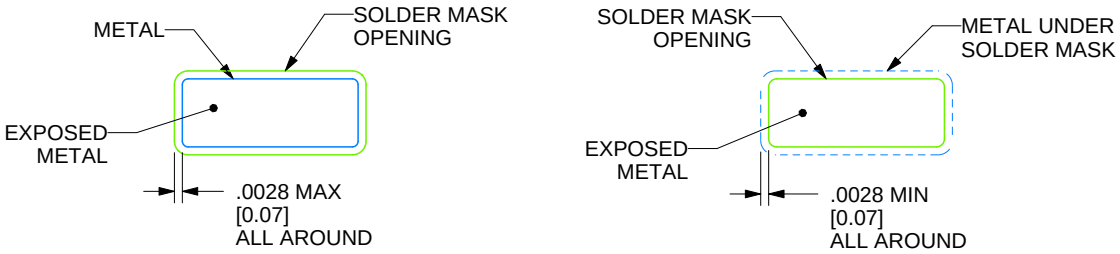


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

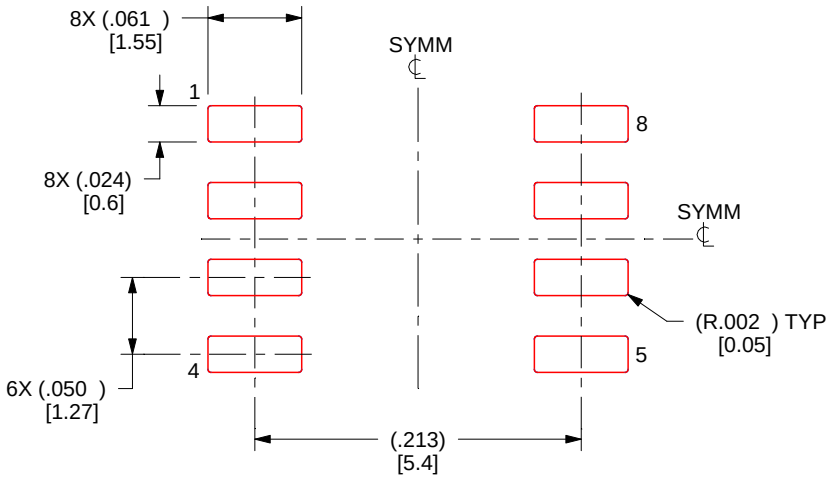
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



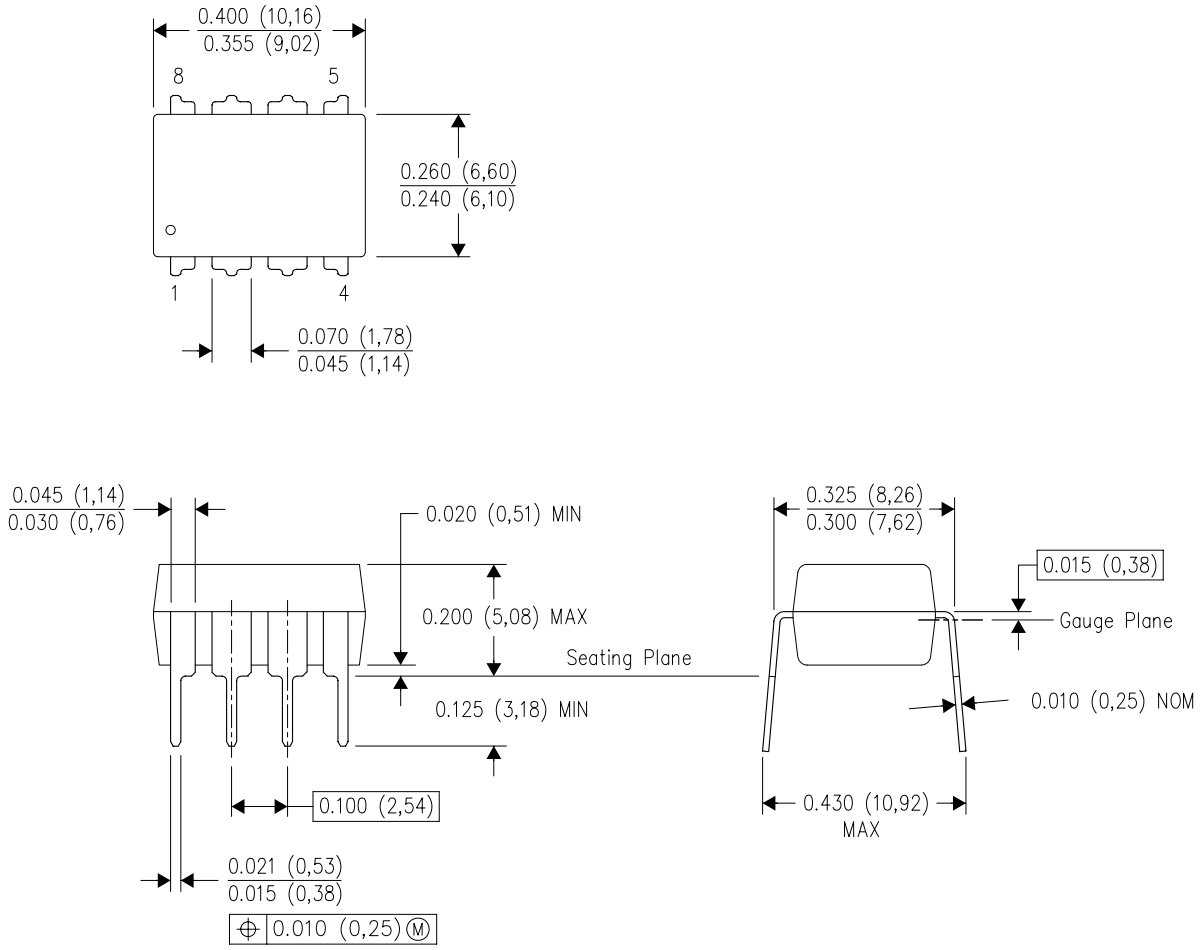
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



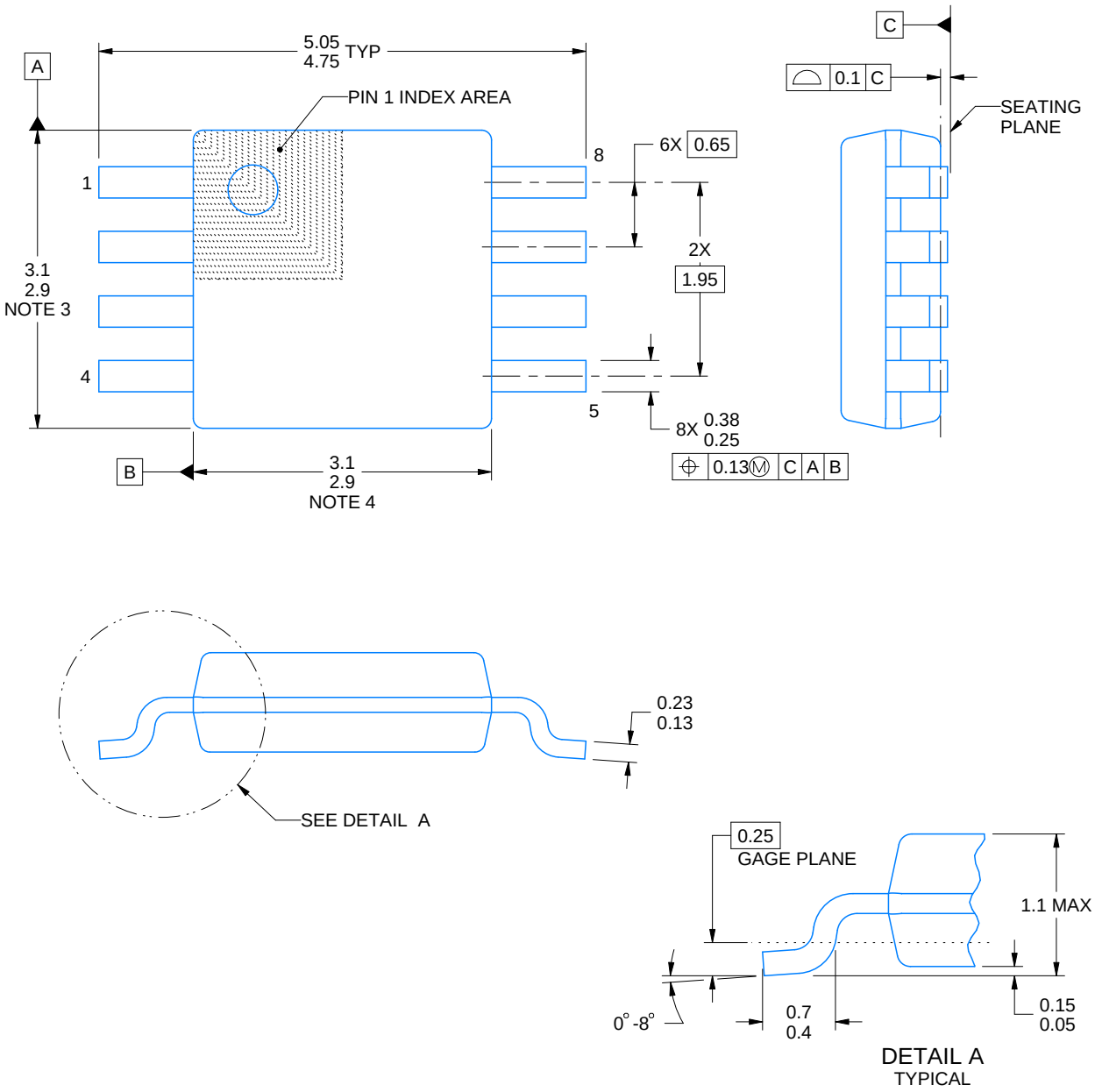
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

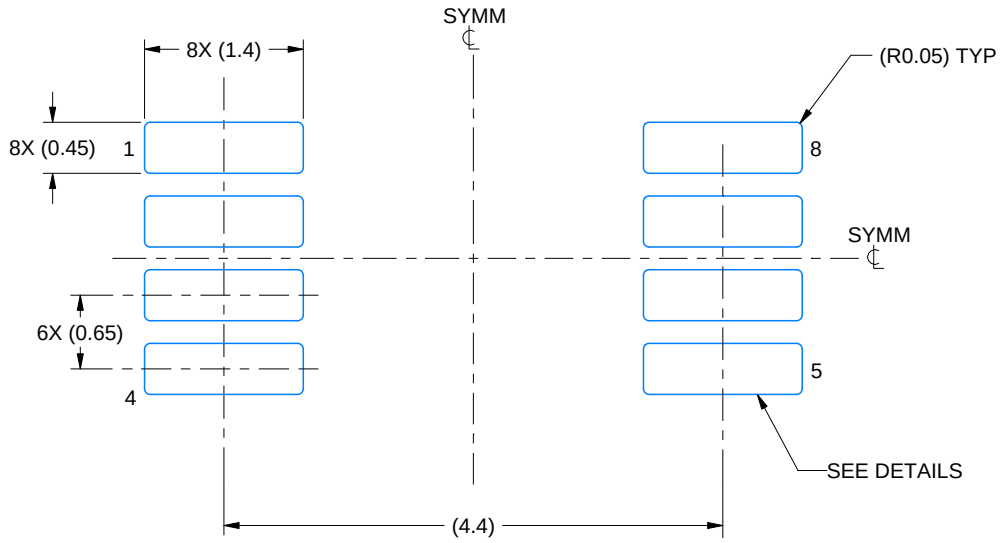
SMALL OUTLINE PACKAGE



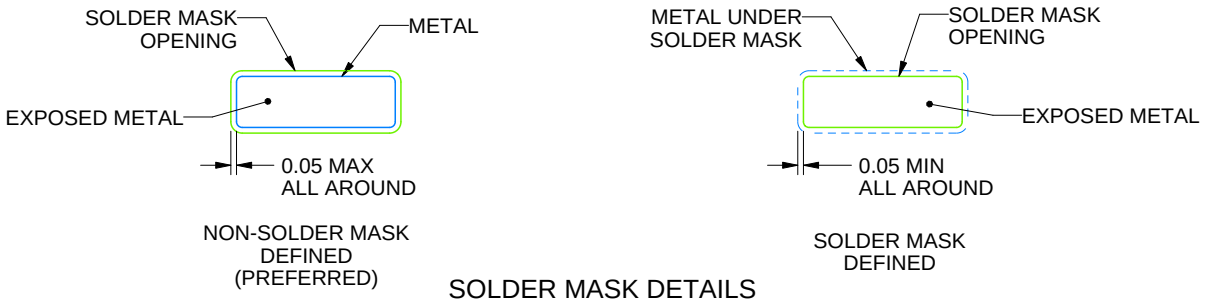
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

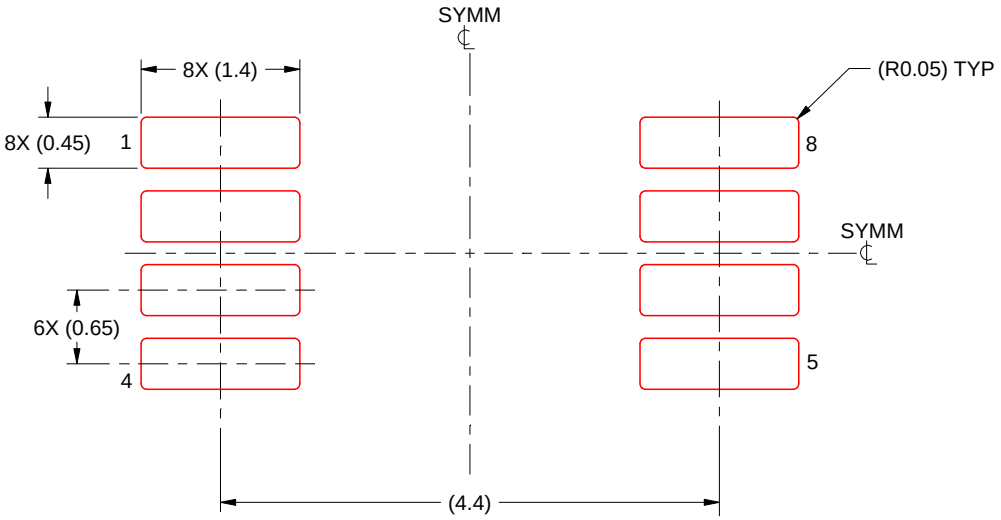


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265