

Advance PXAE184408NB

Thermally-Enhanced High Power RF LDMOS FET 450 W, 28 V, 1805 – 1880 MHz

Description

The PXAE184408NB is a 450-watt LDMOS FET intended for use in multi-standard cellular power amplifier applications in the 1805 to 1880 MHz frequency band. Features include input and output matching, high gain and a thermally-enhanced package with earless flange. Manufactured with Wolfspeed's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.

Advance Specification Data Sheets describe products that are being considered by Wolfspeed for development and market introduction. The target performance shown in Advance Specifications is not final and should not be used for any design activity. Please contact Wolfspeed about the future availability of these products.

Features

- Broadband internal matching
- Typical pulsed CW performance, 1880 MHz, 28 V, Doherty configuration, 10 μ sec pulse width, 10% duty cycle
 - Output power at P_{1dB} = 440 W
 - Output power at P_{3dB} = 540 W
 - Efficiency = 58.5%
 - Gain = 13 dB
- Integrated ESD protection
- Low thermal resistance
- Pb-free and RoHS compliant



PXAE184408NB
Package PG-HB2SOF-8-1

Target RF Characteristics

Single-carrier WCDMA Specifications (tested in Wolfspeed Doherty test fixture)

V_{DD} = 28 V, I_{DQ} = 1.2 A, P_{OUT} = 87 W avg, $V_{GS(PEAK)}$ = 1.5 V, f = 1842.5 MHz. 3GPP WCDMA signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF.

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	16	—	dB
Drain Efficiency	η_D	—	51	—	%
Adjacent Channel Power Ratio	ACPR	—	-29	—	dBc
Output PAR @ 0.01% CCDF	OPAR	—	8	—	dB

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!



DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1	μA
	$V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10	μA
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1	μA
On-State Resistance	(Main) $V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	TBD	—	Ω
	(Peak) $V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	TBD	—	Ω
Operating Gate Voltage	(Main) $V_{DS} = 28\text{ V}$, $I_{DQ} = 200\text{ mA}$	V_{GS}	—	3.0	—	V
	(Peak) $V_{DS} = 28\text{ V}$, $I_{DQ} = 0\text{ mA}$	V_{GS}	—	1.5	—	V

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	−6 to +10	V
Operating Voltage	V_{DD}	0 to +32	V
Junction Temperature	T_J	225	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	−65 to +150	$^{\circ}\text{C}$

Thermal Characteristics

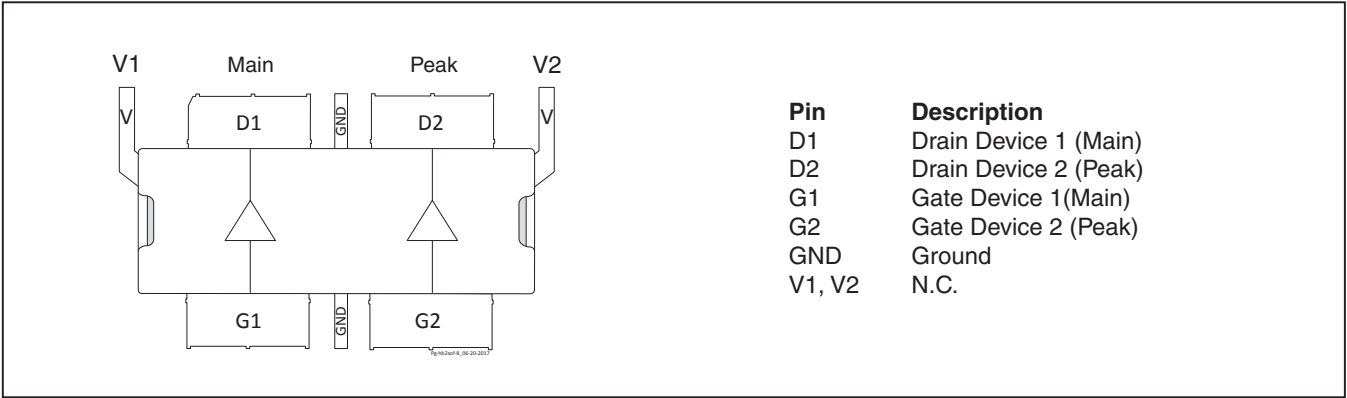
Characteristic	Symbol	Value	Unit
Thermal Resistance	$R_{\theta JC}$	TBD	$^{\circ}\text{C/W}$

Ordering Information

Type and Version	Order Code	Package and Description	Shipping
PXAE184408NB V1 R5	TBD	PG-HB2SOF-8-1, surface mount	Tape & Reel, 500 pcs



Pinout Diagram (top view)



Lead connections for PXAE184408NB

See next page for package dimensions

Package Outline Specifications

Package PG-HB2SOF-8-1

(top and side views)

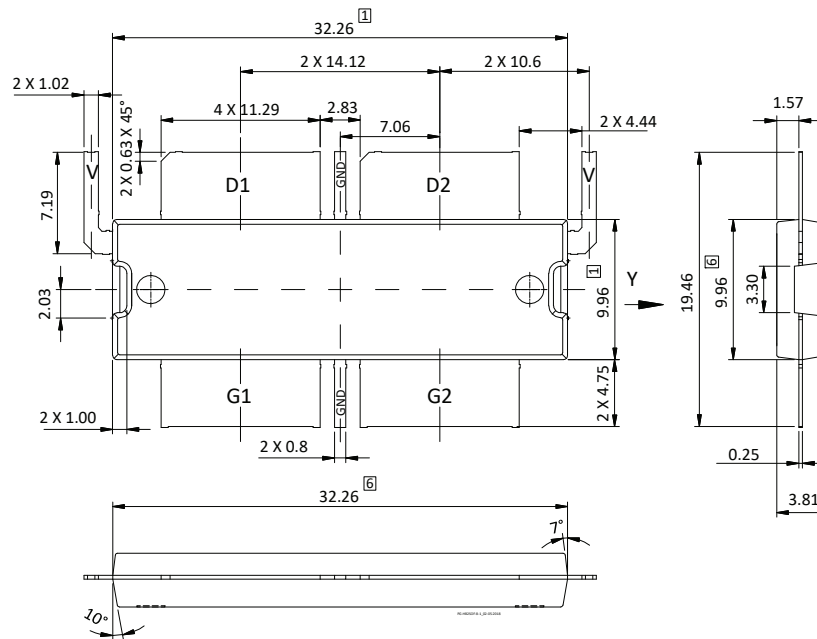


Diagram Notes—unless otherwise specified:

1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included.
2. Fillets and radii: all radii are 0.3 mm max unless specified otherwise.
3. Interpret dimensions and tolerances per ISO 8015.
4. Dimensions are mm.
5. Exposed metal surfaces are tin-plated, may not be covered by mold compound
6. Does not include mold/dam bar and metal protrusion.
7. All tolerances ± 0.1 mm unless specified otherwise.
8. All metal surfaces tin-plated, except area of cut.
9. Lead thickness: 0.25 mm.
10. Pins: D1, D2 – drain; G1, G2 – gate; V – V_{DD} ; GND – ground

Package Outline Specifications

Package PG-HB2SOF-8-1
(bottom view)

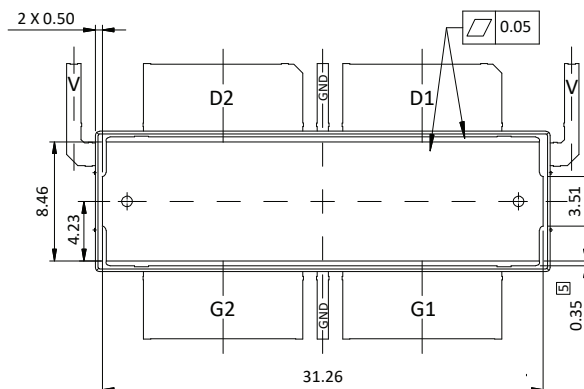


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Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2018-01-09	Advance	All	Data Sheet reflects advance specification for product development
02	2018-02-28	Advance	1, 2 4, 5	Features updated, On-state Resistance updated for Main and Peak Package outline - note #5 added
03	2018-05-01	Advance	All	Converted to Wolfspeed Data Sheet

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Notes

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