
M24256 and M24512 EEPROM devices: compatibility with the I²C-bus specification at 400 kHz and 1 MHz

Introduction

The I²C-bus specification, defined by NXP/Philips, defines how the I²C-bus can be used at various serial clock frequency values.

This note describes how the M24256 and M24512 EEPROM devices are compatible with the 1 MHz and 400 kHz I²C-bus specification.

Table 1. Applicable products

Device	RPN
M24256	M24256-BF
	M24256-BR
	M24256-BW
M24512	M24512-R
	M24512-W

1 M24xxx EEPROM: 400 kHz and 1 MHz clock

1.1 M24xxx 400 kHz AC tables until 2007

In the last revisions of the I²C-bus specification, defined by NXP/Philips, one can see that the 1 MHz serial clock rate was introduced in 2007:

- January 2000: the I²C-bus specification defines a clock rate of either 100 kHz, 400 kHz or 3.4 MHz^(a).
- June 2007: the I²C-bus specification defines a new table offering all timings related to the 1 MHz clock.

Before 2007, the M24xxx EEPROM devices offered by ST were specified with an AC table based on a 400 kHz (max) clock rate.

Two main differences appear when comparing the 400 kHz M24xxx AC table with the I²C-bus specification AC table (see [Table 2](#)):

- the min value of Data out hold time (t_{CLQX}) ;
- the max value of Pulse width ignored (t_{NS}).

Table 2. Access time and Noise filter parameters specified in the 400 kHz AC table

Symbol	Alt	Parameter	M24xxx		I ² C-bus		Unit
			Min	Max	Min	Max	
t_{CLQV}	t_{AA}	Data valid time	-	900	-	900	ns
t_{CLQX}	$t_{HD:DAT}$	Data out hold time	100	-	0	-	ns
t_{NS}	t_{SP}	Pulse width ignored (input filter on SCL and SDA)	-	50 (or more)	0	50	ns

Why such differences?

The M24xxx devices are designed to offer the best performances compatible with the I²C-bus specification, that is:

- t_{CLQX}

The min value of t_{CLQX} provides a delay for the data out time (from the falling edge of the serial clock SCL: time for the data line SDA to hold the previous bit value before changing state). This min value pushes away the SDA change from the SCL falling edge: that is a safe timing condition, as SDA and SCL must never switch at the same time (such an event is a critical event for the I²C-bus, as it could be randomly decoded as either a Start, a Stop or a Data-in event).

- t_{NS}

The greater the value of t_{NS} , the better the filter can screen out spikes added on the I²C bus.

a. The 3.4 MHz clock rate is not supported by the M24xxx EEPROM.

1.2 M24xxx 1 MHz AC tables after 2007

The M24xxx devices running with a 1 MHz clock frequency were introduced by STMicroelectronics from year 2007. Here again, the M24xxx compatible with the new 1 MHz I²C-bus specification were designed with timings able to offer the best performances.

Now, when comparing the 1 MHz I²C-bus specification and the M24xxx AC table, the t_{CLQV} and t_{NS} timing values are as shown in [Table 3](#):

Table 3. Access time and Noise filter parameters specified in the 1 MHz AC table

Symbol	Alt	Parameter	M24xxx		I ² C-bus		Unit
			Min.	Max.	Min.	Max.	
t_{CLQV}	t_{AA}	Data valid time	-	500	-	450	ns
t_{CLQX}	$t_{HD:DAT}$	Data out hold time	50 (or more)	-	0	-	ns
t_{NS}	t_{SP}	Pulse width ignored (input filter on SCL and SDA)		50 (or more)	0	50	ns

- $t_{CLQX}(\text{min})$ is here again specified with a positive value (as this offers a safe timing condition, as explained for the previous 400 kHz table).
- t_{NS} is now equal or better than the value defined in the I²C-bus specification.

1.3 Compatibility of 400 kHz and 1 MHz AC timing specifications

It is important to note that:

- all M24xxx products specified at 1 MHz can run at lower frequencies, and therefore can run at 400 kHz ;
- old products designed only for the 400 kHz AC tables (AC tables before 2007) cannot run at 1 MHz.

[Table 4](#) lists the M24xxx devices that run at 400 kHz only (and hence that cannot be used in any application running at 1 MHz).

Table 4. I²C EEPROM and max operating clock frequency

	400 kHz only	400 kHz and 1 MHz
M24C01	Process letter G or S	Not significant (1 MHz not specified in the data sheet)
M24C02	Process letter G or S	Not significant (1 MHz not specified in the data sheet)
M24C04	Process letter G or S	Not significant (1 MHz not specified in the data sheet)
M24C08	Process letter G or S	Not significant (1 MHz not specified in the data sheet)
M24C16	Process letter G or S	Not significant (1 MHz not specified in the data sheet)
M24C32	Process letter P or A	Process letter K
M24C64	Process letter P or A	Process letter K
M24C128	Process letter P or A	Process letter K
M24256	Process letter A	Process letter K
M24512	Process letter A or B	Process letter K
M24M01		Process letters A and K
M24M02		Process letter K

2 Revision history

Table 5. Document revision history

Date	Revision	Changes
17-Dec-2010	1	Initial release.
21-Feb-2014	2	Revised Table 2 and Table 3 with insertion of t_{CQLX} parameter Revised Section 1.1 and Section 1.2 Revised Table 4

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