# Ultrafast Transient Response, Low Dropout Regulators Adjustable and Fixed

## FEATURES

- **UltraFast™ Transient Response *Eliminates* Tantalum and Electrolytic Output Capacitors**
- **FET $R_{DS(ON)}$ Defines Dropout Voltage**
- **1% Reference/Output Voltage Tolerance Over Temperature**
- Typical Load Regulation: 1mV
- High Side Sense Current Limit
- Multifunction Shutdown Pin with Latchoff

## APPLICATIONS

- Pentium® Processor Supplies
- PowerPC™ Supplies
- 5V to 3.XXV or 3.3V to 2.XXV Microprocessor Supplies
- GTL Termination
- Low Voltage Logic Supplies

| | |
|---|---|
| LT1575CN8/LT1575CS8 | Adjustable |
| LT1575CN8-1.5/LT1575CS8-1.5 | 1.5V Fixed |
| LT1575CN8-2.8/LT1575CS8-2.8 | 2.8V Fixed |
| LT1575CN8-3.3/LT1575CS8-3.3 | 3.3V Fixed |
| LT1575CN8-3.5/LT1575CS8-3.5 | 3.5V Fixed |
| LT1575CN8-5/LT1575CS8-5 | 5V Fixed |
| LT1577CS-ADJ/ADJ | Adjustable, Adjustable |
| LT1577CS-3.3/ADJ | 3.3V Fixed, Adjustable |
| LT1577CS-3.3/2.8 | 3.3V Fixed, 2.8V Fixed |

Consult factory for additional output voltage combinations available in the LT1577.

## DESCRIPTION

The LT®1575/LT1577 are single/dual controller ICs that drive low cost external N-channel MOSFETs as source followers to produce ultrafast transient response, low dropout voltage regulators.

The LT1575/LT1577 achieve unprecedented transient-load performance by eliminating expensive tantalum or bulk electrolytic output capacitors in the most demanding modern microprocessor applications. Precision-trimmed adjustable and fixed output voltage versions accommodate any required microprocessor power supply voltage. Selection of the N-channel MOSFET $R_{DS(ON)}$ allows very low dropout voltages to be achieved.

Unique protection features include a high side current limit amplifier that activates a fault protection timer circuit. A multifunction Shutdown pin provides either current limit time-out with latchoff, overvoltage protection, thermal shutdown or a combination of these functions. The LT1575 is available in 8-pin SO or PDIP and the LT1577 is available in 16-pin narrow body SO.

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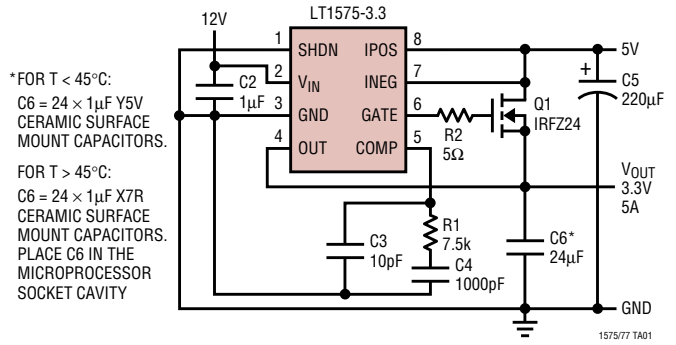
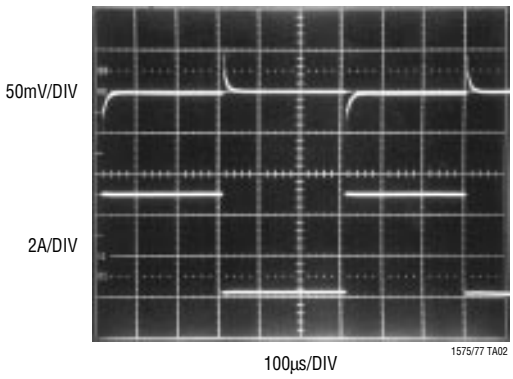
Pentium is a registered trademark of Intel Corporation.
PowerPC is a trademark of IBM Corporation.

## TYPICAL APPLICATION

**Ultrafast Transient Response 5V to 3.3V Low Dropout Regulator (For Schematic Including Current Limit, See Typical Applications)**




**Transient Response for 0.2A to 5A Output Load Step**

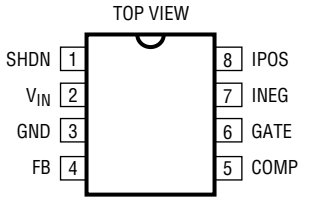


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN}$, IPOS, INEG ..... 22V
SHDN ..... $V_{IN}$
Operating Ambient Temperature Range ..... 0°C to 70°C
Junction Temperature (Note 2) ..... 0°C to 100°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION




N8 PACKAGE 8-LEAD PDIP
S8 PACKAGE 8-LEAD PLASTIC SO

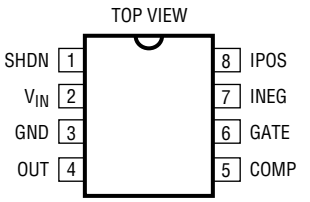
$T_{JMAX}$ = 100°C, $\theta_{JA}$ = 100°C/W (N8)
$T_{JMAX}$ = 100°C, $\theta_{JA}$ = 130°C/W (S8)

ORDER PART NUMBER

LT1575CN8
LT1575CS8

S8 PART MARKING

1575




N8 PACKAGE 8-LEAD PDIP
S8 PACKAGE 8-LEAD PLASTIC SO

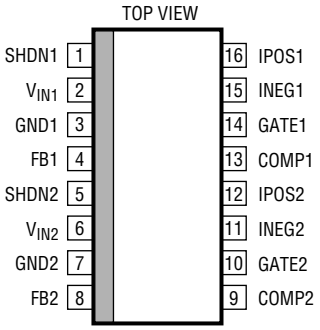
$T_{JMAX}$ = 100°C, $\theta_{JA}$ = 100°C/W (N8)
$T_{JMAX}$ = 100°C, $\theta_{JA}$ = 130°C/W (S8)

ORDER PART NUMBER

LT1575CN8-1.5
LT1575CS8-1.5
LT1575CN8-2.8
LT1575CS8-2.8
LT1575CN8-3.3
LT1575CS8-3.3
LT1575CN8-3.5
LT1575CS8-3.5
LT1575CN8-5
LT1575CS8-5

S8 PART MARKING

157515
157528
157533
157535
15755

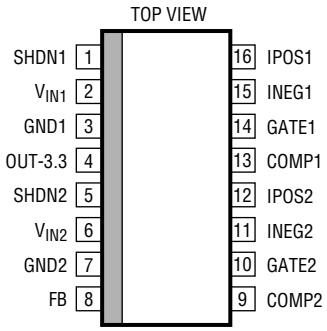



S PACKAGE
16-LEAD PLASTIC NARROW SO

$T_{JMAX}$ = 100°C, $\theta_{JA}$ = 100°C/W

ORDER PART NUMBER

LT1577CS-ADJ/ADJ

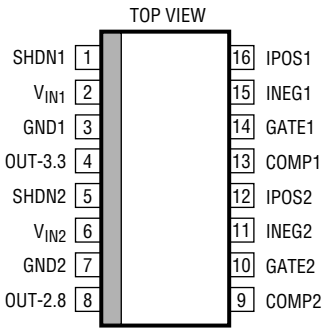



S PACKAGE
16-LEAD PLASTIC NARROW SO

$T_{JMAX}$ = 100°C, $\theta_{JA}$ = 100°C/W

ORDER PART NUMBER

LT1577CS-3.3/ADJ




S PACKAGE
16-LEAD PLASTIC NARROW SO

$T_{JMAX}$ = 100°C, $\theta_{JA}$ = 100°C/W

ORDER PART NUMBER

LT1577CS-3.3/2.8

Consult factory for Industrial and Military grade parts.

## ELECTRICAL CHARACTERISTICS

**$T_A$ = 25°C, $V_{IN}$ = 12V, GATE = 6V, IPOS = INEG = 5V, SHDN = 0.75V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $I_Q$ | Supply Current | | ● | 5 | 12 | 19 | mA |
| $V_{FB}$ | LT1575 Reference Voltage | | <br>● | –0.6<br>–1.0 | 1.210<br>1.210 | 0.6<br>1.0 | %<br>% |
| $V_{OUT}$ | LT1575-1.5 Output Voltage | | <br>● | –0.6<br>–1.0 | 1.500<br>1.500 | 0.6<br>1.0 | %<br>% |
| | LT1575-2.8 Output Voltage | | <br>● | –0.6<br>–1.0 | 2.800<br>2.800 | 0.6<br>1.0 | %<br>% |
| | LT1575-3.3 Output Voltage | | <br>● | –0.6<br>–1.0 | 3.300<br>3.300 | 0.6<br>1.0 | %<br>% |
| | LT1575-3.5 Output Voltage | | <br>● | –0.6<br>–1.0 | 3.500<br>3.500 | 0.6<br>1.0 | %<br>% |
| | LT1575-5 Output Voltage | | <br>● | –0.6<br>–1.0 | 5.000<br>5.000 | 0.6<br>1.0 | %<br>% |
| | Line Regulation | 10V ≤ $V_{IN}$ ≤ 20V | ● | | 0.01 | 0.03 | %/V |
| $I_{FB}$ | FB Input Bias Current | FB = $V_{FB}$ | ● | | –0.6 | –4.0 | µA |
| $I_{OUT}$ | OUT Divider Current | OUT = $V_{OUT}$ | ● | 0.5 | 1.0 | 1.5 | mA |
| $A_{VOL}$ | LT1575 Large-Signal Voltage Gain | $V_{GATE}$ = 3V to 10V | ● | 69 | 84 | | dB |
| | LT1575-1.5 Large-Signal Voltage Gain | $V_{GATE}$ = 3V to 10V | ● | 67 | 82 | | dB |
| | LT1575-2.8 Large-Signal Voltage Gain | $V_{GATE}$ = 3V to 10V | ● | 60 | 76 | | dB |
| | LT1575-3.3 Large-Signal Voltage Gain | $V_{GATE}$ = 3V to 10V | ● | 60 | 75 | | dB |
| | LT1575-3.5 Large-Signal Voltage Gain | $V_{GATE}$ = 3V to 10V | ● | 60 | 74 | | dB |
| | LT1575-5 Large-Signal Voltage Gain | $V_{GATE}$ = 3V to 10V | ● | 56 | 71 | | dB |
| $V_{OL}$ | GATE Output Swing Low (Note 3) | $I_{GATE}$ = 0mA | ● | | 2.5 | 3.0 | V |
| $V_{OH}$ | GATE Output Swing High | $I_{GATE}$ = 0mA | ● | $V_{IN}$ – 1.6 | $V_{IN}$ – 1 | | V |
| | IPOS + INEG Supply Current | 3V ≤ IPOS ≤ 20V | ● | 0.3 | 0.625 | 1.0 | mA |
| | Current Limit Threshold Voltage | | <br>● | 42<br>37 | 50<br>50 | 58<br>63 | mV<br>mV |
| | Current Limit Threshold Voltage Line Regulation | 3V ≤ IPOS ≤ 20V | ● | | –0.20 | –0.50 | %/V |
| | SHDN Sink Current | Current Flows Into Pin | ● | 2.5 | 5.0 | 8.0 | µA |
| | SHDN Source Current | Current Flows Out of Pin | ● | –8 | –15 | –23 | µA |
| | SHDN Low Clamp Voltage | | ● | | 0.1 | 0.25 | V |
| | SHDN High Clamp Voltage | | ● | 1.50 | 1.85 | 2.20 | V |
| | SHDN Threshold Voltage | | ● | 1.18 | 1.21 | 1.240 | V |
| | SHDN Threshold Hysteresis | | ● | 50 | 100 | 150 | mV |

The ● denotes specifications which apply over the full operating temperature range.

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

**Note 2:** $T_J$ is calculated from the ambient temperature $T_A$ and power dissipation $P_D$ according to the following formulas:

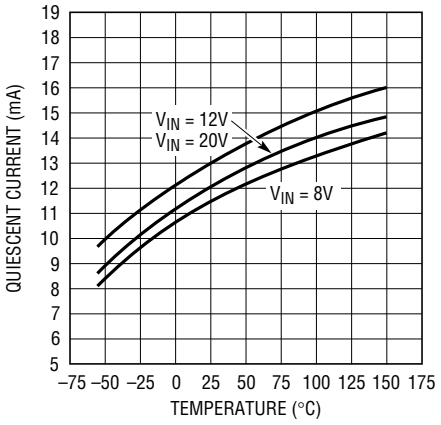
LT1575CN8: $T_J = T_A + (P_D \bullet 100°CW)$
LT1575CS8: $T_J = T_A + (P_D \bullet 130°CW)$
LT1577CS: $T_J = T_A + (P_D \bullet 100°CW)$

Because the LT1577 consists of two regulators in the package, the total LT1577 power dissipation must be used for its junction temperature calculation. The total LT1577 $P_D = P_D$ (Regulator 1) + $P_D$ (Regulator 2).

**Note 3:** The $V_{GS(th)}$ of the external MOSFET must be greater than 3V – $V_{OUT}$.

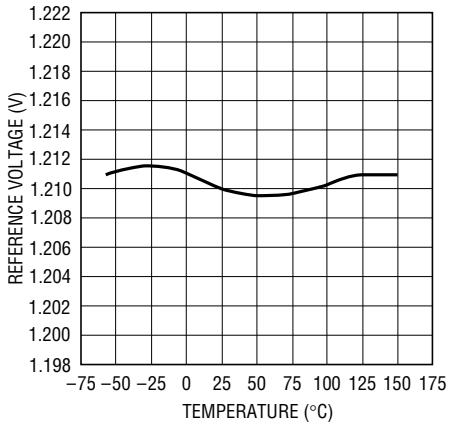
# TYPICAL PERFORMANCE CHARACTERISTICS

### Quiescent Current vs Temperature



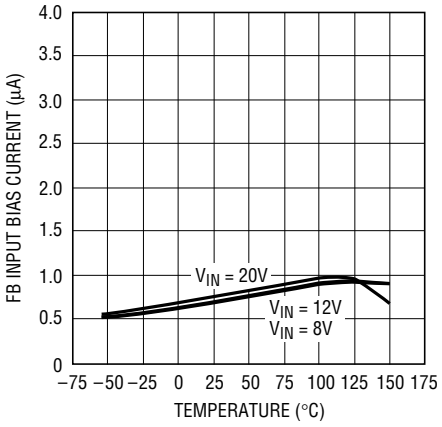

1575/77 G01

### Adjustable LT1575 $V_{REF}$ vs Temperature



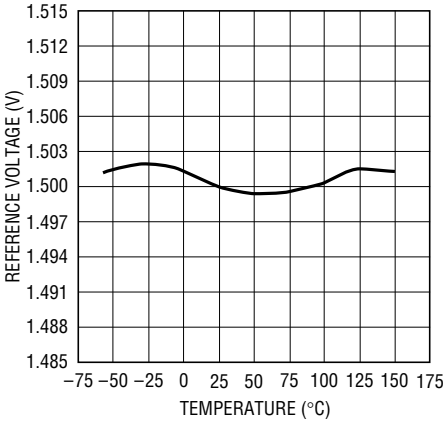

1575/77 G02

### FB Input Bias Current vs Temperature



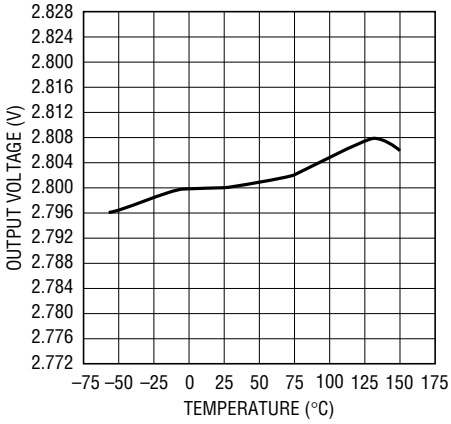

1575/77 G03

### LT1575-1.5 $V_{OUT}$ vs Temperature



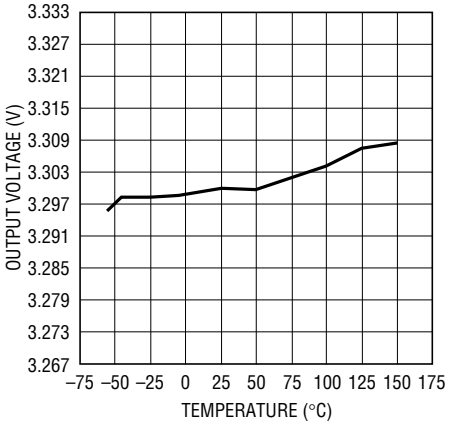

1575/77 G04

### LT1575-2.8 $V_{OUT}$ vs Temperature



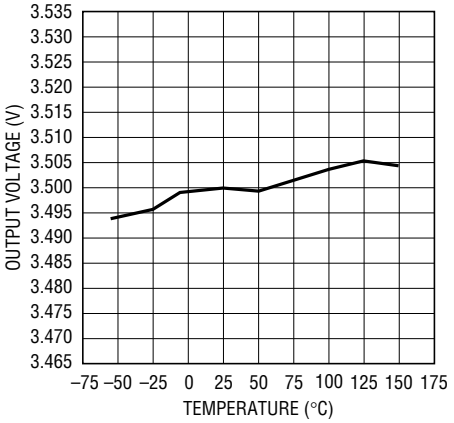

1575/77 G05

### LT1575-3.3 $V_{OUT}$ vs Temperature



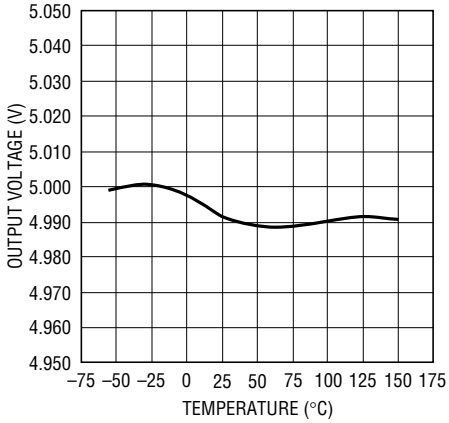

1575/77 G06

### LT1575-3.5 $V_{OUT}$ vs Temperature



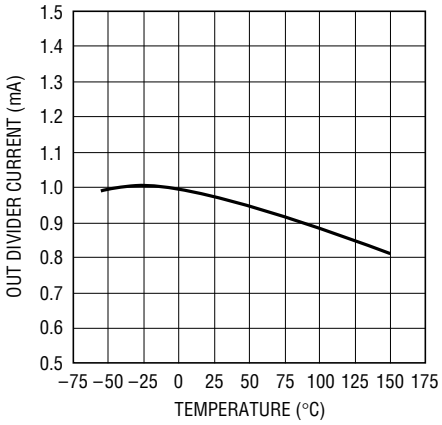

1575/77 G07

### LT1575-5 $V_{OUT}$ vs Temperature




1575/77 G08

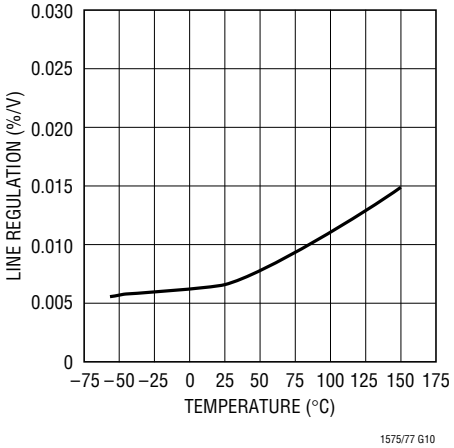
### OUT Divider Current vs Temperature



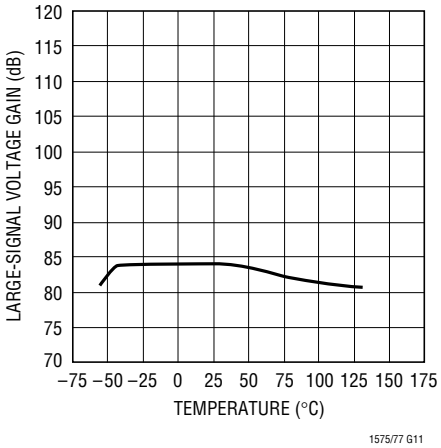

1575/77 G09

# TYPICAL PERFORMANCE CHARACTERISTICS

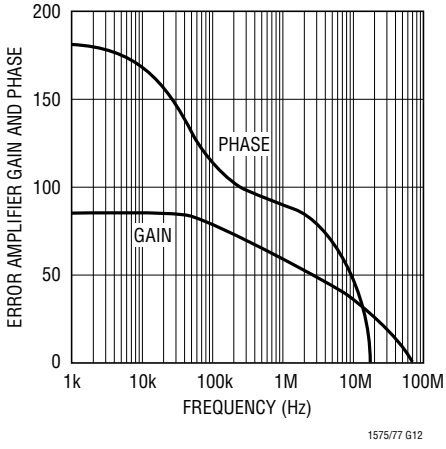
### $V_{REF}/V_{OUT}$ Line Regulation vs Temperature



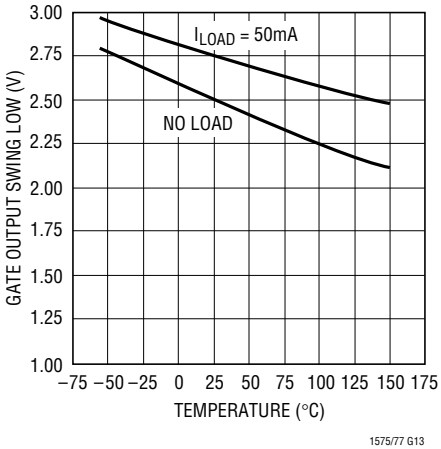

### Error Amplifier Large-Signal Voltage Gain vs Temperature



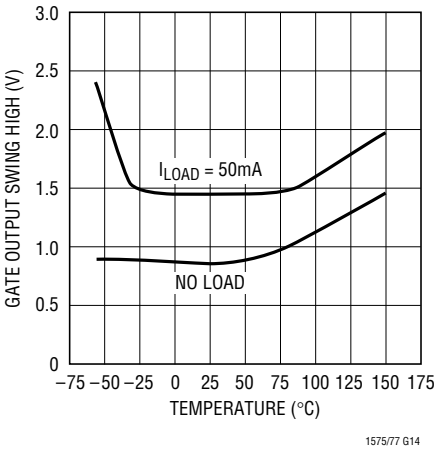

### Gain and Phase vs Frequency



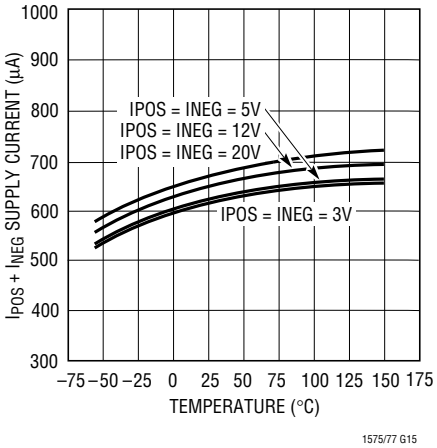

### Gate Output Swing Low vs Temperature



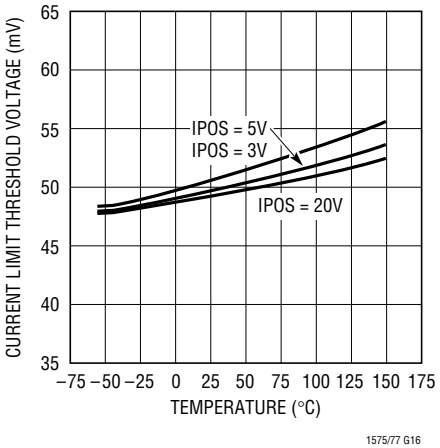

### Gate Output Swing High vs Temperature



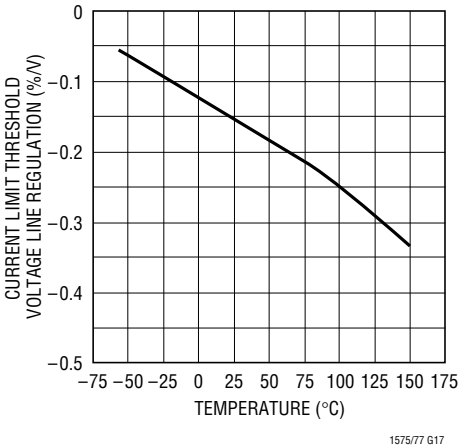

### IPOS + INEG Supply Current vs Temperature




### Current Limit Threshold Voltage vs Temperature

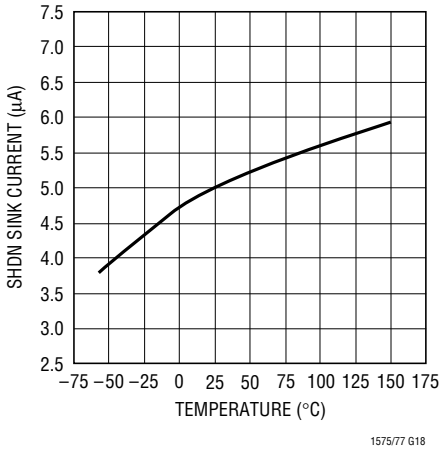



### Current Limit Threshold Voltage Line Regulation vs Temperature

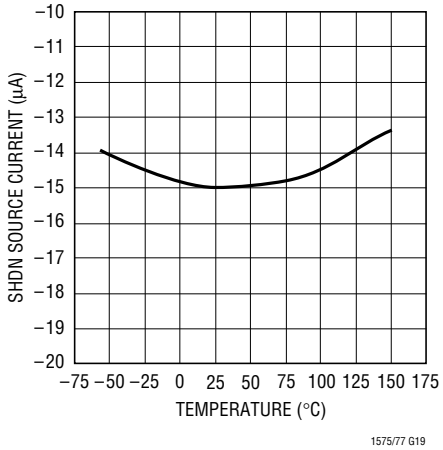


# TYPICAL PERFORMANCE CHARACTERISTICS

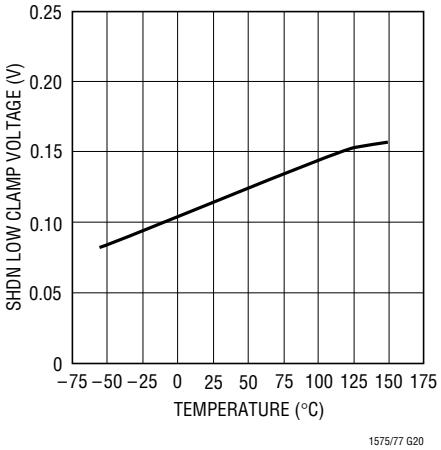
**SHDN Sink Current vs Temperature**



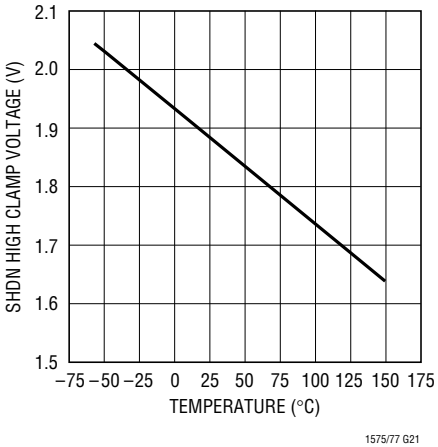

**SHDN Source Current vs Temperature**



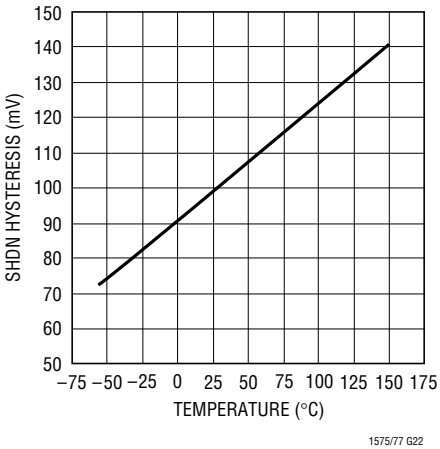

**SHDN Low Clamp Voltage vs Temperature**




**SHDN High Clamp Voltage vs Temperature**




**SHDN Hysteresis vs Temperature**



## PIN FUNCTIONS

**SHDN (Pin 1):** This is a multifunction shutdown pin that provides GATE drive latchoff capability. A 15μA current source, that turns on when current limit is activated, charges a capacitor placed in series with SHDN to GND and performs a current limit time-out function. The pin is also the input to a comparator referenced to $V_{REF}$ (1.21V). When the pin pulls above $V_{REF}$, the comparator latches the gate drive to the external MOSFET off. The comparator typically has 100mV of hysteresis and the Shutdown pin can be pulled low to reset the latchoff function. This pin provides overvoltage protection or thermal shutdown protection when driven from various resistor divider schemes.

**$V_{IN}$ (Pin 2):** This is the input supply for the IC that powers the majority of internal circuitry and provides sufficient gate drive compliance for the external N-channel MOSFET. The typical supply voltage is 12V with 12.5mA of quiescent current. The maximum operating $V_{IN}$ is 20V and the minimum operating $V_{IN}$ is set by $V_{OUT}$ + $V_{GS}$ of the MOSFET at max. $I_{OUT}$ + 1.6V (worst-case $V_{IN}$ to GATE output swing).

**GND (Pin 3):** Analog Ground. This pin is also the negative sense terminal for the internal 1.21V reference. Connect external feedback divider networks that terminate to GND and frequency compensation components that terminate to GND directly to this pin for best regulation and performance.

**FB (Pin 4):** This is the inverting input of the error amplifier for the adjustable voltage LT1575. The noninverting input is tied to the internal 1.21V reference. Input bias current for this pin is typically 0.6μA flowing out of the pin. This pin is normally tied to a resistor divider network to set output voltage. Tie the top of the external resistor divider directly to the output voltage for best regulation performance.

**OUT (Pin 4):** This is the inverting input of the error amplifier for the fixed voltage LT1575. The fixed voltage parts contain a precision resistor divider network to set output voltage. The typical resistor divider current is 1mA into the pin. Tie this pin directly to the output voltage for best regulation performance.

**COMP (Pin 5):** This is the high impedance gain node of the error amplifier and is used for external frequency compensation. The transconductance of the error amplifier is 15 millimhos and open-loop voltage gain is typically 84dB. Frequency compensation is generally performed with a series RC network to ground.

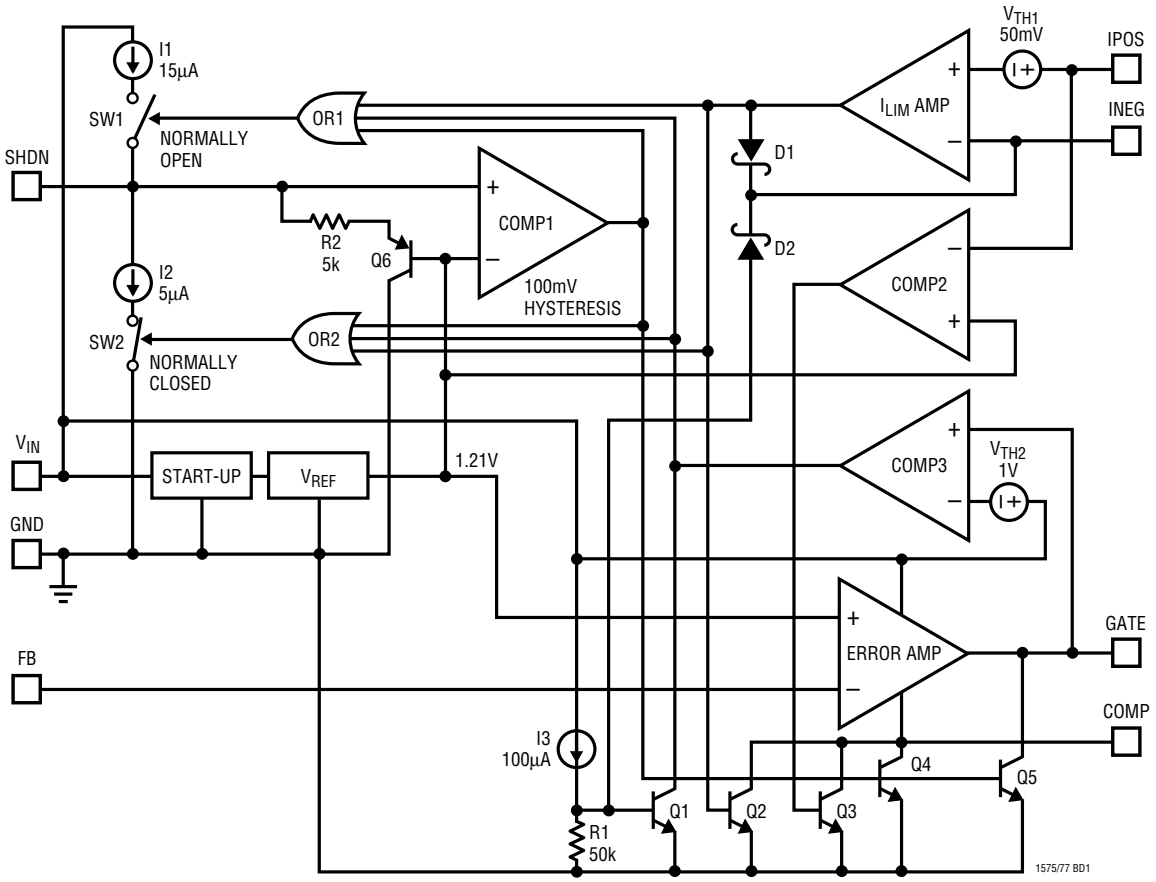
**GATE (Pin 6):** This is the output of the error amplifier that drives N-channel MOSFETs with up to 5000pF of "effective" gate capacitance. The typical open-loop output impedance is 2Ω. When using low input capacitance MOSFETs (<1500pF), a small gate resistor of 2Ω to 10Ω dampens high frequency ringing created by an LC resonance that is created by the MOSFET gate's lead inductance and input capacitance. The GATE pin delivers up to 50mA for a few hundred nanoseconds when slewing the gate of the N-channel MOSFET in response to output load current transients.

**INEG (Pin 7):** This is the negative sense terminal of the current limit amplifier. A small sense resistor is connected in series with the drain of the external MOSFET and is connected between the IPOS and INEG pins. A 50mV threshold voltage in conjunction with the sense resistor value sets the current limit level. The current sense resistor can be a low value shunt or can be made from a piece of PC board trace. If the current limit amplifier is not used, tie the INEG pin to IPOS to defeat current limit. An alternative is to ground the INEG pin. This action disables the current limit amplifier and additional internal circuitry activates the timer circuit on the SHDN pin if the GATE pin swings to the $V_{IN}$ rail. This option provides the user with a "sense-less" current limit function.

**IPOS (Pin 8):** This is the positive sense terminal of the current limit amplifier. Tie this pin directly to the main input voltage from which the output voltage is regulated. The typical input voltage is a 5V logic supply. This pin is also the input to a comparator on the fixed voltage versions that monitors the input/output differential voltage of the external MOSFET. If this differential voltage is less than 0.5V, then the SHDN timer is not allowed to start even if the GATE is at the $V_{IN}$ rail. This allows the regulator to start up normally as the input voltage is ramping up, even with very slow ramp rates.

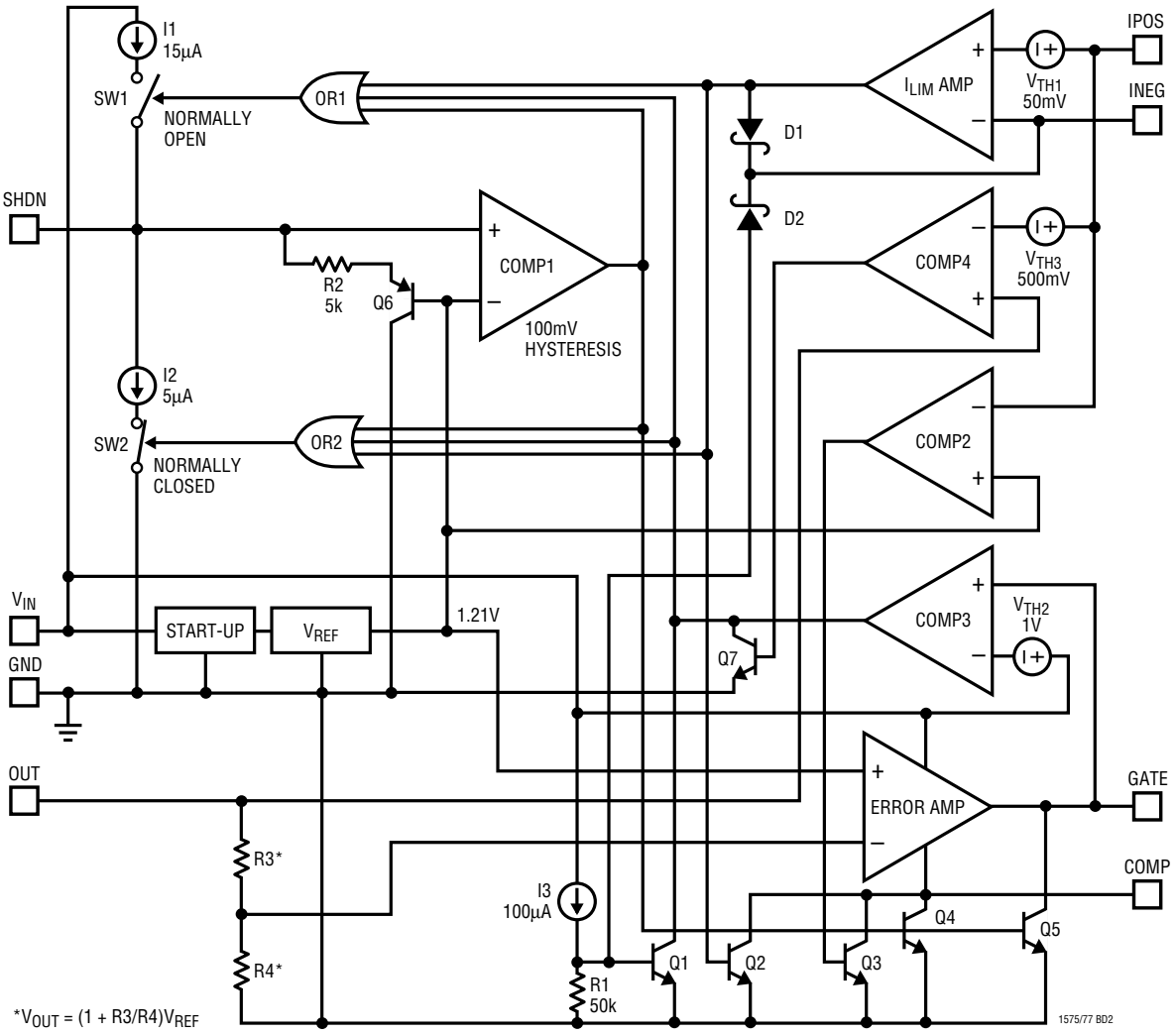
## BLOCK DIAGRAM

**LT1575 Adjustable Voltage**



# BLOCK DIAGRAM

**LT1575 Fixed Voltage**



## APPLICATIONS INFORMATION

### Introduction

The current generation of microprocessors place stringent demands on the power supply that powers the processor core. These microprocessors cycle load current from near zero to amps in tens of nanoseconds. Output voltage tolerances as low as ±100mV include transient response as part of the specification. Some microprocessors require only a single output voltage from which the core and I/O circuitry operate. Other higher performance processors require a separate power supply voltage for the processor core and the I/O circuitry. These requirements mandate the need for very accurate, very high speed regulator circuits.

Previously employed solutions included monolithic 3-terminal linear regulators, PNP transistors driven by low cost control circuits and simple buck converter switching regulators. The 3-terminal regulator achieves a high level of integration, the PNP driven regulator achieves very low dropout performance and the switching regulator achieves high electrical efficiency.

However, the common trait manifested by these solutions is that transient response is measured in many microseconds. This fact translates to a regulator output decoupling capacitor scheme that requires several hundred microfarads of very low ESR bulk capacitance using multiple capacitors surrounding the CPU. This required bulk capacitance is in addition to the ceramic decoupling capacitor network that handles the transient load response during the first few hundred nanoseconds as well as providing microprocessor clock frequency noise immunity. The combined cost of all capacitors is a significant percentage of the total power supply cost.

The LT1575/LT1577 family of single/dual controller ICs are unique, easy to use devices that drive external N-channel MOSFETs as source followers and permit a user to realize an extremely low dropout, ultrafast transient response regulator. These circuits achieve superior regulator bandwidth and transient load performance by completely eliminating expensive tantalum or bulk electrolytic capacitors in the most modern and demanding microprocessor applications. For example, a 200MHz Pentium processor can operate with only the recommended 24 1µF ceramic capacitors. Users benefit directly by saving significant cost as all additional bulk capacitance is removed. The additional savings of insertion cost, purchasing/inventory cost and board space are readily apparent.

Precision-trimmed adjustable and fixed output voltage versions accommodate any required microprocessor power supply voltage. Proper selection of the N-channel MOSFET $R_{DS(ON)}$ allows user-settable dropout voltage performance. The only output capacitors required are the high frequency ceramic decoupling capacitors. This regulator design provides ample bandwidth and responds to transient load changes in a few hundred nanoseconds versus regulators that respond in many microseconds. The ceramic capacitor network generally consists of 10 to 24 1uF capacitors for individual microprocessor requirements. The LT1575/LT1577 family also incorporates current limiting for no additional system cost, provides on/off control and overvoltage protection or thermal shutdown with simple external components.

Therefore, the unique design of these new ICs combines the benefits of low dropout voltage, high functional integration, precision performance and ultrafast transient response, as well as providing significant cost savings on the output capacitance needed in fast load transient applications. As lower input/output differential voltage applications become increasingly prevalent, an LT1575-based solution achieves comparable efficiency performance with a switching regulator at an appreciable cost savings.

The new LT1575/LT1577 family of low dropout regulator controller ICs step to the next level of performance required by system designers for the latest generation motherboards and microprocessors. The simple versatility and benefits derived from these circuits allow the power supply needs of today's high performance microprocessors to be met with ease.

### Block Diagram Operation

The primary block diagram elements consist of a simple feedback control loop and the secondary block diagram elements consist of multiple protection functions. Examining the block diagram for the LT1575, a start-up circuit provides controlled start-up for the IC, including the precision-trimmed bandgap reference, and establishes all internal current and voltage biasing.

## APPLICATIONS INFORMATION

Reference voltage accuracy for the adjustable version and output voltage accuracy for the fixed voltage versions are specified as ±0.6% at room temperature and as ±1% over the full operating temperature range. This places the LT1575/LT1577 family among a select group of regulators with a very tightly specified output voltage tolerance. The accurate 1.21V reference is tied to the noninverting input of the main error amplifier in the feedback control loop.

The error amplifier consists of a single high gain $g_m$ stage with a transconductance equal to 15 millimhos. The inverting terminal is brought out as the FB pin in the adjustable voltage version and as the OUT pin in fixed voltage versions. The $g_m$ stage provides differential-to-single ended conversion at the COMP pin. The output impedance of the $g_m$ stage is about 1MΩ and thus, 84dB of typical DC error amplifier open-loop gain is realized along with a typical 75MHz uncompensated unity-gain crossover frequency. Note that the overall feedback loop's DC gain decreases from the gain provided by the error amplifier by the attenuation factor in the resistor divider network which sets the DC output voltage. These attenuation factors are already built into the Open-Loop Voltage Gain specifications for the LT1575 fixed voltage versions in the Electrical Characteristics table to simplify user calculations. External access to the high impedance gain node of the error amplifier permits typical loop compensation to be accomplished with a series RC network to ground.

A high speed, high current output stage buffers the COMP node and drives up to 5000pF of "effective" MOSFET gate capacitance with almost no change in load transient performance. The output stage delivers up to 50mA peak when slewing the MOSFET gate in response to load current transients. The typical output impedance of the GATE pin is typically 2Ω. This pushes the pole due to the error amplifier output impedance and the MOSFET input capacitance well beyond the loop crossover frequency. If the capacitance of the MOSFET used is less than 1500pF, it may be necessary to add a small value series gate resistor of 2Ω to 10Ω. This gate resistor helps damp the LC resonance created by the MOSFET gate's lead inductance and input capacitance. In addition, the pole formed by this resistance and the MOSFET input capacitance can be fine tuned.

Because the MOSFET pass transistor is connected as a source follower, the power path gain is much more predictable than designs that employ a discrete PNP transistor as the pass device. This is due to the significant production variations encountered with PNP Beta. MOSFETs are also very high speed devices which enhance the ability to produce a stable wide bandwidth control loop. An additional advantage of the follower topology is inherently good line rejection. Input supply disturbances do not propagate through to the output. The feedback loop for a regulator circuit is completed by providing an error signal to the FB pin in the adjustable voltage version and the OUT pin in the fixed voltage version. In both cases, a resistor divider network senses the output voltage and sets the regulated DC bias point. In general, the LT1575 regulator feedback loop permits a loop crossover frequency on the order of 1MHz while maintaining good phase and gain margins. This unity-gain frequency is a factor of 20 to 30 times the bandwidth of currently implemented regulator solutions for microprocessor power supplies. This significant performance benefit is what permits the elimination of all bulk output capacitance.

Several other unique features are included in the design that increase its functionality and robustness. These functions comprise the remainder of the block diagram.

A high side sense, current limit amplifier provides active current limiting for the regulator. The current limit amplifier uses an external low value shunt resistor connected in series with the external MOSFET's drain. This resistor can be a discrete shunt resistor or can be manufactured from a Kelvin-sensed section of "free" PC board trace. All load current flows through the MOSFET drain and thus, through the sense resistor. The advantage of using high side current sensing in this topology is that the MOSFET's gain and the main feedback loop's gain remain unaffected. The sense resistor develops a voltage equal to $I_{OUT}(R_{SENSE})$. The current limit amplifier's 50mV threshold voltage is a good compromise between power dissipation in the sense resistor, dropout voltage impact and noise immunity. Current limit activates when the sense resistor voltage equals the 50mV threshold.

Two events occur when current limit activates: the first is that the current limit amplifier drives Q2 in the block

## APPLICATIONS INFORMATION

diagram and clamps the positive swing of the COMP node in the main error amplifier to a voltage that provides an output load current of 50mV/$R_{SENSE}$. This action continues as long as the output current overload persists. The second event is that a timer circuit activates at the SHDN pin. This pin is normally held low by a 5μA active pull-down that limits to ≈ 100mV above ground. When current limit activates, the 5μA pull-down turns off and a 15μA pull-up current source turns on. Placing a capacitor in series with the SHDN pin to ground generates a programmable time ramp voltage.

The SHDN pin is also the positive input of COMP1. The negative input is tied to the internal 1.21V reference. When the SHDN pin ramps above $V_{REF}$, the comparator drives Q4 and Q5. This action pulls the COMP and GATE pins low and latches the external MOSFET drive off. This condition reduces the MOSFET power dissipation to zero. The time period until the latched-off condition occurs is typically equal to $C_{SHUT}$(1.11V)/15μA. For example, a 1μF capacitor on the SHDN pin yields a 74ms ramp time. In short, this unique circuit block performs a current limit time-out function that latches off the regulator drive after a predefined time period. The time-out period selected is a function of system requirements including start-up and safe operating area. The SHDN pin is internally clamped to typically 1.85V by Q6 and R2. The comparator tied to the SHDN pin has 100mV of typical hysteresis to provide noise immunity. The hysteresis is especially useful when using the SHDN pin for thermal shutdown.

Restoring normal operation after the load current fault is cleared is accomplished in two ways. One option is to recycle the nominal 12V LT1575 supply voltage as long as an external bleed path for the Shutdown pin capacitor is provided. The second option is to provide an active reset circuit that pulls the SHDN pin below $V_{REF}$. Pulling the SHDN pin below $V_{REF}$ turns off the 15μA pull-up current source and reactivates the 5μA pull-down. If the SHDN pin is held below $V_{REF}$ during a fault condition, the regulator continues to operate in current limit into a short. This action requires being able to sink 15μA from the SHDN pin at less than 1V. The 5μA pull-down current source and the 15μA pull-up current source are designed low enough in value so that an external resistor divider network can drive the SHDN pin to provide overvoltage protection or to provide thermal shutdown with the use of a thermistor in the divider network. Diode-ORing these functions together is simple to accomplish and provides multiple functionality for one pin.

If the current limit amplifier is not used, two choices present themselves. The simplest choice is to tie the INEG pin directly to the IPOS pin. This action defeats current limit and provides the simplest, no frills circuit. An application in which the current limit amplifier is not used is where an extremely low dropout voltage must be achieved and the 50mV threshold voltage cannot be tolerated.

However, a second available choice permits a user to provide short-circuit protection with no external sensing. This technique is activated by grounding the INEG pin. This action disables the current limit amplifier because Schottky diode D1 clamps the amplifier's output and prevents Q2 from pulling down the COMP node. In addition, Schottky diode D2 turns off pull-down transistor Q1. Q1 is normally on and holds internal comparator COMP3's output low. This comparator circuit, now enabled, monitors the GATE pin and detects saturation at the positive rail. When a saturated condition is detected, COMP3 activates the shutdown timer. Once the time-out period occurs, the output is shut down and latched off. The operation of resetting the latch remains the same. Note that this technique does not limit the FET current during the time-out period. The output current is only limited by the input power supply and the input/output impedance. Setting the timer to a short period in this mode of operation keeps the external MOSFET within its SOA (safe operating area) boundary and keeps the MOSFET's temperature rise under control.

Unique circuit design incorporated into the LT1575 alleviates all concerns about power supply sequencing. The issue of power supply sequencing is an important topic as the typical LT1575 application has inputs from two separate power supply voltages. If the typical 12V $V_{IN}$ supply voltage is slow in ramping up, insufficient MOSFET gate drive is present and therefore, the output voltage does not come up. If the $V_{IN}$ supply voltage is present, but the typical 5V supply voltage tied to the IPOS pin has not started yet, then the feedback loop wants to drive the GATE pin to the positive $V_{IN}$ rail. This would result in a

## APPLICATIONS INFORMATION

very large current spike as soon as the 5V supply started to ramp up. However, undervoltage lockout circuit COMP2, which monitors the IPOS supply voltage, holds Q3 on and pulls the COMP pin low until the IPOS voltage increases to greater than the internal 1.21 reference voltage. The undervoltage lockout circuit then smoothly releases the COMP pin and allows the output voltage to come up in dropout from the input supply voltage. An additional benefit derived from the speed of the LT1575 feedback loop is that turn-on overshoot is virtually nonexistent in a properly compensated system.

An additional circuit feature is built-in to the LT1575 fixed voltage versions. When the regulator circuit starts up, it must charge up the output capacitors. The output voltage typically tracks the input voltage supply as it ramps up with the difference in input/output voltage defined by the dropout voltage. Until the feedback loop comes into regulation, the circuit operation results in the GATE pin being at the positive $V_{IN}$ rail, which starts the timer at the SHDN pin if the current limit amplifier is disabled. However, internal comparator COMP4 monitors the input/output voltage differential. This comparator does not permit the shutdown timer to start until the differential voltage is greater than 500mV. This permits normal start-up to occur.

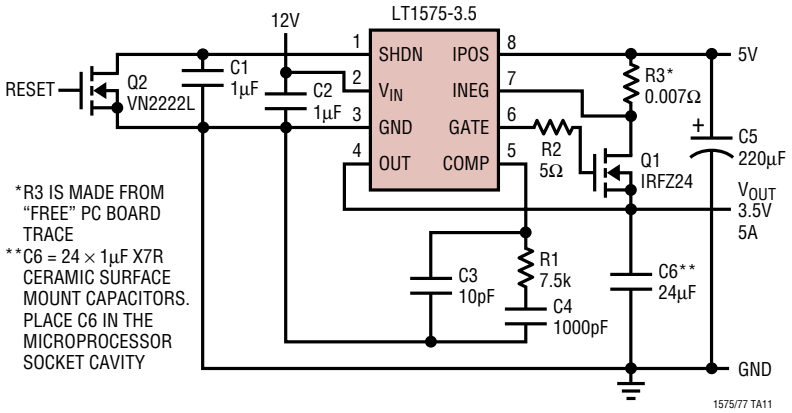
One final benefit is derived in using an LT1575 fixed voltage version. Today's highest performance microprocessors dictate that precision resistors must be used with currently available adjustable voltage regulators to meet the initial set point tolerance. The LT1575 fixed voltage versions incorporate the precision resistor divider into the IC and still maintain a 1% output voltage tolerance over temperature. Thus, the LT1575 fixed voltage versions completely eliminate the requirement for precision resistors and this results in additional system cost savings.

### Applications Support

Linear Technology invests an enormous amount of time, resources and technical expertise in understanding, designing and evaluating microprocessor power supply solutions for system designers. As processor speeds and power increase, the power supply challenges presented to the motherboard designer increase as well. Application Note 69, "Using the LT1575 Linear Regulator Controller," has been written and serves as an extremely useful guide for this new family of ICs. This Application Note covers topics including PC board layout for the LT1575/LT1577 family, MOSFET selection criteria, external component selection (capacitors) and loop compensation. Linear Technology welcomes the opportunity to discuss, design, evaluate and optimize a microprocessor power supply solution with a customer. For additional information, consult the factory.

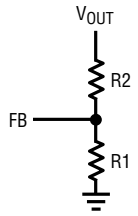
## TYPICAL APPLICATIONS

**UltraFast Transient Response 5V to 3.5V Low Dropout Regulator with Current Limit and Timer Latchoff**



# TYPICAL APPLICATIONS

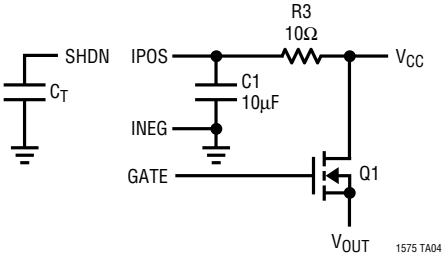
### Setting Output Voltage with the Adjustable LT1575




$V_{OUT} = 1.21V(1 + R2/R1)$

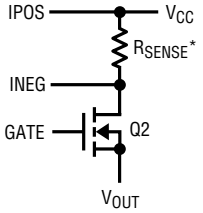
1575 TA03

### Using "Sense-Less" Current Limit




1575 TA04

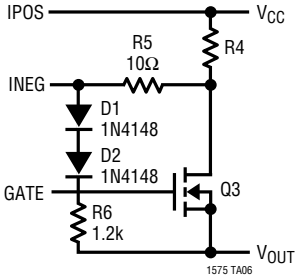
### Setting Current Limit




$^*I_{LIM} = 50mV/R_{SENSE}$
$R_{SENSE}$ = DISCRETE SHUNT RESISTOR OR
$R_{SENSE}$ = KELVIN-SENSED PC BOARD TRACE
ACTIVATING CURRENT LIMIT ALSO ACTIVATES THE SHDN PIN TIMER

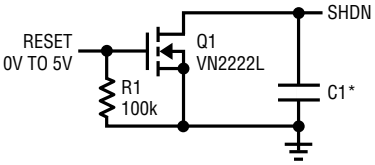
1575 TA05

### Setting Current Limit with Foldback Limiting




1575 TA06

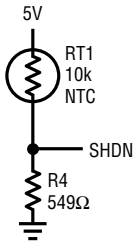
### Shutdown Time-Out with Reset




*C1 = 15µA(t)/1.11V
t = SHUDOWN LATCHOFF TIME

1575 TA07

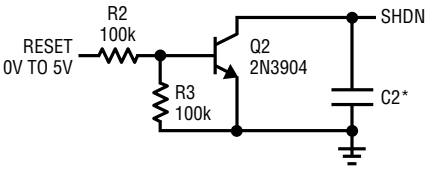
### Basic Thermal Shutdown




RT1 = DALE NTHS-1206N02 THERMALLY MOUNT RT1 IN CLOSE PROXIMITY TO THE EXTERNAL N-CHANNEL MOSFET

1575 TA08

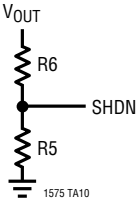
### Shutdown Time-Out with Reset




*C2 = 15µA(t)/1.11V
t = SHUTDOWN LATCH-OFF TIME

1575 TA09

### Overvoltage Protection

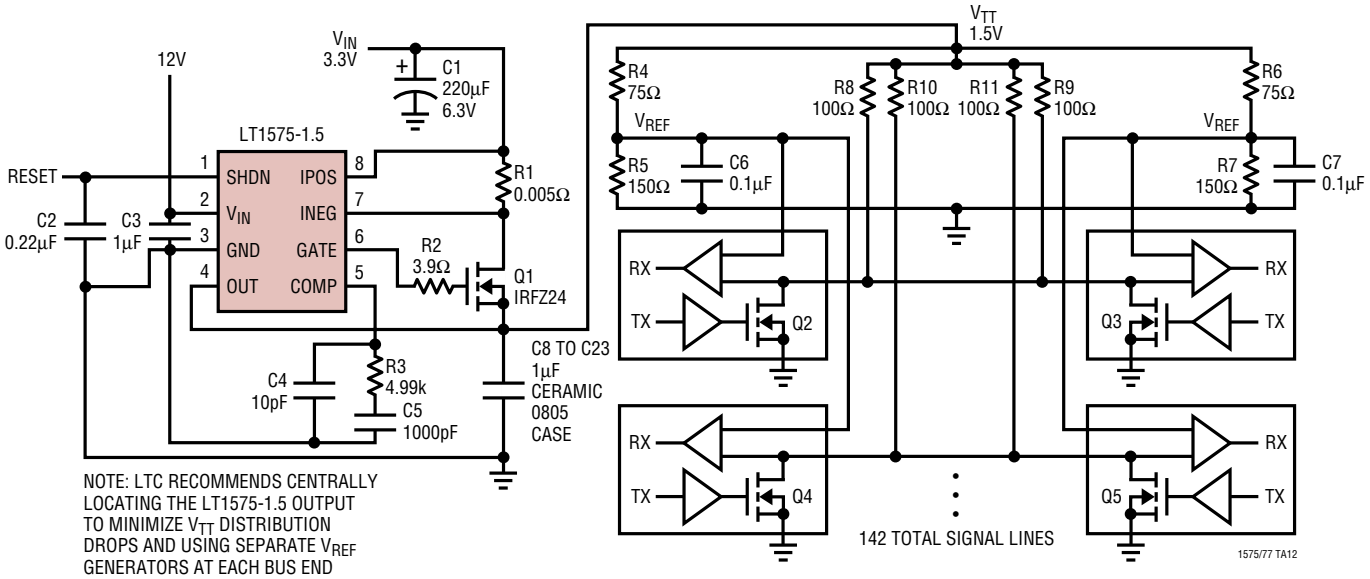



1575 TA10

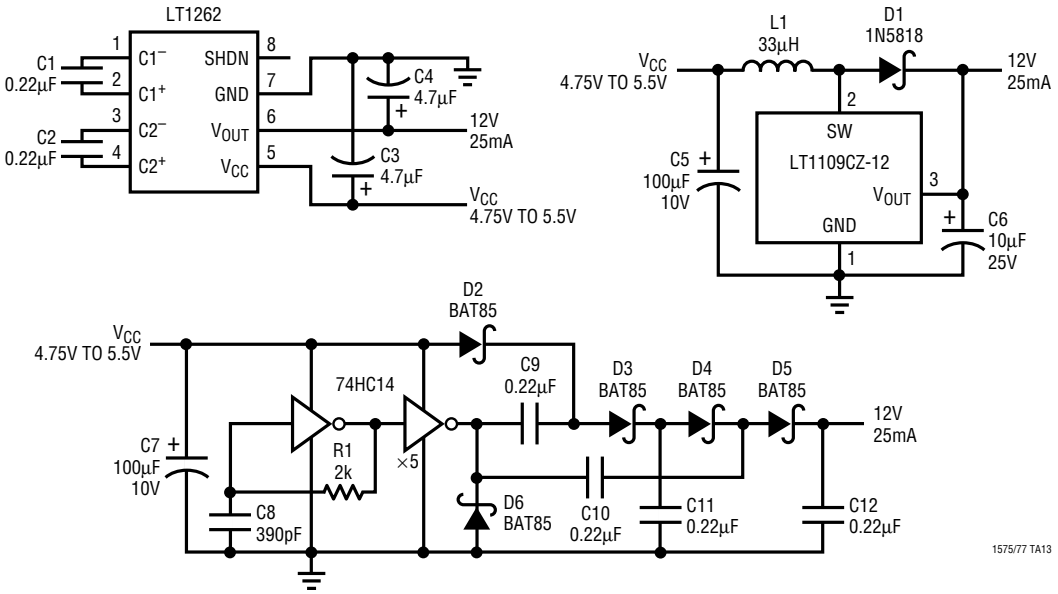
$V_{OUT(uth)} = 1.21(R6/R5) + 5\mu A(R6)$
$V_{OUT(lth)} = 1.11(R6/R5) - 15\mu A(R6)$

# TYPICAL APPLICATIONS

**Pentium® II Processor GTL+ Power Supply**



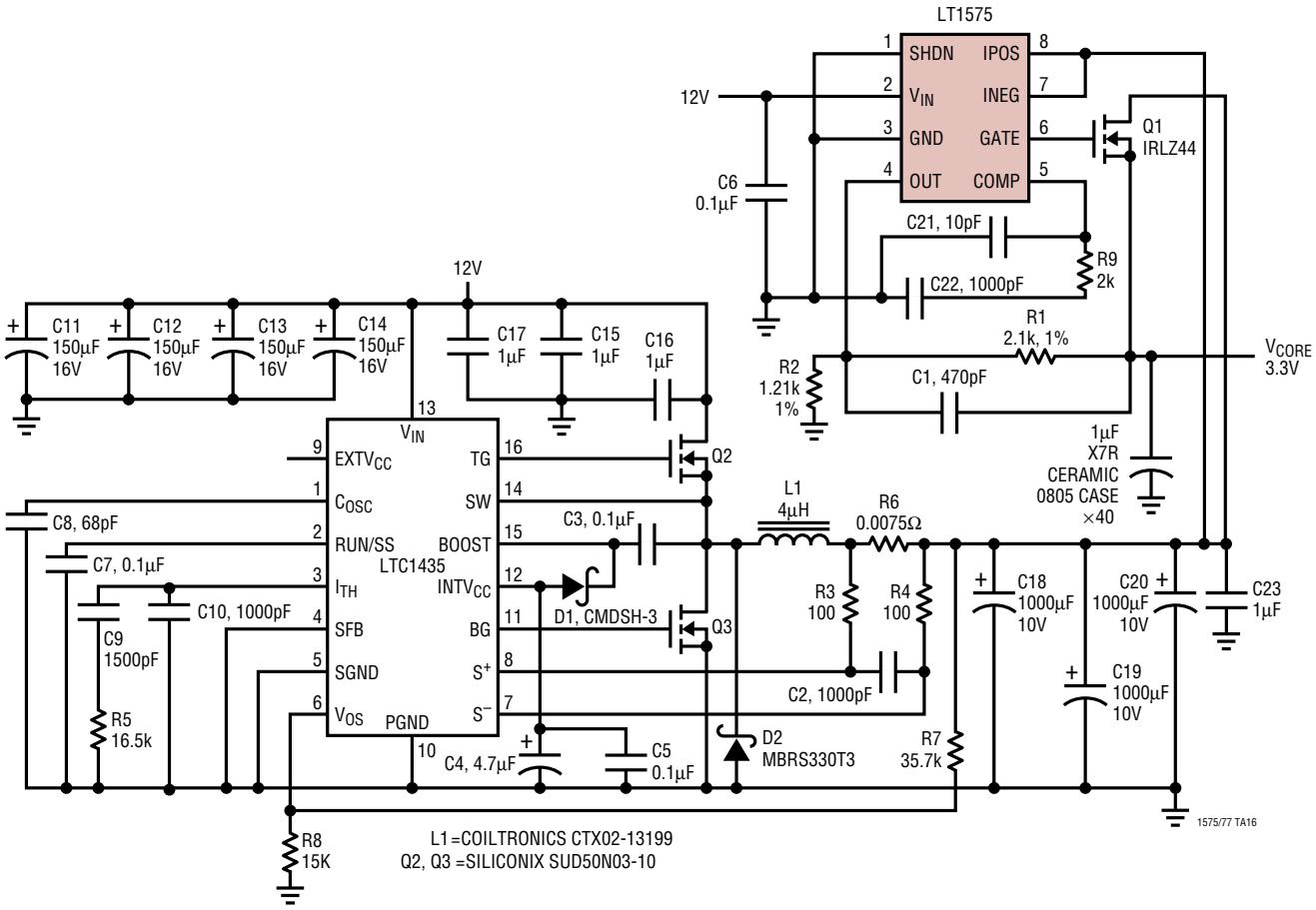

**Generating 12V Gate Drive from a 5V Power Supply**



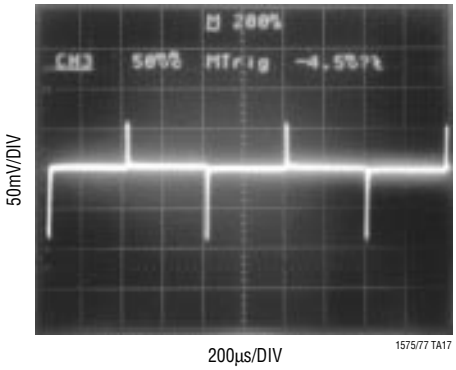

Pentium is a registered trademark of Intel Corporation.

## TYPICAL APPLICATIONS

**12V to 3.3V/9A (14A Peak) Hybrid Regulator**

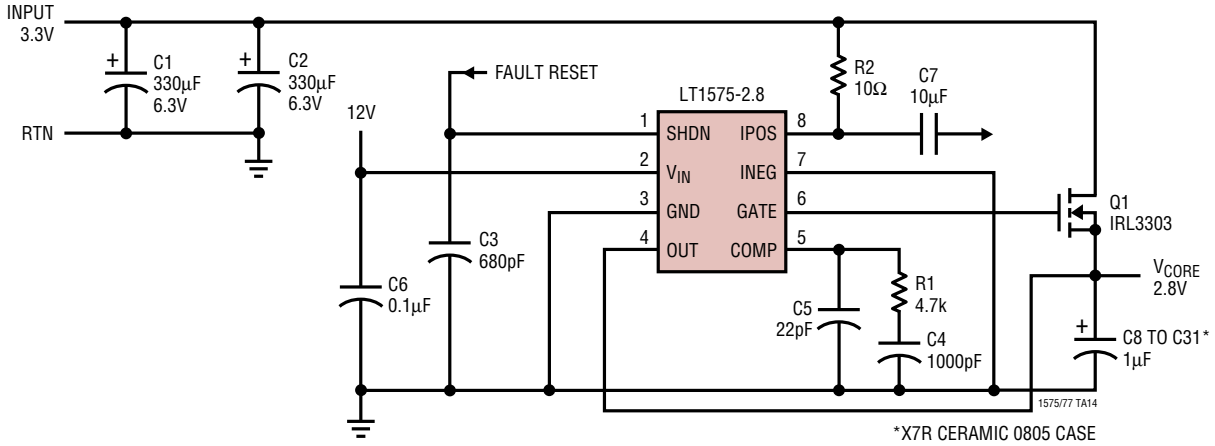



**Transient Response to a 10A Load Step**



# TYPICAL APPLICATIONS

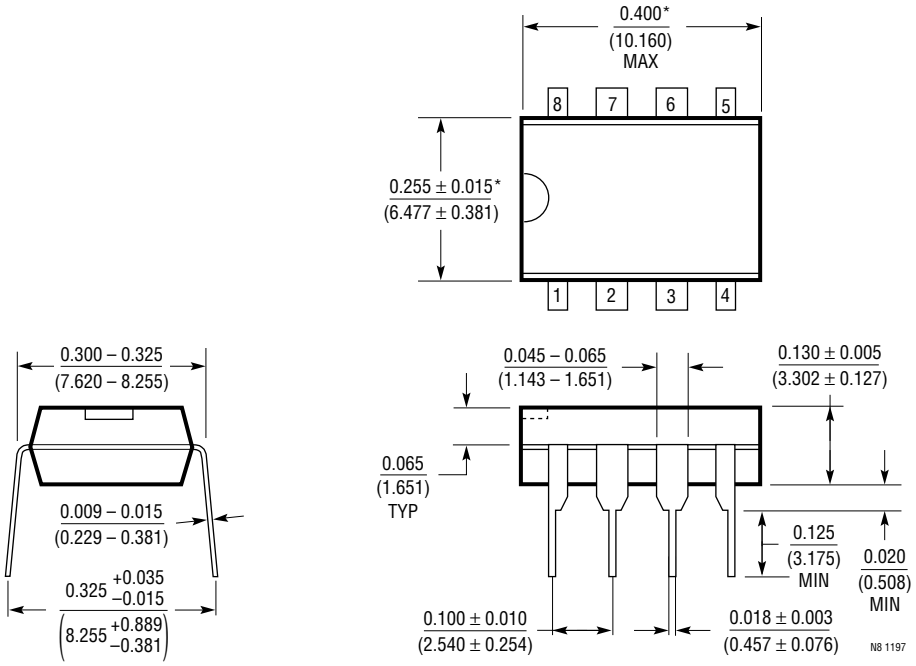
**3.3V to 2.8V ±100mV at 5.7A with Sense-Less Current Limit and Timer Latchoff**




# PACKAGE DESCRIPTION

**Dimensions in inches (millimeters) unless otherwise noted.**

**N8 Package**
**8-Lead PDIP (Narrow 0.300)**
(LTC DWG # 05-08-1510)

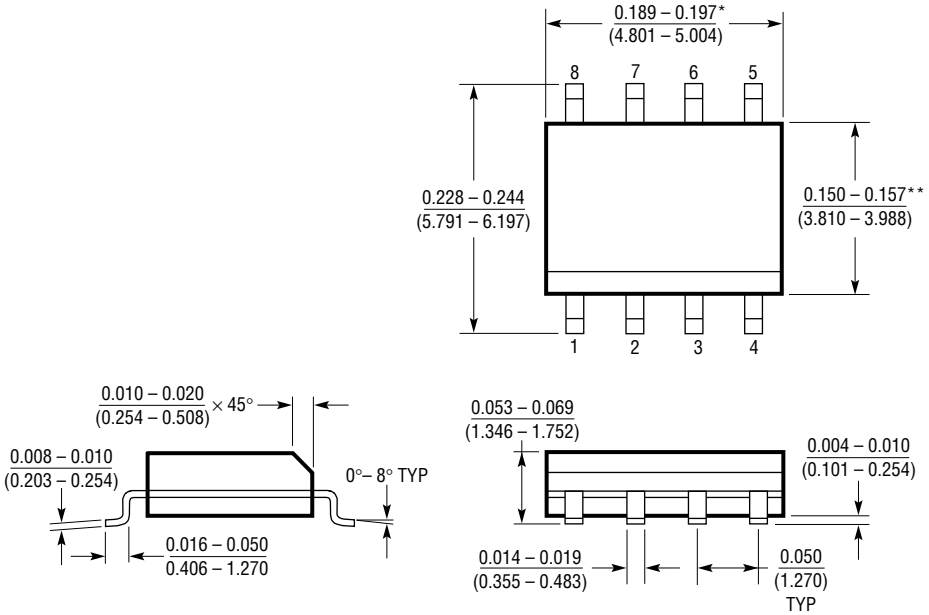



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

## PACKAGE DESCRIPTION

**Dimensions in inches (millimeters) unless otherwise noted.**

**S8 Package**
**8-Lead Plastic Small Outline (Narrow 0.150)**
(LTC DWG # 05-08-1610)




*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

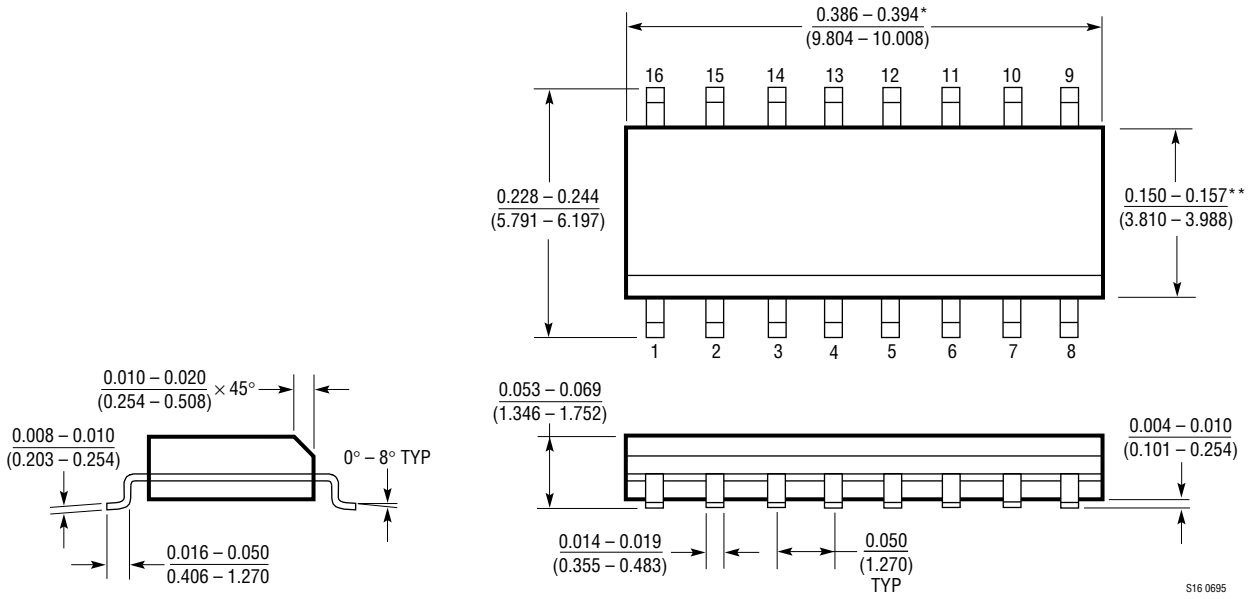
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SO8 0996

## PACKAGE DESCRIPTION

**Dimensions in inches (millimeters) unless otherwise noted.**

**S Package**
**16-Lead Plastic Small Outline (Narrow 0.150)**
(LTC DWG # 05-08-1610)



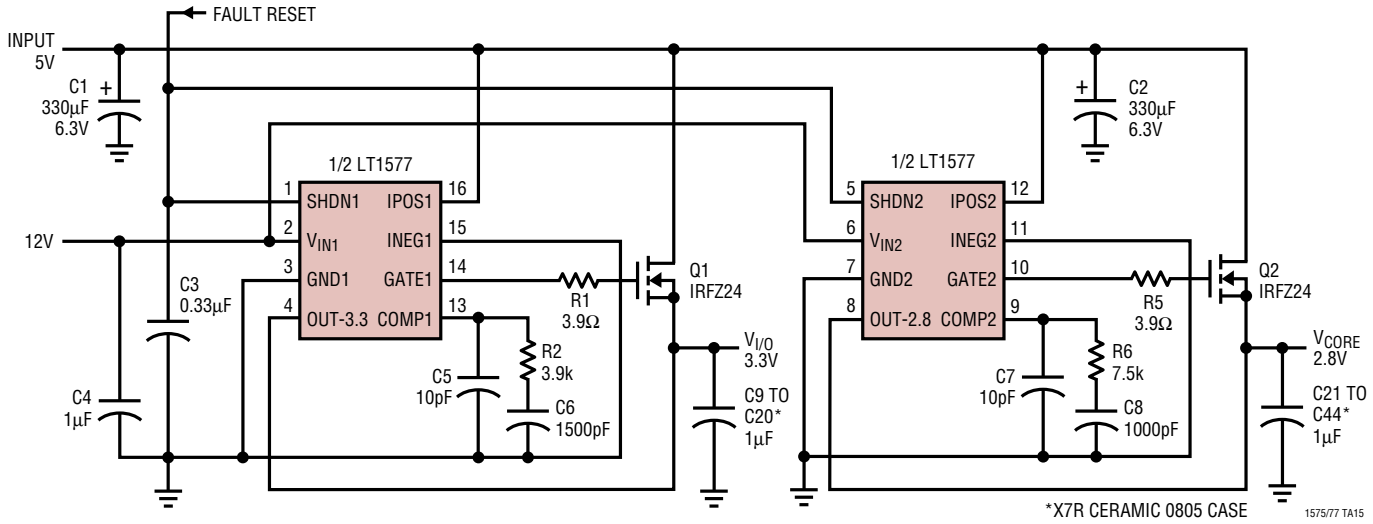

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

## TYPICAL APPLICATION

**LT1577 Split Plane System**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1266 | Current Mode, Step-Up/Down Switching Regulator Controller | Synchronous N- or P-Channel FETs, Comparator/Low Battery Detector |
| LTC1392 | Micropower Temperature, Power Supply and Differential Voltage Monitor | Temperature to Bits Control |
| LTC1430 | High Power Step-Down Switching Regulator Controller | Voltage Mode, 5V to 3.xxV at >10A |
| LTC1435 | High Efficiency, Low Noise Synchronous Step-Down Switching Regulator | Current Mode with Wide Input Voltage Range |
| LTC1553 | Digitally Controlled Synchronous Switching Regulator Controller | Controller for Pentium II Processor, Buck Conversion from 5V or 12V Main Power |
| LTC1553L | Digitally Controlled Synchronous Switching Regulator Controller | Controller for Pentium II Processor, Buck Conversion from 5V Main Power |
| LT1573 | Low Dropout Regulator Driver | Drives Low Cost PNP Transistor for High Power, Low Dropout Applications |
| LT1580 | 7A, Very Low Dropout Linear Regulator | 0.54V Dropout at 7A, Fixed 2.5$V_{OUT}$ and Adjustable |
| LT1585-1.5 | Fixed 1.5V, 5A Low Dropout Fast Response Regulator | GTL+ Regulator |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