FOUR-CHANNEL IMAGE SENSOR ANALOG FRONT-END

Check for Samples: VSP7500, VSP7502

FEATURES

- **Four-Channel Signal Paths**
  - **VSP7500: Supports CDS Input**
  - **VSP7502: Supports SH Input**
- **Maximum Data Throughput: 56 MHz**
- **Dual Inputs for Each Signal Path**
- **16-Bit A/D Conversion:**
  - **No Missing Codes Ensured**
- **Programmable Gain Amplifier (PGA):**
  - **Analog Front Gain: 0 dB to +9.6 dB (0.28-dB Step)**
  - **Digital Gain: 0 dB to +32 dB (0.032-dB Step)**
- **Wide Range of Input Common Voltage**
- **Operation Voltage and Power Consumption:**
  - **Voltage: 1.65 V to 1.95 V and 2.7 V to 3.6 V**
- **Power: 400 mW (at VDD = 1.8 V, f_{MCLK} = 50 MHz)**

APPLICATIONS

- **Digital Video Cameras (DVCs)**
- **Digital Still Cameras (DSCs)**
- **Front End for Multichannel Sensors**
- **High-Speed Machine Vision**
- **High-Resolution Surveillance Cameras**
- **High-Speed/High-Resolution Scanners**
- **Medical**

DESCRIPTION

The VSP7500/VSP7502 are four-channel analog front-ends (AFEs) for imaging signals. These devices include a correlated double sampler (CDS), programmable gain amplifier (PGA), analog-to-digital converter (ADC), input clamp, optical black (OB) level clamp loop, serial interface, and adjustable sampling timing control. The VSP7502 provides the same functionality with a sample/hold (S/H) mode to support CMOS and CIS sensors. The VSP7500/VSP7502 are offered in a BGA-159 package.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUATITY
VSP7500	BGA-159	ZWV	–25°C to +85°C	VSP7500ZWV	VSP7500ZWV	Tray, 360
					VSP7500ZWVR	Tape and Reel, 3000
VSP7502	BGA-159	ZWV	–25°C to +85°C	VSP7502ZWV	VSP7502ZWV	Tray, 360
					VSP7502ZWVR	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	VSP7500, VSP7502	UNIT
Supply voltage (AVDD2, DLLVDD2, REFVDD, DRVDD2, DVDD2, DVDD2_SPI)	2.4	V
Supply voltage (AVDD3, RGVDD3, H1VDD3, H2VDD3, DVDD3, DVDD3_SPI)	4	V
Supply voltage differences (among power-supply pins)	±0.1	V
Ground voltage differences (among GND pins)	±0.1	V
Digital input voltage (ATPG, MN_DM, MN_KBLK, MN_OB, MN_PBLK)	–0.15 to (DVDD2 + 0.15)	V
Digital input voltage (HD, VD, MCLK, RST, SCLK, SCS, SDI)	–0.3 to (DVDD3 + 0.3)	V
Analog input voltage (IN_W, IN_X, IN_Y, IN_Z, IP_W, IP_X, IP_Y, IP_Z)	–0.3 to (AVDD3 + 0.3)	V
Input current (all pins except supplies)	±10	mA
Ambient temperature under bias	–40 to +125	°C
Storage temperature	–55 to +150	°C
Junction temperature	+150	°C
Package temperature (reflow, peak)	+260	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

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ELECTRICAL CHARACTERISTICS(1)

All specifications at T_A = +25°C, all power-supply voltages = +3 V, and conversion rate = 36 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP7500, VSP7502			UNIT
			MIN	TYP	MAX	
POWER SUPPLY						
Analog supply voltage	AVDD2		1.65	1.8	1.95	V
	REFVDD					
	DLLVDD2					
	LVAVDD					
	LVDLLVDD					
	AVDD3		2.7	3	3.6	V
Digital supply voltage	DVDD2		1.65	1.8	1.95	V
	DVDD2_SPI					
	DRVDD2					
	DVDD2_SPI					
	LVDVDD					
	DRVDD2					
	DVDD3		2.7	3	3.6	V
	DVDD3_SPI					
H-TG supply voltage	HVDD3		2.7	3	3.6	V
Power dissipation		VDD = typ, f_{MCLK} = 50MHz		400		mW
		Power-down mode (f_{MCLK} = 0 MHz)		10		mW
RESOLUTION						
Resolution				16		Bits
THROUGHPUT RATE						
Maximum data throughput rate				50	56	MHz
SIGNAL PATHS						
Signal paths		VCC = 3 V		4		Channels
DIGITAL INPUTS						
Logic family				CMOS		
I_{IH}	Input current	Logic high, V_{IN} = +1.8 V			1	µA
I_{IL}		Logic low, V_{IN} = 0 V			1	µA
MCLK clock duty cycle			40	50	60	%
Input capacitance				5		pF
DIGITAL OUTPUT (CMOS Buffer RG, H1, H2, LH)						
V_{OH}	Output voltage	Logic high, I_{OH} = –2 mA	VDD – 0.3			V
V_{OL}		Logic low, I_{OL} = 2 mA			VDD + 0.3	V
ANALOG INPUT						
Input signal level for full-scale out		Gain = 0 dB		1		V_{PP}
Input voltage	for INP pin				VCC	V
	for INN pin		GND			V
Input capacitance				10		pF
Input limit			GND – 0.3		VCC + 0.3	V
REFERENCE						
Positive reference voltage				1.25		V
Negative reference voltage				0.75		V
INPUT CLAMP						
Clamp-on resistance				2		kΩ
Clamp level				1.8		V

(1) All values listed are preliminary. Final values to be determined after evaluation.

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ELECTRICAL CHARACTERISTICS[1] (continued)

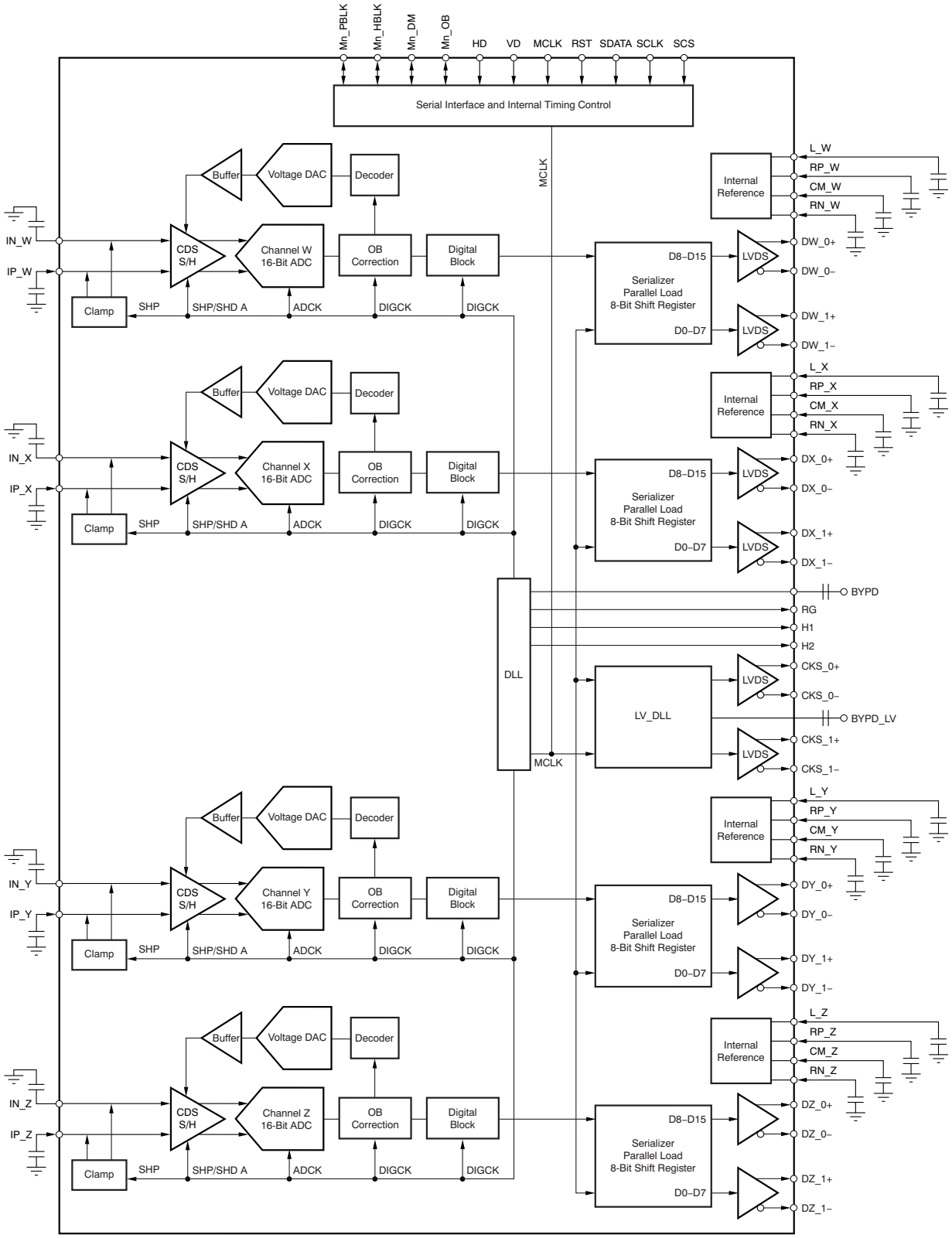
All specifications at T_A = +25°C, all power-supply voltages = +3 V, and conversion rate = 36 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP7500, VSP7502			UNIT
			MIN	TYP	MAX	
TRANSFER CHARACTERISTICS						
Differential nonlinearity (DNL)				±1		LSB
Integral nonlinearity (INL)				±32		LSB
No missing codes				Ensured		
Step response settling time		Full-scale step input		1		Pixels
Overload recovery time		Step input from 1.8 V to 0 V		2		Pixels
Data latency					11	Clocks
Signal-to-noise ratio[2]		Grounded input capacitor		77		dB
Sensor offset correction range			–200		200	mV
Channel isolation		Among each channel		–77		dB
PROGRAMMABLE GAIN (Analog)						
Analog gain programmable range			0		+9.6	dB
Analog gain programmable step				0.28		dB
Analog gain step monotonocity				Ensured		
Analog gain error		For setting gain			0.5	dB
PROGRAMMABLE GAIN (Digital)						
Digital gain programmable range			0		32	dB
Digital gain programmable step				0.032		dB
OPTICAL BLACK CLAMP (OBCLP) LOOP						
Loop time constant				40.7		µs
Optical black clamp level		Programmable range of clamp level	1024		3072	LSB
		OBCLP level at code = 1000 0000 0000b (center)		2048		LSB
		OB level program step		1		LSB
PRIMARY ANALOG OB CLAMP LOOP						
OB DAC resolution				6		Bits
OB DAC full-scale voltage				±250		mV
LVDS BUFFER (D0, D1, CKS)						
R_L	Differential load impedance		90	100	110	Ω
$\|V_{OD}\|$	Differential steady-state output voltage magnitude	R_L = 100 Ω	90		110	mV
$\Delta\|V_{OD}\|$	Change in the steady-state differential output voltage magnitude between opposite binary states	R_L = 100 Ω			15	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	COM_SEL = 0 (0.9 V mode)	0.7		1.1	V
		COM_SEL = 1 (1.2 V mode)	1		1.4	V
$V_{OC(PP)}$	Peak-to-peak common-mode output			20	50	mV
I_{OS}	Short-circuit output current	Output = GND	–6		6	mA
I_{OZ}	High-impedance state output current	V_O = 0 V to VCC	–10		10	µA
TEMPERATURE RANGE						
Operating temperature			–25		+85	°C

(2) SNR = 20 log (full-scale voltage/rms noise).

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FUNCTIONAL BLOCK DIAGRAM



NOTE: VSP7500 = CDS, VSP7502 = SH.

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SYSTEM DESCRIPTION

SAMPLE-AND-HOLD (S/H) MODE

In S/H mode, the VSP7502 input circuit is configured for sample-and-hold operation by the serial interface setting. Figure 1 shows a simplified input circuit of the S/H mode. In this mode, the input signal is sampled by the SHD signal.

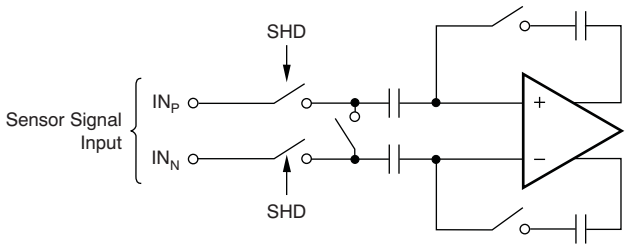


Figure 1. S/H Input Mode Block Diagram

CORRELATED DOUBLE SAMPLER (CDS) MODE

In CDS mode, the VSP7500/VSP7502 input circuit is reconfigured as a CDS by the serial interface setting. Figure 2 shows a simplified input circuit of the CDS mode.

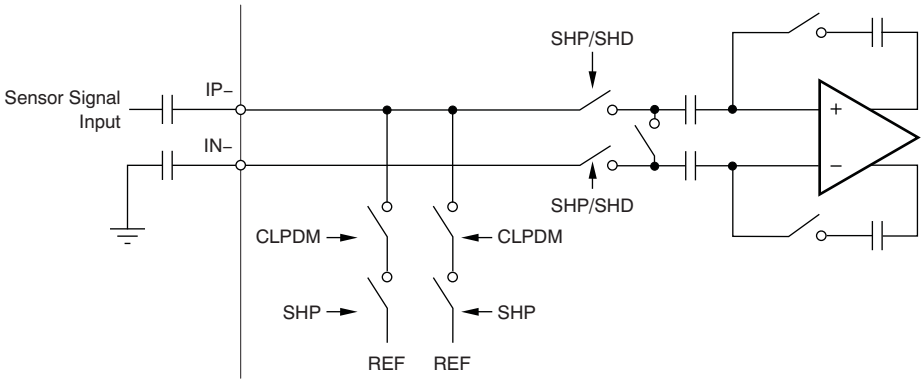


Figure 2. CDS Input Mode Block Diagram

INPUT CLAMP

In the charge-coupled device (CCD) input mode, the IN_P pin of the VSP7500/VSP7502 are connected to the buffered CCD output through capacitive coupling; therefore, an input clamp is necessary. The purpose of the input clamp is to restore the dc component of the input signal that is lost during ac coupling and establish the desired dc bias point for CDS. Figure 2 also illustrates the input clamp. The input level is clamped to the internal reference voltage during the dummy pixel interval. More specifically, the clamping function becomes active when both CLPDM and SHP are active.

16-BIT ADC

The VSP7500/VSP7502 also provide a high-speed, 16-bit ADC. This ADC uses a fully-differential, pipelined architecture with a correction feature. This architecture achieves better linearity at lower signal levels because large linearity errors tend to occur at specific points in the full-scale range, and linearity improves for a signal level below that specific point. The ADC ensures 16-bit resolution for the entire full-scale range.

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OPTICAL BLACK (OB) LOOP AND OB CLAMP (OBCLP) LEVEL

The VSP7500/VSP7502 have a built-in optical black (OB) offset self-calibration circuit (OB loop) that compensates the OB level by using OB pixels that are output from the CCD image sensor. This device also provides a digital OB clamp loop. CCD offset is compensated by converging both OB loops while activating CLPOB during a period when OB pixels are output from the CCD. 20 pixels of the CLPOB period may be enough for stable OB loop operation.

CLOCKING AND DLL

The VSP7500/VSP7502 require the following clocks for proper operation: MCLK, the system clock; CLPOB, the optical black level clamp; and CLPDM, the input clamp.

The HBLK timing signal transmits the horizontal blanking period timing. In this period, high-speed HTG pulses are masked. The PBLK timing signal transmits the data output blanking period timing. In this period, outputting the ADC data is masked.

The VSP7500/VSP7502 have built-in DLL circuits that enable the required sampling clocks and the horizontal timing pulse and logic clocks for outputting LVDS data to be generated.

VOLTAGE REFERENCE

All reference voltages and bias currents used on the VSP7500/VSP7502 are created from internal bandgap circuitry. The device has a symmetrically independent voltage reference for each channel.

Both channels of the S/H, CDS, and the ADC use three primary reference voltages: REFP (1.25 V), REFN (0.75 V), and CM (1 V) of individual references. REFP and REFN are buffered on-chip. CM is derived as the midrange voltage of the resistor chain internally connecting REFP and REFN. The ADC full-scale range is determined by twice the difference voltage between REFP and REFN.

REFP, REFN, and CM should be heavily decoupled with appropriate capacitors.

HOT PIXEL REJECTION

Sometimes, OB pixel output signals from the CCD include unusual level signals that are caused by pixel defection. If this level reaches a full-scale level, it may affect OB level stability. The VSP7500/VSP7502 have a function that rejects the unusually large pixel levels (hot pixels) in the OB pixel. This function may contribute to CCD yield improvement that is caused by OB pixel failure.

Rejection level for hot pixels is programmable through the serial interface. When hot pixels come from the CCD, the VSP7500/VSP7502 omit them and replace the previous pixel level with the OB level calculation.

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2010) to Revision A	Page
• Added last four bullets to *Applications* section	1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
VSP7500ZWV	ACTIVE	NFBGA	ZWV	159	348	Pb-Free (RoHS)	SNAGCU	Level-2-260C-1 YEAR	
VSP7500ZWVR	ACTIVE	NFBGA	ZWV	159	1000	Pb-Free (RoHS)	SNAGCU	Level-2-260C-1 YEAR	
VSP7502ZWV	ACTIVE	NFBGA	ZWV	159	260	TBD	Call TI	Call TI	
VSP7502ZWVR	ACTIVE	NFBGA	ZWV	159	1000	Pb-Free (RoHS)	SNAGCU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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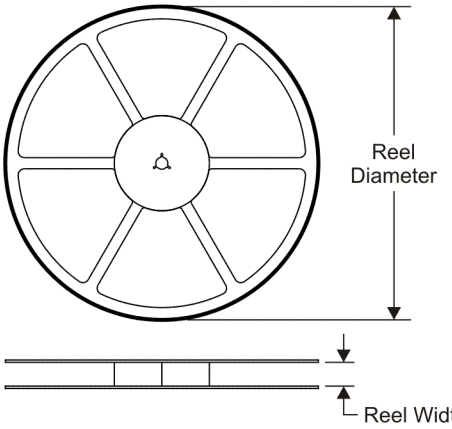
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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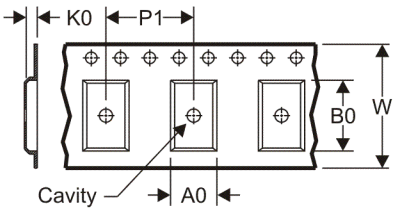
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

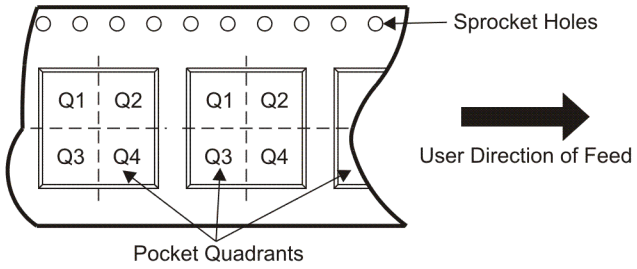


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

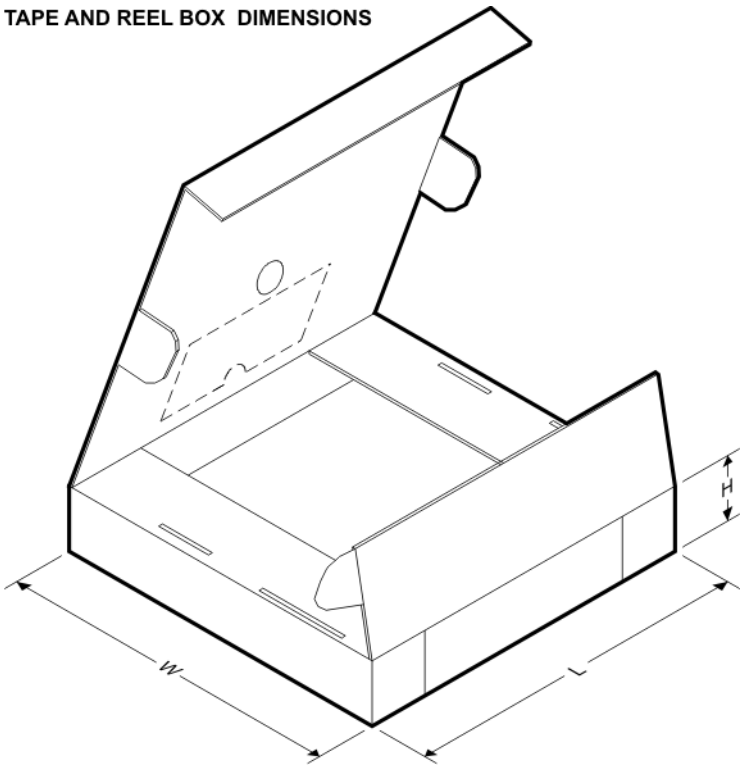
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VSP7500ZWVR	NFBGA	ZWV	159	1000	330.0	16.4	8.3	8.3	1.85	12.0	16.0	Q1
VSP7502ZWVR	NFBGA	ZWV	159	1000	330.0	16.4	8.3	8.3	1.85	12.0	16.0	Q1

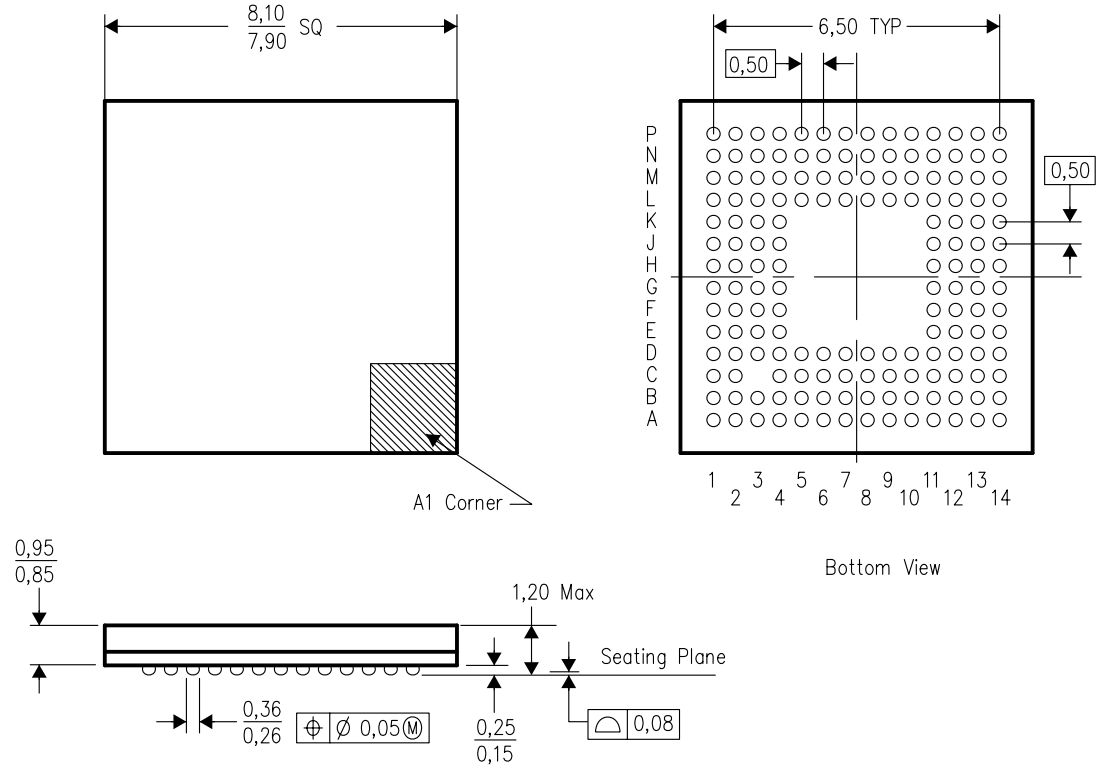
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VSP7500ZWVR	NFBGA	ZWV	159	1000	342.0	336.0	34.0
VSP7502ZWVR	NFBGA	ZWV	159	1000	342.0	336.0	34.0

ZWV (S–PBGA–N159) PLASTIC BALL GRID ARRAY



4206430–2/D 09/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

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