National Semiconductor

December 1988

DP8228/DP8228M/DP8238/DP8238M System Controller and Bus Driver

General Description

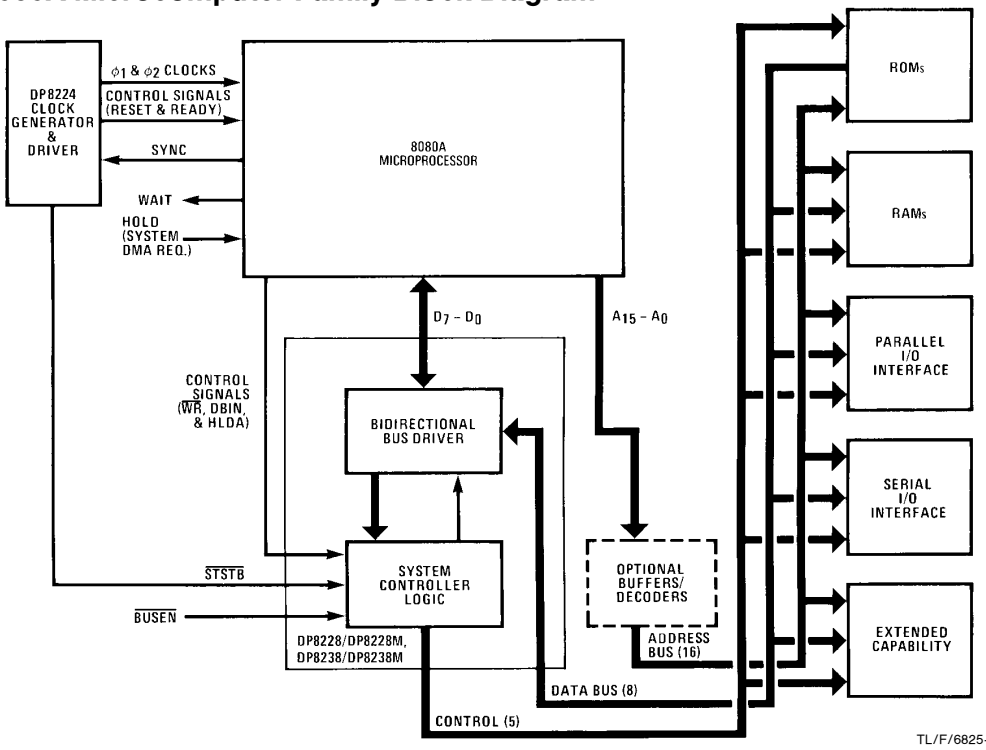
The DP8228/DP8228M, DP8238/DP8238M are system controller/bus drivers contained in a standard, 28-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates all the read and write control signals required to directly interface the memory and input/output components of the 8080A microcomputer family. The chip also provides drive and isolation for the bidirectional data bus of the 8080A microprocessor. Data bus isolation enables the use of slower memory and input/output components in a system, and provides for enhanced system noise immunity.

A user-selected signal-level interrupt vector (RST 7) is provided by the device for use in the interrupt structure of small systems that need only one basic vector. No additional components (such as an interrupt instruction port) are required to use the single interrupt vector in these systems. The devices also generate an Interrupt Acknowledge ($\overline{INTA}$) control signal for each byte of a multibyte CALL instruction when an interrupt is acknowledged by the 8080A. This feature permits the use of a multilevel priority interrupt structure in large, interrupt-driven systems.

Features

- Single chip system controller and bus driver for 8080A Microcomputer Systems
- Allows use of multibyte CALL instructions for Interrupt Acknowledge
- Provides user-selected single-level interrupt vector (RST 7)
- Provides isolation of data bus
- Supports a wide variety of system bus structures
- Reduces system component count
- DP8238/DP8238M provides advanced Input/Output Write and Memory Write control signals for large system timing control

8080A Microcomputer Family Block Diagram



TL/F/6825–1

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Supply Voltage, V_{CC}	−0.5 to +7V
Input Voltage	−1.5V to +7V
Output Current	100 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	2179 mW
Molded Package	2361 mW

*Derate cavity package 14.5 mW/°C above 25°C; derate molded package 18.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP8228M, DP8238M	4.50	5.50	V_{DC}
DP8228, DP8238	4.75	5.25	V_{DC}
Operating Temperature (T_A)			
DP8228M, DP8238M	−55	+125	°C
DP8228, DP8238	0	+70	°C

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.*

Electrical Characteristics Min ≤ T_A ≤ Max, Min ≤ V_{CC} ≤ Max, unless otherwise noted

Symbol	Parameter		Conditions		Min	Typ (Note 1)	Max	Units
V_C	Input Clamp Voltage, All Inputs		V_{CC} = Min, I_C = −5 mA			0.6	−1.0	V
I_F	Input Load Current	$\overline{STSTB}$	V_{CC} = Max V_F = 0.45V for DP8228, DP8238 V_F = 0.40V for DP8228M, DP8238M				500	μA
		D2 and D6					750	μA
		D0, D1, D4, D5 and D7					250	μA
		All Other Inputs					250	μA
I_R	Input Leakage Current	DB0–DB7	V_{CC} = Max, V_R = V_{CC}				20	μA
		All Other Inputs					100	μA
V_{TH}	Input Threshold Voltage, All Inputs		V_{CC} = 5V		0.8		2.0	V
I_{CC}	Power Supply Current		V_{CC} = Max	DP8228, DP8238		185	230	mA
				DP8228M, DP8238M		160	230	mA
V_{OL}	Output Low Voltage	D0–D7	V_{CC} = Min, I_{OL} = 2 mA	DP8228M, DP8238M			0.50	V
				DP8228, DP8238			0.45	V
		All Other Outputs	V_{CC} = Min, I_{OL} = 10 mA	DP8228M, DP8238M			0.50	V
				DP8228, DP8238			0.45	V
V_{OH}	Output High	D0–D7	V_C = Min, I_{OL} = −10 μA	DP8228M, DP8238M	3.3	3.8		V
				DP8228, DP8238	3.6	3.8		V
		All Other Outputs	V_{CC} = Min, I_{OH} = −1 mA		2.4	3.8		V
I_{OS}	Short Circuit Current, All Outputs		V_{CC} = 5V, V_O = 0V		15		90	mA
$I_{O\ (OFF)}$	OFF State Output Current All Control Outputs		V_{CC} = Max, V_O = V_{CC}				100	μA
			V_{CC} = Max, V_O = 0.45V				−100	μA
I_{INT}	INTA Current		(See Test Conditions, *Figure 3*)				5	mA

Note 1: Typical values are for T_A = 25°C and typical supply voltages.

Capacitance* $V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1\ MHz$

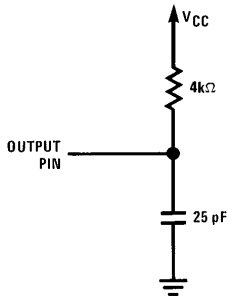
Symbol	Parameter	Min	Typ (Note 1)	Max	Units
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

*This parameter is periodically sampled and not 100% tested.

Switching Characteristics $Min \le V_{CC} \le Max, Min \le T_A \le Max$

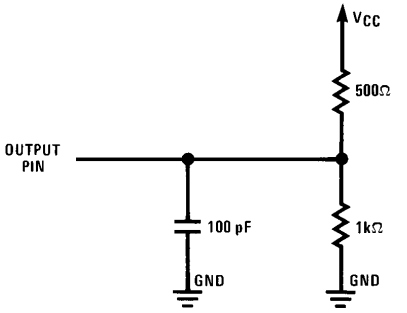
Symbol	Parameter	Conditions	DP8228M, DP8238M		DP8228, DP8238		Units
			Min	Max	Min	Max	
t_{PW}	Width of Status Strobe		25		22		ns
t_{SS}	Set-Up Time, Status Inputs D0–D7		8		8		ns
t_{SH}	Hold Time, Status Inuts D0–D7		5		5		ns
t_{DC}	Delay from $\overline{STSTB}$ to Any Control Signal	*(Figure 2)*	20	75	20	60	ns
t_{RR}	Delay from DBIN to Control Outputs	*(Figure 2)*		30		30	ns
t_{RE}	Delay from DBIN to Enable/ Disable 8080 Bus	*(Figure 1)*		45		45	ns
t_{RD}	Delay from System Bus to 8080 Bus During Read	*(Figure 1)*		45		30	ns
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	*(Figure 2)*	5	60	5	45	ns
t_{WE}	Delay to Enable System Bus DB0–DB7 after $\overline{STSTB}$	*(Figure 2)*		30		30	ns
t_{WD}	Delay from 8080 Bus D0–D7 to System Bus DB0–DB7 During Write	*(Figure 2)*	5	40	5	40	ns
t_E	Delay from System Bus Enable to System Bus DB0–DB7	*(Figure 2)*		30		30	ns
t_{HD}	HLDA to Read Status Outputs	*(Figure 2)*		25		25	ns
t_{DS}	Set-Up Time, System Bus Inputs to HLDA		10		10		ns
t_{DH}	Hold Time, System Bus Inputs to HLDA		20		20		ns

Test Conditions



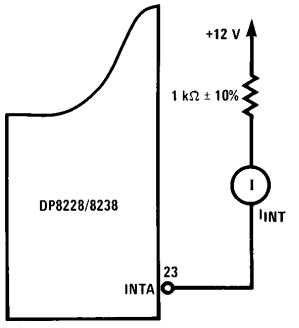
TL/F/6825–2

FIGURE 1. Test Load



TL/F/6825–3

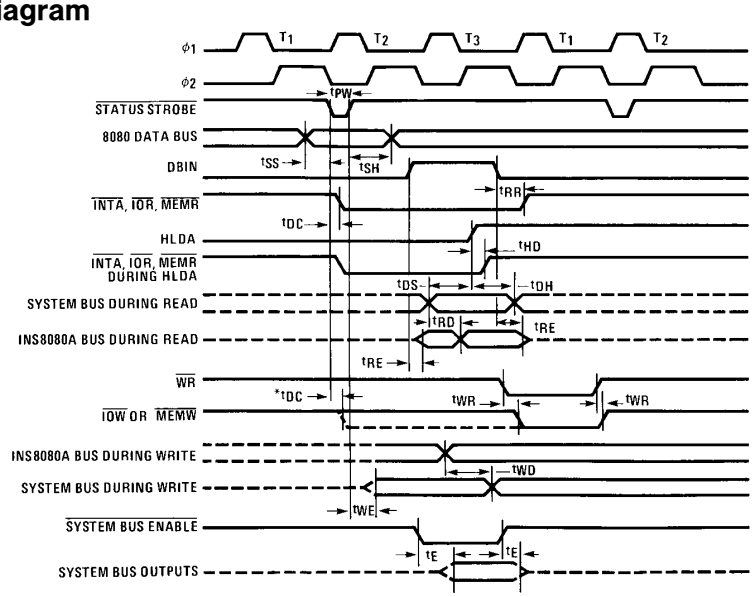
FIGURE 2. Test Load



TL/F/6825–4

FIGURE 3. INTA Test Circuit (For RST 7)

Timing Diagram



TL/F/6825–5

VOLTAGE MEASUREMENT POINTS: D_0–D_7 (when outputs) Logic "0" = 0.8V, Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.
*Advanced $\overline{I/OW}$ $\overline{MEMW}$ for 8238 only.

Functional Pin Definitions

The following describes the function of all of the DP8228/DP8228M, DP8238/DP8238M pinouts. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Status Strobe ($\overline{STSTB}$): Activated (low) at the start of each new machine cycle. The $\overline{STSTB}$ input is used to store a status word (refer to chart) from the 8080A microprocessor into the internal status latch of the DP8228, DP8238. The status word is latched when the $\overline{STSTB}$ returns to the high state. The 8080A outputs this status word onto its data bus during the first state (SYNC interval) of each machine cycle.

Data Bus In (DBIN): When high, indicates that the 8080A data bus is in the input mode. The DBIN signal is used to gate data from memory or an input/output device onto the data bus.

Write ($\overline{WR}$): When low, indicates that the data on the 8080A data bus are stable for WRITE memory or output operation.

Hold Acknowledge (HLDA): When high, indicates that the 8080A data and address buses will go to their high impedance state. When in the data bus read mode, DBIN input in the high state, a high HLDA input will latch the data bus information into the driver circuits and gate off the applicable control signal $\overline{I/OR}$, $\overline{MEMR}$, or $\overline{INTA}$ (return to the output high state).

Bus Enable ($\overline{BUSEN}$): Asynchronous DMA input to the internal gating array. When low, normal operation of the internal bidirectional bus driver and gating array occurs. When high, the bus driver and gating array are driven to their high impedance state.

V_{CC} Supply: +5V.

Ground: 0V reference.

OUTPUT SIGNALS

Memory Read ($\overline{MEMR}$): When low, signals data to be loaded in from memory. The $\overline{MEMR}$ signal is generated by strobing in status word 1, 2, or 4. (Refer to status word chart.)

Memory Write ($\overline{MEMW}$): When low, signals data to be stored in memory. The $\overline{MEMW}$ signal is generated for the DP8238 by strobing in status word 3 or 5. (Refer to status word chart.) For the DP8228, the $\overline{MEMW}$ signal is generated by gating a low-level $\overline{WR}$ input with the strobed in status word 3 or 5.

Input/Output Read ($\overline{I/OR}$): When low, signals data to be loaded in from an addressed input/output device. The $\overline{I/OR}$ signal is generated by strobing in status word 6.

Input/Output Write ($\overline{I/OW}$): When low, signals data to be transferred to an addressed input/output device. The $\overline{I/OW}$ signal for the DP8238 is generated by strobing in status word 7. For the DP8238 the $\overline{I/OW}$ signal is generated by gating in a low-level $\overline{WR}$ input with the strobed in status word 7.

Interrupt Acknowledge ($\overline{INTA}$): When low, indicates that an interrupt has been acknowledged by the 8080A microprocessor. The $\overline{INTA}$ signal is generated by strobing in staus word 8 or 10.

Signal Level Interrupt (RST 7): When the $\overline{INTA}$ output is tied to 12V through a 1 kΩ resistor, strobing in status word 8 or 10 will cause the CPU data bus outputs, when active, to go to the high state.

INPUT/OUTPUT SIGNALS

CPU Data (D_7–D_0) Bus: This bus comprises eight TRI-STATE® input/output lines that connect to the 8080A microprocessor. The bus provides bidirectional communica-

Functional Pin Definitions (Continued)

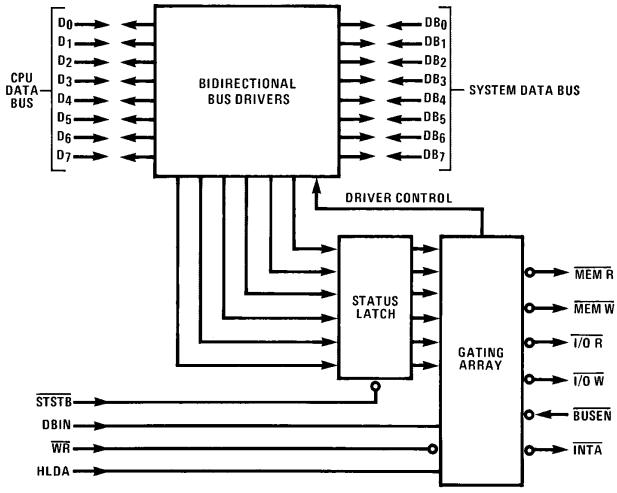
tion between the CPU, memory, and input/output devices for instructions and data transfers. A status word (which describes the current machine cycle) is also outputted on this data bus during the first microcycle of each machine cycle (SYNC = logic 1).

System Data (DB_7–DB_0) Bus: This bus comprises eight TRI-STATE input/output lines that connect to the memory and input/output components of the system. The internal bidirectional bus driver isolates the DB_7–DB_0 Data Bus from the D_7–D_0 Data Bus.

Status Word Chart

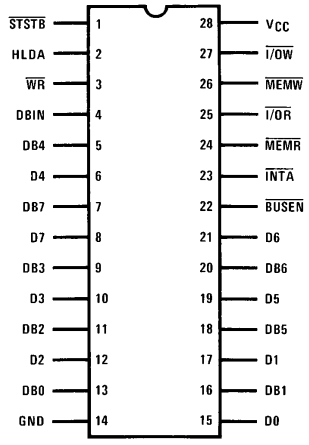
Machine Cycle	Status Word	Data Bus Bit								Control Signal
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Instruction Fetch	1	1	0	1	0	0	0	1	0	$\overline{MEMR}$
Memory Read	2	1	0	0	0	0	0	1	0	$\overline{MEMR}$
Memory Write	3	0	0	0	0	0	0	0	0	$\overline{MEMW}$
Stack Read	4	1	0	0	0	0	1	1	0	$\overline{MEMR}$
Stack Write	5	0	0	0	0	0	1	0	0	$\overline{MEMW}$
Input Read	6	0	1	0	0	0	0	1	0	$\overline{I/OR}$
Output Write	7	0	0	0	1	0	0	0	0	$\overline{I/OW}$
Interrupt Acknowledge	8	0	0	1	0	0	0	1	1	$\overline{INTA}$
Halt Acknowledge	9	1	0	0	0	1	0	1	0	(none)
Interrupt Acknowledge While Halt	10	0	0	1	0	1	0	1	1	$\overline{INTA}$

Block and Connection Diagrams



TL/F/6825–6

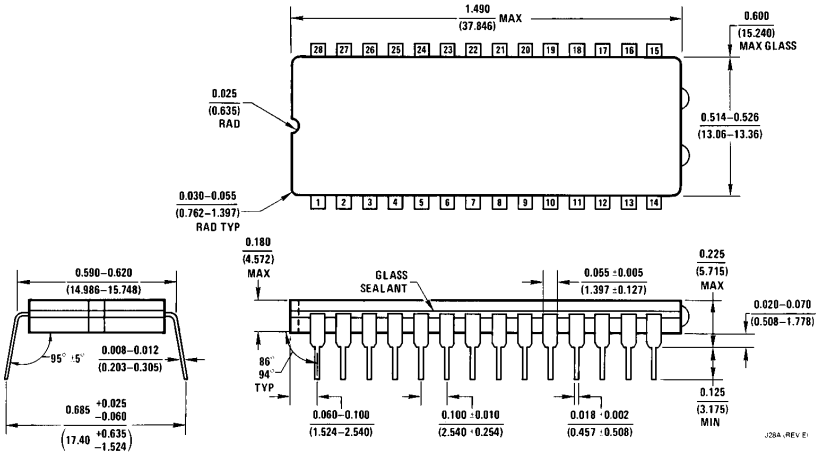
Dual-In-Line Package



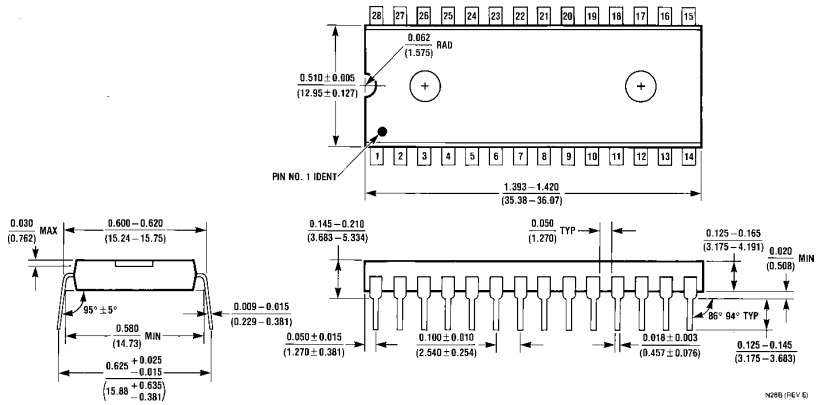
TL/F/6825–7

Order Number DP8228J, DP8228MJ, DP8228N, DP8238J, DP8238MJ or DP8238N
See NS Package Number J28A or N28B

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number DP8228J, DP8228MJ, DP8238J or DP8238MJ
NS Package Number J28A



Molded Dual-In-Line Package (N)
Order Number DP8228N or DP8238N
NS Package Number N28B

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