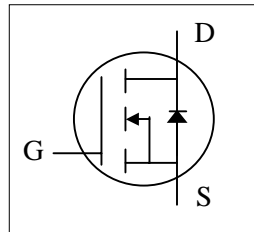
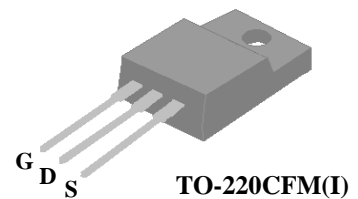




- ▼ 100% Avalanche Test
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free



$BV_{DSS}$	150V
$R_{DS(ON)}$	100m $\Omega$
$I_D^3$	20A



## Description

AP20N15 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220CFM package is widely preferred for all commercial-industrial through hole applications. The mold compound provides a high isolation voltage capability and low thermal resistance between the tab and the external heat-sink.

## Absolute Maximum Ratings@ $T_J=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	150	V
$V_{GS}$	Gate-Source Voltage	+20	V
$I_D@T_C=25^\circ\text{C}$	Drain Current, $V_{GS}$ @ 10V <sup>3</sup>	20	A
$I_D@T_C=100^\circ\text{C}$	Drain Current, $V_{GS}$ @ 10V <sup>3</sup>	12	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	80	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	34.7	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

## Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	3.6	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	65	$^\circ\text{C}/\text{W}$



**Electrical Characteristics @T<sub>j</sub>=25°C(unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =1mA	150	-	-	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	-	-	100	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	2	-	4	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =10A	-	16	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =120V, V <sub>GS</sub> =0V	-	-	25	uA
	Drain-Source Leakage Current (T <sub>j</sub> =125°C)	V <sub>DS</sub> =120V, V <sub>GS</sub> =0V	-	-	250	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Q <sub>g</sub>	Total Gate Charge	I <sub>D</sub> =14A	-	22	35	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =120V	-	6	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =10V	-	7.7	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DS</sub> =75V	-	10	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =14A	-	33	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =10Ω	-	27	-	ns
t <sub>f</sub>	Fall Time	V <sub>GS</sub> =10V	-	26	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	1070	1700	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =25V	-	230	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	9	-	pF
R <sub>g</sub>	Gate Resistance	f=1.0MHz	-	1.6	3.2	Ω

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =10A, V <sub>GS</sub> =0V	-	-	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =14A, V <sub>GS</sub> =0V,	-	0.13	-	us
Q <sub>rr</sub>	Reverse Recovery Charge	dI/dt=100A/μs	-	0.77	-	uC

**Notes:**

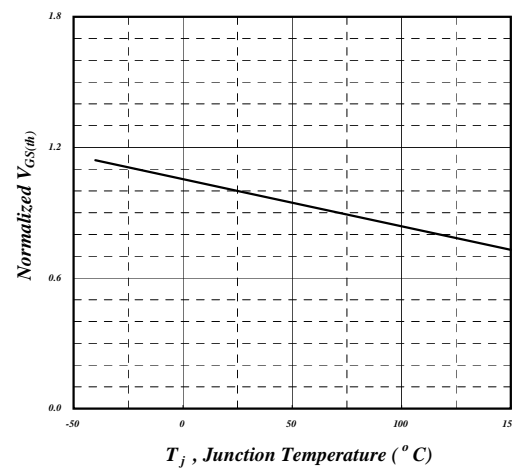
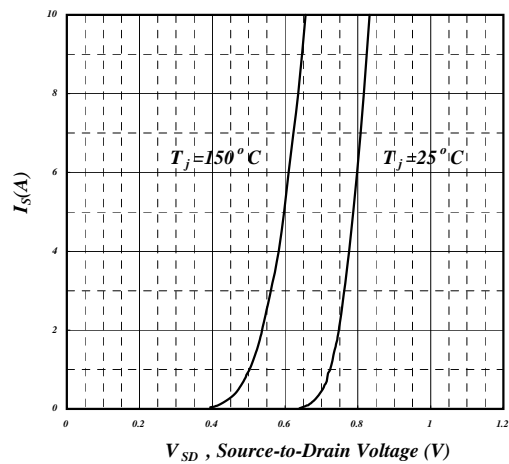
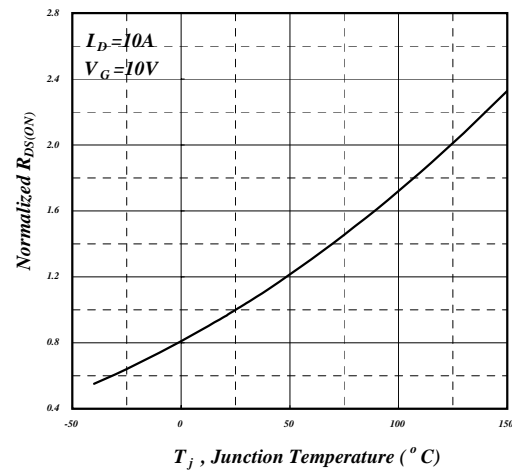
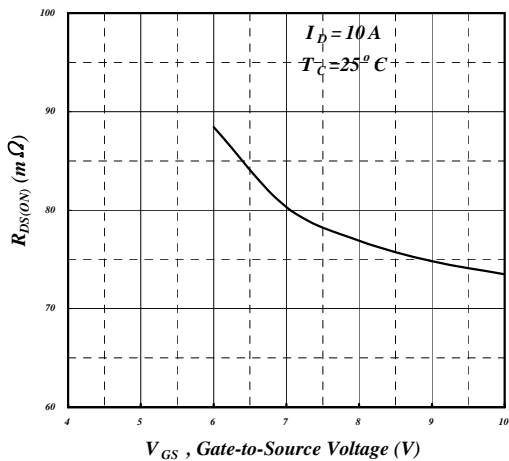
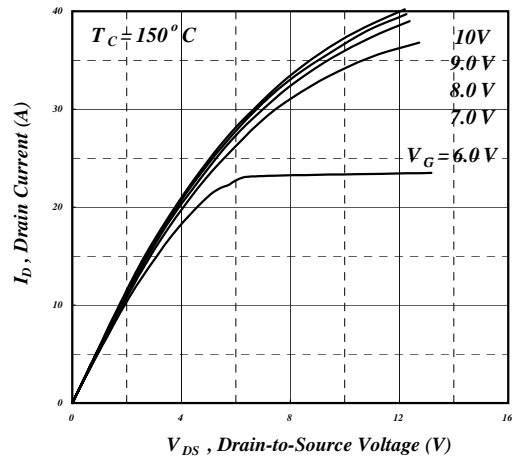
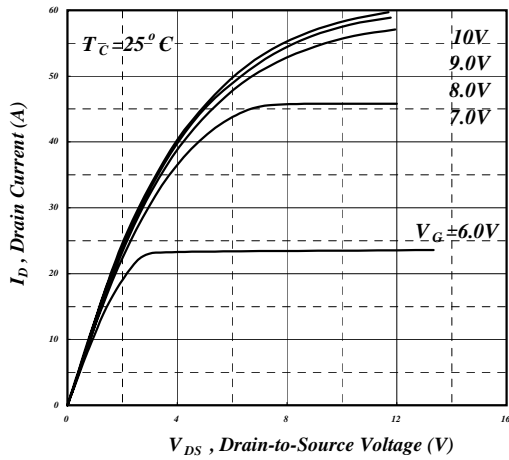
- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Ensure that the junction temperature does not exceed T<sub>Jmax</sub>.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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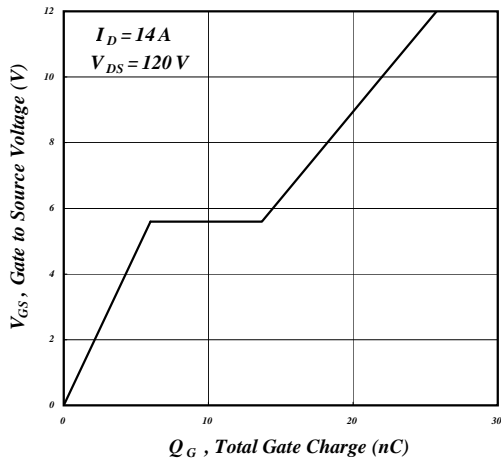


Fig 7. Gate Charge Characteristics

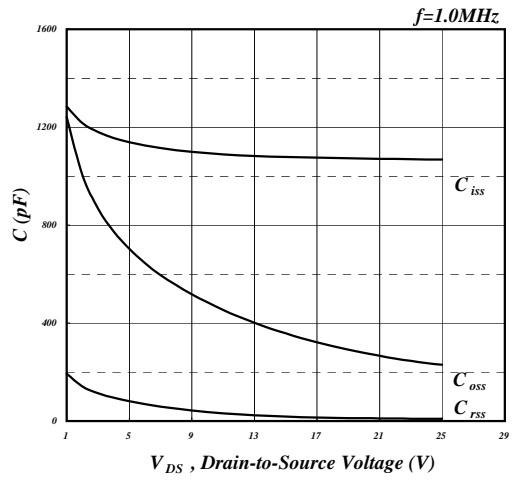


Fig 8. Typical Capacitance Characteristics

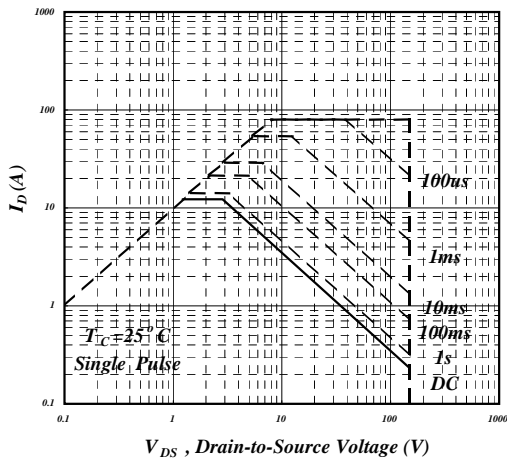


Fig 9. Maximum Safe Operating Area

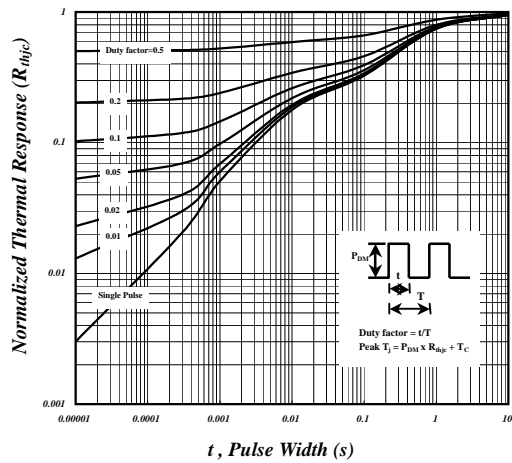


Fig 10. Effective Transient Thermal Impedance

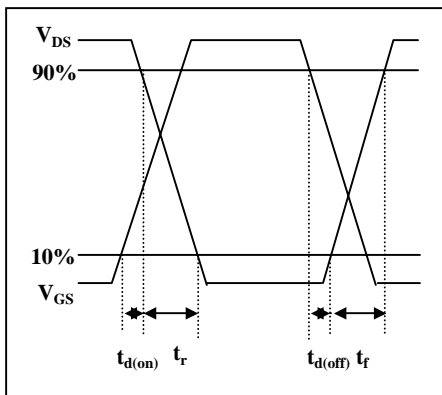


Fig 11. Switching Time Waveform

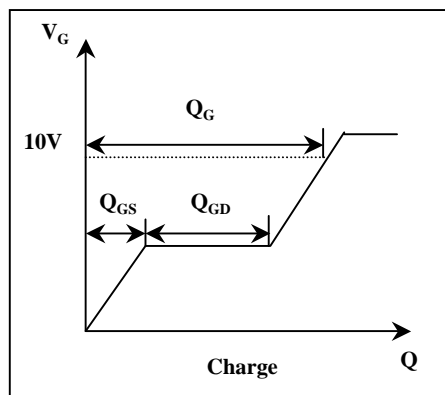


Fig 12. Gate Charge Waveform



**MARKING INFORMATION**

