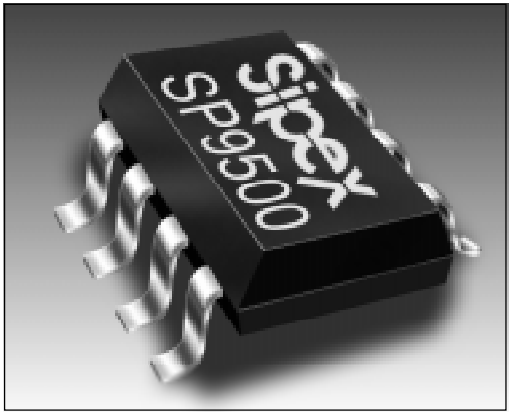
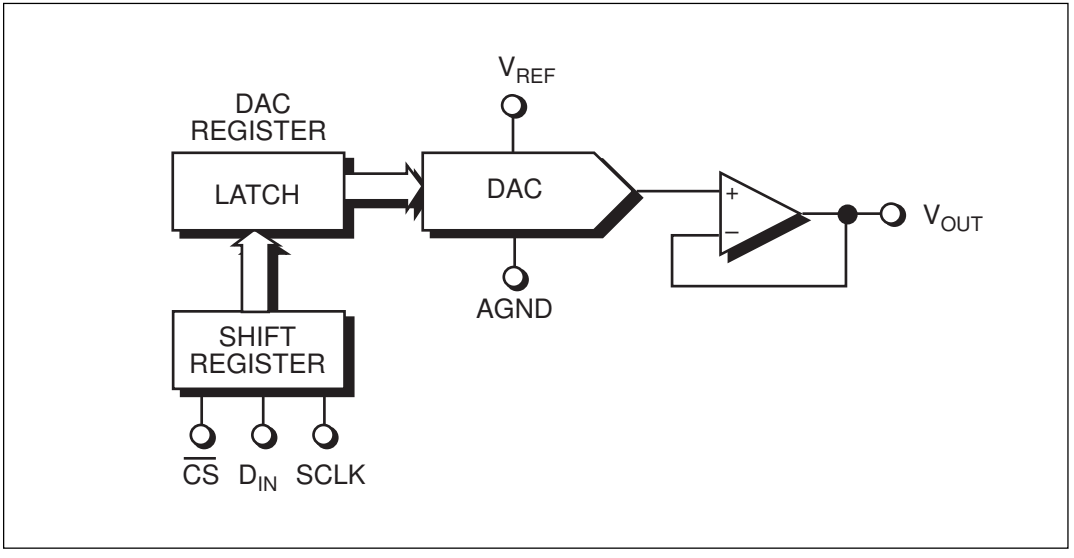
12–Bit, Voltage Output D/A Converter

- Low Power – 1.1mW
- Voltage Output, 0.5V to 4.5V Range
- Single +5 Volt Supply
- 1.4 MHz Multiplying Bandwidth (2-Quadrant)
- Standard 3-Wire Serial Interface
- 8–pin (0.15") SOIC and Plastic DIP Packages



DESCRIPTION…

The **SP9500** is a low power 12-Bit Digital-to-Analog Converter. It features 0.5 to 4.5V output swing when using +5volt supply. The converter uses a standard 3–wire serial interface compatible with SPI™, QSPI™ and Microwire™. The output settling-time is specified at 7.5µs. The **SP9500** is available in 8–pin 0.15" SOIC and DIP packages, specified over commercial and industrial temperature ranges.



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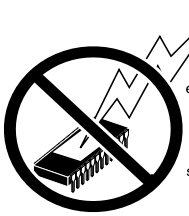
ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{DD} - DGND ..... -0.3V,+6.0V
V_{REF} ..... DGND, V_{DD}
AGND ..... DGND, V_{REF}
D_{IN} ..... DGND, V_{DD}
Power Dissipation
Plastic DIP 375mW
(derate 7mW/°C above +70°C)
Small Outline 375mW
(derate 7mW/˚C above +70˚C)



CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

(Typical at 25˚C; $T_{MIN} \le T_A \le T_{MAX}$; V_{DD} = +5V, DGND = 0V, V_{REF} = +3.5V; AGND = +1.5V; CMOS logic level digital inputs; specifications apply to all grades unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DIGITAL INPUTS					
Logic Levels					
V_{IH}	2.4			Volts	
V_{IL}			0.8	Volts	
2 Quad, Input Coding		Binary			
REFERENCE INPUTS					Note 5
V_{REF} Voltage Range	0.5		4.5	Volts	
AGND Voltage Range	0.5		4.5	Volts	
Input Resistance	11	13.9		kΩ	D_{IN} = 1365; code dependent
ANALOG OUTPUT					
Gain					
–B, –K		±0.5	±2.0	LSB	Note 3
–A, –J		±1.0	±4.0	LSB	Note 3
		±1.0	±5.0	LSB	V_{REF} = 4.5V; AGND = 0.5V
Initial Offset Bipolar		±0.25	±3.0	LSB	D_{IN} = 0
Voltage Range	0.5		4.5	Volts	
Output Current	±1.0			mA	
STATIC PERFORMANCE					
Resolution	12			Bits	
Integral Linearity					
–B, –K		±0.25	±0.5	LSB	Note 3
–A, –J		±0.5	±1.0	LSB	Note 3
		±0.5		LSB	V_{REF} = 4.5V; AGND = 0.5V
Differential Linearity					
–B, –K		±0.25	±0.75	LSB	
–A, –J		±0.25	±1.0	LSB	
Monotonicity		Guaranteed			
DYNAMIC PERFORMANCE					
Settling Time					
Small Signal		1		µs	to 0.012%
Full Scale		7.5		µs	to 0.012%, V_{OUT} = 0.5 to 4.5V
Slew Rate		0.6		V/µs	
Multiplying Bandwidth		1.4		MHz	
STABILITY					
Gain		15		ppm/˚C	t_{MIN} to t_{MAX}
Scale Zero		15		ppm/˚C	t_{MIN} to t_{MAX}

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SPECIFICATIONS (continued)

(Typical at 25˚C; $T_{MIN} \leq T_A \leq T_{MAX}$; V_{DD} = +5V, DGND = 0V, V_{REF} = +3.5V; AGND = +1.5V; CMOS logic level digital inputs; specifications apply to all grades unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
POWER REQUIREMENTS					Note 5
V_{DD}					+5V, ±3%; Note 4, 5
–J, –K		0.22	0.34	mA	
–A, –B		0.22	0.50	mA	
Power Dissipation		1.1		mW	
SWITCHING CHARACTERISTICS					
CS Setup Time (t_{CSS})	25			ns	
SCLK Fall to CS Fall Hold Time (t_{CSH0})	20			ns	
SCLK Fall to CS Rise Hold Time (t_{CSH1})	0			ns	
SCLK High Width (t_{CH})	40			ns	
SCLK Low Width (t_{CL})	40			ns	
DIN Setup Time (t_{DS})	50			ns	
DIN Hold Time (t_{DH})	0			ns	
CS High Pulse Width (t_{CSW})	30			ns	
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
–J, –K	0		+70	°C	
–A, –B	–40		+85	°C	
Storage	–60		+150	°C	
Package					
–_N	8-pin Plastic DIP				
–_S	8-pin 0.15" SOIC				

Notes:

1. Integral Linearity, for the **SP9500**, is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value for any given input condition.
2. Differential Linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
3. 1 LSB = (V_{REF}-AGND)/4,096.
4. V_{REF} = AGND = 2.5V.
5. The following Power up sequence is recommended: V_{DD} (+5V), V_{REF}.

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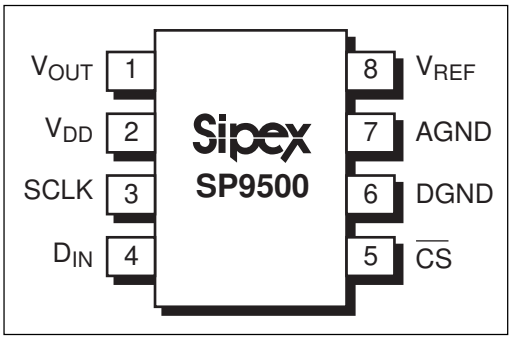
PINOUT – 8-PIN PLASTIC DIP & SOIC



PIN ASSIGNMENTS

Pin 1- V_{OUT} - Voltage Output.

Pin 2- V_{DD} - +5V Power Supply Input.

Pin 3- SCLK - Serial Clock Input.

Pin 4- D_{IN} - Serial Data Input.

Pin 5- $\overline{CS}$ - Chip Select Input.

Pin 6 - DGND - Digital Ground

Pin 7- AGND - Analog Ground.

Pin 8- V_{REF} - Reference Input.

FEATURES...

The **SP9500** is a low power 12–Bit Digital-to-Analog Converter. The converter features 0.5 to 4.5 volt output swings with a single +5V supply. The input coding format used is standard binary, *Table 1*.

This Digital-to Analog Converter uses a standard 3–wire interface compatible with SPI™, QSPI™ and Microwire™. The output settling time is specified at 7.5 µs to full 12-bit accuracy when driving a 10KΩ, 10pF load combination.

The **SP9500** Digital-to-Analog Converter is ideally suited for applications such as ATE, process controllers, robotics and instrumentation. The **SP9500** is available in an 8-pin 0.15" SOIC and 0.3" PDIP packages, specified over commercial and industrial temperature ranges.

THEORY OF OPERATION

The **SP9500** consists of four main functional blocks – the input shift register, DAC register, 12-Bit D/A converter and a output buffer amplifier, *Figure 1*.

The input shift register is used to convert the serial input data stream to a parallel 12–Bit digital word. The input data is shifted on positive clock (SCLK) edges when the Chip Select ($\overline{CS}$) signal is in the "low" state. The MSB is loaded first and LSB last. No shifting of the input data occurs when the Chip Select ($\overline{CS}$) signal is in the "high" state.

The DAC register is used to store the digital word which is sent to the R–2R DAC. Its value is updated on the positive transition of the Chip Select ($\overline{CS}$) signal.

The 12–Bit D/A converter is an "inverted" R-2R ladder network. The DAC itself is implemented with precision thin-film resistors and CMOS transmission gate switches. The resistor network is laser-trimmed to achieve better than 12–Bit accuracy. The D/A converter is used to convert the 12-bit input word to a precision voltage.

The operational amplifier is a rail-to-rail input, rail-to-rail output CMOS amplifier. It is capable of supplying 1mA of load current in the 1.5 to 3.5 output voltage range. The initial offset voltage is laser-trimmed to improve accuracy. Settling time is 7.5 µs for a full scale output transition to 0.012% accuracy.

INPUT			OUTPUT
MSB		LSB	
1111	1111	1111	V_{REF} - 1 LSB
1111	1111	1110	V_{REF} - 2 LSB
0000	0000	0001	AGND + 1 LSB
0000	0000	0000	AGND
$1\ LSB = \frac{(V_{REF}-AGND)}{2^{12}}$			

Table 1. Binary Coding

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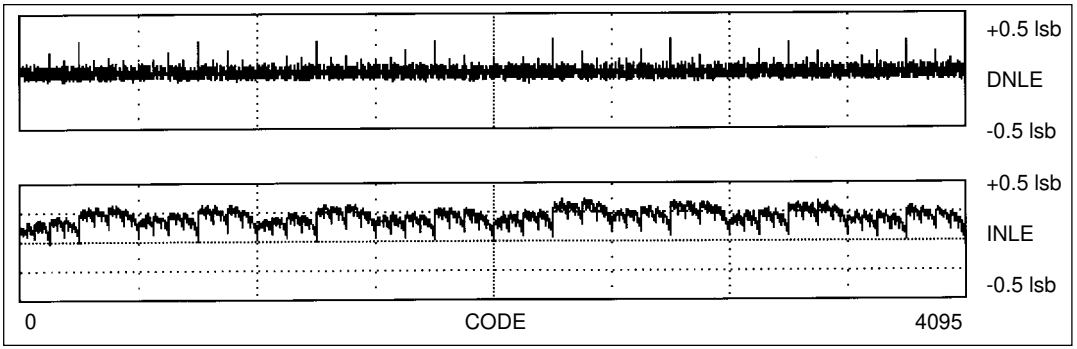

DNLE, INLE Plots

USING THE SP9500

External Reference

The R-2R DAC input resistance is code dependent and is minimum (11kΩ) at code 1365 and 2731. And, it is nearly infinite at code 0. Because of the code-dependent nature of the reference inputs, a high quality, low output impedance amplifier should be used to drive the V_{REF} and AGND inputs.

Serial Clock and Update Rate

The **SP9500** maximum serial clock rate (SCLK) is given by $1/(t_{CH}+t_{CL})$ which is approximately 12.5 MHz. The digital word update rate is limited by the chip select period, which is 12 X SCLK periods plus the $\overline{CS}$ high pulse width t_{CSW}. This is equal to a 1 µs or 1 MHz update rate. However, the DAC settling time to 12–Bits is 7.5 µs, which for full scale output transitions would limit the update rate to 125 kHz.

Logic Interface

The **SP9500** is designed to be compatible with TTL and CMOS logic levels. However, driving the digital inputs with TTL level signals will increase the power consumption of the part by 300 µA. In order to achieve the lowest power consumption use rail-to-rail CMOS levels to drive the digital inputs.

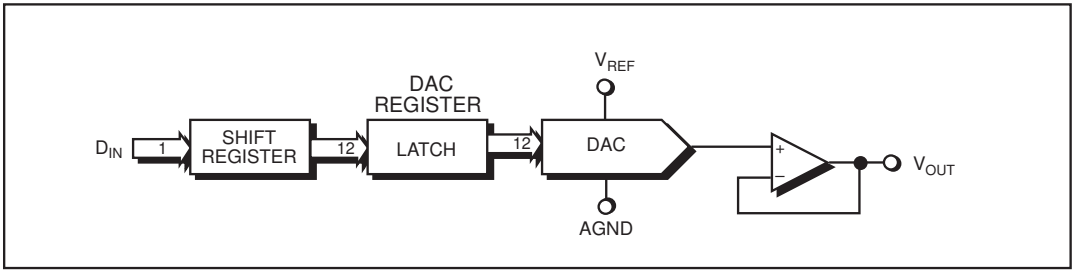

Figure 1. Detailed Block Diagram

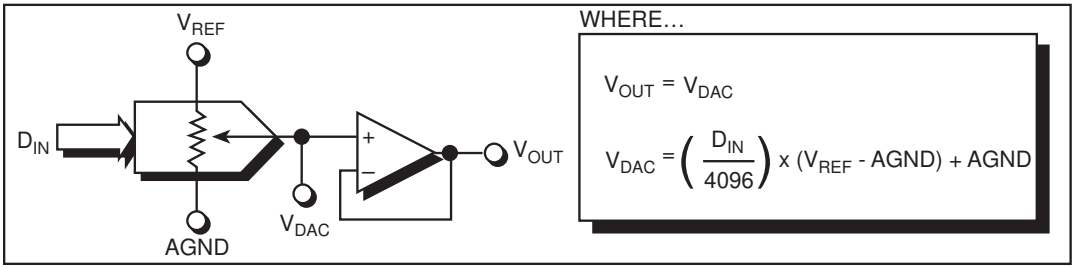

Figure 2. Transfer Function

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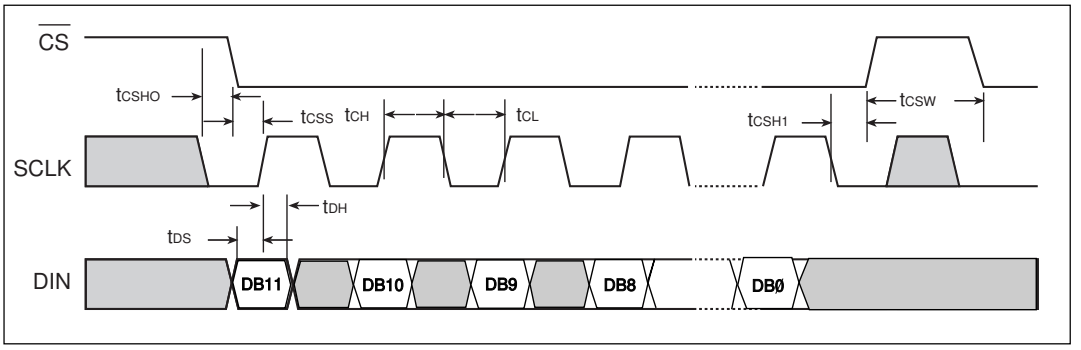

Figure 3. Timing Diagram

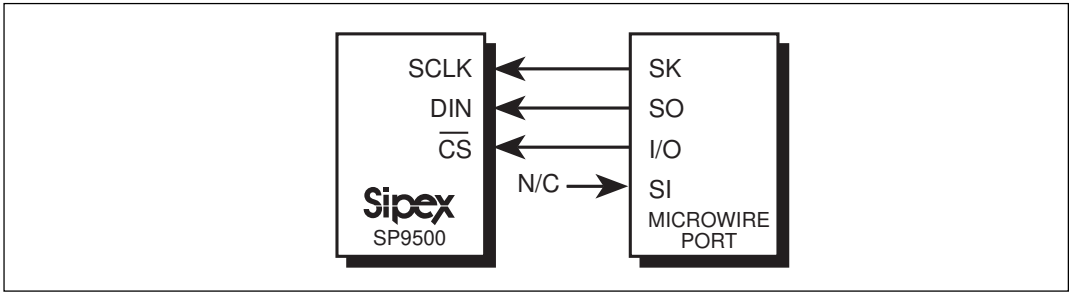

Figure 4. Microwire Connection

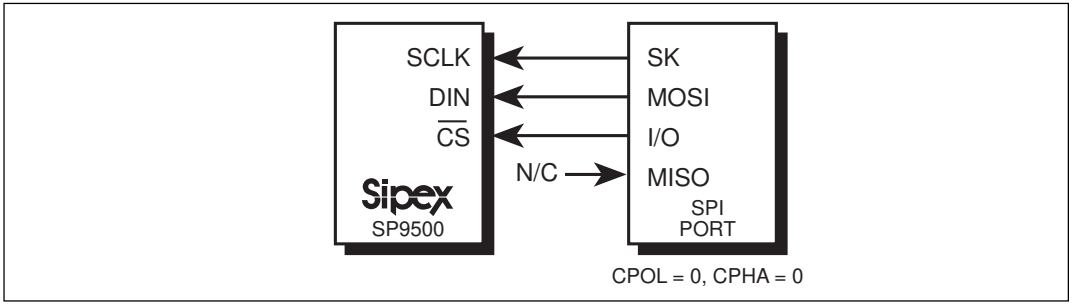

Figure 5. SPI Connection

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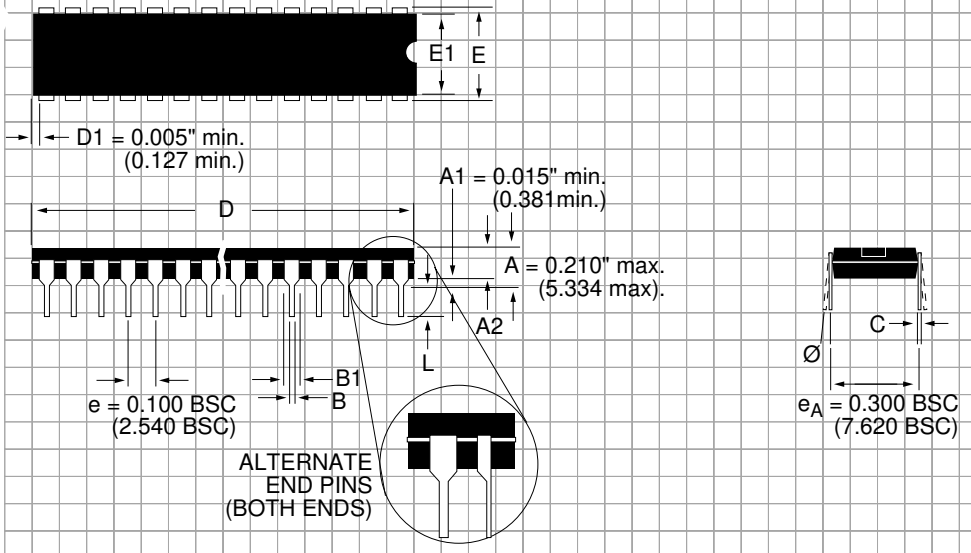
PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)



DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN	18–PIN	20–PIN	22–PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)	0.735/0.775 (18.669/19.685)	0.780/0.800 (19.812/20.320)	0.880/0.920 (22.352/23.368)	0.980/1.060 (24.892/26.924)	1.145/1.155 (29.083/29.337)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)

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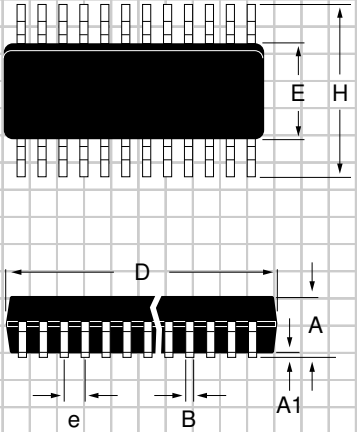
PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (NARROW)



DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN			
A	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)			
A1	0.004/0.010 (0.102/0.249	0.004/0.010 (0.102/0.249)	0.004/0.010 (0.102/0.249)			
B	0.014/0.019 (0.35/0.49)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)			
D	0.189/0.197 (4.80/5.00)	0.337/0.344 (8.552/8.748)	0.386/0.394 (9.802/10.000)			
E	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)			
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)			
H	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)			
h	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)			
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)			
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)			

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ORDERING INFORMATION

Model	Temperature Range	Package
Monolithic 12-Bit DAC Voltage Output:		
SP9500JN	0˚C to +70˚C	8-pin, 0.3" Plastic DIP
SP9500KN	0˚C to +70˚C	8-pin, 0.3" Plastic DIP
SP9500JS	0˚C to +70˚C	8–pin, 0.15" SOIC
SP9500KS	0˚C to +70˚C	8–pin, 0.15" SOIC
SP9500AN	–40˚C to +85˚C	8-pin, 0.3" Plastic DIP
SP9500BN	–40˚C to +85˚C	8-pin, 0.3" Plastic DIP
SP9500AS	–40˚C to +85˚C	8–pin, 0.15" SOIC
SP9500BS	–40˚C to +85˚C	8–pin, 0.15" SOIC

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SIGNAL PROCESSING EXCELLENCE

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