

DATA SHEET

O K I A S I C P R O D U C T S

0.8µm Mixed 3-V/5-V MSM38S0000 Sea of Gates and MSM98S000 Customer Structured Arrays

February 1995



OKI Semiconductor

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OKI Semiconductor

MSM38S0000/MSM98S000

0.8µm Mixed 3-V/5-V Sea of Gates and Customer Structured Arrays

DESCRIPTION

OKI's 0.8µm ASIC products, specially designed for mixed 3-V / 5-V applications, are now available in both Sea Of Gates (SOG) and Customer Structured Array (CSA) architectures. Both the SOG-based MSM38S Series and the CSA-based MSM98S Series use a three-layer-metal process on 0.8µm drawn (0.6µm L-effective) CMOS technology. The semiconductor process is adapted from OKI's production-proven 16-Mbit DRAM manufacturing process.

Ideal for low-power portable applications, the MSM38S / 98S are constructed with separate power busses for internal core logic and configurable I / O functions. Altogether, the architecture provides maximum flexibility, meeting the needs of all 3-V, 5-V, and mixed 3-V / 5-V signal requirements.

The MSM38S SOG Series is available in seven sizes with up to 420 I / O pads and over 135,000 usable gates. SOG array sizes are designed to fit the most popular quad flat pack (QFP) packages, such as 100-, 136-, 160-, and 208-pin QFPs. MSM38S SOG-based designs are therefore ideal for pad-limited circuits that require rapid prototyping turnaround times.

The MSM98S CSA Series is an all-mask-level superset of the SOG series, available in 29 sizes. The CSA offerings combine the SOG architecture's logic flexibility with the higher integration yielded by optimized diffusion for faster and more compact memory blocks. The MSM98S is ideal for core-limited applications or circuits with large and / or multiple memory functions. Customer modification to the structure of any of the 29 predefined masterslices, rather than creation of a new masterslice every time, improves the prototyping turnaround time over cell-based manufacturing techniques.

Both product families are supported by OKI's proprietary MEMGEN tool which quickly and easily generates SOG memories (for the MSM38S) as well as optimized memories for the MSM98S Series. The families also feature floorplanning to control pre-layout timing, clock-skew management software that guarantees worst-case clock skew of 1 ns or less, and scan-path design techniques that support ATVG for fault coverage approaching 100%.

FEATURES

- 0.8µm drawn three-layer metal CMOS
- Mixed 3-V / 5-V operation for low power and high speed
- SOG and CSA architecture availability
- Clock tree cells with ≤ 1.0-ns clock skew, worst-case (fan-out = 2000 at 70 MHz)
- Usable density from 6.5k to 135k gates
- I / Os may be VSS, 3 V, 5 V, VDD, CMOS, TTL, and 3-state, with 2-mA to 48-mA drive
- I / O level shifter cells, allowing any buffer (input, output, or bidirectional) to interface with 3 V or 5 V
- Slew-rate-controlled outputs for low radiated noise
- User-configurable single and multi-port memories
- Specialized 3-V and 5-V macrocells, including phase-locked loop, and PCI cells
- Floorplanning for front-end simulation and back-end layout controls
- JTAG boundary scan and scan-path ATVG

MSM38S/98S FAMILY LISTING

CSA Part # MSM...	SOG Part # MSM...	I/O Pads	Rows[1]	Columns	Raw Gates	Usable Gates [2]
98S020x020	—	80	44	148	6,512	4,689
98S023x023	—	92	51	176	8,976	6,463
—	38S0110	100	56	194	10,752	7,741
98S026x026	—	104	59	200	11,800	8,496
98S029x029	—	116	66	228	15,048	10,835
98S032x032	—	128	74	252	18,648	13,427
—	38S0210	136	79	270	21,172	15,244
98S035x035	—	140	81	276	22,356	16,096
98S038x038	—	152	89	304	27,056	19,480
—	38S0300	160	94	322	30,080	21,658
98S041x041	—	164	96	328	31,488	22,671
98S044x044	—	176	104	356	37,024	25,917
98S047x047	—	188	111	380	42,180	29,526
98S050x050	—	200	119	408	48,552	33,986
98S053x053	—	212	126	432	54,432	38,102
—	38S0570	216	129	442	56,760	39,732
98S056x056	—	224	134	456	61,104	42,162
98S059x059	—	236	141	484	68,244	47,088
98S062x062	—	248	149	508	75,692	51,471
98S065x065	—	260	156	536	83,616	56,859
98S068x068	—	272	164	560	91,840	62,451
—	38S0980	280	169	580	97,344	66,194
98S071x071	—	284	171	588	100,548	67,367
98S074x074	—	296	179	612	109,548	72,302
98S077x077	—	308	186	636	118,296	75,709
98S080x080	—	320	194	664	128,816	82,442
98S083x083	—	332	201	688	138,288	88,504
98S086x086	38S1500	344	209	716	149,644	95,772
98S089x089	—	356	216	740	159,840	99,101
98S092x092	—	368	224	768	172,032	103,219
98S095x095	—	380	231	792	182,952	109,771
98S098x098	—	392	239	816	195,024	117,014
98S101x101	—	404	246	844	207,624	124,574
98S104x104	—	416	254	868	220,472	132,283
—	38S2250	420	256	880	224,256	134,554

[1] Row and column numbers are used to evaluate the number and size of mega macrocells that may be included into each array. For example, a 7,600-gate mega macrocell with a size and aspect ratio of 36 rows by 245 columns can be used on the MSM98S032x032 or any larger array base, but not on the MSM98S029x029.

[2] Usable gate count is design dependent and varies based upon the number of fan-outs per net, internal busses, floor plan, RAM/ROM blocks, etc.

ARRAY ARCHITECTURE

The primary components of a 0.8µm MSM38S/98S circuit include:

- I/O base cells
- Configurable I/O pads for V_{DD}, V_{SS}, or I/O (I/O in both 3V and 5V)
- V_{DD} and V_{SS} pads dedicated to wafer probing
- Separate power bus for output buffers
- Separate power bus for internal core logic and input buffers
- Core base cells containing N-channel and P-channel pairs, arranged in column of gates
- Isolated gate structure for reduced input capacitance and increased routing flexibility

Each array has 16 dedicated corner pads for power and ground use during wafer probing, with four pads per corner. The arrays also have separate power rings for the internal core functions (V_{DDC} and V_{SSC}) and output drive transistors (V_{DDO} for 3 V and V_{SSO}).

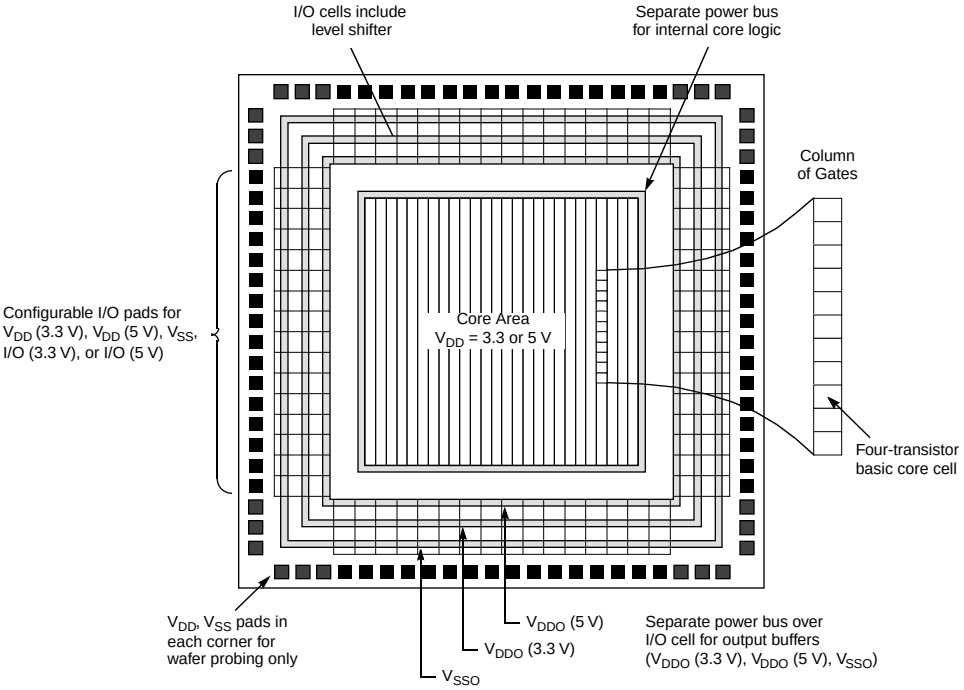


Figure 1. MSM38S/98S Array Architecture

MSM98S000 CSA Layout Methodology

The procedure to design, place, and route a CSA follows.

1. Select suitable base array frame from the available predefined sizes. To select an array size:
    - Identify the macrocell functions required and the minimum array size to hold the macrocell functions.

- Add together all the area occupied by the required random logic and macrocells and select the optimum array.

2. Make a floor plan for the design's megacells.
   - OKI Design Center engineers verify the master slice and review simulation.
   - OKI Design Center engineers floorplan the array using OKI's proprietary floorplanner and customer performance specifications.
   - Using OKI CAD software, Design Center engineers remove the SOG transistors and replace them with diffused memory macrocells to the customer's specifications.

*Figure 2*shows an array base after placement of the optimized memory macrocells.

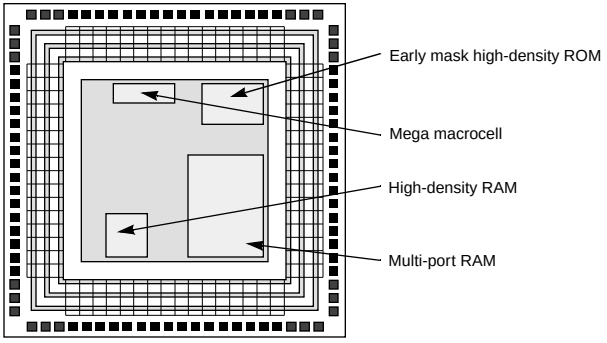


Figure 2. Optimized Memory Macrocell Floor Plan

3. Place and route logic into the array transistors.
   - OKI Design Center engineers use layout software and customer performance specifications to connect the random logic and optimized memory macrocells.

*Figure 3*marks the area in which placement and routing is performed with light shading.

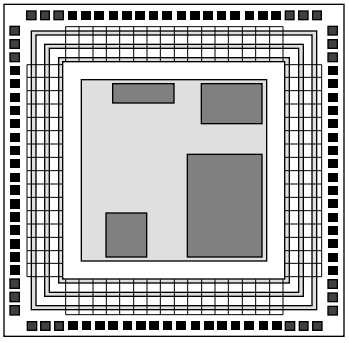


Figure 3. Random Logic Place and Route

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions [1]	Value	Unit
Power supply voltage	V_{DD}	T_j = 25° C V_{SS} = 0 V	-0.5 to +6.5	V
Input voltage	V_I		-0.5 to V_{DD}+0.5	V
Output voltage	V_O		-0.5 to V_{DD}+0.5	V
Output current per I/O base cell	I_O		-24 to + 24	mA
Current per power PAD	I_{PAD}		-90 to +90	mA
Storage temperature	T_{stg}	–	-65 to +150	° C

[1] Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the other sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (V_{SS} = 0 V)

Parameter	Symbol	Rated Value			Unit
		Min	Typ	Max	
Power supply voltage	V_{DD}	2.7	3.3	3.6	V
		4.5	5.0	5.5	V
Operating temperature	T_a	-40	+25	+85	°C
Input rise/fall time (normal type)[1][2]	tr_A, tf_A	–	2	500	ns
	tr_B, tf_B	–	2	500	ns
Input rise/fall time (Schmitt Trigger type)[3][4]	tr_C, tf_C	–	–	60	µs
	tr_D, tf_D	–	–	200	µs

[1] tr_A, tf_A – TTL interface, normal input buffer.
[2] tr_B, tf_B – CMOS interface, normal input buffer.
[3] tr_C, tf_C – TTL interface, Schmitt Trigger input buffer.
[4] tr_D, tf_D – CMOS interface, Schmitt Trigger input buffer.

Operating Range (V_{SS} = 0 V)

Parameter	Symbol	Rated Value	Unit
Supply voltage	V_{DD}	2.7 to 5.5	V
Ambient temperature	T_a	-40 to +85	° C
Oscillation frequency [1]	f_{OSC}	30 k to 50 M	Hz

[1] 50-MHz oscillator frequency for V_{DD} is 4.5 ~ 5.5 V.

DC Characteristics
(V_{DD} = 4.5 ~ 5.5 V, V_{SS} = 0 V, T_j = -40° C ~ +85° C)

Parameter	Symbol	Conditions	Rated Value			Unit
			Min	Typ[1]	Max	
High-level input voltage	V_{IH}	TTL input	2.2	–	V_{DD}+0.5	V
		CMOS input	0.7xV_{DD}	–	V_{DD}+0.5	V
Low-level input voltage	V_{IL}	TTL input	-0.5	–	0.8	V
		CMOS input	-0.5	–	0.3xV_{DD}	V
TTL-level Schmitt Trigger input threshold voltage	V_{t+}	–	–	1.7	2.2	V
	V_{t-}	–	0.8	1.3	–	V
	ΔVT	V_{t+} - V_{t-}	0.2	0.4	–	V
CMOS-level Schmitt Trigger input threshold voltage	V_{t+}	–	–	3.1	0.76xV_{DD}	V
	V_{t-}	–	0.24xV_{DD}	1.8	–	V
	ΔVT	V_{t+} - V_{t-}	0.6	1.3	–	V
High-level output voltage	V_{OH}	I_{OH} = 2, 4, 8, 12, 16, 24 mA	3.7	–	–	V
Low-level output voltage	V_{OL}	I_{OL} = 2, 4, 8, 12, 16, 24 mA	–	–	0.4	V
		I_{OL} = 48 mA	–	–	0.5	V
High-level input current	I_{IH}	V_{IH} = V_{DD}	–	0.01	10	µA
		V_{IH} = V_{DD}(50 kΩ pull down)	20	100	250	µA
Low-level input current	I_{IL}	V_{IL} = V_{SS}	-10	-0.01	–	µA
		V_{IL} = V_{SS} (50 kΩ pull up)	-250	-100	-20	µA
		V_{IL} = V_{SS} (3 kΩ pull up)	-5	-1.6	-0.5	mA
3-state output leakage current	IOZ_H	V_{OH} = V_{DD}	–	0.01	10	µA
	IOZ_L	V_{OL} = V_{SS}	-10	-0.01	–	µA
		V_{OL} = V_{SS} (50 kΩ pull up)	-250	-100	-20	µA
		V_{OL} = V_{SS} (3 kΩ pull up)	-5	-1.6	-0.5	mA
Stand-by current[2]	I_{DDS}	Output open V_{IH} = V_{DD}, V_{IL} = V_{SS}	–	0.1	100	µA

[1] Typical condition is V_{DD} = 5.0 V and T_j = 25° C for a typical process.

[2] RAM/ROM should be in power-down mode.

DC Characteristics
(V_{DD} = 2.7 ~ 3.6 V, V_{SS} = 0 V, T_j = -40° C ~ +85° C)

Parameter	Symbol	Conditions	Rated Value			Unit
			Min	Typ[1]	Max	
High-level input voltage	V_{IH}	CMOS input	0.7xV_{DD}	–	V_{DD}+0.5	V
Low-level input voltage	V_{IL}	CMOS input	-0.5	–	0.3xV_{DD}	V
CMOS-level Schmitt Trigger input threshold voltage	V_{t+}	–	–	2	0.76xV_{DD}	V
	V_{t-}	–	0.24xV_{DD}	1	–	V
	ΔVT	V_{t+} - V_{t-}	0.1xV_{DD}	1	–	V
High-level output voltage	V_{OH}	I_{OH} = 1, 2, 4, 6, 8, 12 mA	2.2	–	–	V
Low-level output voltage	V_{OL}	I_{OL} = 1, 2, 4, 6, 8, 12, 24 mA	–	–	0.4	V
High-level input current	I_{IH}	V_{IH} = V_{DD}	–	0.01	1	µA
		V_{IH} = V_{DD} (100 kΩ pull down)	5	35	120	µA
Low-level input current	I_{IL}	V_{IL} = V_{SS}	-1	-0.01	–	µA
		V_{IL} = V_{SS} (100 kΩ pull up)	-120	-35	-5	µA
		V_{IL} = V_{SS} (6 kΩ pull up)	-2	-.55	-.120	mA
3-state output leakage current	IOZ_H	V_{OH} = V_{DD}	–	0.01	1	µA
	IOZ_L	V_{OL} = V_{SS}	-1	-0.01	–	µA
		V_{OL} = V_{SS} (100 kΩ pull up)	-120	-35	-5	µA
		V_{OL} = V_{SS} (6 kΩ pull up)	-2	-.55	-.12	mA
Stand-by current[2]	I_{DDS}	Output open V_{IH} = V_{DD}, V_{IL} = V_{SS}	–	0.1	10	µA

[1] Typical condition is V_{DD} = 3.3 V and T_j = 25° C for a typical process.

[2] RAM/ROM should be in power-down mode.

AC Characteristics
(Core V_{DD} = 5 V, V_{SS} = 0 V, T_j = 25° C)

Parameter		Driving Type	Conditions	Rated Value [1][2]	Unit
Internal gate delay times	Inverter 2-input NAND 2-input NOR	1x 1x 1x	Input tr/tf = V_{DD} /1.0 ns Output loading: FO = 1, L = 0 mm	0.20 0.25 0.28	ns
	Inverter	1x 2x 4x	Input tr/tf = V_{DD} /1.0 ns Output loading: FO = 2, L = 2 mm L = Metal length	0.47 0.35 0.22	ns
	2-input NAND	1x 2x 4x		0.57 0.36 0.25	ns
	2-input NOR	1x 2x 4x		0.69 0.53 0.51	ns
Flip-flop (FD1A)	Delay time: Set-up time: Hold time:	CLK↑ to Q D to CLK↑ CLK↑ to D		1.63 1.5 0.1[3]	ns
Toggle frequency of flip-flop			FO = 1, L = 0 mm	500	MHz

[1] For the purpose of this table, Rated Value is calculated as an average of the LH and HL delay times of each macro type.

[2] Characteristics are quoted for a typical process.

[3] th_L (C,D) ≥ 0.1 ns. For I/O information, please refer to the AC Characteristics listed in the I/O table.

AC Characteristics
(Core V_{DD} = 3.3 V, V_{SS} = 0 V, T_j = 25° C)

Parameter		Driving Type	Conditions	Rated Value [1][2]	Unit
Internal gate delay times	Inverter 2-input NAND 2-input NOR	1x 1x 1x	Input tr/tf = V_{DD} /1.0 ns Output loading: FO = 1, L = 0 mm	0.31 0.38 0.43	ns
	Inverter	1x 2x 4x	Input tr/tf = V_{DD} /1.0 ns Output loading: FO = 2, L = 2 mm L = Metal length	0.72 0.54 0.34	ns
	2-input NAND	1x 2x 4x		0.87 0.55 0.38	ns
	2-input NOR	1x 2x 4x		1.06 0.81 0.78	ns
Flip-flop (FD1A)	Delay time: Set-up time: Hold time:	CLK↑ to Q D to CLK↑ CLK↑ to D		2.66 2.29 0.15[3]	ns
Toggle frequency of flip-flop			FO = 1, L = 0 mm	327	MHz

[1] For the purpose of this table, Rated Value is calculated as an average of the LH and HL delay times of each macro type

[2] Characteristics are quoted for a typical process.

[3] th_L (C,D) ≥ 0.15 ns. For I/O information, please refer to the AC Characteristics listed in the I/O table.

AC Characteristics
(I/O V_{DD} = 3.3 V or 5 V, V_{SS} = 0 V, T_j = 25° C)

Parameter	Type		Conditions	Rated Values For $V_{DD\ Conditon}$ [1][2] LL 3-V Ext 3-V Core	HL 3-V Ext [3] 5-V Core	LH 5-V Ext [3] 3-V Core	HH 5-V Ext 5-V Core	Unit
Input buffer delay times	TTL input		Input tr, tf = 0.2 ns/3.3 V FO = 2, L = 2 mm[4]	–	–	–	0.82	ns
	CMOS input		Input tr, tf = 0.3 ns/5 V (LH, HH) tr, tf = 0.2 ns/3.3 V (LL, HL) FO = 2, L = 2 mm [4]	0.95	1.78	0.96	0.71	ns
Output buffer delay times (t_{in} = 0.3 ns/5 V for LH & HL or t_{in} = 0.2 ns/3.3 V for LL & HL)	Push-pull for HH & LH	4 mA	C_L = 20 pF	–	–	2.90	1.39	ns
		8 mA	C_L = 50 pF	–	–	3.86	1.86	
		16 mA	C_L = 100 pF	–	–	3.87	2.03	
		24 mA	C_L = 150 pF	–	–	3.69	2.51	
	Push-pull for LL & HL	2 mA	C_L = 20 pF	2.30	1.53	–	–	ns
		4 mA	C_L = 50 pF	3.11	1.99	–	–	
		8 mA	C_L = 100 pF	3.34	2.18	–	–	
		12 mA	C_L = 150 pF	3.76	2.58	–	–	
Output buffer transition time (20-80%)	Push-pull		C_L = 150 pF for 24 mA buffer [5]	–	–	3.38 (r)	2.66 (r)	ns
				–	–	3.59 (f)	3.04 (f)	
	Push-pull with slew rate control			–	–	9.20 (r)	3.60 (r)	ns
				–	–	7.86 (f)	3.62 (f)	

[1] Rated values are calculated as an average of the L-H and the H-L delay times for each macro type.

[2] Characteristics are quoted for a typical process.

[3] Parameters include level shifter cell where appropriate.

[4] For L = 2 mm, metal capacitance value of 0.304 pF has been chosen.

[5] Output rising and falling times are specified.

MACRO LIBRARY

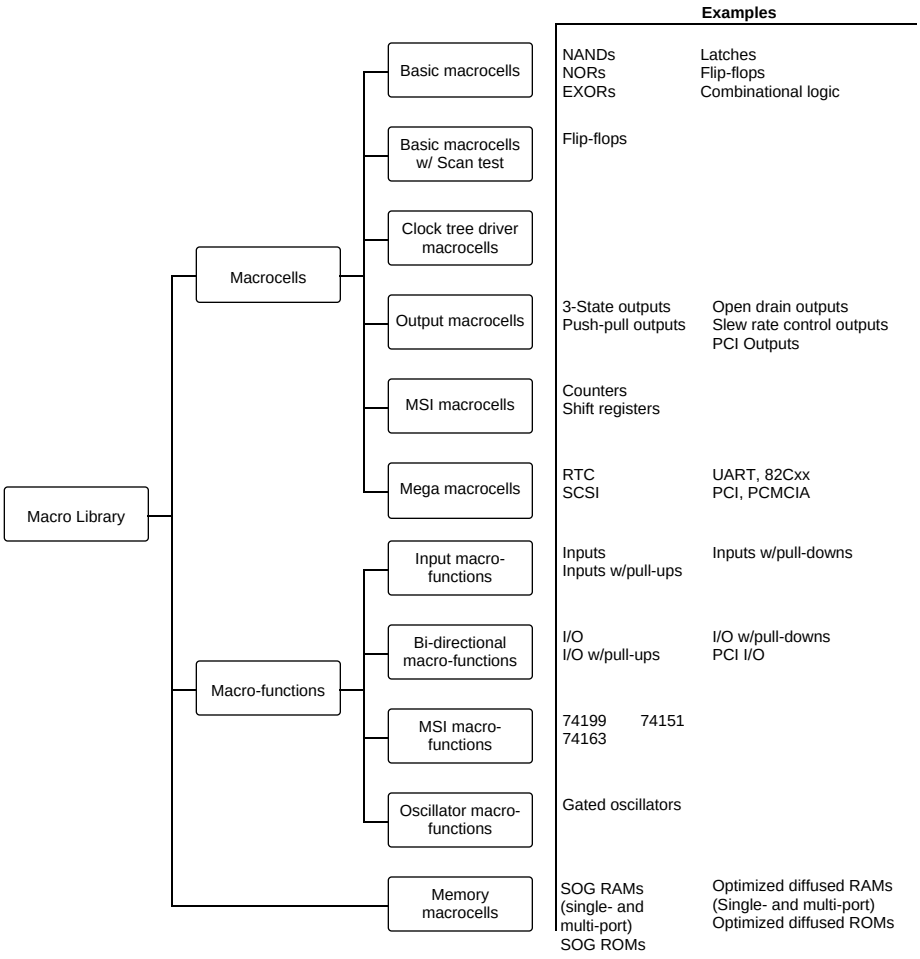


Figure 4. OKI Macro Library

MACROCELLS FOR DRIVING CLOCK TREES

OKI offers clock-tree drivers that guarantee a skew time of less than 1.0 ns. The advanced layout software uses dynamic driver placement and sub-trunk allocation to optimize the clock-tree implementation for a particular circuit. Features of the clock-tree driver-macrocells include:

- Clock skew ≤ 1.0 ns
- Automatic fan-out balancing

- Dynamic sub-trunk allocation
- Single clock tree driver logic symbol
- Single-level clock drivers
- Automatic branch length minimization
- Dynamic driver placement
- Up to four clock trunks

The clock-skew management scheme is described in detail in the *0.8µm Technology Clock Skew Management Application Note*

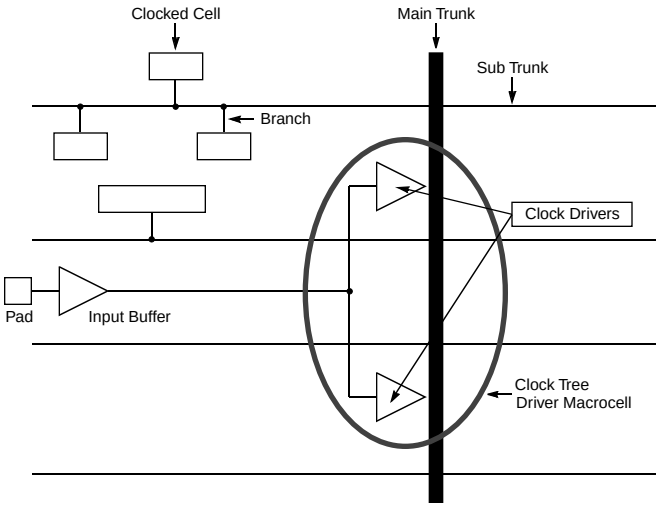


Figure 5. Clock Tree Structure

OUTPUT DRIVER MACROCELLS FOR SLEW RATE CONTROL

The slew-rate-control output driver macrocells reduce both simultaneous-switching noise and output-ringing noise. The output transistors are split into two sets; first, one set of output transistors drive the output pads, then, after the output passes the threshold, the second set of output transistors drive the I/O pads.

Figure 6 below shows output drivers configured for slew-rate control. All outputs with a drive of 8 mA or more are available with slew-rate control.

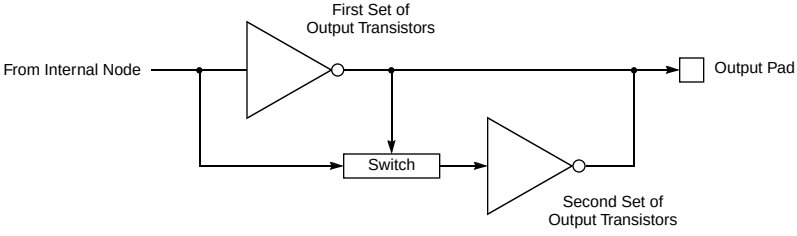


Figure 6. Slew Rate Control Output Buffer

AUTOMATIC TEST VECTOR GENERATION

OKI's 0.8µm ASIC technologies support Automatic Test Vector Generation (ATVG) using full scan-path design techniques, including the following:

- Increases fault coverage ≥ 95%
- Uses Synopsys Test Compiler
- Automatically inserts scan structures
- Connects scan chains
- Traces and reports scan chains
- Checks for rule violations
- Generates complete fault reports
- Allows multiple scan chains
- Supports vector compaction

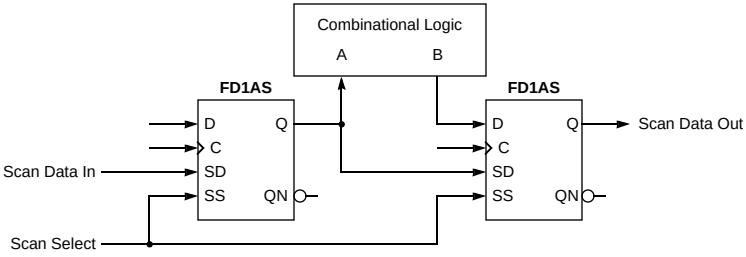
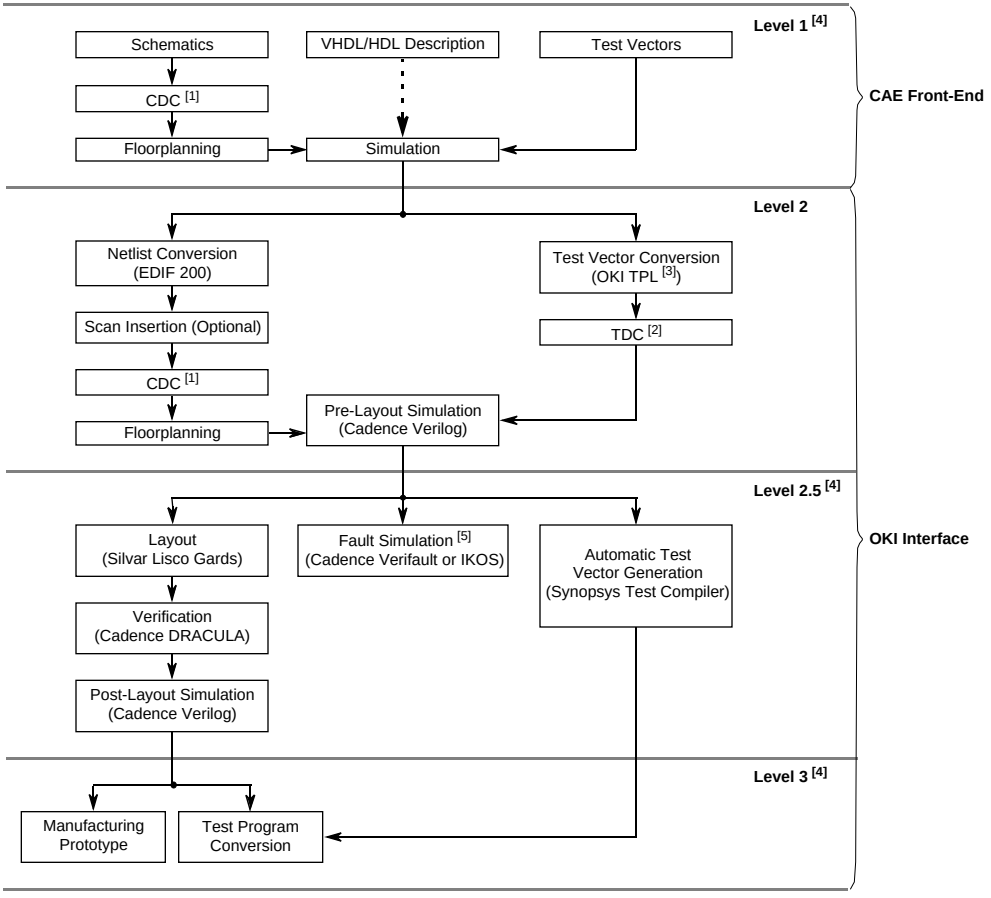


Figure 7. Full Scan Path Configuration

DESIGN PROCESS



[1] OKI Circuit Data Check program (CDC) verifies logic design rules
[2] OKI Test Data Check program (TDC) verifies test vector rules
[3] OKI Test Pattern Language (TPL)
[4] Alternate Customer-OKI design interfaces available in addition to standard level 2
[5] Standard design process includes fault simulation

Figure 8. OKI Design Process

OKI ADVANCED DESIGN CENTER CAD TOOLS

- Floorplanning for front-end simulation and back-end layout controls
- Clock tree structures improve first-time silicon success by eliminating clock skew problems
- Power calculation which predicts circuit power under simulation conditions to accurately model package requirements

Design Kits

Vendor	Platform	Operating System [1]	Vendor Software [1]	Description
Cadence	Sun[2]	SunOS Solaris [3]	Composer Verilog Veritime Verifault Synergy Concept Leapfrog	Design capture Simulation Timing analysis Fault grading Design synthesis Design capture VHDL simulation
	HP9000, 7xx	HP-UX	Composer Verilog Veritime Verifault Synergy	Design capture Simulation Timing analysis Fault simulation Design synthesis
	IBM RS6000	AIX	Composer Verilog Synergy	Design capture Simulation Design synthesis
IKOS	Sun [2]	SunOS Solaris [3]	Alchemy	Simulation Fault grading
Mentor Graphics	HP9000, 7xx	HP-UX	IDEA QuickVHDL QuickSim II QuickPath QuickFault QuickGrade AutoLogic DFT Advisor	Design capture VHDL simulation Logic simulation Timing analysis Fault grading Fault grading Design synthesis Test synthesis
	Sun [2]	SunOS Solaris [3]		
Synopsys	(Interface to Mentor Graphics, VIEWLogic) Sun [2] HP9000, 7xx IBM RS6000	SunOS Solaris [3] HP-UX AIX	Design Compiler HDL/VHDL Compiler Test Compiler VSS	Compilation Design synthesis Test synthesis VHDL simulation
VIEWLogic	Sun [2]	SunOS Solaris [3]	Workview Plus Powerview Vantage Optium ViewTime/Motive [3] ViewRetargeter ViewSynthesis ViewSim with VSO	Design capture Simulation VHDL simulation Timing analysis Design migration Design synthesis Simulation
	PC	DOS Windows Windows NT[3]		

[1] Contact OKI Application Engineering for current software versions.

[2] Sun® or Sun-compatible.

[3] In development.

PACKAGE OPTIONS

MSM38S0000 42-Alloy QFP Package Menu

Master Slice MSM38S...	I/O Pads[1]	QFP (42-Alloy)							
		44	60	80	100	128	136	144	160
0110	100	●	●	●	●				
0210	136				●	●	●		
0300	160				●	●	●	●	●
0570	216					●	●	●	●
0980	280					●	●	●	●
1500	344							●	●
2250	420								●
Body Size (mm)		9.5 x 10.5	15 x 19	14 x 20	14 x 20	28 x 28	28 x 28	28 x 28	28 x 28
Lead Pitch (mm)		0.8	1	0.8	0.65	0.8	0.65	0.65	0.65

[1] I/O pads can be used for input, output, bidirectional, power, or ground signals.

● = Available now

MSM38S0000 Cu-Alloy QFP and TQFP Package Menu

Master Slice MSM38S...	I/O Pads[1]	QFP (Cu-Alloy)					TQFP				
		176	208	240	272	304	44[2]	64[2]	80[2]	100[2]	144[3]
0110	100						●	●	●	●	
0210	136						●	●	●	●	●
0300	160	●						●	●	●	●
0570	216	●	●						●	●	●
0980	280	●	●	●							●
1500	344	●	●	●	●						●
2250	420	●	●	●	●	●					
Body Size (mm)		24 x 24	28 x 28	32 x 32	36 x 36	40 x 40	10 x 10	10 x 10	12 x 12	14 x 14	20 x 20
Lead Pitch (mm)		0.5	0.5	0.5	0.5	0.5	0.8	0.5	0.5	0.5	0.5

[1] I/O Pads can be used for input, output, bidirectional, power, or ground signals.

[2] 1.0mm thick

[3] 1.4mm thick

● = Available now

MSM38S0000 PLCC and CPGA Package Menu

Master Slice MSM38S...	I/O Pads[1]	PLCC		CPGA				
		44	84	88	132	176	208	401
0110	100	●		●				
0210	136	●	●	●	●			
0300	160	●	●	●	●			
0570	216		●		●	●		
0980	280				●	●	●	
1500	344				●	●	●	
2250	420				●			●
Body Size (mm)		17x17	28x28	33x33	35x35	38x38	44x44	50x50
Lead Pitch (mm)		1.27	1.27	2.54	2.54	2.54	2.54	1.27

[1] I/O Pads can be used for input, output, bi-directional, power or ground.

● = Available now

MSM98S000 QFP Package Menu

Master Slice MSM98S...	I/O Pads [1]	PQFP (42-Alloy)								PQFP (Cu-Alloy)					TQFP			
		44	60	80	100	128	136	144	160	176	208	240	272	304	44	64	80	100
020x020	80	❍	❍	❍											❍	❍	❍	
023x023	92	●	❍	❍											❍	❍	●	
026x026	104	●	❍	❍	❍										●	❍	❍	●
029x029	116	❍	❍	❍	❍										●	❍	●	●
032x032	128	❍	❍	❍	❍	●									●	❍	❍	●
035x035	140	❍	❍	❍	❍	●	●								❍	●	●	❍
038x038	152	❍	❍	●	❍	●	●	❍								●	❍	●
041x041	164	❍	❍	●	●	●	●	●	❍							❍	●	❍
044x044	176	❍	❍	❍	❍	●	●	●	❍								❍	●
047x047	188	❍	❍	❍	●	●	●	●	●	❍							●	●
050x050	200	❍	❍	❍	❍	❍	●	●	●	❍							●	❍
053x053	212	❍	❍	❍	❍	●	●	●	●	❍	❍						●	❍
056x056	224	❍	❍	❍	❍	●	●	●	●	❍	●						●	●
059x059	236	❍	❍	❍	❍	●	❍	●	●	●	●						❍	●
062x062	248	❍	❍	❍	●	●	●	●	●	❍	❍						❍	●
065x065	260	❍	❍	❍	❍	●	●	●	●	❍	●	❍					❍	●
068x068	272	❍	❍	❍	❍	❍	●	●	●	●	●	●					❍	❍
071x071	284					●	●	●	●	❍	❍	❍						
074x074	296					●	●	●	●	❍	❍	❍						
077x077	308					●	●	●	●	❍	●	❍						
080x080	320					●	●	●	●	❍	●	❍						
083x083	332					●	●	●	●	❍	●	❍						
086x086	344					❍	❍	●	❍	●	●	●	●					
089x089	356					❍	●	❍	❍	●	●	●	❍					
092x092	368					●	●	●	❍	❍	●	●	❍					
095x095	380					●	❍	●	●	❍	●	❍	❍					
098x098	392					●	❍	●	●	❍	❍	❍	❍					
101x101	404					❍	●	❍	●	❍	❍	❍	❍					
104x104	416					❍	●	❍	●	●	●	❍	●	●				
Body Size		9.5 x 10.5	15 x 19	14 x 20	14 x 20	28 x 28	28 x 28	28 x 28	28 x 28	28 x 28	24 x 24	32 x 32	36 x 36	40 x 40	10 x 10	10 x 10	12 x 12	14 x 14
Lead Pitch (mm)		0.8	1	0.8	0.65	0.8	0.65	0.65	0.65	0.5	0.5	0.5	0.5	0.5	0.8	0.5	0.5	0.5

[1] I/O pads can be used for input, output, bidirectional, power, or ground connections.

● = Available now

❍ = In development

MSM98S000 PLCC and CPGA Package Menu

Master Slice MSM98S...	I/O Pads [1]	PLCC		CPGA				
		44	84	72	88	132	176	208
020x020	80	❍		❍				
023x023	92	❍		❍	❍			
026x026	104	❍		❍	❍			
029x029	116	●	●	❍	●			
032x032	128	●	●	❍	●	❍		
035x035	140	●	●	❍	●	❍		
038x038	152		●	❍	●	❍		
041x041	164		●	❍	●	❍		
044x044	176		●	❍	●	●		
047x047	188		●	❍	●	●	❍	
050x050	200		●	●	●	●	❍	
053x053	212		●	●	●	●	❍	
056x056	224		●	●	❍	●	❍	❍
059x059	236		●	●	❍	●	❍	❍
062x062	248		●	●	❍	●	❍	❍
065x065	260		●	●	❍	●	❍	❍
068x068	272		●	●	❍	●	●	❍
071x071	284		●	●	❍	●	●	❍
074x074	296			●	❍	●	●	❍
077x077	308			❍	❍	●	●	❍
080x080	320			❍	❍	●	●	●
083x083	332			❍	❍	●	●	●
086x086	344			❍	❍	●	●	●
089x089	356			❍	❍	●	●	●
092x092	368			❍	❍	●	●	●
095x095	380			❍	❍	●	●	●
098x098	392			❍	❍	●	❍	●
101x101	404			❍	❍	●	❍	●
104x104	416			❍	❍	●	❍	●
Body Size		17 x 17	28 x 28	28 x 28	33 x 33	35 x 35	38 x 38	44 x 44
Lead Pitch (mm)		1.27	1.27	2.54	2.54	2.54	2.54	2.54

[1] I/O pads can be used for input, output, bidirectional, power, or ground signals.

● = Available now

❍ = In development

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OKI Semiconductor

Corporate Headquarters

785 N. Mary Avenue
Sunnyvale, CA 94086-2909
Tel: 408/720-1900
Fax: 408/720-1918