Ultra-Low Noise, High-Speed Operational Amplifier with Shutdown

Check for Samples: LMH6629

FEATURES

- **Specified for V_S = 5V, R_L = 100Ω, A_V = 10V/V WSON-8 Package, unless Specified**
- **–3dB Bandwidth 900 MHz**
- **Input Voltage Noise 0.69 nV/√Hz**
- **Input Offset Voltage Max. Over Temperature ±0.8 mV**
- **Slew Rate 1600 V/ µs**
- **HD2 @ f = 1MHz, $2V_{PP}$ −90 dBc**
- **HD3 @ f = 1MHz, $2V_{PP}$ −94 dBc**
- **Supply Voltage Range 2.7V to 5.5V**
- **Typical Supply Current 15.5 mA**
- **Selectable Min. Gain ≥4 or ≥10 V/V**
- **Enable Time 75 ns**
- **Output Current ±250 mA**
- **WSON-8 and SOT-23-5 Packages**

APPLICATIONS

- **Instrumentation Amplifiers**
- **Ultrasound Pre-amps**
- **Wide-band Active Filters**
- **Opto-Electronics**
- **Medical Imaging Systems**
- **Base-Station Amplifiers**
- **Low-Noise Single Ended to Differential Conversion**
- **Trans-Impedance Amplifier**

DESCRIPTION

The LMH6629 is a high-speed, ultra low-noise amplifier designed for applications requiring wide bandwidth with high gain and low noise such as in communication, test and measurement, optical and ultrasound systems.

The LMH6629 operates on 2.7 to 5.5V supply with an input common mode range that extends below ground and outputs that swing to within 0.8V of the rails for ease of use in single supply applications. Heavy loads up to ±250 mA can be driven by high-frequency large signals with the LMH6629's –3dB bandwidth of 900 MHz and 1600 V/µs slew rate. The LMH6629 (WSON-8 package only) has user-selectable internal compensation for minimum gains of 4 or 10 controlled by pulling the COMP pin low or high, thereby avoiding the need for external compensation capacitors required in competitive devices. Compensation for the SOT-23-5 package is internally set for a minimum stable gain of 10 V/V. The WSON-8 package also provides the power-down enable/ disable feature.

The low-input noise (0.69nV/√Hz and 2.6 pA/√Hz), low distortion (HD2/ HD3 = −90 dBc/−94 dBc) and ultra-low DC errors (800 µV V_{OS} maximum over temperature, ±0.45 µV/°C drift) allow precision operation in both AC- and DC-coupled applications.

The LMH6629 is fabricated in National Semiconductor's proprietary SiGe process and is available in a 3mm x 3mm 8-pin WSON, as well as the SOT-23-5, package.

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Typical Application Circuit

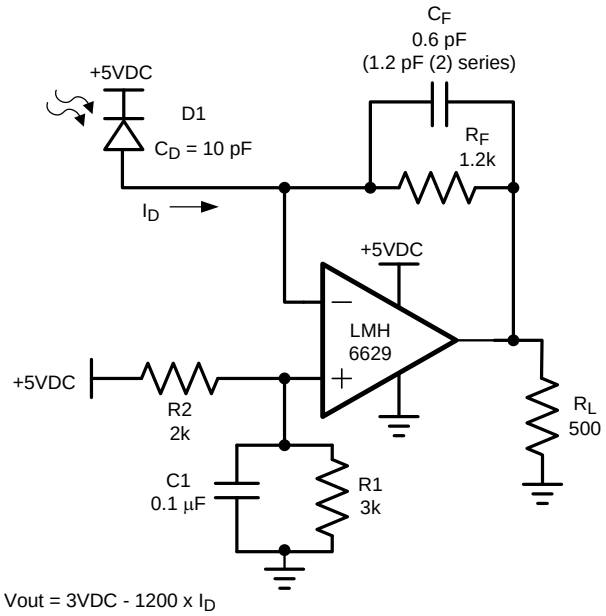


Figure 1. Transimpedance Amplifier

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Connection Diagram

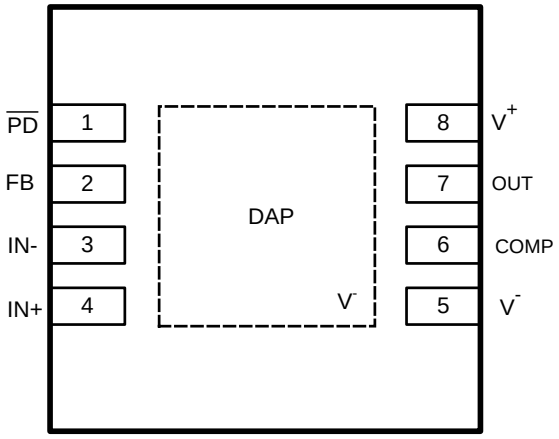


Figure 2. WSON-8 (Top View)
See Package Number NGQ0008A

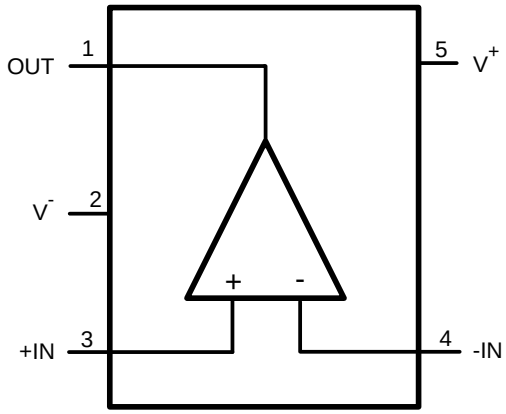


Figure 3. SOT-23-5 (Top View)
See Package Number DBV

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Absolute Maximum Ratings (1)(2)(3)

ESD Tolerance (4)	
Human Body Model	2kV
Machine Model	200V
Charge-Device Model	750V
Positive Supply Voltage	−0.5 to 6.0V
Differential Input Voltage	3V
Analog Input Voltage Range	−0.5 to V_S
Digital Input Voltage	−0.5 to V_S
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Soldering Information http://www.ti.com/lit/SNOA549	

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Human Body Model, applicable std. JESD22-A114C. Machine Model, applicable std. JESD22-A115-A. Field Induced Charge Device Model, applicable std. JESD22-C101-C.

Operating Ratings (1)

Supply Voltage ($V^+ - V^-$)	2.7V to 5.5V
Operating Temperature Range	−40°C to +125°C
Package	(θ_{JA})
WSON-8	71°C/W
SOT-23-5	179°C/W

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

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5V Electrical Characteristics

The following specifications apply for single supply with V_S = 5V, R_L = 100Ω terminated to 2.5V, gain = 10V/V, V_O = $2V_{PP}$, V_{CM} = V_S/2, COMP Pin = HI (WSON-8 package), unless otherwise noted. **Boldface** limits apply at the temperature extremes. (1).

Symbol	Parameter	Conditions	Min (2)	Typ (2)	Max (2)	Units
DYNAMIC PERFORMANCE						
SSBW	Small signal −3dB bandwidth	V_O = 200 mV_{PP}, WSON-8 package		900		MHz
		V_O = 200 mV_{PP}, SOT-23-5 package		1000		
		A_V= 4, V_O = 200 mV_{PP}, COMP Pin = LO		800		
LSBW	Large signal −3dB bandwidth	V_O = $2V_{PP}$		380		MHz
		COMP Pin = LO, A_V= 4, V_O = $2V_{PP}$		190		
	0.1 dB bandwidth	A_V= 10, V_O = 200 mV_{PP}, WSON-8 package		330		MHz
		A_V= 10, V_O = 200 mV_{PP}, SOT-23-5 package		190		
		A_V= 4, V_O = 200 mV_{PP}, COMP Pin = LO		95		
	Peaking	V_O = 200 mV_{PP}, WSON-8 package		0		dB
		V_O = 200 mV_{PP}, SOT-23-5 package		2		
SR	Slew rate	A_V= 10, 2V step		1600		V/µs
		A_V= 4, 2V step, COMP Pin = LO		530		
t_r/ t_f	Rise/fall time	A_V= 10, 2V step, 10% to 90%, WSON-8 package		0.90		ns
		A_V= 10, 2V step, 10% to 90%, SOT-23-5 package		0.95		
		A_V= 4, 2V step, 10% to 90%, COMP Pin = LO, (Slew Rate Limited)		2.8		
T_s	Settling time	A_V= 10, 1V step, ±0.1%		42		
	Overload Recovery	V_{IN} = $1V_{PP}$		2		
NOISE AND DISTORTION						
HD2	2nd order distortion	fc = 1MHz, V_O = $2V_{PP}$		−90		dBc
		COMP Pin = LO, A_V= 4, fc = 1 MHz, V_O = $2V_{PP}$		−88		
		fc = 10 MHz, V_O = $2V_{PP}$		−70		
		COMP Pin = LO, fc = 10 MHz, A_V= 4V, V_O = $2V_{PP}$		−65		
HD3	3rd order distortion	fc = 1MHz, V_O = $2V_{PP}$		−94		dBc
		COMP Pin = LO, A_V= 4, fc = 1MHz, V_O = $2V_{PP}$		−87		
		fc = 10 MHz, V_O = $2V_{PP}$		−82		
		COMP Pin = LO, fc = 10 MHz, V_O = $2V_{PP}$		−75		
OIP3	Two-tone 3rd order intercept point	fc = 25 MHz, V_O = 2 V_{PP} composite		31		dBm
		fc = 75 MHz, V_O = $2V_{PP}$ composite		27		
e_n	Noise Voltage	Input referred f > 1MHz		0.69		nV/√Hz
i_n	Noise current			2.6		pA/√Hz
NF	Noise Figure	R_S = R_T = 50Ω		8.0		dB

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.

(2) Negative input current implies current flowing out of the device.

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5V Electrical Characteristics (continued)

The following specifications apply for single supply with V_S = 5V, R_L = 100Ω terminated to 2.5V, gain = 10V/V, V_O = $2V_{PP}$, V_{CM} = V_S/2, COMP Pin = HI (WSON-8 package), unless otherwise noted. **Boldface** limits apply at the temperature extremes. (1).

Symbol	Parameter	Conditions	Min (2)	Typ (2)	Max (2)	Units
ANALOG I/O						
CMVR	Input voltage range	CMRR > 70 dB, WSON-8 package	−0.30		3.8	V
		CMRR > 70 dB, SOT-23-5 package		−0.30 to 3.8		
V_O	Output voltage range	R_L = 100Ω to V_S/2	0.89 **0.95**	0.82 to 4.19	4.0 **3.9**	V
		No Load	0.76 **0.85**	0.72 to 4.28	4.1 **4.0**	
I_{OUT}	Linear output current	V_O = 2.5V (3)		250		mA
V_{OS}	Input offset voltage			±150	±780 **±800**	µV
TcV_{OS}	Input offset voltage temperature drift	(4)		±0.45		µV/°C
I_{BI}	Input bias current	(5)		−15	−23 **−37**	µA
I_{OS}	Input offset current			±0.1	±1.8 **±3.0**	µA
T_CI_{OS}	Input offset voltage temperature drift	(4)		±2.8		nA/°C
C_{CM}	Input capacitance	Common Mode		1.7		pF
R_{CM}	Input resistance	Common Mode		450		kΩ
MISCELLANEOUS PARAMETERS						
CMRR	Common mode rejection ratio	V_{CM} from 0V to 3.7V, WSON-8 package	82 **70**	87		dB
		V_{CM} from 0V to 3.7V, SOT-23-5 package		87		
PSRR	Power supply rejection ratio		81 **78**	83		
A_{VOL}	Open loop gain	WSON-8 package	74 **72**	78		
		SOT-23-5 package		78		
DIGITAL INPUTS/TIMING						
V_{IL}	Logic low-voltage threshold	$\overline{PD}$ and COMP pins, WSON-8 package			0.8	V
V_{IH}	Logic high-voltage threshold	$\overline{PD}$ and COMP pins, WSON-8 package	2.5			
I_{IL}	Logic low-bias current	$\overline{PD}$ and COMP pins = 0.8V, WSON-8 package (5)	−23 **−19**	−28	−34 **−38**	µA
I_{IH}	Logic high-bias current	$\overline{PD}$ and COMP pins = 2.5V, WSON-8 package (5)	−16 **−14**	−22	−27 **−29**	
T_{en}	Enable time	WSON-8 package		75		ns
T_{dis}	Disable time	WSON-8 package		80		
POWER REQUIREMENTS						
I_S	Supply Current	No Load, Normal Operation ($\overline{PD}$ Pin = HI or open for WSON-8 package)		15.5	16.7 **18.2**	mA
		No Load, Shutdown ($\overline{PD}$ Pin =LO for WSON-8 package)		1.1	1.85 **2.0**	

(3) The maximum continuous output current (I_{OUT}) is determined by device power dissipation limitations. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C
(4) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(5) Negative input current implies current flowing out of the device.

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3.3V Electrical Characteristics

The following specifications apply for single supply with V_S = 3.3V, R_L = 100Ω terminated to 1.65V, gain = 10V/V, V_O = 1V_{PP}, V_{CM} = V_S/2, COMP Pin = HI (WSON-8 package), unless otherwise noted. **Boldface** limits apply at the temperature extremes. (1)

Symbol	Parameter	Conditions	Min (2)	Typ (2)	Max (2)	Units
DYNAMIC PERFORMANCE						
SSBW	Small signal −3dB bandwidth	V_O = 200 mV_{PP}, WSON-8 package		820		MHz
		V_O = 200 mV_{PP}, SOT-23-5 package		950		
		COMP Pin = LO, A_V= 4, V_O = 200 mV_{PP}		730		
LSBW	Large signal −3dB bandwidth	V_O = 1V_{PP}		540		MHz
		COMP Pin = LO, A_V= 4, V_O = 1V_{PP}		320		
	0.1 dB bandwidth	A_V= 10, V_O = 200 mV_{PP}, WSON-8 package		330		MHz
		A_V= 10, V_O = 200 mV_{PP}, SOT-23-5 package		190		
		COMP Pin = LO, A_V= 4, V_O = 200 mV_{PP}		85		
	Peaking	V_O = 200 mV_{PP}, WSON-8 package		0		dB
		V_O = 200 mV_{PP}, SOT-23-5 package		1.8		
SR	Slew rate	A_V= 10, 1.3V step		1100		V/µs
		COMP Pin = LO, A_V= 4, 1.3V step		500		
t_r/ t_f	Rise/fall time	A_V= 10, 1V step, 10% to 90%, WSON-8 package		0.7		ns
		A_V= 10, 1V step, 10% to 90%, SOT-23-5 package		0.55		
		A_V= 4, COMP Pin = LO, 1V step, 10% to 90% (Slew Rate Limited)		1.3		
T_s	Settling time	A_V= 10, 1V step, ±0.1%		70		
	Overload Recovery	V_{IN} = 1V_{PP}		2		
NOISE AND DISTORTION						
HD2	2nd order distortion	fc = 1MHz, V_O = 1V_{PP}		–82		dBc
		COMP Pin = LO, A_V= 4, fc = 1MHz, V_O = 1V_{PP}		-88		
		fc = 10 MHz, V_O = 1V_{PP}		-67		
		COMP Pin = LO, fc = 10 MHz, A_V= 4V, V_O = 1V_{PP}		-74		
HD3	3rd order distortion	fc = 1MHz, V_O = 1V_{PP}		-94		dBc
		COMP Pin = LO, A_V= 4, fc = 1MHz, V_O = 1V_{PP}		-112		
		fc = 10 MHz, V_O = 1V_{PP}		-79		
		COMP pin = LO, fc = 10 MHz, V_O = 1V_{PP}		–96		
OIP3	Two-tone 3rd Order Intercept Point	fc = 25 MHz, V_O = 1V_{PP} composite		30		dBm
		fc = 75 MHz, V_O = 1V_{PP} composite		26		
e_n	Noise voltage	Input referred, f > 1MHz		0.69		nV/√HZ
i_n	Noise current			2.6		pA/√HZ
NF	Noise figure	R_S = R_T = 50Ω		8.0		dB

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.

(2) Typical numbers are the most likely parametric norm. Bold numbers refer to over-temperature limits.

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3.3V Electrical Characteristics (continued)

The following specifications apply for single supply with V_S = 3.3V, R_L = 100Ω terminated to 1.65V, gain = 10V/V, V_O = $1V_{PP}$, V_{CM} = V_S/2, COMP Pin = HI (WSON-8 package), unless otherwise noted. **Boldface** limits apply at the temperature extremes. (1)

Symbol	Parameter	Conditions	Min (2)	Typ (2)	Max (2)	Units
ANALOG I/O						
CMVR	Input voltage range	CMRR > 70 dB, WSON-8 package	−0.30		2.1	V
		CMRR > 70 dB, SOT-23-5 package		−0.30 to 2.1		
V_O	Output voltage range	R_L = 100Ω to V_S/2	0.90 **0.95**	0.79 to 2.50	2.4 **2.3**	V
		No load	0.76 **0.80**	0.70 to 2.60	2.5 **2.4**	
I_{OUT}	Linear output current	V_O = 1.65V (3)		230		mA
V_{OS}	Input Offset Voltage			±150	±680 **±700**	µV
TcV_{OS}	Input offset voltage temperature drift	(4)		±1		µV/°C
I_{BI}	Input Bias Current	(5)		−15	−23 **−35**	µA
I_{OS}	Input Offset Current			±0.13	±1.8 **±3.0**	µA
T_CI_{OS}	Input offset voltage temperature drift	(4)		±3.2		nA/°C
C_{CM}	Input Capacitance	Common Mode		1.7		pF
R_{CM}	Input Resistance	Common Mode		1		MΩ
MISCELLANEOUS PARAMETERS						
CMRR	Common Mode Rejection Ratio	V_{CM} from 0V to 2.0V, WSON-8 package	84 **81**	87		dB
		V_{CM} from 0V to 2.0V, SOT-23-5 package		87		
PSRR	Power supply rejection ratio		82 **79**	84		
A_{VOL}	Open Loop Gain	WSON-8 package	78 **73**	79		
		SOT-23-5 package		79		
DIGITAL INPUTS/TIMING						
V_{IL}	Logic low-voltage threshold	$\overline{PD}$ and COMP pins, WSON-8 package			0.8	V
V_{IH}	Logic high-voltage threshold		2.0			
I_{IL}	Logic low-bias current	$\overline{PD}$ and COMP pins = 0.8V, WSON-8 package (5)	-17 **−14**	−23	−28 **−32**	µA
I_{IH}	Logic high-bias current	$\overline{PD}$ and COMP pins = 2.0V, WSON-8 package (5)	−16 **−13**	−22	−27 **−31**	
T_{en}	Enable time	WSON-8 package		75		ns
T_{dis}	Disable time	WSON-8 package		80		
POWER REQUIREMENTS						
I_S	Supply Current	No Load, Normal Operation ($\overline{PD}$ Pin = HI or open for WSON-8 package)		13.7	14.9 **16.0**	mA
		No Load, Shutdown ($\overline{PD}$ Pin = LO for WSON-8 package)		0.89	1.4 **1.5**	

(3) The maximum continuous output current (I_{OUT}) is determined by device power dissipation limitations. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C
(4) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(5) Negative input current implies current flowing out of the device.

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Typical Performance Characteristics

Unless otherwise specified, V_S = ±2.5V, R_f = 240Ω, R_L = 100Ω, V_O = $2V_{PP}$, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).

Inverting Frequency Response

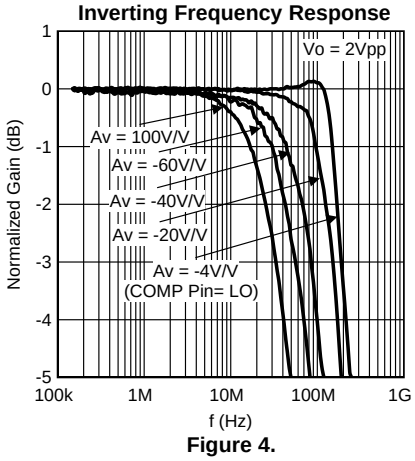


Figure 4.

Inverting Frequency Response

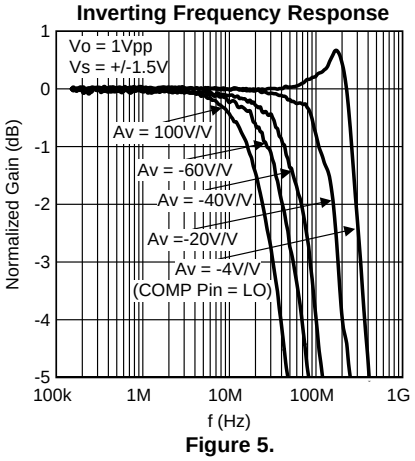


Figure 5.

Non-Inverting Frequency Response

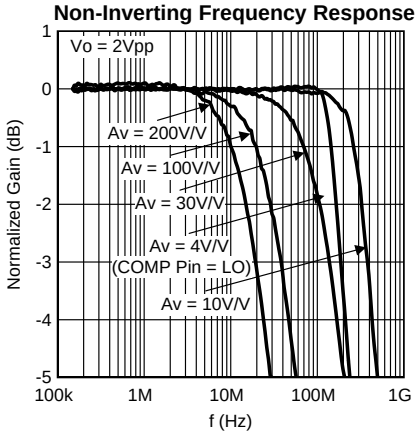


Figure 6.

Non-Inverting Frequency Response

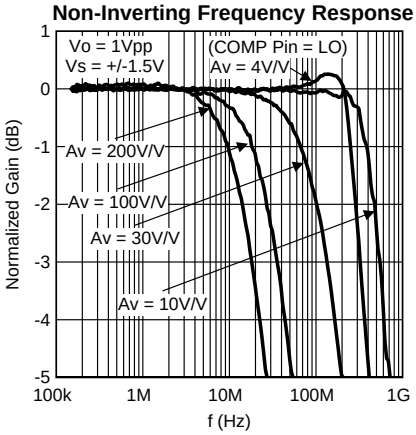


Figure 7.

Non-Inverting Frequency Response, WSON-8 Package

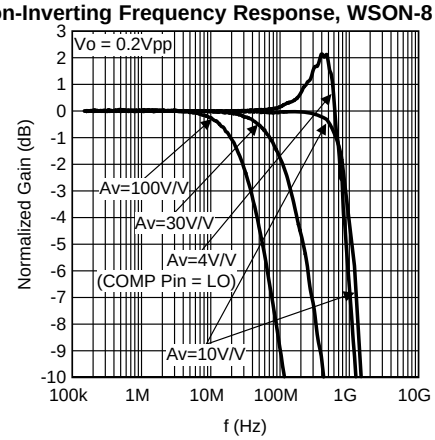


Figure 8.

Non-Inverting Frequency Response, SOT-23-5 Package

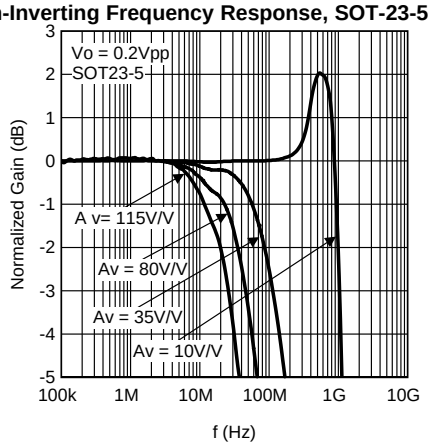


Figure 9.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±2.5V, R_f = 240Ω, R_L = 100Ω, V_O = $2V_{PP}$, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).

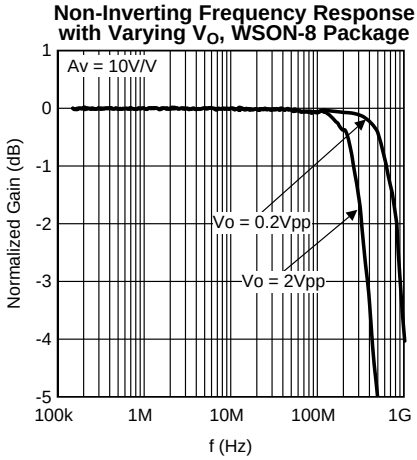


Figure 10.

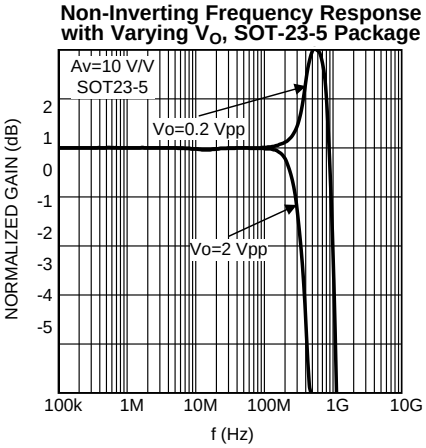


Figure 11.

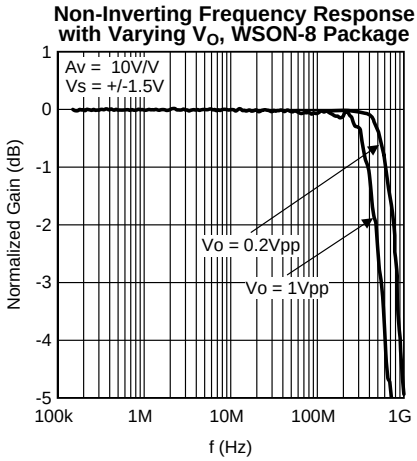


Figure 12.

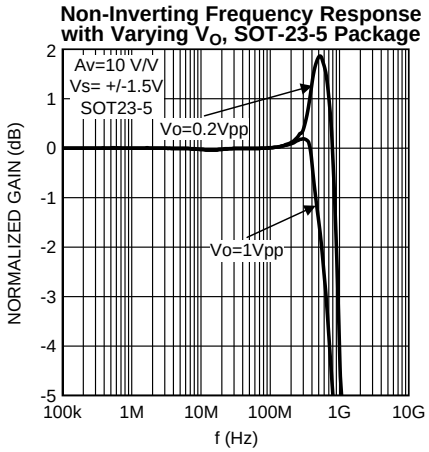


Figure 13.

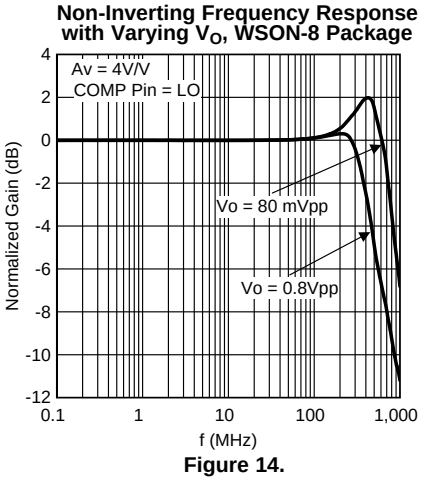


Figure 14.

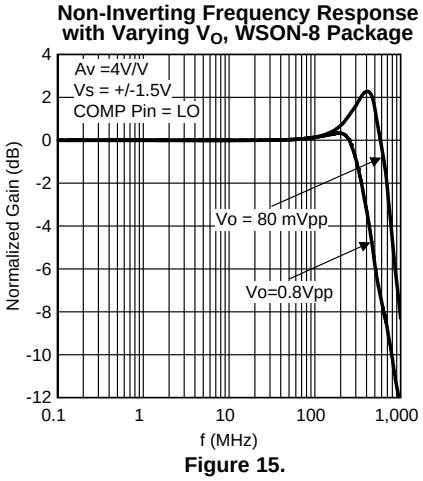


Figure 15.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±2.5V, R_f = 240Ω, R_L = 100Ω, V_O = $2V_{PP}$, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).

Frequency Response with Cap. Loading

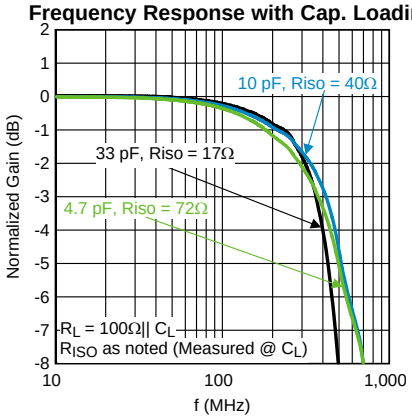


Figure 16.

Frequency Response Cap. Loading, WSON-8 Package

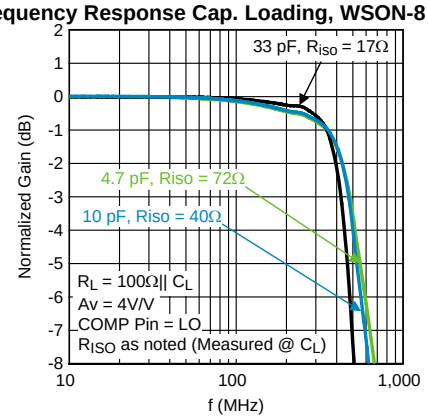


Figure 17.

Frequency Response vs. R_f, WSON-8 Package

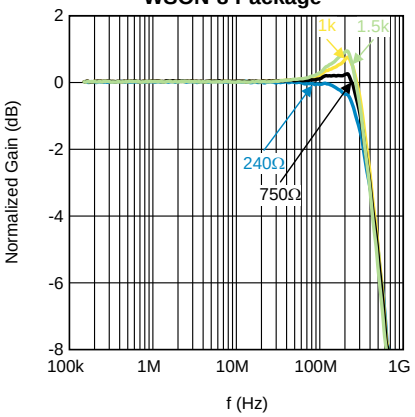


Figure 18.

Frequency Response vs. R_f, SOT-23-5 Package

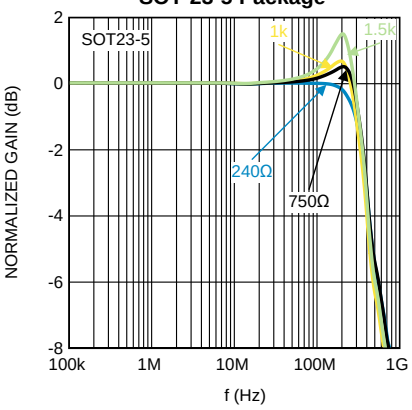


Figure 19.

Frequency Response vs. R_f, WSON-8 Package

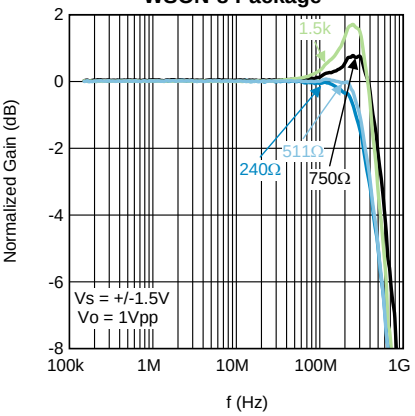


Figure 20.

Frequency Response vs. R_f, SOT-23-5 Package

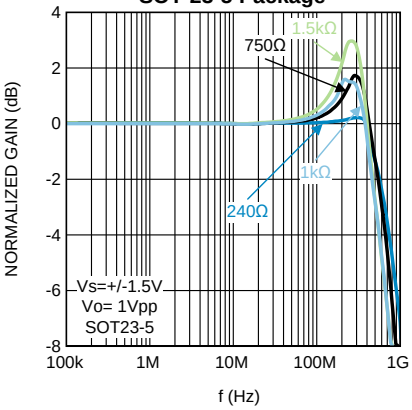


Figure 21.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±2.5V, R_f = 240Ω, R_L = 100Ω, V_O = $2V_{PP}$, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).

Distortion vs. Swing, WSON-8 Package

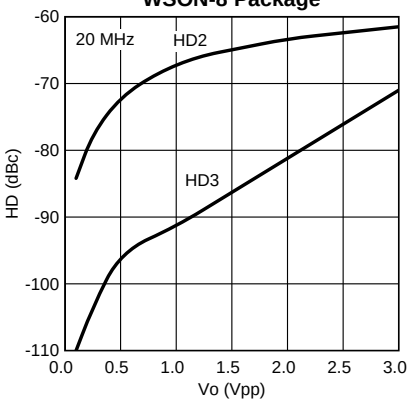


Figure 22.

Distortion vs. Swing, SOT-23-5 Package

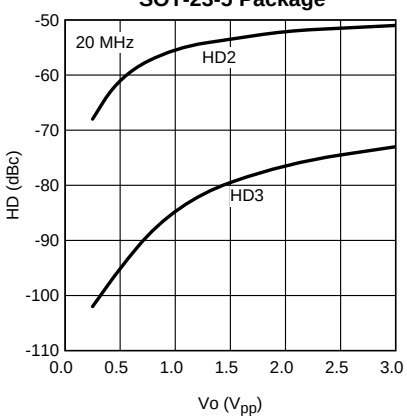


Figure 23.

Distortion vs. Swing, WSON-8 Package

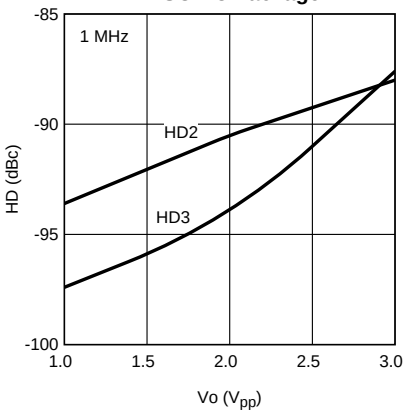


Figure 24.

Distortion vs. Swing, SOT-23-5 Package

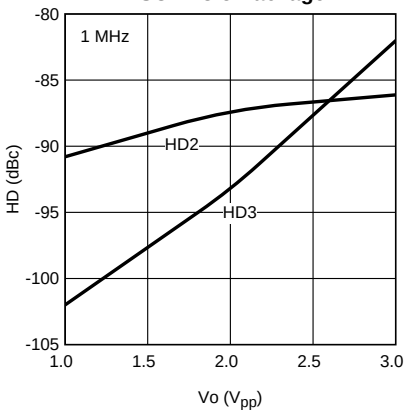


Figure 25.

Distortion vs. Gain, WSON-8 Package

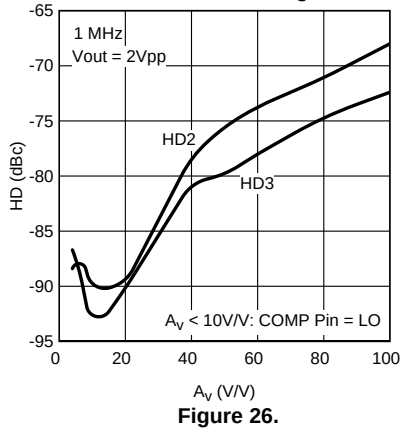


Figure 26.

Distortion vs. Gain, SOT-23-5 Package

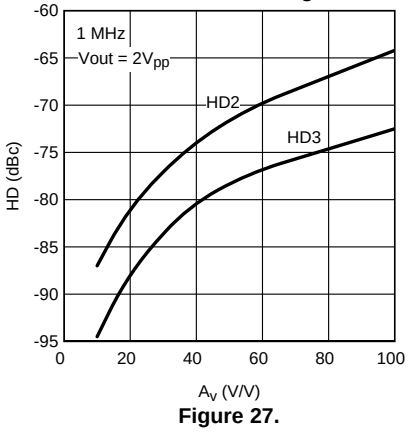


Figure 27.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±2.5V, R_f = 240Ω, R_L = 100Ω, V_O = $2V_{PP}$, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).

Distortion vs. Frequency, WSON-8 Package

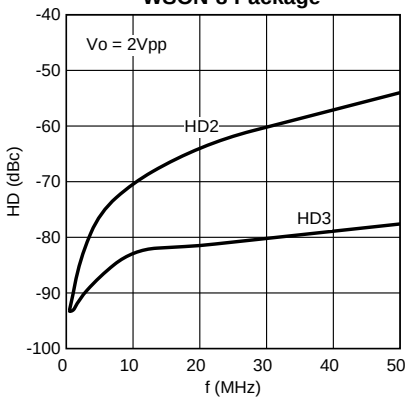


Figure 28.

Distortion vs. Frequency, SOT-23-5 Package

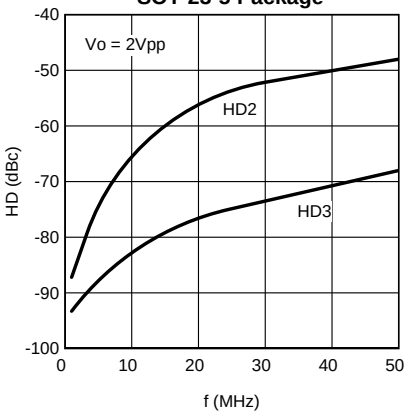


Figure 29.

3rd Order Intermodulation Distortion vs. Output Voltage

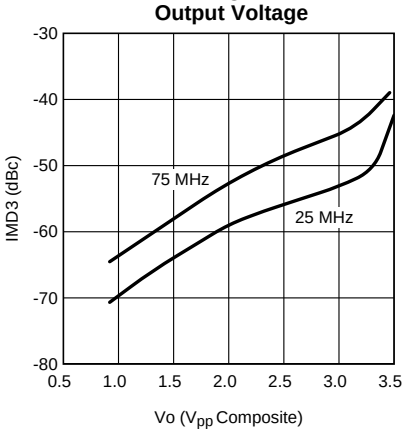


Figure 30.

Input Noise Voltage vs. Frequency

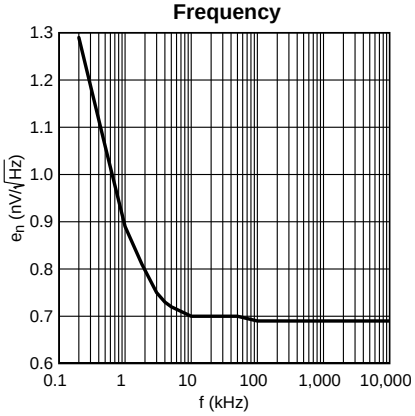


Figure 31.

Input Noise Current vs. Frequency

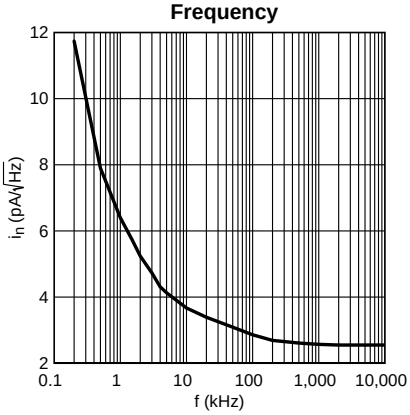


Figure 32.

PSRR vs. Frequency

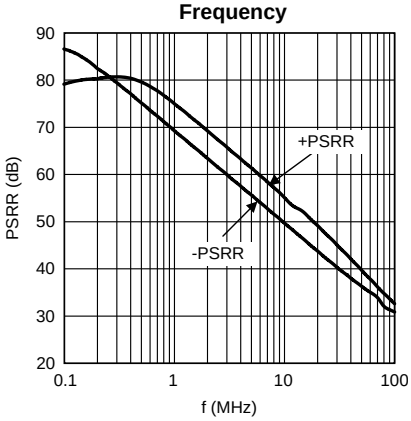


Figure 33.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±2.5V, R_f = 240Ω, R_L = 100Ω, V_O = $2V_{PP}$, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).

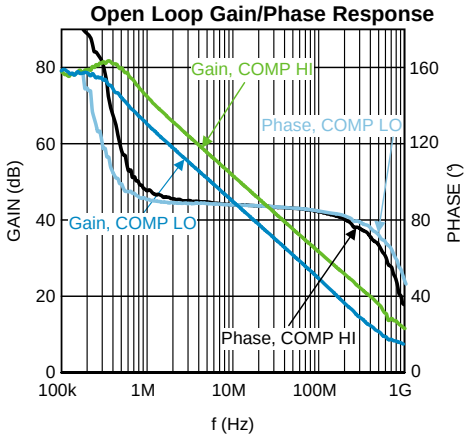


Figure 34.

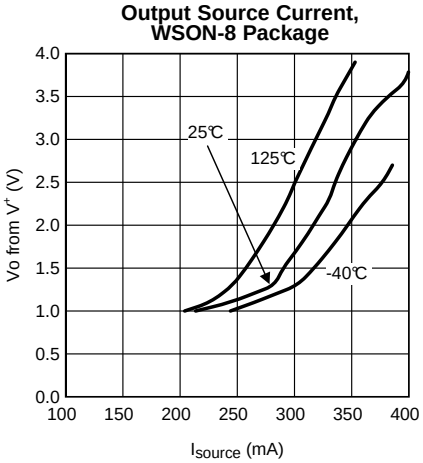


Figure 35.

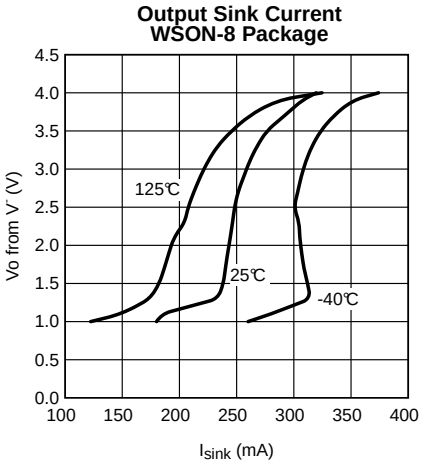


Figure 36.

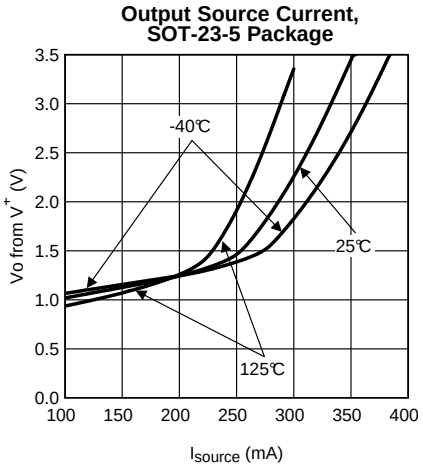


Figure 37.

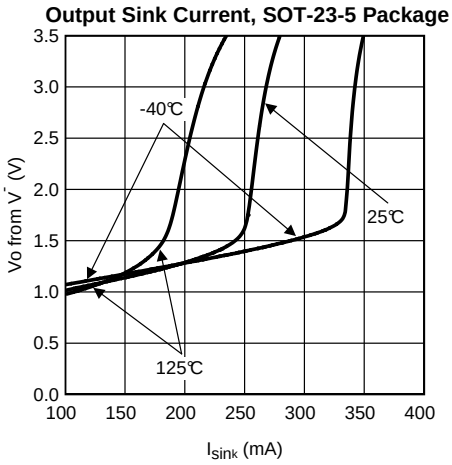


Figure 38.

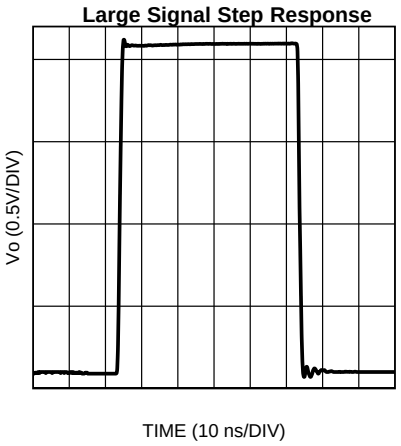


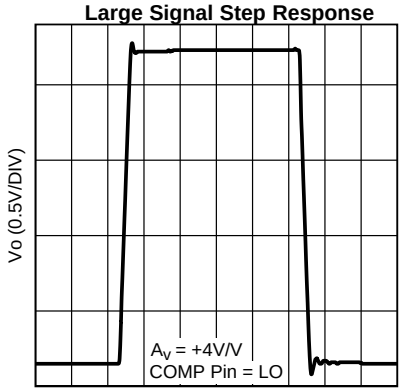
Figure 39.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±2.5V, R_f = 240Ω, R_L = 100Ω, V_O = $2V_{PP}$, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).

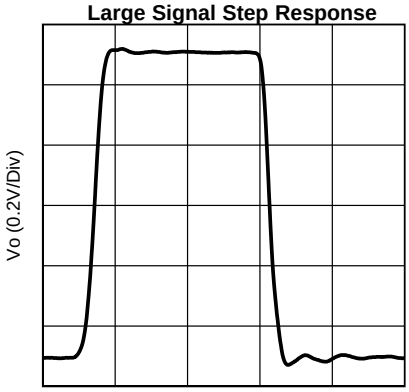
Large Signal Step Response



TIME (10 ns/DIV)

Figure 40.

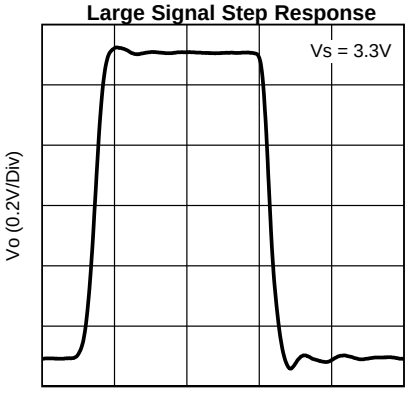
Large Signal Step Response



Time (4 ns/Div)

Figure 41.

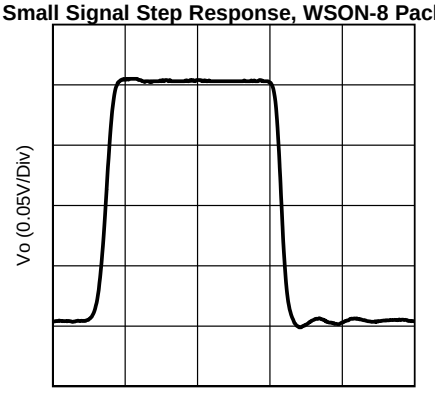
Large Signal Step Response



Time (4 ns/Div)

Figure 42.

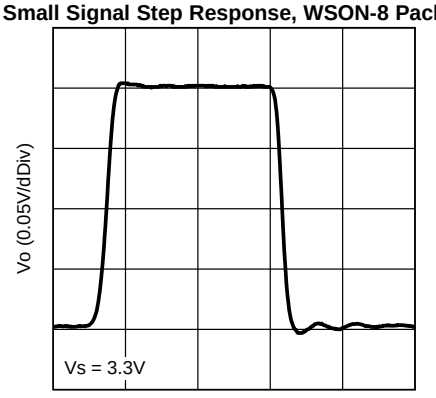
Small Signal Step Response, WSON-8 Package



Time (2 ns/Div)

Figure 43.

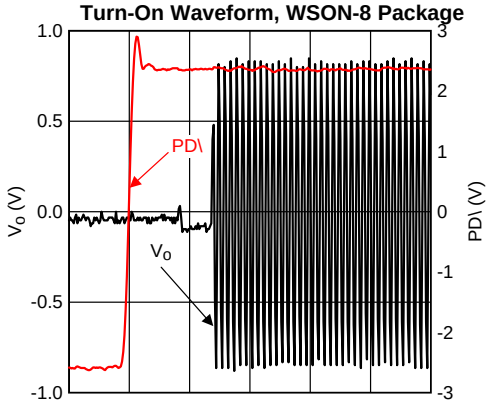
Small Signal Step Response, WSON-8 Package



Time (2 ns/Div)

Figure 44.

Turn-On Waveform, WSON-8 Package



Time (50 ns/DIV)

Figure 45.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±2.5V, R_f = 240Ω, R_L = 100Ω, V_O = $2V_{PP}$, COMP pin = HI, A_V = +10 V/V, WSON-8 and SOT-23-5 packages (unless specifically noted).

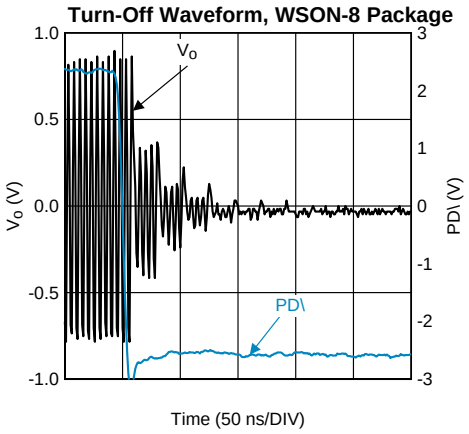


Figure 46.

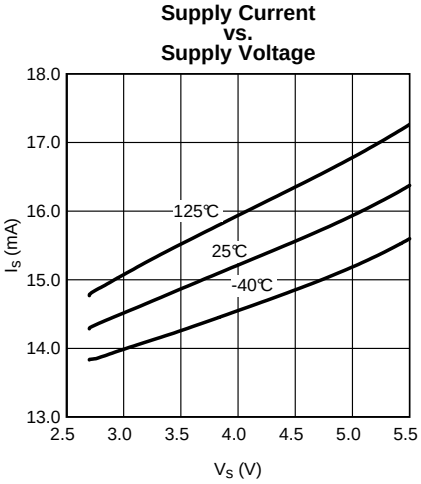


Figure 47.

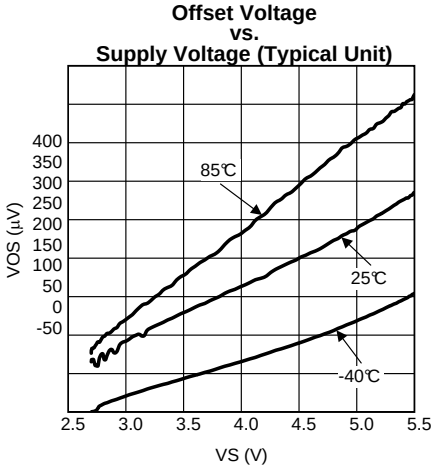


Figure 48.

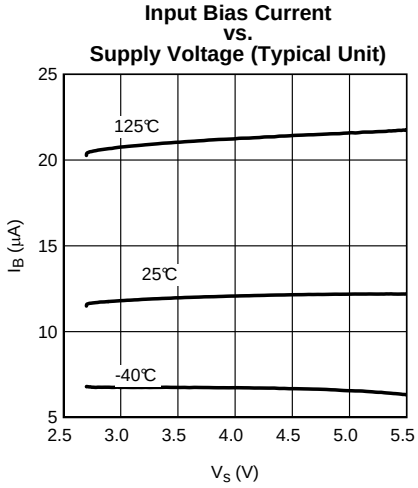


Figure 49.

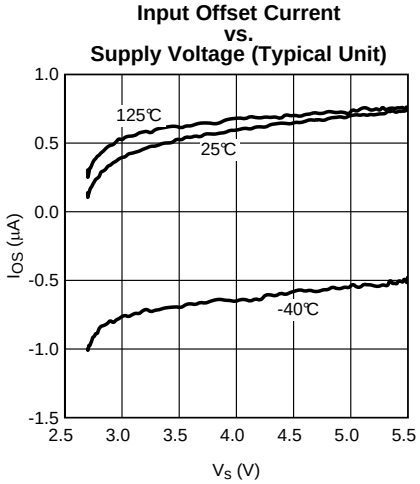


Figure 50.

APPLICATION SECTION

INTRODUCTION

The LMH6629 is a high gain bandwidth, ultra low-noise voltage feedback operational amplifier. The excellent noise and bandwidth enables applications such as medical diagnostic ultrasound, magnetic tape & disk storage and fiberoptics to achieve maximum high frequency signal-to-noise ratios. The following discussion will enable the proper selection of external components to achieve optimum system performance.

The LMH6629 (WSON-8 package only) has some additional features to allow maximum flexibility. As shown in Figure 51 there are provisions for low-power shutdown and two internal compensation settings, which are further discussed below under the COMPENSATION heading. Also provided is a feedback (FB) pin which allows the placement of the feedback resistor directly adjacent to the inverting input (IN-) pin. This pin simplifies printed circuit board layout and minimizes the possibility of unwanted interaction between the feedback path and other circuit elements.

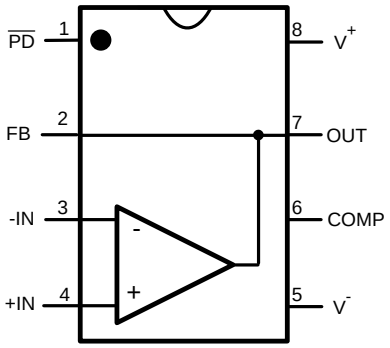


Figure 51. 8-Pin WSON Pinout Diagram

The WSON-8 package requires the bottom-side Die Attach Paddle (DAP) to be soldered to the circuit board for proper thermal dissipation and to get the thermal resistance number specified. The DAP is tied to the V- potential within the LMH6629 package. Thus, the circuit board copper area devoted to DAP heatsinking connection should be at the V- potential as well. Please refer to the package drawing for the recommended land pattern and recommended DAP connection dimensions.

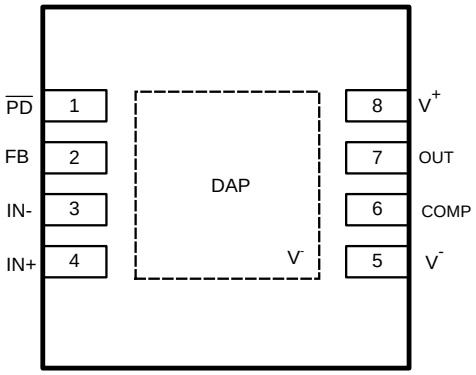


Figure 52. WSON–8 DAP(Top View)

WSON-8 CONTROL PINS & SOT-23-5 COMPARISON

The LMH6629 WSON-8 package has two digital control pins; $\overline{PD}$ and COMP pins. The $\overline{PD}$ pin, used for powerdown, floats high (device on) when not driven. When the $\overline{PD}$ pin is pulled low, the amplifier is disabled and the amplifier output stage goes into a high impedance state so the feedback and gain set resistors determine the output impedance of the circuit. The other control pin, the COMP pin, allows control of the internal compensation and defaults to the lower gain mode or logic 0.

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The SOT-23-5 package has the following differences relative to the WSON-8 package:

1. No power down (shutdown) capability.
2. No COMP pin to set the minimum stable gain. SOT-23–5 package minimum stable gain is internally fixed to be 10V/V.
3. No feedback (FB) pin.

From a performance point of view, the WSON-8 and the SOT-23-5 packages perform very similarly except in the following areas:

1. **SSBW, Peaking, and 0.1 dB Bandwidth:** These differences are highlighted in the Typical Performance Characteristics and the Electrical Characteristics tables. Most notable differences are with small signal (0.2 Vpp) and close to the minimum stable gain of 10V/V.
2. **Distortion:** It is possible to get slightly different distortion performance. The board layout, decoupling capacitor return current routing strongly influences this
3. **Output Current:** In heavy current applications, there will be differences between these package types because of the difference in their respective Thermal Resistances (θ_{JA}).

COMPENSATION

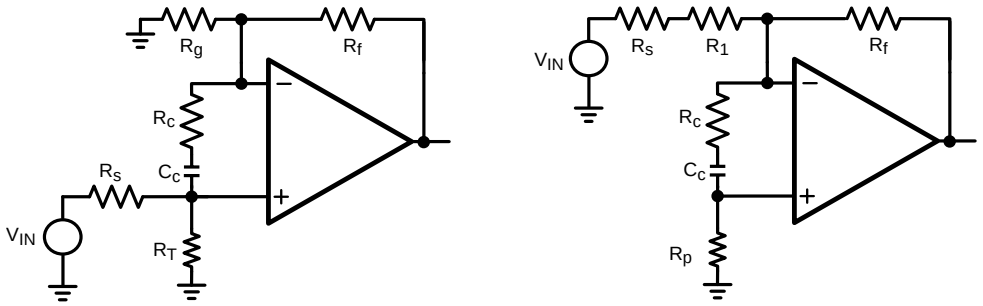
The LMH6629 has two compensation settings that can be controlled by the COMP pin (WSON-8 package only). The default setting is set through an internal pull down resistor and places the COMP pin at the logic 0 state. In this configuration the on-chip compensation is set to the maximum and bandwidth is reduced to enable stability at gains as low as 4V/V.

When this pin is driven to the logic 1 state, the internal compensation is decreased to allow higher bandwidth at higher gains. In this state, the minimum stable gain is 10V/V. Due to the reduced compensation, slew rate and large signal bandwidth are significantly enhanced for the higher gains.

As mentioned earlier, the SOT-23-5 package does not offer the two compensation settings that the WSON-8 offers. The SOT-23-5 is internally set for a minimum gain of 10 V/V.

It is possible to externally compensate the LMH6629 for any of the following reasons, as shown in Figure 53:

- To operate the SOT-23-5 package (which does not offer the COMP pin) at closed loop gains < 10V/V.
- To operate the WSON-8 package at gains below the minimum stable gain of 4V /V when the COMP pin is LO. **Note:** In this case, Figure 53 “Constraint 1” may be changed to ≥ 4 V/V instead of ≥ 10 V/V.
- To operate either package at low gain and need maximum slew rate (COMP pin HI).



a) Non-inverting

$R_p = R_s \| R_T$

COMP pin = HI

$R_{EQ} = R_f \| R_g$

b) Inverting

$R_g = R_s + R_1$

$$\text{Constraint 1:}\ \left(1+\frac{R_f}{R_g}\right)\left(1+\frac{R_p+R_{EQ}}{R_c}\right) \geq 10\,V/V$$

$$\text{Costraint 2:}\ \frac{1}{2\pi C_c R_c} \leq 90\,MHz$$

Figure 53. External Compensation

This circuit operates by increasing the Noise Gain (NG) beyond the minimum stable gain of the LMH6629 while maintaining a positive loop gain phase angle at 0dB. There are two constraints shown in Figure 53; "Constraint 1" ensures that NG has increased to at least 10 V/V when the loop gain approaches 0dB, and "Constraint 2" places an upper limit on the feedback phase lead network frequency to make sure it is fully effective in the frequency range when loop gain approaches 0dB. These two constraints allow one to estimate the "starting value" for R_c and C_c which may need to be fine tuned for proper response.

Here is an example worked out for more clarification:

Assume that the objective is to use the SOT-23-5 version of the LMH6629 for a closed loop gain of +3.7 V/V using the technique shown in Figure 53.

Selecting R_f = 249Ω → R_g = 91Ω → R_{EQ}= 66.6Ω.

For 50Ω source termination (R_s= 50Ω), select R_T= 50Ω → R_p = 25Ω.

Using "Constraint 1" (= 10V/V) allows one to compute Rc ≅ 56Ω. Using "Constraint 2" (= 90 MHz) defines the appropriate value of C_c≅ 33 pF.

The frequency response plot shown in Figure 54 is the measured response with R_c and C_c values computed above and shows a -3dB response of about 1GHz.

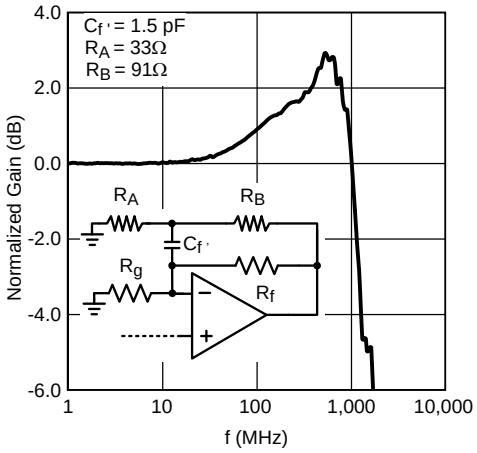


Figure 54. SOT-23-5 Package Low Closed Loop Gain Operation with External Compensation

For the Figure 54 measured results, a compensation capacitor ($C_{f'}$) was used across R_f to compensate for the summing node net capacitance due to the board and the SOT-23–5 LMH6629. The R_A and R_B combination reduces the effective capacitance of Cf' by the ratio of 1+R_B / R_A, with the constraint that R_B << R_f, thereby allowing a practical capacitance value (> 1pF) to be used. The WSON-8 package does not need this compensation across R_f due to its lower parasitics.

With the COMP pin HI (WSON-8 package only) or with the SOT-23–5 package, this circuit achieves high slew rate and takes advantage of the LMH6629's superior low-noise characteristics without sacrificing stability, while enabling lower gain applications. It should be noted that the R_c, C_c combination *does* lower the input impedance and increases noise gain at higher frequencies. With these values, the input impedance reduces by 3dB at 490 MHz. The Noise Gain transfer function "zero" is given by the equation below and it has a 3dB increase at 32.8 MHz with these values:

$$\text{Noise Gain "zero"} \cong \frac{1}{2\pi(R_C + R_p + R_{EQ})C_C} \quad (1)$$

Equation 1: External Compensation Noise Gain Increase

CANCELLATION OF OFFSET ERRORS DUE TO INPUT BIAS CURRENTS

The LMH6629 offers exceptional offset voltage accuracy. In order to preserve the low offset voltage errors, care must be taken to avoid voltage errors due to input bias currents. This is important in both inverting and non inverting applications.

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The non-inverting circuit is used here as an example. To cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain setting (R_g) and feedback (R_f) resistors should equal the equivalent source resistance (R_{seq}) as defined in Figure 55. Combining this constraint with the non-inverting gain equation also seen in Figure 55 allows both R_f and R_g to be determined explicitly from the following equations:

$$R_f = A_V R_{seq} \text{ and } R_g = R_f/(A_V-1) \quad (2)$$

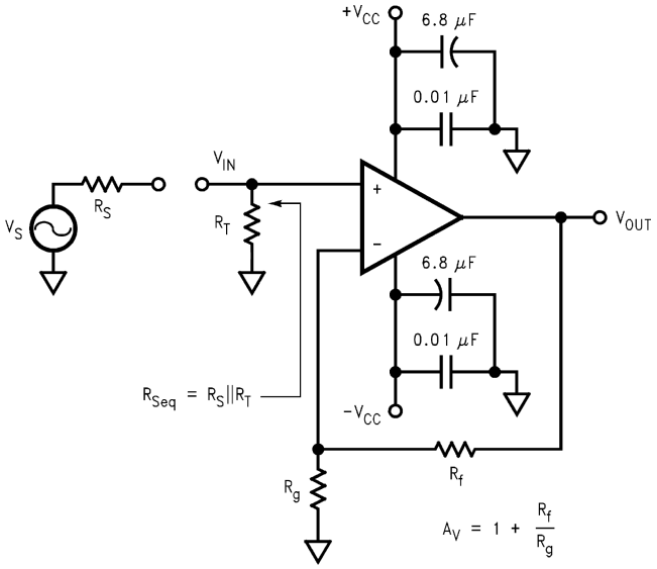


Figure 55. Non-Inverting Amplifier Configuration

When driven from a 0Ω source, such as the output of an op amp, the non-inverting input of the LMH6629 should be isolated with at least a 25Ω series resistor.

As seen in Figure 56, bias current cancellation is accomplished for the inverting configuration by placing a resistor (R_b) on the non-inverting input equal in value to the resistance seen by the inverting input (R_f || (R_g+R_s)). R_b should to be no less than 25Ω for optimum LMH6629 performance. A shunt capacitor (not shown) can minimize the additional noise of R_b.

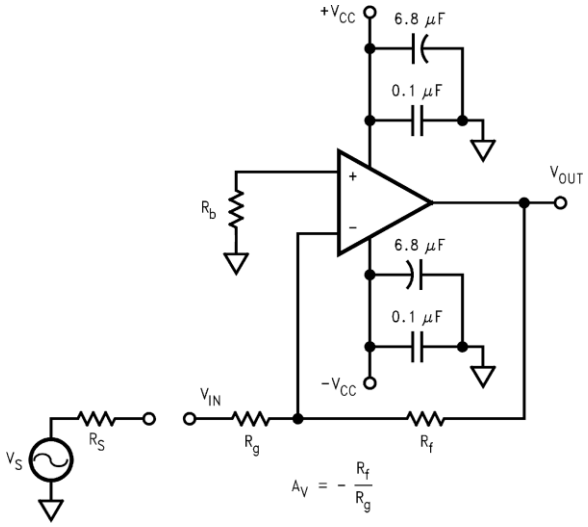


Figure 56. Inverting Amplifier Configuration

TOTAL INPUT NOISE vs. SOURCE RESISTANCE

To determine maximum signal-to-noise ratios from the LMH6629, an understanding of the interaction between the amplifier's intrinsic noise sources and the noise arising from its external resistors is necessary. Figure 57 describes the noise model for the non-inverting amplifier configuration showing all noise sources. In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n = i_n^+ = i_n^-$) source, there is also thermal voltage noise ($e_t = \sqrt{(4KTR)}$) associated with each of the external resistors.

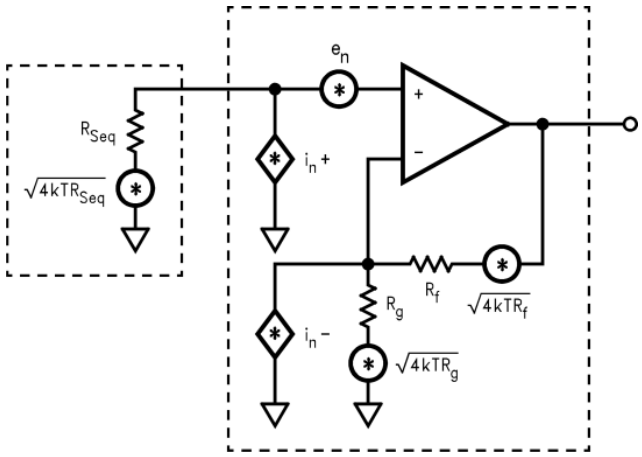


Figure 57. Non-Inverting Amplifier Noise Model

Equation 3 provides the general form for total equivalent input voltage noise density (e_{ni}).

$$e_{ni} = \sqrt{e_n^2 + \left(i_{n+} R_{Seq}\right)^2 + 4kTR_{Seq} + \left(i_{n-}\left(R_f \| R_g\right)\right)^2 + 4kT\left(R_f \| R_g\right)}$$

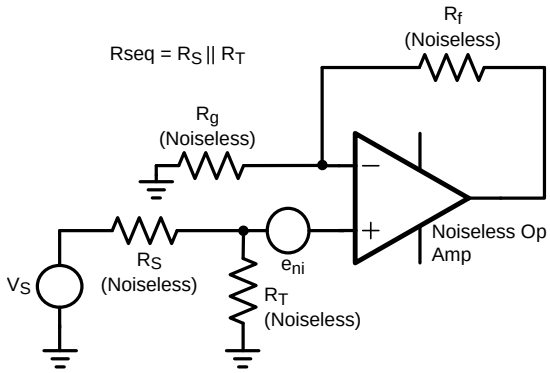
Equation 3: General Noise Equation (3)

Equation 4 is a simplification of Equation 3 that assumes $R_f \| R_g = R_{seq}$ for bias current cancellation:

$$e_{ni} = \sqrt{e_n^2 + 2(i_n R_{Seq})^2 + 4kT(2R_{Seq})}$$

Equation 4: Noise Equation with $R_f \| R_g = R_{seq}$ (4)

Figure 58 schematically shows e_{ni} alongside V_{IN} (the portion of V_S source which reaches the non-inverting input of Figure 55) and external components affecting gain ($A_v = 1 + R_f / R_g$), all connected to an ideal noiseless amplifier.



Set $R_{Seq} = R_f \| R_g$ for bias current offset cancellation

Figure 58. Non-Inverting Amplifier Equivalent Noise Source Schematic

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Figure 59 illustrates the equivalent noise model using this assumption. Figure 60 is a plot of e_{ni} against equivalent source resistance (R_{seq}) with all of the contributing voltage noise source of Equation 4. This plot gives the expected e_{ni} for a given (R_{seq}) which assumes $R_f||R_g = R_{seq}$ for bias current cancellation. The total equivalent output voltage noise (e_{no}) is $e_{ni}*A_V$.

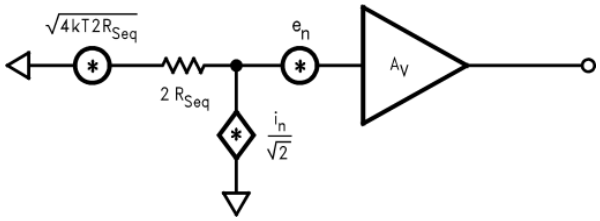


Figure 59. Noise Model with $R_f||R_g = R_{seq}$

As seen in Figure 60, e_{ni} is dominated by the intrinsic voltage noise (e_n) of the amplifier for equivalent source resistances below 15Ω. Between 15Ω and 2.5 kΩ, e_{ni} is dominated by the thermal noise ($e_t = \sqrt{(4kT(2R_{seq}))}$ of the equivalent source resistance R_{seq}; incidentally, this is the range of R_{seq} values where the LMH6629 has the best (lowest) Noise Figure (NF) for the case where $R_{seq} = R_f \,||\, R_g$.

Above 2.5 kΩ, e_{ni} is dominated by the amplifier's current noise ($i_n = \sqrt{(2)}\, i_n R_{seq}$). When R_{seq} = 190Ω (i.e., $R_{seq} = e_n/\sqrt{(2)}\, i_n$), the contribution from voltage noise and current noise of LMH6629 is equal. For example, configured with a gain of +10V/V giving a −3dB of 825 MHz and driven from $R_{seq} = R_f \,||\, R_g$ = 20Ω (e_{ni} = 1.07 nV√Hz from Figure 60), the LMH6629 produces a total equivalent output noise voltage (e_{ni} * 10 V/V * √(1.57 * 825 MHz)) of 385 μV_{rms}.

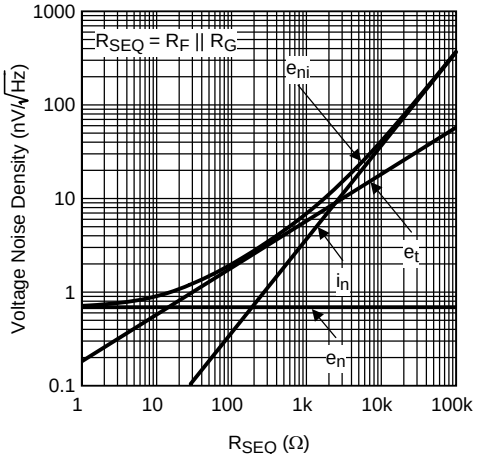


Figure 60. Voltage Noise Density vs. Source Resistance

If bias current cancellation is not a requirement, then $R_f \,||\, R_g$ need not equal R_{seq}. In this case, according to Equation 3, $R_f \,||\, R_g$ should be as low as possible to minimize noise. Results similar to Equation 3 are obtained for the inverting configuration of Figure 56 if R_{seq} is replaced by R_b and R_g is replaced by $R_g + R_s$. With these substitutions, Equation 3 will yield an e_{ni} referred to the non-inverting input. Referring e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ratio of non-inverting to inverting gains ($1+R_g/R_f$).

NOISE FIGURE

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

$$NF = 10LOG\left\{\frac{S_i / N_i}{S_o / N_o}\right\} = 10LOG\left\{\frac{e_{ni}^2}{e_t^2}\right\}$$

Equation 5: General Noise Figure Equation (5)

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Looking at the two parts of the NF expression (inside the log function) yields:

$S_i / S_o \rightarrow$ Inverse of the power gain provided by the amplifier

$N_o / N_i \rightarrow$ Total output noise power, including the contribution of R_S, divided by the noise power at the input due to R_S

To simplify this, consider N_a as the noise power added by the amplifier (reflected to its input port):

$S_i / S_o \rightarrow 1 / G$

$N_o / N_i \rightarrow G * (N_i + N_a) / N_i$ (where $G*(N_i + N_a) = N_o$)

Substituting these two expressions into the NF expression:

$$NF = 10 \log \left[\frac{1}{G} \left(\frac{G(N_i + N_a)}{N_i} \right) \right] = 10 \log \left(1 + \frac{N_a}{N_i} \right)$$

Equation 6: Simplified Noise Figure Equation (6)

The noise figure expression has simplified to depend only on the ratio of the noise power added by the amplifier at its input (considering the source resistor to be in place but noiseless in getting N_a) to the noise power delivered by the source resistor (considering all amplifier elements to be in place but noiseless in getting N_i).

For a given amplifier with a desired closed loop gain, to minimize noise figure:

- Minimize $R_f \parallel R_g$
- Choose the Optimum R_S (R_{OPT})

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \approx e_n / i_n \quad (7)$$

Figure 61 is a plot of NF vs R_S with the circuit of Figure 55 (R_f = 240Ω, A_V = +10V/V). The NF curves for both Unterminated (R_T = open) and Terminated systems ($R_T = R_S$) are shown. Table 1 indicates NF for various source resistances including $R_S = R_{OPT}$.

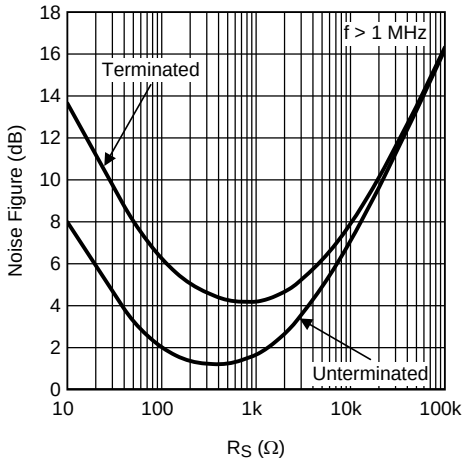


Figure 61. Noise Figure vs. Source Resistance

Table 1. Noise Figure for Various R_s

R_S (Ω)	NF (Terminated) (dB)	NF (Unterminated) (dB)
50	8	3.2
R_{OPT}	4.1 (R_{OPT} = 750Ω)	1.1 (R_{OPT} = 350Ω)

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SINGLE-SUPPLY OPERATION

The LMH6629 can be operated with single power supply as shown in Figure 62. Both the input and output are capacitively coupled to set the DC operating point.

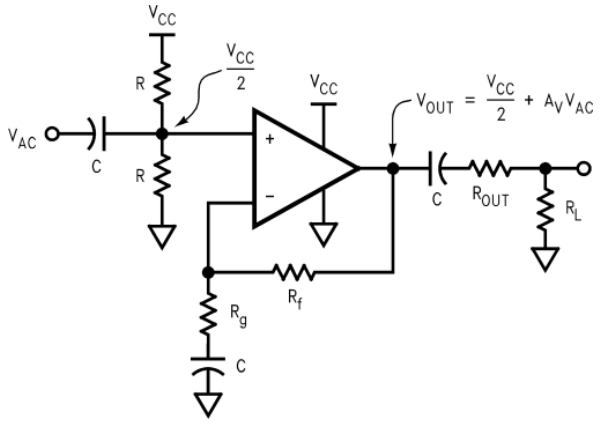


Figure 62.

LOW-NOISE TRANSIMPEDANCE AMPLIFIER

Figure 63 implements a high-speed, single-supply, low-noise Transimpedance amplifier commonly used with photo-diodes. The transimpedance gain is set by R_F.

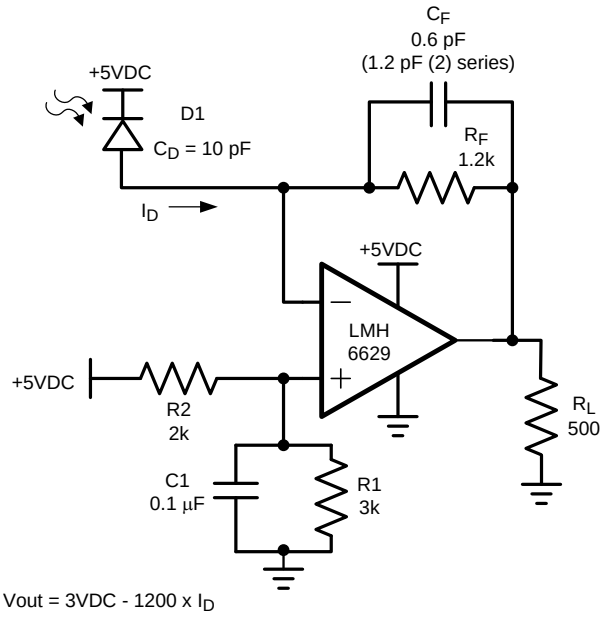


Figure 63.

Figure 64 shows the Noise Gain (NG) and transfer function (I-V Gain). As with most Transimpedance amplifiers, it is required to compensate for the additional phase lag (Noise Gain zero at f_Z) created by the total input capacitance (C_D (diode capacitance) + C_{CM} (LMH6629 input capacitance)) looking into R_F; this is accomplished by placing C_F across R_F to create enough phase lead (Noise Gain pole at f_P) to stabilize the loop.

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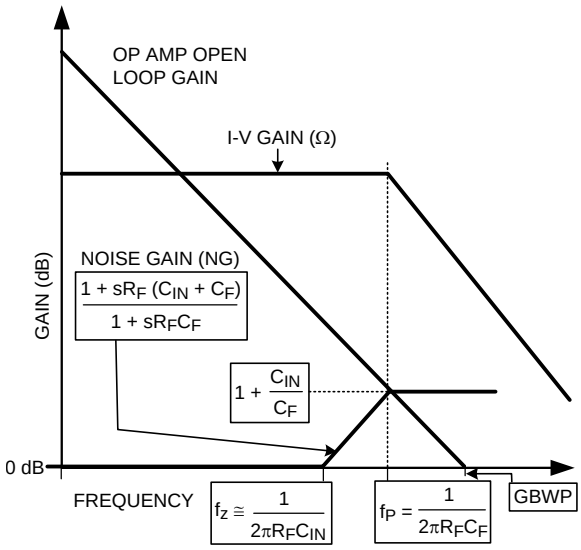


Figure 64.

The optimum value of C_F is given by Equation 8 resulting in the I-V -3dB bandwidth shown in Equation 9, or around 200 MHz in this case (assuming GBWP= 4GHz with COMP pin = HI for WSON-8 package). This C_F value is a "starting point" and C_F needs to be tuned for the particular application as it is often less than 1pF and thus is easily affected by board parasitics, etc. For maximum speed, the LMH6629 COMP pin should be HI (for WSON-8 package). This CF value is a "starting point" and CF needs to be tuned for the particular application as it is often less than 1pF and thus is easily affected by board parasitics, etc. For maximum speed, the LMH6629 COMP pin should be HI (or use the SOT-23 package).

$$C_F = \sqrt{\frac{C_{IN}}{2\pi(GBWP)R_F}}$$

Equation 8: Optimum C_F Value (8)

$$f_{-3\,dB} \cong \sqrt{\frac{GBWP}{2\pi R_F C_{IN}}}$$

Equation 9: Resulting -3dB Bandwidth (9)

Equation 10 provides the total input current noise density (i_{ni}) equation for the basic Transimpedance configuration and is plotted against feedback resistance (R_F) showing all contributing noise sources in Figure 65. The plot indicates the expected total equivalent input current noise density (i_{ni}) for a given feedback resistance (R_F). This is depicted in the schematic of Figure 66 where total equivalent current noise density (i_{ni}) is shown at the input of a noiseless amplifier and noiseless feedback resistor (R_F). The total equivalent output voltage noise density (e_{no}) is i_{ni}*R_F.

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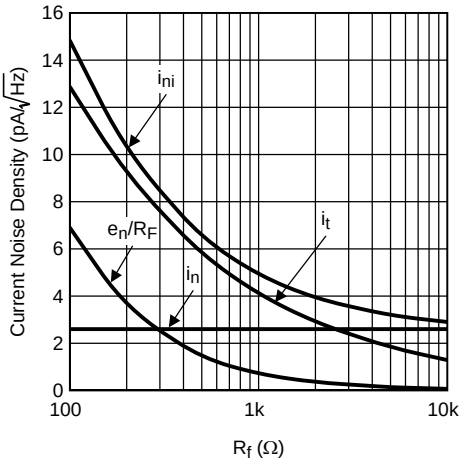


Figure 65.

$$i_{ni} = \sqrt{i_n^2 + \left(\frac{e_n}{R_f}\right)^2 + \frac{4kT}{R_f}}$$

Equation 10: Noise Equation for Transimpedance Amplifier (10)

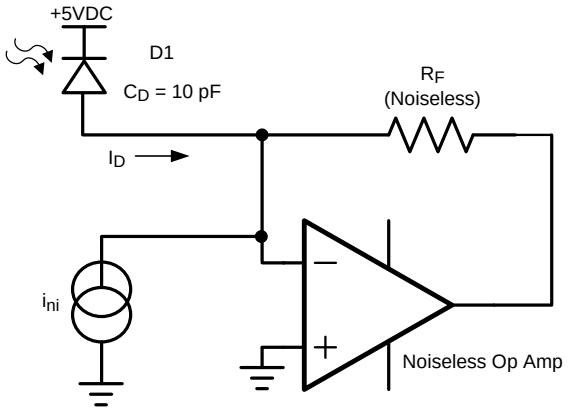


Figure 66.

From Figure 65, it is clear that with LMH6629's extremely low-noise characteristics, for R_F < 2.5kΩ, the noise performance is entirely dominated by R_F thermal noise. Only above this R_F threshold, LMH6629's input noise current (i_n) starts being a factor and at no R_F setting does the LMH6629 input noise voltage play a significant role. This noise analysis has ignored the possible noise gain increase, due to photo-diode capacitance, at higher frequencies.

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LOW-NOISE INTEGRATOR

Figure 67 shows a deBoo integrator implemented with the LMH6629. Positive feedback maintains integration linearity. The LMH6629's low input offset voltage and matched inputs allow bias current cancellation and provide for very precise integration. Keeping R_G and R_S low helps maintain dynamic stability.

$$V_O \cong V_{IN} \frac{K_O}{sR_SC} \quad ; \quad K_O = 1 + \frac{R_F}{R_G}$$

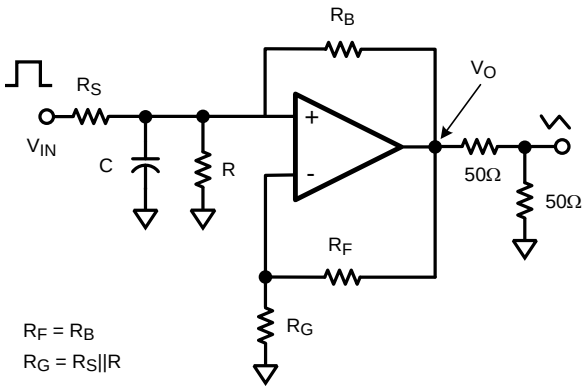
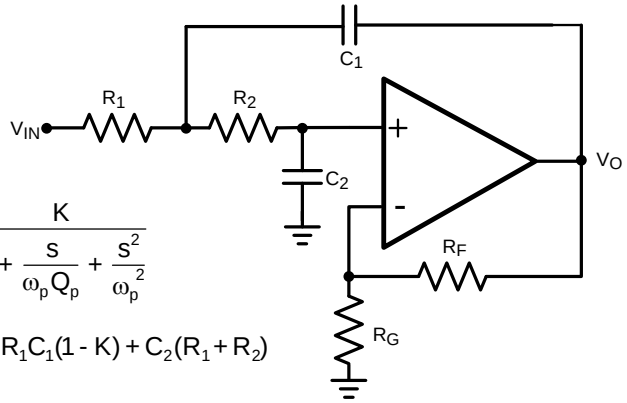


Figure 67.

HIGH-GAIN SALLEN-KEY ACTIVE FILTERS

The LMH6629 is well suited for high-gain Sallen-Key type of active filters. Figure 68 shows the 2nd order Sallen-Key low-pass filter topology. Using component predistortion methods discussed in OA-21 enables the proper selection of components for these high-frequency filters.



$$\frac{V_o}{V_{IN}} \cong \frac{K}{1 + \frac{s}{\omega_p Q_p} + \frac{s^2}{\omega_p^2}}$$

$$\frac{1}{\omega_p Q_p} = R_1C_1(1 - K) + C_2(R_1 + R_2)$$

$$\frac{1}{\omega_p^2} = R_1R_2C_1C_2$$

Figure 68.

LOW-NOISE MAGNETIC MEDIA EQUALIZER

Figure 69 shows a high-performance low-noise equalizer for such applications as magnetic tape channels using the LMH6629. The circuit combines an integrator (used to limit noise) with a bandpass filter (used to boost the response centered at a frequency or over a band of interest) to produce the low-noise equalization. The circuit's simulated frequency response is illustrated in Figure 70.

In this circuit, the bandpass filter center frequency is set by

$$f_C = \frac{1}{2\pi\sqrt{LC}} \tag{11}$$

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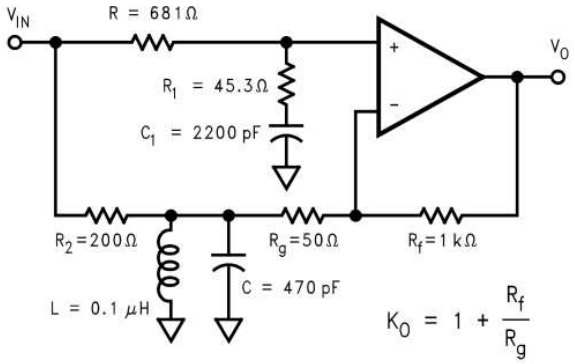
For higher selectivity, use high C values; for wider bandwidth, use high L values, while keeping the product of L and C values the same to keep f_c intact. The integrator's -3dB roll-off is set by

$$\frac{1}{2\pi C_1(R_1 + R)} \tag{12}$$

If

$$\frac{1}{2\pi C_1 R_1} << f_C \tag{13}$$

the integrator and the bandpass filter frequency interaction is minimized so that the operating frequencies of each can be set independently. Lowering the value of R2 increases the bandpass gain (boost) without affecting the integrator frequencies. With the LMH6629's wide Gain Bandwidth (4GHz), the center frequency could be adjusted higher without worries about loop gain limitation. This increases flexibility in tuning the circuit.



$$\frac{V_O}{V_{IN}} = K_0 \left(\frac{sC_1 R_1 + 1}{sC_1 (R_1 + R) + 1} - \left(\frac{R_f}{R_f + R_g} \right) \frac{sLR_g}{s^2 LCR_2 R_g + sL(R_2 + R_g) + R_2 R_g} \right)$$

Figure 69.

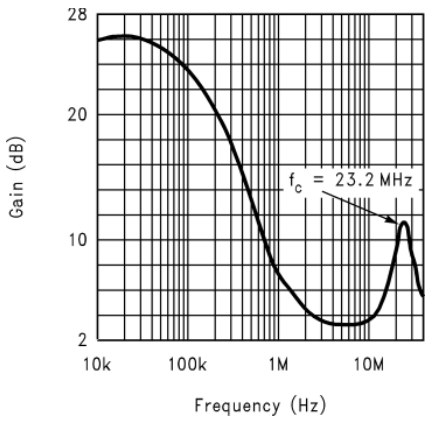


Figure 70.

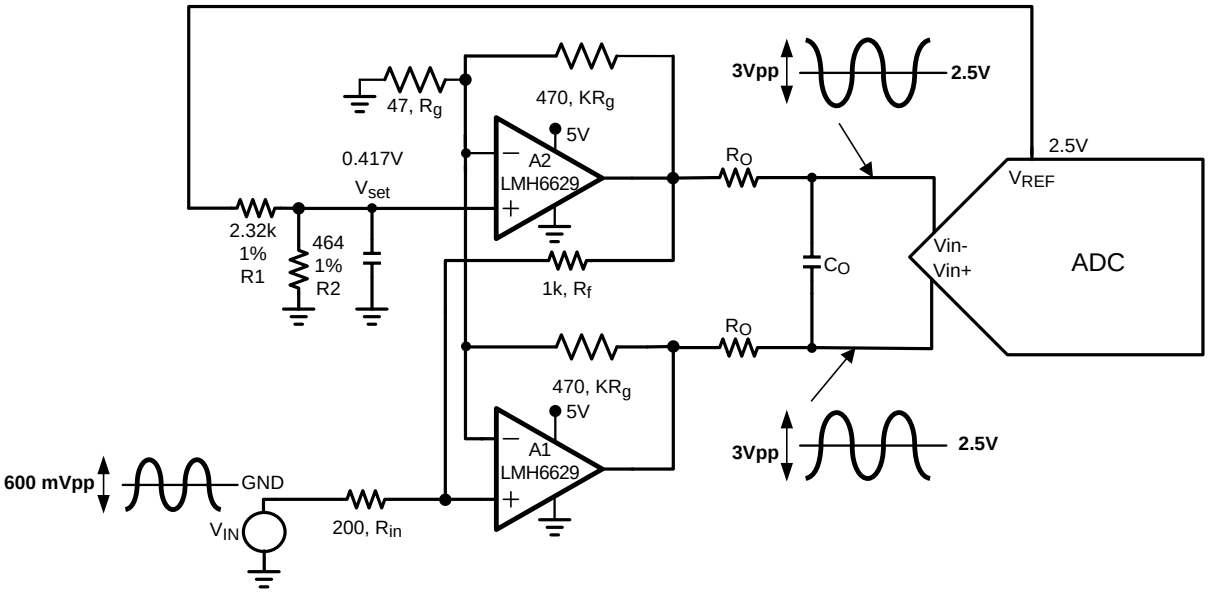
LOW-NOISE SINGLE ENDED TO DIFFERENTIAL CONVERTER / DRIVER

Many high-resolution data converters (ADC's) require a differential input driver. In order to preserve the ADC's dynamic range, the analog input driver must have a noise floor which is lower than the ADC's noise floor. For an ADC with N bits, the quantization Signal-to-noise ratio (SNR) is 6.02* N + 1.76 in dB. For example, a 12-bit ADC has a SNR of 74 dB (= 5000 V/V). Assuming a full-scale differential input of 2Vpp (0.707 V_RMS), the quantization noise referred to the ADC's input is ~140 µV_RMS (= 0.707 V_RMS / 5000 V/V) over the bandwidth "visible" to the ADC. Assuming an ADC input bandwidth of 20 MHz, this translates to just 25 nV/RtHz (= 141µV_RMS / SQRT(20 MHz * π/2)) noise density at the output of the driver. Using an amplifier to form the

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single-ended (SE) to Differential converter / driver for such an application is challenging, especially when there is some gain required. In addition, the input driver's linearity (harmonic distortion) must also be high enough such that the spurs that get through to the ADC input are below the ADC's LSB threshold or -73 dBc (= 20*log (1/ 2^{12})) or lower in this case. Therefore, it is essential to use a low-noise / low-distortion device to drive a high resolution ADC in order to minimize the impact on the quantization noise and to make sure that the driver's distortion does not dominate the acquired data.

Figure 71 shows a ground referenced bipolar input (symmetrical swing around 0V) SE to differential converter used to drive a high resolution ADC. The combination of LMH6629's low noise and the converter architecture reduces the impact on the ADC noise.



Governing Expressions:

$$K = \frac{V_{o_diff}}{V_{in}}$$

$$R_{in} = \frac{2R_f}{K}$$

$$V_{set} = \frac{2V_{o_CM}}{K+2}$$

Example:

$V_{o_CM} = 2.5V$; $K = 10$, Let $R_f = 1k\Omega \rightarrow Rin = 200\Omega$

$V_{o_diff} = 6Vpp$; $V_{set} = \frac{2 \times 2.5V}{10+2} = 0.417V$

$V_{in} = 600\,mVpp$

Figure 71. Low-Noise Single-Ended (SE) to Differential Converter

In this circuit, the required gain dictates the resistor ratio "K". With "K" and the driver output CM voltage (V_{O_CM}) known, V_{SET} can be established. Reasonable values for R_f and R_g can be set to complete the design.

In terms of output swing, with the LMH6629 output swing capability which requires ~0.85V of headroom from either rail, the maximum total output swing into the ADC is limited to 6.6 V_{PP} (=(5 – 2 x 0.85V) x 2); that is true with V_{O_CM} set to mid-rail between V^+ and V^-. It should also be noted that the LMH6629's input CMVR range includes the lower rail (V^-) and that is the reason there is great flexibility in setting V_{o_CM} by controlling V_{SET}. Another feature is that A1 and A2 inputs act like "virtual grounds" and thus do not see any signal swing. Note that due to the converter's biasing, the source, V_{IN}, needs to sink a current equal to V_{SET} / R_{IN}.

The converter example shown in Figure 71 operates with a noise gain of 6 (=1+ K / 2) and thus requires that the COMP pin to be tied low (WSON-8 package only). The 1st order approximated small signal bandwidth will be 280 MHz (=1.7 GHz / 6V/V) which is computed using 1.7GHz as the GBWP with COMP pin LO.

From a noise point of view, concentrating only on the dominant noise sources involved, here is the expression for the expected differential noise density at the input of the ADC:

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$$V_{noise} \cong \sqrt{[e_n(1+K/2)]^2 .2^3 + [(e_{Rin_thermal})K/2)]^2 .2^2 + [(e_{Rg_thermal})K)]^2}$$

Equation 14: Converter Noise Expression (14)

e_n is the LMH6629 input noise voltage and $e_{Rin_thermal}$ is the thermal noise of R_{IN}. The "2^3" and the "2^2" multipliers account for the different instances of each noise source (2 for e_n, and 1 for $e_{Rin_thermal}$).

Equation 14 evaluated for the circuit example of Figure 71 is shown below:

$$V_{noise} \cong \sqrt{[0.69\,nV/RtHz\ x\,6]^2 .2^3 + [1.82\,nV/RtHz\ x\,5]^2 .2^2 + [0.88\,nV/RtHz\ x\,10]^2} = 23.4\,nV/RtHz$$

Equation 15: Converter Noise Expression Evaluated (15)

Because of the LMH6629's low input noise voltage (e_n), noise is dominated by the thermal noise of R_{IN}. It is evident that the input resistor, R_{IN}, can be reduced to lower the noise with lower input impedance as the trade-off.

LAYOUT CONSIDERATIONS

National Semiconductor offers evaluation board(s) to aid in device testing and characterization and as a guide for proper layout. As is the case with all high-speed amplifiers, accepted-practice RF design technique on the PCB layout is mandatory. Generally, a good high-frequency layout exhibits a separation of power supply and ground traces from the inverting input and output pins. Parasitic capacitances between these nodes and ground may cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). Use high-quality chip capacitors with values in the range of 1000 pF to 0.1F for power supply bypassing. One terminal of each chip capacitor is connected to the ground plane and the other terminal is connected to a point that is as close as possible to each supply pin as allowed by the manufacturer's design rules. In addition, connect a tantalum capacitor with a value between 4.7 µF and 10 µF in parallel with the chip capacitor.

Harmonic Distortion, especially HD2, is strongly influenced by the layout and in particular can be affected by decoupling capacitors placed between the V^+ and V^-terminals as close to the device leads as possible.

Signal lines connecting the feedback and gain resistors should be as short as possible to minimize inductance and microstrip line effect. Place input and output termination resistors as close as possible to the input/output pins. Traces greater than 1 inch in length should be impedance matched to the corresponding load termination.

Symmetry between the positive and negative paths in the layout of differential circuitry should be maintained to minimize the imbalance of amplitude and phase of the differential signal.

Component value selection is another important parameter in working with high-speed / high-performance amplifiers. Choosing external resistors that are large in value compared to the value of other critical components will affect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These parasitic capacitors could either be inherent to the device or be a by-product of the board layout and component placement. Moreover, a large resistor will also add more thermal noise to the signal path. Either way, keeping the resistor values low will diminish this interaction. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation and high distortion.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH6629MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AE7A	Samples
LMH6629MFE/NOPB	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AE7A	Samples
LMH6629MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AE7A	Samples
LMH6629SD/NOPB	ACTIVE	WSON	NGQ	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L6629	Samples
LMH6629SDE/NOPB	ACTIVE	WSON	NGQ	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L6629	Samples
LMH6629SDX/NOPB	ACTIVE	WSON	NGQ	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L6629	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

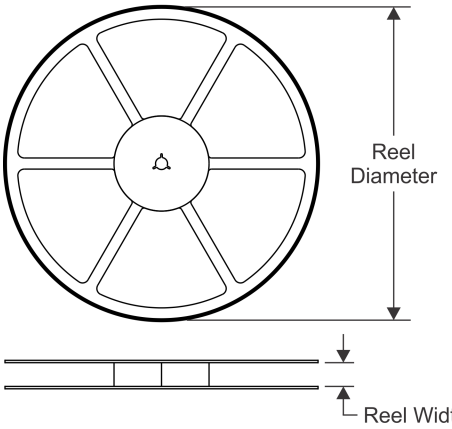
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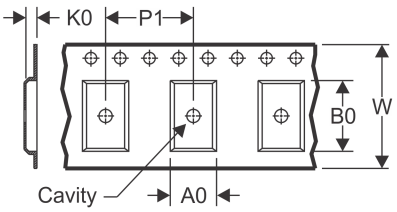
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

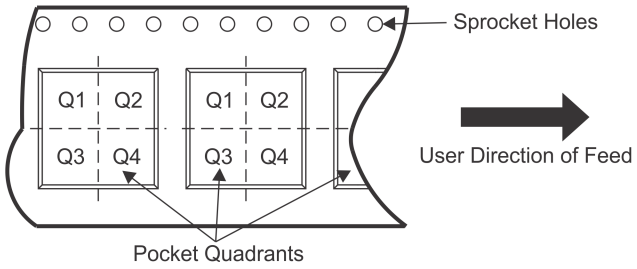


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

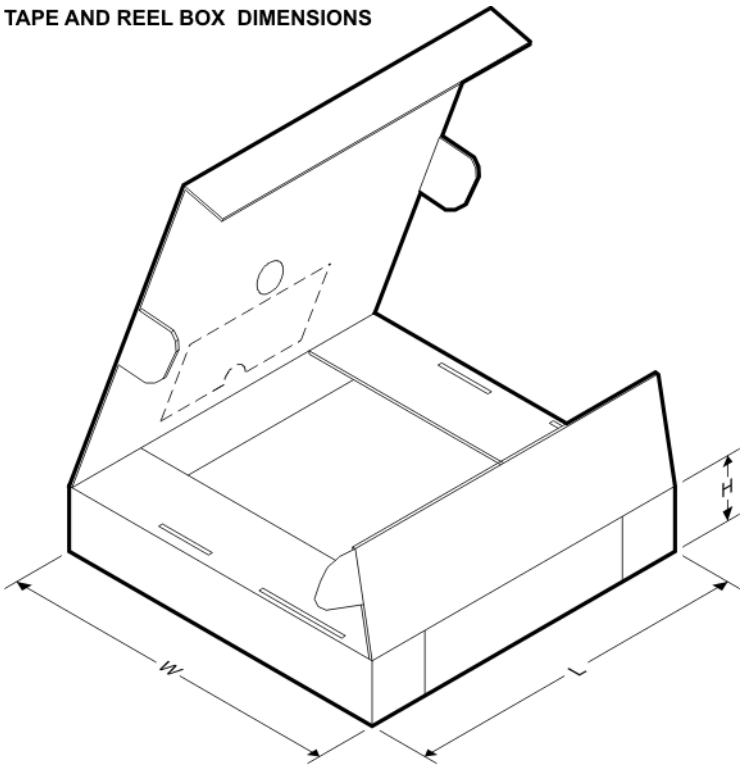
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6629MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6629MFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6629MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6629SD/NOPB	WSON	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMH6629SDE/NOPB	WSON	NGQ	8	250	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMH6629SDX/NOPB	WSON	NGQ	8	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

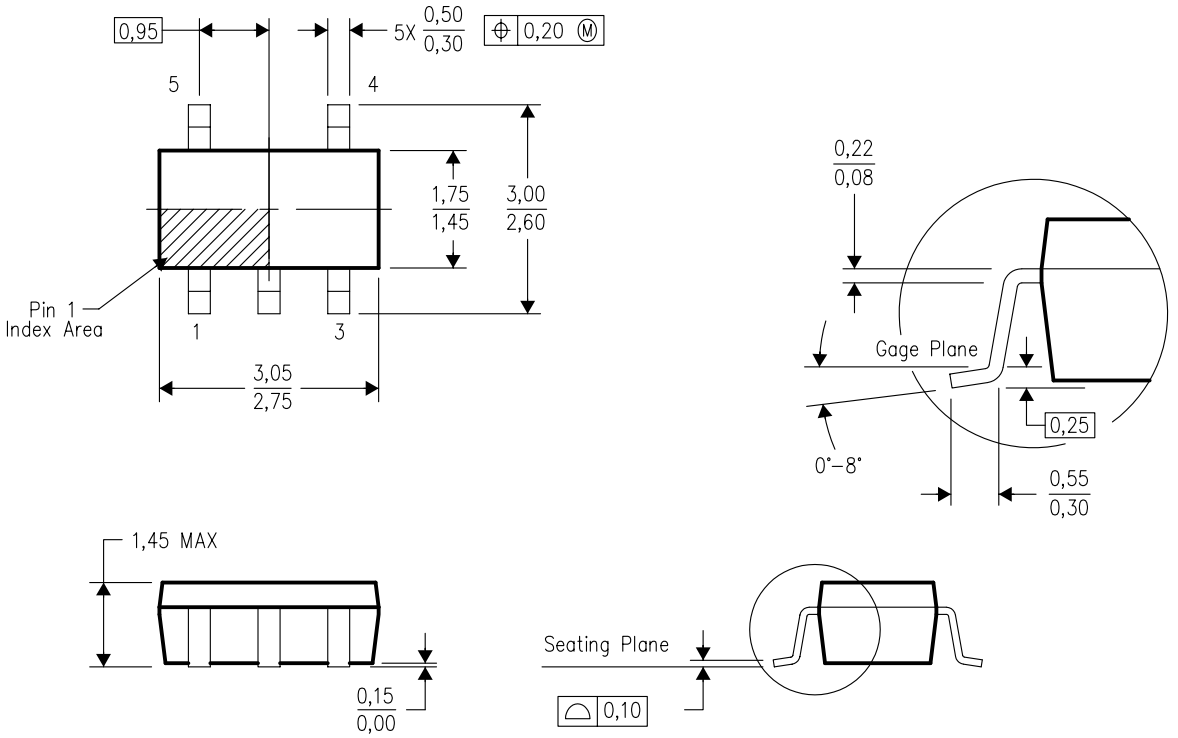
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6629MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6629MFE/NOPB	SOT-23	DBV	5	250	210.0	185.0	35.0
LMH6629MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMH6629SD/NOPB	WSON	NGQ	8	1000	203.0	190.0	41.0
LMH6629SDE/NOPB	WSON	NGQ	8	250	203.0	190.0	41.0
LMH6629SDX/NOPB	WSON	NGQ	8	4500	358.0	343.0	63.0

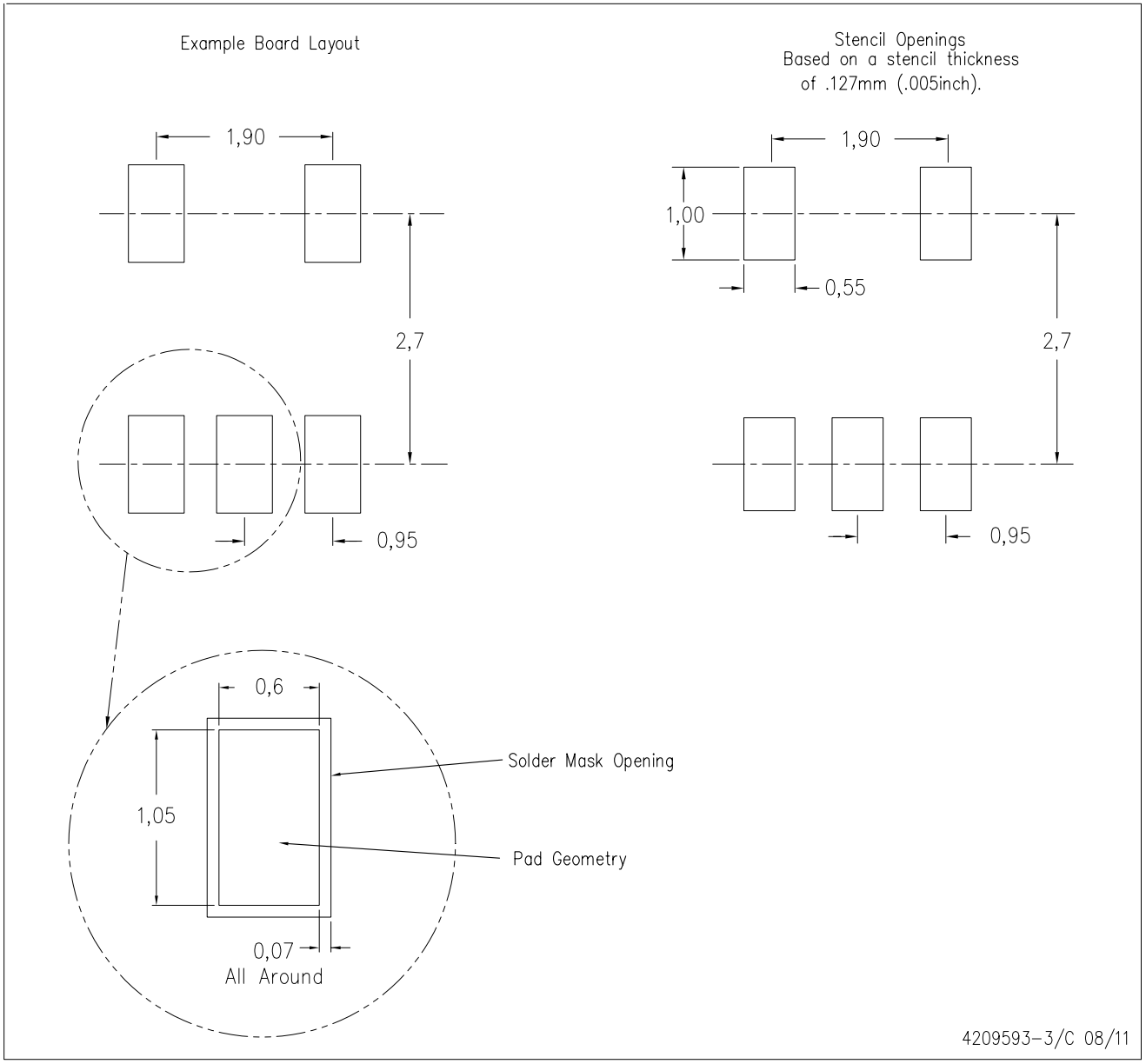
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

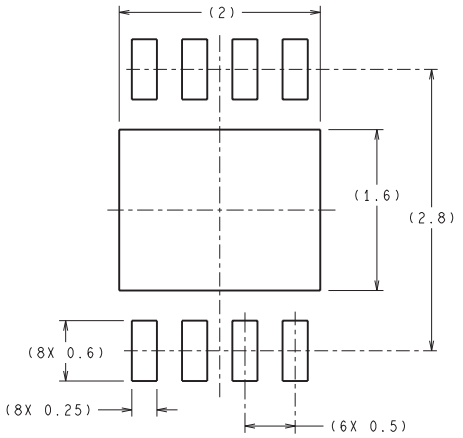
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



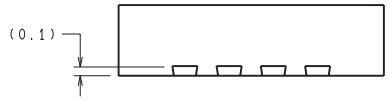
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

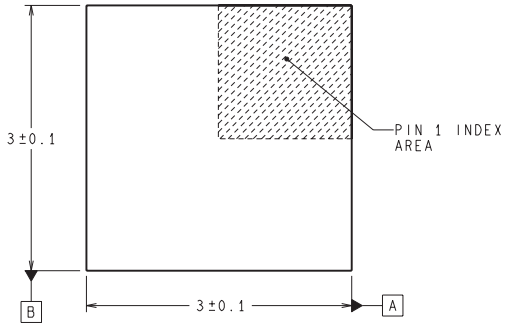
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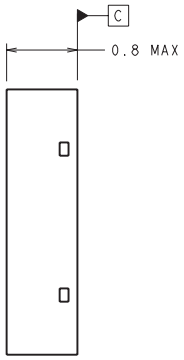


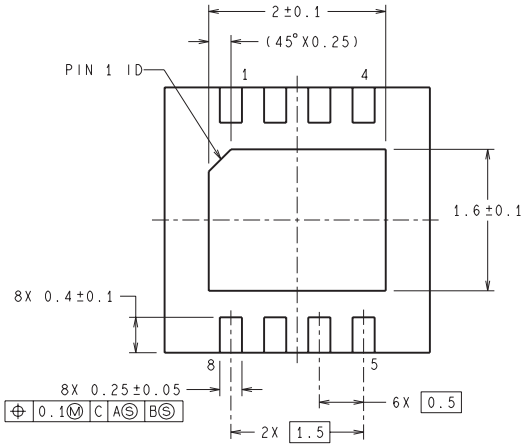
RECOMMENDED LAND PATTERN

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SDA08A (Rev A)

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