4AM17

Silicon N/P Channel MOS FET
High Speed Power Switching

HITACHI

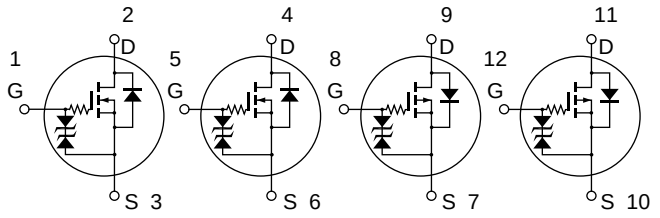
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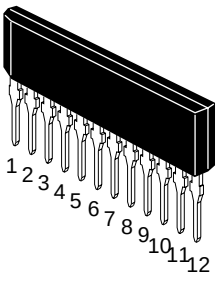
Features

- Low on-resistance
  N Channel: $R_{DS(on)}$ ≤0.17 Ω, V_{GS} = 10 V, I_D = 4 A
  P Channel : $R_{DS(on)}$ ≤ 0.2 Ω, V_{GS} = –10 V, I_D = –4 A
- 4 V gate drive devices.
- High density mounting

Outline

SP-12





1, 5, 8, 12. Gate
2, 4, 9, 11. Drain
3, 6, 7, 10. Source

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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings		Unit
		Nch	Pch	
Drain to source voltage	V_{DSS}	60	–60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	8	–8	A
Drain peak current	$I_{D(pulse)}$ Note1	32	–32	A
Body-drain diode reverse drain current	I_{DR}	8	–8	A
Channel dissipation	Pch (Tc = 25°C) Note2	28		W
Channel dissipation	Pch Note2	4.0		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

Note: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. 4 devices operation

Electrical Characteristics (Ta = 25°C)

(N Channel)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.13	0.17	Ω	I_D = 4 A, V_{GS} = 10 V Note3
	$R_{DS(on)}$	—	0.19	0.24	Ω	I_D = 4 A, V_{GS} = 4 V Note3
Forward transfer admittance	$\|y_{fs}\|$	3.5	5.5	—	S	I_D = 4 A, V_{DS} = 10 V Note3
Input capacitance	Ciss	—	33	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	220	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	5.2	—	pF	f = 1 MHz
Gate series resistance	Rg	—	1.5	—	kΩ	V_{DS} = 10 V, V_{GS} = 0 f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	0.15	—	ns	V_{GS} = 10 V, I_D = 4 A
Rise time	t_r	—	0.5	—	ns	R_L = 7.5 Ω
Turn-off delay time	$t_{d(off)}$	—	3.2	—	ns	
Fall time	t_f	—	1.4	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.5	—	V	I_F = 8 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	850	—	ns	I_F = 8 A, V_{GS} = 0 diF/ dt = 50 A/ µs

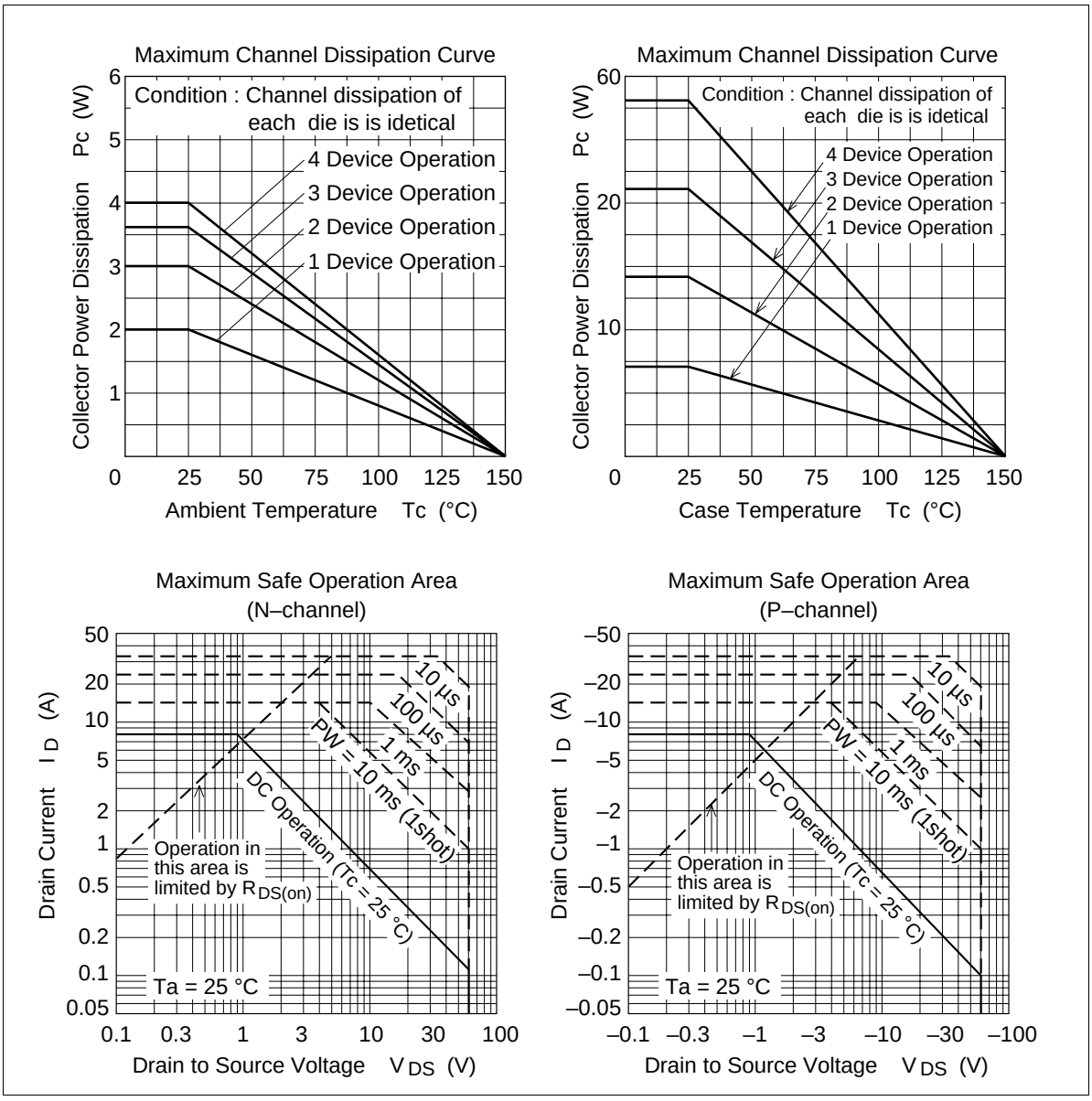
Note: 3. Pulse test

(P Channel)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.15	0.2	Ω	I_D = –4 A, V_{GS} = –10 V [Note3]
	$R_{DS(on)}$	—	0.2	0.27	Ω	I_D = –4 A, V_{GS} = –4 V [Note3]
Forward transfer admittance	$\|y_{fs}\|$	3.5	6.0	—	S	I_D = –4 A, V_{DS} = –10 V [Note3]
Input capacitance	Ciss	—	17	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	460	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	1.2	—	pF	f = 1 MHz
Gate series resistance	Rg	—	3.2	—	kΩ	V_{DS} = 0, V_{GS} = 0 f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	0.6	—	ns	V_{GS} = –10 V, I_D = –4 A
Rise time	t_r	—	2.1	—	ns	R_L = 7.5 Ω
Turn-off delay time	$t_{d(off)}$	—	12	—	ns	
Fall time	t_f	—	5.8	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.2	—	V	I_F = –8 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	2.5	—	ns	I_F = –8 A, V_{GS} = 0 diF/ dt = 50 A/ µs

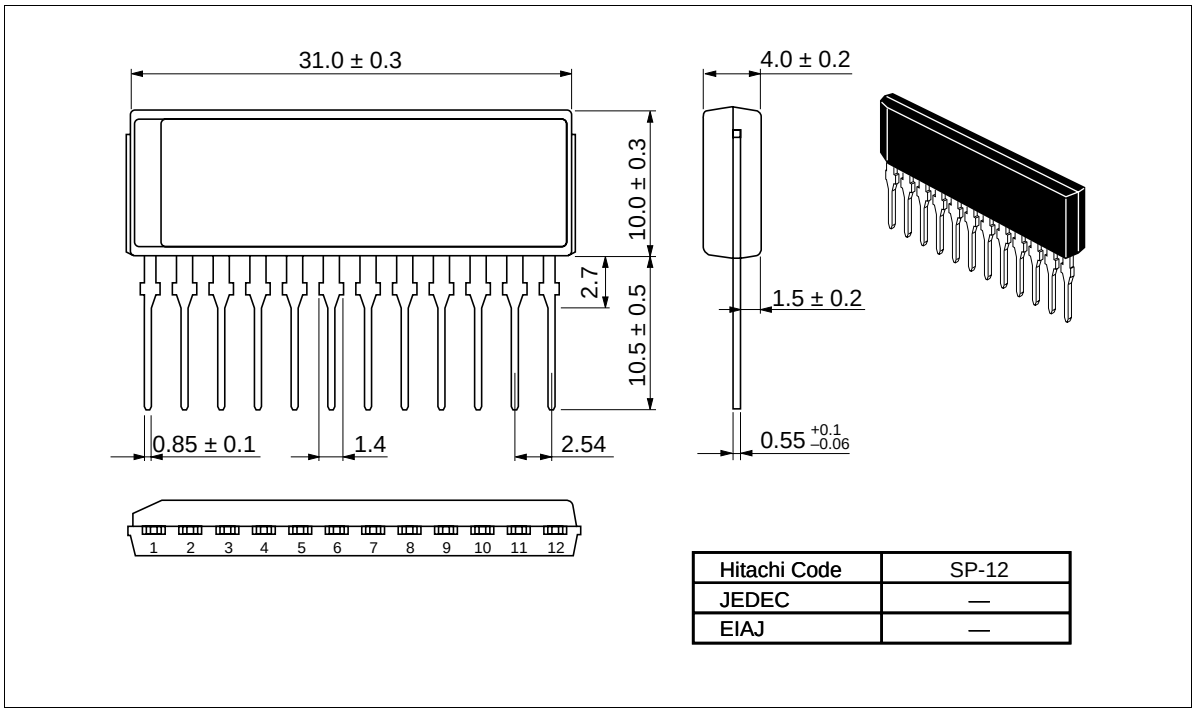
Note: 3. Pulse test

Main Characteristics



Package Dimensions

Unit: mm



Hitachi Code	SP-12
JEDEC	—
EIAJ	—

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HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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