MN38664S

NTSC-Compatible CCD Video Signal Delay Element

■ Overview

The MN38664S is a CCD signal delay element for video signal processing applications.

It contains such components as a threefold-frequency circuit, a shift register clock driver, charge I/O blocks, two CCD analog shift registers switchable between 679, 680.5, and 605 stages, a clamp bias circuit, resampling output amplifiers, and booster circuits.

When the switch input is "L" level, the MN38664S samples the input using the supplied clock signal with a frequency three times the NTSC color signal subcarrier frequency (3.579545 MHz) and, after adding in the attached filter delay, produces independent delays of 1 H (the horizontal scan period) each for the two lines. When the switch input is "H" level, the MN38664S disables the threefold-frequency circuit and samples the input with the image sensor drive frequency (9.545454 MHz) for the camera's 510 horizontal pixels and, after adding in the attached filter delay, produces independent delays of 1 H (the horizontal scan period) each for the two lines.

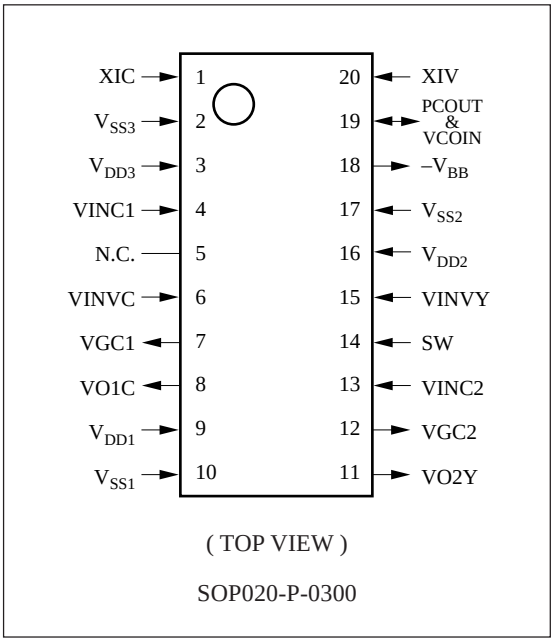
■ Features

- Single 4.4-V power supply
- Choice of camera and VCR modes, so that both the camera and VCR portions of a video camera with 510 horizontal pixels can use the same MN38664S for signal processing

■ Applications

- Video cameras

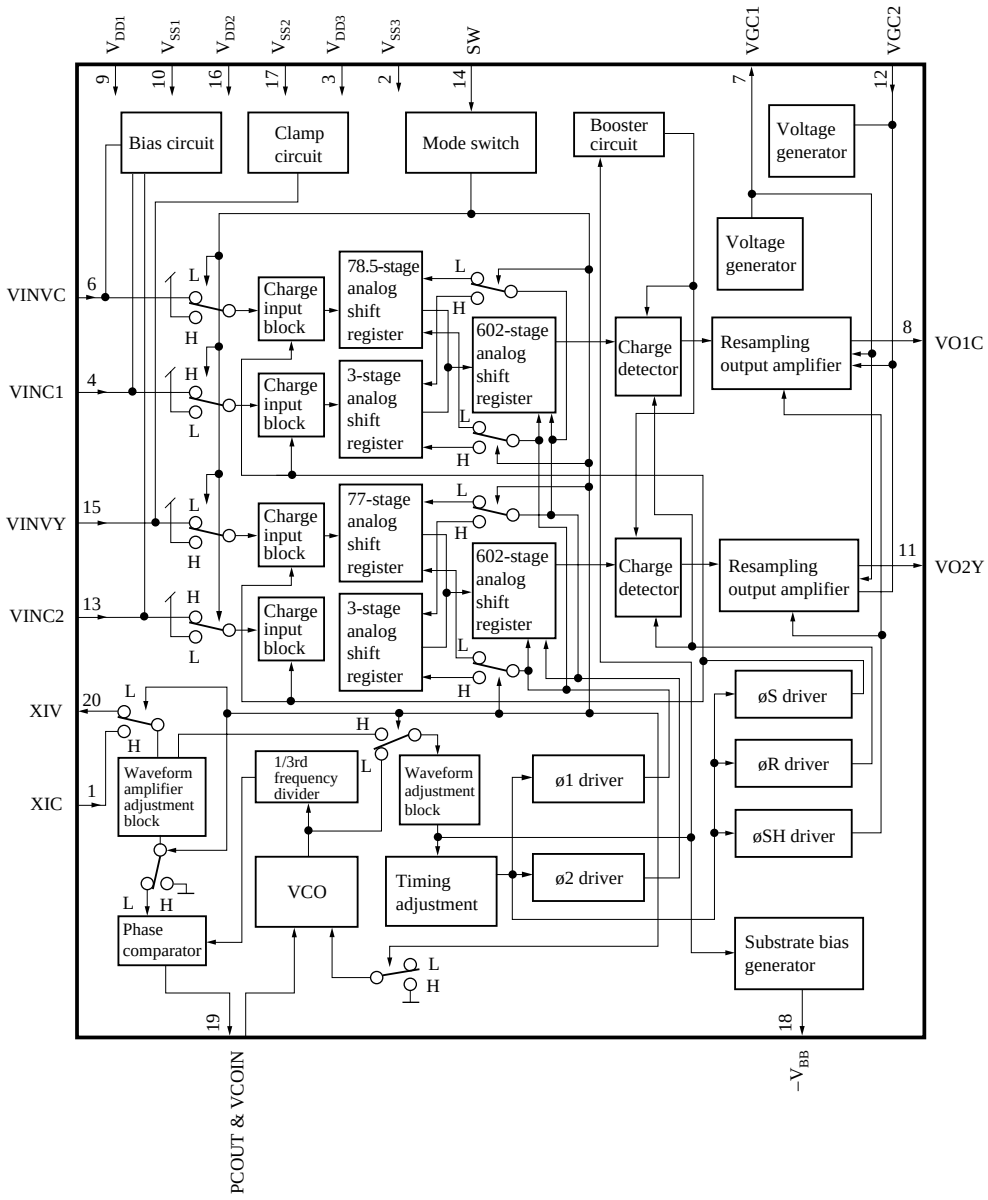
■ Pin Assignment



(TOP VIEW)

SOP020-P-0300

■ Block Diagram



■ Package Dimensions (Unit:mm)

SOP020-P-0300

