Features

- Operating voltage: 2.7V~5.5V
- LED display: 28 rows and 8 commons
- LED data RAM1: 28×8×6 bits=1344 bits for Gray mode
- LED data RAM2: 28×8×6 bits=1344 bits for FADE mode
- LED data RAM3: 28×8 bits=224 bits for Binary mode or Matrix masking
- LED data RAM4: 28×8 bits=224 bits for Universal Segment function
- LED data RAM5: 8×8 bits=64 bits for Universal COM function
- Integrated 4.92MHz RC oscillator
- 64-level global brightness scale
- Binary scale mode or Gray scale mode
- Global blinking or fade function
- Universal COM and Universal Segment function
- Automatic scroll function: up/down/left/right
- Continuous lighting function for ROW24~ROW27
- External current reference control using external resistor
- Supports row port max. 45mA sink constant current
- 8-level current reference adjustment
- Over temperature protection circuit
- I^2C-bus or SPI 3-wire interface
- Cascade function for extend applications
- Package Type: 48-pin LQFP-EP

Applications

- Industrial control displays
- Mobile phones
- Traffic signboards and information displays
- Digital clocks, thermometers, counters, electronic meters
- Instrumentation readouts
- Other consumer applications
- LED displays

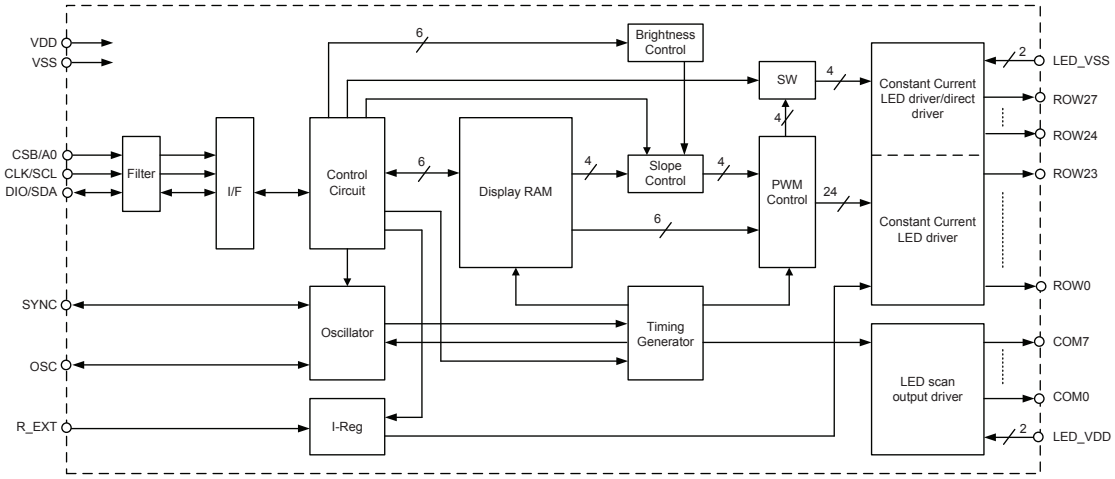
General Description

The HT16D35A/HT16D35B are high accuracy constant current and memory mapping LED display controller/drivers. The maximum display capacity of the devices is 224 patterns composed of 28 rows and 8 commons. The devices can generate a 64 step Gray Scale (PWM data) using software controlled PWM circuitry and 64 LED illumination levels using software controlled PWM circuitry. The devices provide constant current outputs control using external resistors for each row output terminal. A serial interface is provided to allow the devices to receive instructions for its command mode and data mode. Only three lines are required for device interfacing to a host controller. The display capacity can be easily extended by cascading the devices thus expanding its application possibilities. The devices are compatible with most microcontrollers offering easy interfacing via their two serial interfaces, an I^2C interface or a SPI 3-wire serial interface.

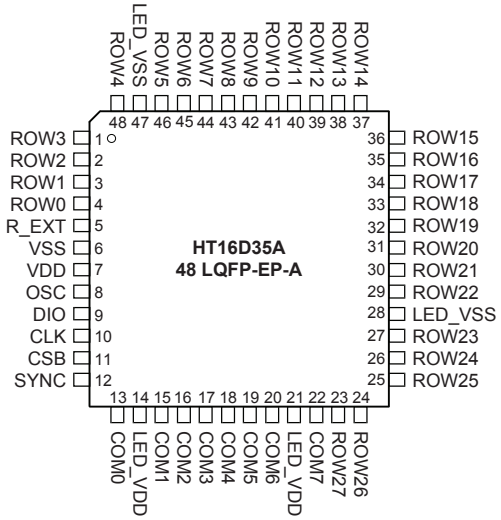
Selection Table

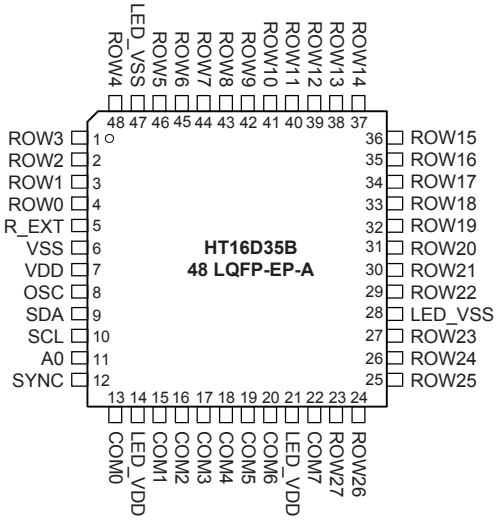
Part Number	Interface
HT16D35A	3-wire SPI
HT16D35B	I^2C

Block Diagram



Pin Assignment





Pin Description

Pin Name	Type	Function
VDD	—	Positive power supply for logic circuits
VSS	—	Negative power supply for logic circuits – ground
LED_VDD	—	Positive power supply for driver circuits
LED_VSS	—	Negative power supply for driver circuits – ground
A0/CSB	I	I^2C interface device address data input pin for I^2C interface Chip Select pin for SPI 3-wire Interface
SCL/CLK	I	Serial clock input pin Serial Clock (SCL) Input for I^2C interface Serial Clock (CLK) Input for SPI 3-wire Interface
SDA/DIO	I/O	Serial data input/output pin. Data is input to or comes out from the shift register at the clock rising edge. I^2C interface serial data (SDA) Input/Output – NMOS open-drain output. SPI 3-wire serial interface serial data input/output – CMOS output.
OSC	I/O	System OSC Input / output pin. If the IRC Mode command is programmed, the system clock is sourced from the internal RC oscillator and the system clock is output on the OSC pin. If the Slave Mode or ERC Mode command is programmed, the system clock is sourced from an external clock on the OSC pin.
SYNC	I/O	If the MASTER MODE command is programmed, the synchronous signal is output on the SYNC pin. If the SLAVE MODE command is programmed, the synchronous signal is input on the SYNC pin.
R_EXT	I	External resistor connection input. Connected to an external resistor to setup the output port current level.
COM0~COM7	O	LED common output pins.
ROW0~ROW27	O	LED row output pins.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+6.0V
Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V
Operating Temperature ..... -40°C to 85°C
Storage Temperature ..... -50°C to 125°C
Thermal Resistance (Rth) ..... 40°C/W
Max junction Temperature (Tj) ..... 125°C

Power Dissipation (PD):
(@Ta=25°C) 2.5W
(@Ta=85°C) 1.0W
ROW Output Current (Single pin) 100mA
Total Power Line Current (Ta=25°C) 1000mA

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{DD}=5V, LED_V_{DD}=5V; Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Logic Supply Voltage	—	—	2.7	—	5.5	V
LED_V_{DD}	LED Supply Voltage	—	—	4.5	—	5.5	V
I_{STB}	Standby Current	5V	No load, Power down mode (System OSC off, LED display off)	—	1	2	μA
I_{DD}	Operating Current	5V	No load, LED ON, R_EXT=500Ω Internal RC OSC, ROW output all on	—	4.5	7.0	mA
I_{LED_VDD}	Operating Current	5V	No load, LED ON, R_EXT=500Ω Internal RC OSC, ROW output all on	—	2.1	3.5	mA
V_{IH}	Input High Voltage	5V	DIO, CLK, SDA, SCL, CSB, OSC, SYNC	0.7V_{DD}	—	5	V
V_{IL}	Input Low Voltage	5V	DIO, CLK, SDA, SCL, CSB, OSC, SYNC	0	—	0.3V_{DD}	V
I_{OH1}	High level output current	5V	V_{OH}=4.5V, OSC, SYNC, DIO	-10	-13	—	mA
I_{OL1}	Low level output current	5V	V_{OL}=0.5V, OSC, SYNC, DIO, SDA	18	25	—	mA
I_{OH2}	COM Source Current	5V	V_{OH}=4.5V	250	400	—	mA
I_{OL2}	COM Sink Current	5V	V_{OL}=0.5V	-45	-60	—	mA
I_{ROW}	ROW Sink current	5V	R_EXT=500Ω, V_{DS}=1V	—	30	—	mA
		5V	R_EXT=1500Ω, V_{DS}=1V	—	10	—	mA
dI_{ROW1}	Bit Current Skew	5V	R_EXT=500Ω, V_{DS}=1V (1)	—	±3.0	—	%
		5V	R_EXT=1500Ω, V_{DS}=1V (1)	—	±3.0	—	%
dI_{ROW2}	Channel Current Skew	5V	R_EXT=500Ω, V_{DS}=1V (2)	—	±3.0	—	%
		5V	R_EXT=1500Ω, V_{DS}=1V (2)	—	±3.0	—	%
%/dV_{DS}	Output Current vs. Output Voltage Regulation	5V	V_{DS}=0.7V~2.0V, V_{DD}=5.0V (3)	—	±0.3	—	%/V
%/dV_{DD}	Output Current vs. Supply Voltage Regulation	—	V_{DD}=4.5V~5.5V, V_{DS}=1.0V (4)	—	±0.3	—	%/V

Note: 1. Bit Skew

$$\text{PIN } dI_{ROW}\ (\%) = \frac{I_{ROW\_(n+1)}\ (V_{DS} = 1V) - I_{ROW\_n}\ (V_{DS} = 1V)}{(I_{ROW\_(n+1)}\ (V_{DS} = 1V) + I_{ROW\_n}\ (V_{DS} = 1V))/2} \times 100\%, \text{ (n: ROW number)}$$

2. Channel Skew

$$+ dI_{ROW}\ (\%) = \frac{I_{ROW\_MAX} - I_{ROW\_AVG}}{I_{ROW\_AVG}} \times 100\%, \text{ (n: ROW number)}$$

$$- dI_{ROW}\ (\%) = \frac{I_{ROW\_MIN} - I_{ROW\_AVG}}{I_{ROW\_AVG}} \times 100\%, \text{ (n: ROW number)}$$

I_{ROW_AVG}: the average current for (I_{ROW_MAX} + I_{ROW_MIN})/2 of all test ROW pins on V_{DS} = 1V

I_{ROW_MAX}: the max current of all test ROW pins on V_{DS} = 1.0V

I_{ROW_MIN}: the min current of all test ROW pins on V_{DS} = 1.0V

3. $$\%/dV_{DS}\ (\%/V) = \frac{I_{ROW\_MAX} - I_{ROW\_MIN}}{(2.0V - 0.7V) \times I_{ROW\_AVG}} \times 100\%$$

I_{ROW_AVG}: the average current for (I_{ROW_MAX} + I_{ROW_MIN})/2 of all test ROW pins between V_{DS} = 0.7V and 2.0V

I_{ROW_MAX}: the max current of all test ROW pins between V_{DS} = 0.7V and 2.0V

I_{ROW_MIN}: the min current of all test ROW pins between V_{DS} = 0.7V and 2.0V

4. $\%/dV_{DD}\ (\%/V) = \dfrac{I_{ROW\_MAX} - I_{ROW\_MIN}}{(5.5V - 4.5V) \times I_{ROW\_AVG}}$

I_{ROW_AVG}: the average current for $(I_{ROW\_MAX} + I_{ROW\_MIN})/2$ of all test ROW pins between V_{DD} = 4.5V and 5.5V

I_{ROW_MAX}: the max current of all test ROW pins between V_{DD} = 4.5V and 5.5V

I_{ROW_MIN}: the min current of all test ROW pins between V_{DD} = 4.5V and 5.5V

V_{DS} = 1V

A.C. Characteristics

V_{DD}=2.7~5.5V; Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS}	System Clock	—	On-chip RC oscillator	4.33	4.92	5.51	MHz
f_{LED}	LED frame rate	—	COM Duty Select, n=1~8	—	$f_{SYS}/(4160\times n)$	—	Hz
V_{POR}	V_{DD} Start voltage to ensure Power on reset	—	—	—	—	100	mV
RR_{VDD}	V_{DD} Rise Rate to ensure Power on reset	—	—	0.05	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} to remain at V_{POR} to ensure Power on reset	—	—	10	—	—	ms

A.C. Characteristics – SPI 3-wire Serial Bus

V_{DD}=2.7~5.5V; Ta=25°C

Symbol	Parameter	Test Condition			Min.	Typ.	Max.	Unit
		V_{DD}	Condition					
t_{CLK}	Clock cycle time	—	—		250	—	—	ns
t_{CW}	Clock Pulse Width	—	—		100	—	—	ns
t_{DS}	Data Setup Time	—	—		50	—	—	ns
t_{DH}	Data Hold Time	—	—		50	—	—	ns
t_{CSW}	“H” CSB Pulse Width	—	—		100	—	—	ns
t_{CSL}	CSB Setup Time (CSB↓ – CLK↑)	—	—		50	—	—	ns
t_{CSH}	CSB Hold Time (CLK↑ – CSB↑)	—	—		2	—	—	μs
t_{PD}	DATA Output Delay Time (CLK – DIO)	—	C_O=15pF	t_{PD}=10 to 90%	—	—	350	ns
				t_{PD}=10 to 10%				

A.C. Characteristics – I²C Serial Bus

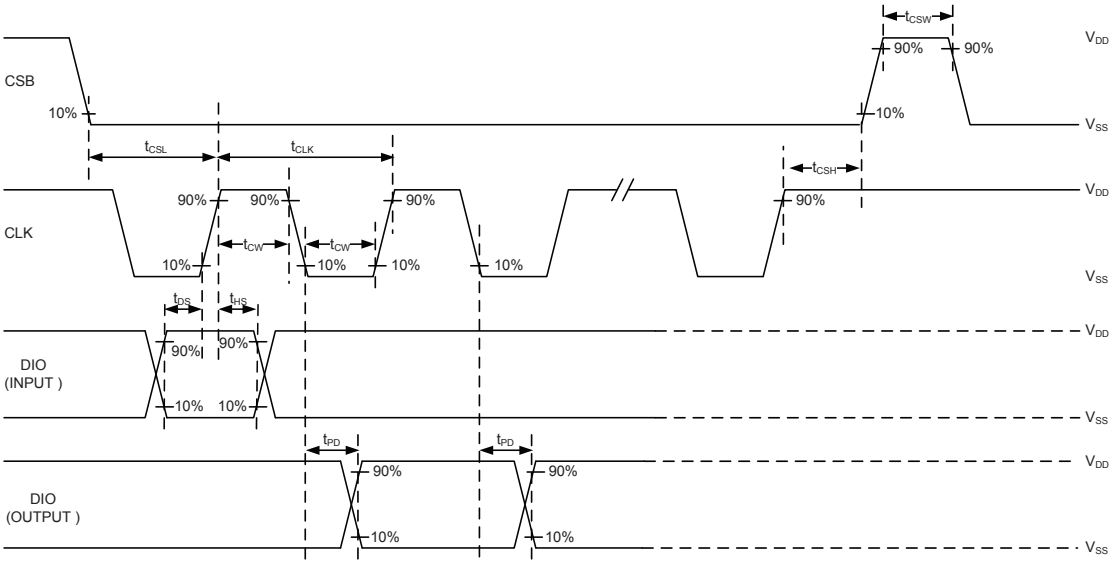
Ta=25°C

Symbol	Parameter	Condition	V_{DD}=2.4V to 5.5V		V_{DD}=3.0V to 5.5V		Unit
			Min.	Max.	Min.	Max.	
f_{SCL}	Clock frequency	—	—	100	—	400	kHz
t_{BUF}	Bus free time	Time in which the bus must be free before a new transmission can start	4.7	—	1.3	—	μs
$t_{HD: STA}$	Start condition hold time	After this period, the first clock pulse is generated	4	—	0.6	—	μs
t_{LOW}	SCL Low time	—	4.7	—	1.3	—	μs
t_{HIGH}	SCL High time	—	4	—	0.6	—	μs
$t_{SU: STA}$	Start condition setup time	Only relevant for repeated START condition	4.7	—	0.6	—	μs
$t_{HD: DAT}$	Data hold time	—	0	—	0	—	ns
$t_{SU: DAT}$	Data setup time	—	250	—	100	—	ns
t_R	SDA and SCL rise time	Note	—	1	—	0.3	μs
t_F	SDA and SCL fall time	Note	—	0.3	—	0.3	μs
$t_{SU: STO}$	Stop condition set-up time	—	4	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	3.5	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	20	—	20	ns

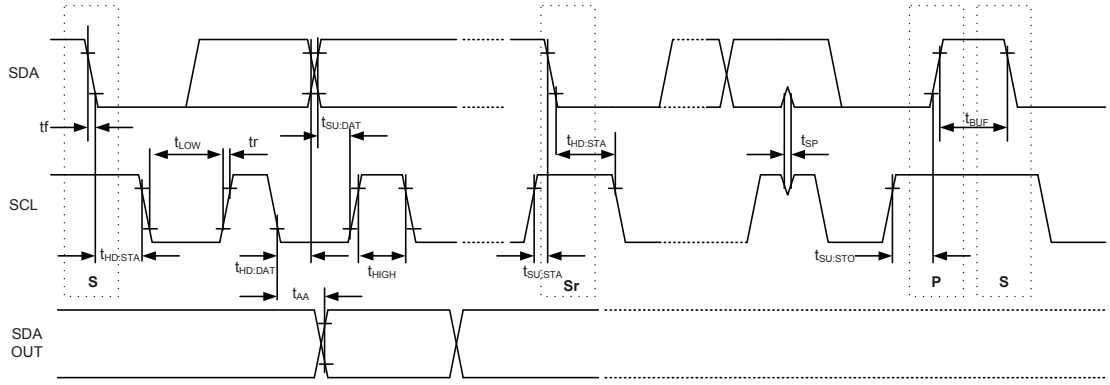
Note: These parameters are periodically sampled but not 100% tested.

Timing Diagrams

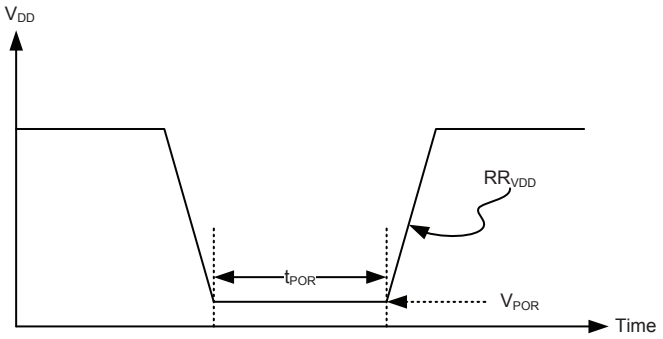
SPI 3-Wire Serial Bus Timing



I²C Bus Timing



Power on Reset Timing



Note: 1. If the reset timing conditions are not satisfied during the power ON/OFF sequence, the internal Power on Reset (POR) circuit will not operate normally.

2. If it is difficult to meet power on reset timing conditions, execute software reset command after Power on.

Functional Description

Power-on Reset

After power is applied the device will be initialised by an internal power-on reset circuit. The internal circuit status after initialisation is as follows:

- All registers are set to their default value but the contents of the DDRAM are not affected
- System Oscillator will be off
- All COM outputs will be high impedance
- All ROW outputs will be high impedance
- The LED display will be in an off state

Data transfers on the I^2C-bus or SPI 3-wire serial bus should be avoided for 1ms following a power-on to allow the reset initialisation operation to complete.

LED Driver

The HT16D35A/HT16D35B is a 224 (28×8) pattern LED driver which can be configured to have 1 or 8 commons using the Number of COM output Command configuration. This feature makes the HT16D35A/HT16D35B suitable for multiple LED applications.

System Oscillator

The internal logic and the LED drive signals of the HT16D35A/HT16D35B are timed by the integrated RC oscillator.

The System Clock frequency determines the LED frame frequency. A clock signal must always be supplied to the device; removing the clock may freeze the device if the standby mode command is executed. At initial system power on, the System Oscillator is in the stop state.

ROW Driver Outputs

The LED drive section includes 28 ROW outputs. ROW0 to ROW27 which should be connected directly to the LED panel. The ROW output signals are generated in accordance with the multiplexed column signals and with the data resident in the display latch. When less than 28 ROW outputs are required the unused ROW outputs should be left open-circuit.

Column Driver Outputs

The LED drive section includes eight column outputs, COM0 to COM7, which should be connected directly to the LED panel. The column output signals are generated in accordance with the selected LED drive mode. When less than 8 column outputs are required the unused column outputs should be left open-circuit

Address Pointer

The addressing mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialisation of the address pointer using the Address pointer command.

Over Temperature Protection

The devices include thermal protection circuitry. When the junction temperatures exceed a certain temperature the temperature protection circuit is activated. The TSD flag bit will be set to “1”, the display will be off and the direct pins will be turned off.

When the chip junction temperature exceeds 150°C, the entire IC display is turned off and the direct pins will be turned off along with the TSD flag bit being set to “1”. The device will resume operation and turn on the direct pins and the TSD flag bit will be cleared to “0” when the chip junction temperatures falls below 125°C.

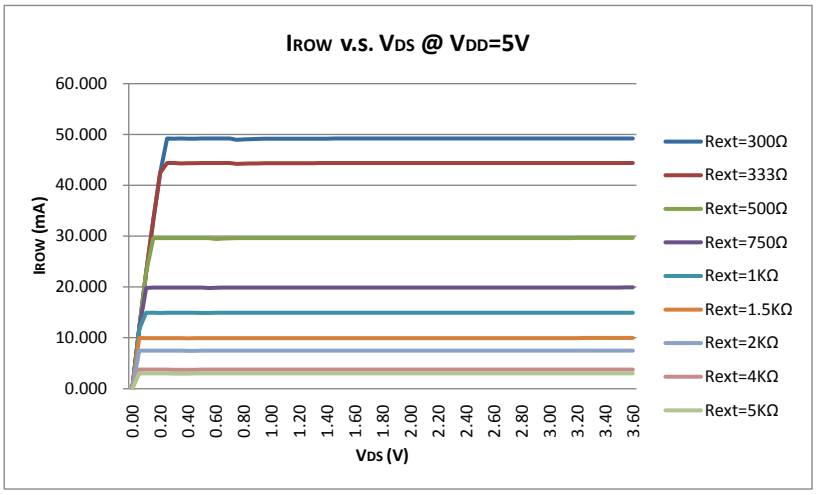
The temperature protection function detect temperature has a value of about 150°C but as the detect temperature function includes hysteresis, its release temperature is about 125°C.

Constant Current Output

The constant current output of each row output channel is setup using an external resistor connected between the R_EXT pin and GND. The current scale range can be adjusted by changing the resistor value. The maximum current variation between channels is less than ±3%. The characteristic curve of the output stage in the saturation region is flat for which users can refer to the charts below. The output current remains constant regardless of the LED forward voltage (V_F) variations. The constant current can be calculated using the following formula:

V_{R_EXT}=1.25V, I_{ROW}=(V_{R_EXT}/R_EXT)×12=15/R_EXT for current range

The following IV curve is supplied for reference.



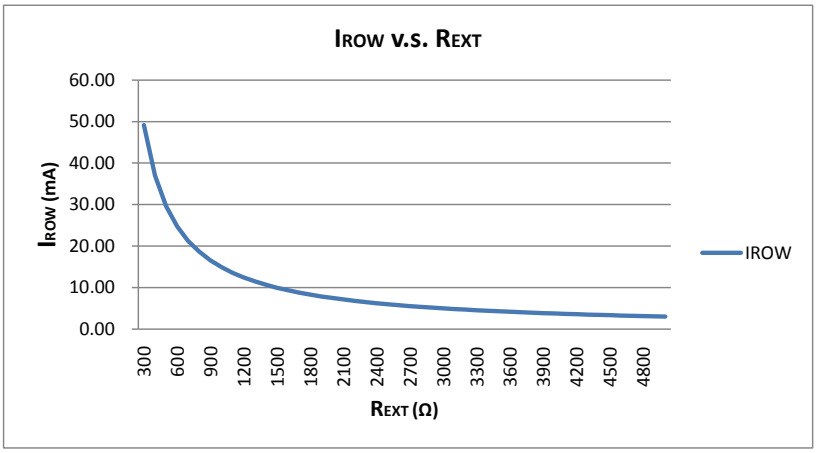
Setting the Output Current

The output current (I_{ROW}) is setup using an external resistor, R_EXT. The maximum LED current can be calculated using the following formula:

$$I_{ROW\_MAX}\ [A] = 15 / R\_EXT\ (\Omega)\ (Typ.)$$

As a warning it should be noted that the maximum LED current value is 45mA.

The default relationship between I_{ROW} and R_EXT is shown in the following figure.

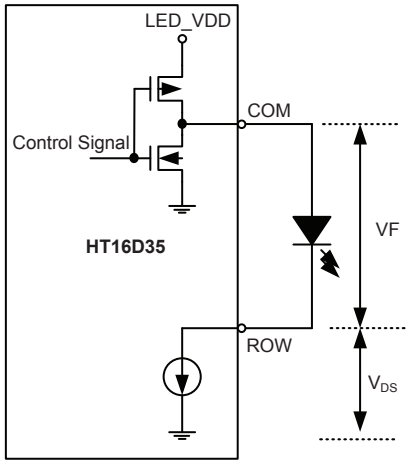


The Maximum ROW current and Delta ROW current values are shown in the next table. If the R_EXT value is changed, the new LED current step can be seen from the table. The recommended value for R_EXT is 500Ω.

R_EXT (Ω)	5K	3K	2.5K	1.5K	1K	750	600	500	375	300
I_{ROW_MAX} (mA)	3	5	6	10	15	20	25	30	40	50

Load Supply Voltage – LED_V_{DD}

The devices can be operated satisfactorily when V_{DS} lies between a value of 0.7V to 2.0V. It is recommended to use a low supply voltage for LED_V_{DD} to reduce the V_{DS} value which will reduce the device power consumption and subsequent device temperature.



Display Data RAM – DDRAM

In the Binary Mode, the display RAM is a static 28×8-bit capacity RAM in which is stored the LED data. A logic "1" in the RAM bit-map indicates an "on" state of the corresponding LED ROW. Similarly a logic 0 indicates an "off" state. There is a one-to-one correspondence between the display memory addresses and the ROW outputs and between the individual bits of a RAM word and the column outputs. The following shows the mapping from the RAM to the LED pattern.

Output	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	Address A[7:0]
ROW0	D7	D6	D5	D4	D3	D2	D1	D0	00h
ROW1	D7	D6	D5	D4	D3	D2	D1	D0	01h
ROW2	D7	D6	D5	D4	D3	D2	D1	D0	02h
ROW3	D7	D6	D5	D4	D3	D2	D1	D0	03h
ROW4	D7	D6	D5	D4	D3	D2	D1	D0	04h
ROW5	D7	D6	D5	D4	D3	D2	D1	D0	05h
ROW6	D7	D6	D5	D4	D3	D2	D1	D0	06h
ROW7	D7	D6	D5	D4	D3	D2	D1	D0	07h
ROW8	D7	D6	D5	D4	D3	D2	D1	D0	08h
ROW9	D7	D6	D5	D4	D3	D2	D1	D0	09h
ROW10	D7	D6	D5	D4	D3	D2	D1	D0	0Ah
ROW11	D7	D6	D5	D4	D3	D2	D1	D0	0Bh
ROW12	D7	D6	D5	D4	D3	D2	D1	D0	0Ch
ROW13	D7	D6	D5	D4	D3	D2	D1	D0	0Dh
ROW14	D7	D6	D5	D4	D3	D2	D1	D0	0Eh
ROW15	D7	D6	D5	D4	D3	D2	D1	D0	0Fh
ROW16	D7	D6	D5	D4	D3	D2	D1	D0	10h
ROW17	D7	D6	D5	D4	D3	D2	D1	D0	11h
ROW18	D7	D6	D5	D4	D3	D2	D1	D0	12h
ROW19	D7	D6	D5	D4	D3	D2	D1	D0	13h
ROW20	D7	D6	D5	D4	D3	D2	D1	D0	14h

Output	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	Address A[7:0]
ROW21	D7	D6	D5	D4	D3	D2	D1	D0	15h
ROW22	D7	D6	D5	D4	D3	D2	D1	D0	16h
ROW23	D7	D6	D5	D4	D3	D2	D1	D0	17h
ROW24	D7	D6	D5	D4	D3	D2	D1	D0	18h
ROW25	D7	D6	D5	D4	D3	D2	D1	D0	19h
ROW26	D7	D6	D5	D4	D3	D2	D1	D0	1Ah
ROW27	D7	D6	D5	D4	D3	D2	D1	D0	1Bh
Bits	D7	D6	D5	D4	D3	D2	D1	D0	Data

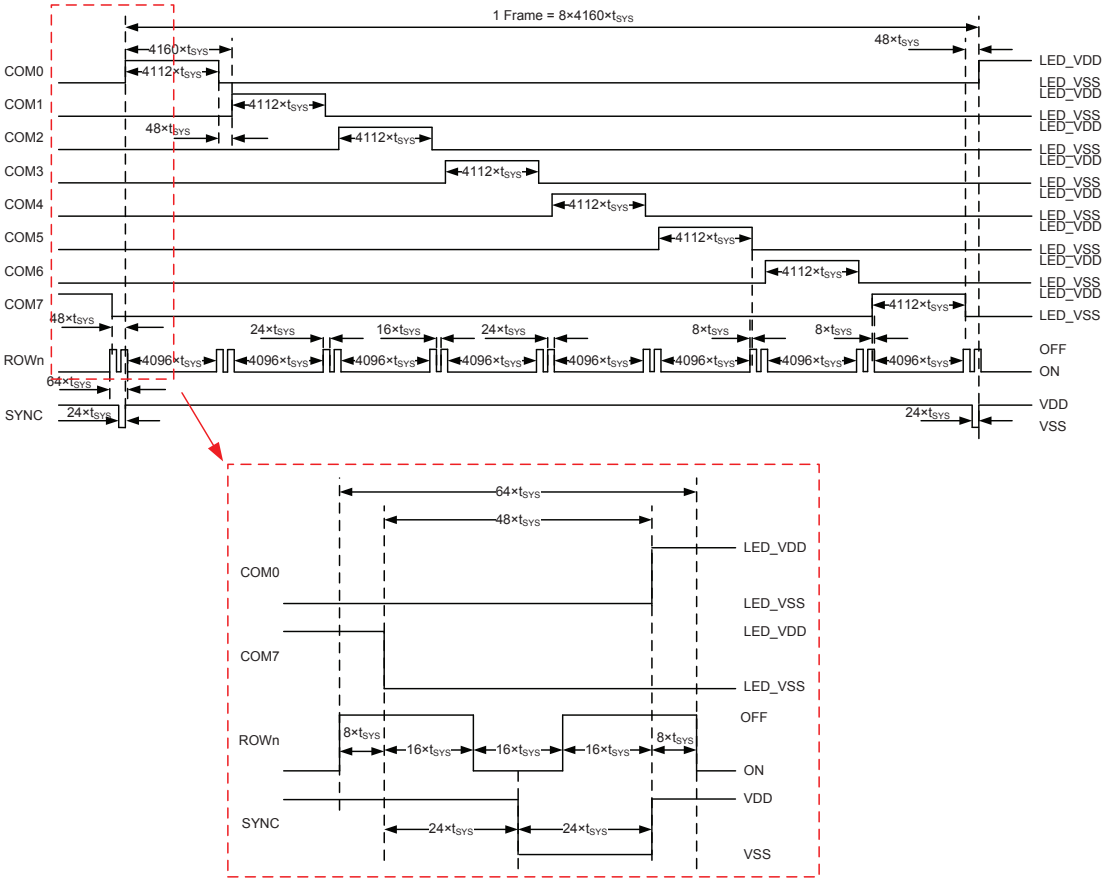
In the Gray Mode, the display RAM is a static 28×8×6-bit RAM in which is stored the LED data. A logic "1" in the RAM bit-map indicates an "on" state of the corresponding LED ROW. Similarly a logic 0 indicates an "off" state. There is a one-to-one correspondence between the display memory addresses and the ROW outputs and between the individual bits of a RAM word and the column outputs. The following shows the mapping from the RAM to the LED pattern.

Output	ROW0	ROW1	ROW2	-----	ROW25	ROW26	ROW27	Address A[7:0]
COM0	00h	01h	02h	-----	19h	1Ah	1Bh	00h~1Bh
COM1	20h	21h	22h	-----	39h	3Ah	3Bh	20h~3Bh
COM2	40h	41h	42h	-----	59h	5Ah	5Bh	40h~5Bh
COM3	60h	61h	62h	-----	79h	7Ah	7Bh	60h~7Bh
COM4	80h	81h	82h	-----	99h	9Ah	9Bh	80h~9Bh
COM5	A0h	A1h	A2h	-----	B9h	BAh	BBh	A0h~BBh
COM6	C0h	C1h	C2h	-----	D9h	DAh	DBh	C0h~DBh
COM7	E0h	E1h	E2h	-----	F9h	FAh	FBh	E0h~FBh
Byte	D7~D0	D7~D0	D7~D0	-----	D7~D0	D7~D0	D7~D0	Data

LED Driver Output Waveform

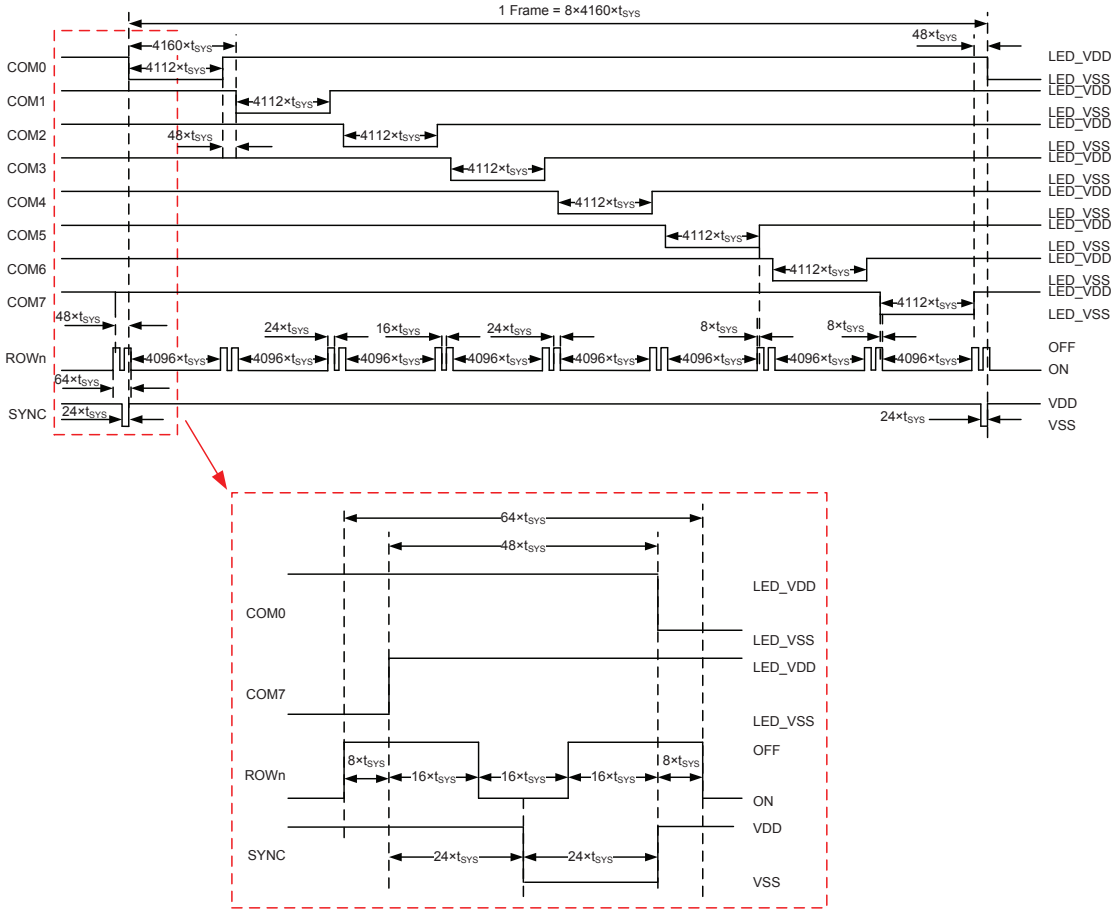
The device includes a 224 (28×8) pattern LED driver. This can be setup in a 224×8 format for the COM outputs. This feature allows the device to be used in multiple LED applications. The LED drive mode waveforms and scanning format is as follows:

1. P-MOS Open Drain for 28×8 Driver Mode and Disable Discharge Function



Note: $t_{SYS}=1/f_{SYS}$ (1/4.92MHz).

2. N-MOS Open Drain for 28 ×8 Driver Mode and Disable Discharge Function



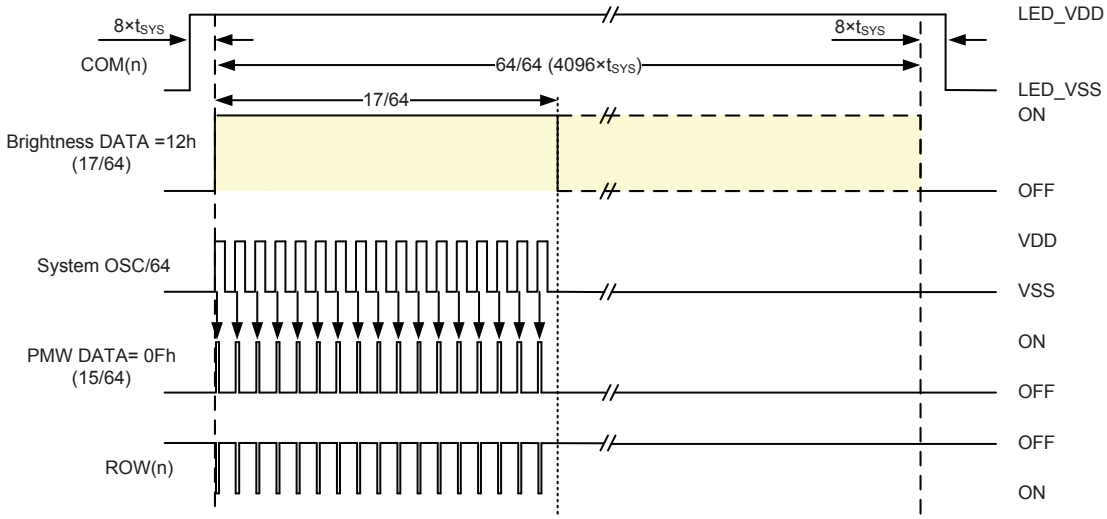
Note: $t_{SYS}=1/f_{SYS}$ (1/4.92MHz).

Output Signal Timing

The relationship between the ROW and COM digital dimming duty times are shown in the accompanying diagram.

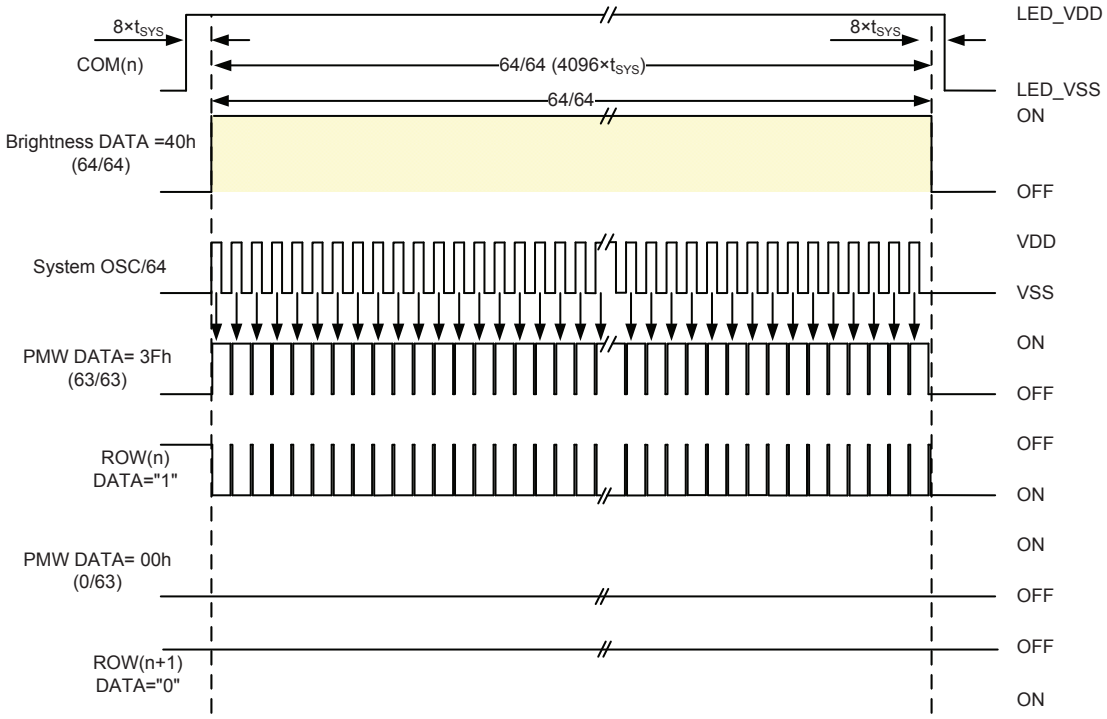
1. The setup condition is shown as follows:

- Gray mode
- COM0~COM7, Scan High type
- Brightness PWM duty=17/64



2. The setup condition is shown as follows:

- Binary mode
- COM0~COM7, Scan High type
- Brightness PWM duty=64/64



Fade Data RAM

The fade RAM is a static 28×8×6-bit RAM which stores the mode function, delay time function and slope cycle time function for each dot. There is a one-to-one correspondence between the fade function memory addresses and the ROW outputs and between the individual bits of a RAM word and the column outputs.

The following shows a mapping from the fade RAM to the LED pattern:

Output	ROW0	ROW1	ROW2	-----	ROW25	ROW26	ROW27	Address A[7:0]
COM0	00h	01h	02h	-----	19h	1Ah	1Bh	00h~1Bh
COM1	20h	21h	22h	-----	39h	3Ah	3Bh	20h~3Bh
COM2	40h	41h	42h	-----	59h	5Ah	5Bh	40h~5Bh
COM3	60h	61h	62h	-----	79h	7Ah	7Bh	60h~7Bh
COM4	80h	81h	82h	-----	99h	9Ah	9Bh	80h~9Bh
COM5	A0h	A1h	A2h	-----	B9h	BAh	BBh	A0h~BBh
COM6	C0h	C1h	C2h	-----	D9h	DAh	DBh	C0h~DBh
COM7	E0h	E1h	E2h	-----	F9h	FAh	FBh	E0h~FBh
Byte	D7~D0	D7~D0	D7~D0	-----	D7~D0	D7~D0	D7~D0	Data

Note: The addresses will continuously increment automatically. The address will be wrapped around to address 0x00H when it exceeds the maximum address value of 0xFBH.

Universal COM (UCOM) RAM Data

The Universal COM (UCOM) RAM is a static 8×8-bit RAM which stores 8 types of symbol patterns per timing (T0~T7). The symbol data specified by the UCOM is directly driven onto the COM outputs. There is a one-to-one correspondence between the duty time (T0~T7) addresses and the COM outputs and also between the individual bits of a RAM word and the symbol patterns per timing (T0~T7).

The following shows the mapping from the patterns per timing (T0~T7) to the COM output:

Timing	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	Address
T0	D7	D6	D5	D4	D3	D2	D1	D0	00h
T1	D7	D6	D5	D4	D3	D2	D1	D0	01h
T2	D7	D6	D5	D4	D3	D2	D1	D0	02h
T3	D7	D6	D5	D4	D3	D2	D1	D0	03h
T4	D7	D6	D5	D4	D3	D2	D1	D0	04h
T5	D7	D6	D5	D4	D3	D2	D1	D0	05h
T6	D7	D6	D5	D4	D3	D2	D1	D0	06h
T7	D7	D6	D5	D4	D3	D2	D1	D0	07h
Bits	D7	D6	D5	D4	D3	D2	D1	D0	Data

Note: 1. The Universal COM RAM is a static 8×8-bit RAM in which is stored the COM pin on/off data. A logic "1" in the RAM bit-map indicates an "on" state of the corresponding COM pin. Similarly a logic 0 indicates an "off" state.

2. The addresses will continuously increment automatically. The address will be wrapped around to address 0x00H when it exceeds the maximum address value of 0x07H.

Universal SEG (USEG) RAM Data

The display contents of every ROW may be setup according to the USEG to redirect the display ROW address. This command parameter is validated during the Timing 1 period of each frame when the command is set.

The Universal SEG (USEG) RAM is a static 28×8-bit RAM which stores 28 symbol pattern Universal ROW addresses. The symbol data specified by the USEG is directly output to the ROW. There is a one-to-one correspondence between the Universal ROW address and the ROW outputs and between the individual bits of a RAM word and the symbol pattern Universal ROW address.

The following shows the mapping for the Universal ROW address to the ROW output.

USEG RAM Address	Universal ROW address data set								ROW Output
	X	X	X	US4	US3	US2	US1	US0	
00h	X	X	X	D4	D3	D2	D1	D0	ROW0
01h	X	X	X	D4	D3	D2	D1	D0	ROW1
02h	X	X	X	D4	D3	D2	D1	D0	ROW2
03h	X	X	X	D4	D3	D2	D1	D0	ROW3
04h	X	X	X	D4	D3	D2	D1	D0	ROW4
05h	X	X	X	D4	D3	D2	D1	D0	ROW5
06h	X	X	X	D4	D3	D2	D1	D0	ROW6
07h	X	X	X	D4	D3	D2	D1	D0	ROW7
08h	X	X	X	D4	D3	D2	D1	D0	ROW8
09h	X	X	X	D4	D3	D2	D1	D0	ROW9
0Ah	X	X	X	D4	D3	D2	D1	D0	ROW10
0Bh	X	X	X	D4	D3	D2	D1	D0	ROW11
0Ch	X	X	X	D4	D3	D2	D1	D0	ROW12
0Dh	X	X	X	D4	D3	D2	D1	D0	ROW13
0Eh	X	X	X	D4	D3	D2	D1	D0	ROW14
0Fh	X	X	X	D4	D3	D2	D1	D0	ROW15
10h	X	X	X	D4	D3	D2	D1	D0	ROW16
11h	X	X	X	D4	D3	D2	D1	D0	ROW17
12h	X	X	X	D4	D3	D2	D1	D0	ROW18
13h	X	X	X	D4	D3	D2	D1	D0	ROW19
14h	X	X	X	D4	D3	D2	D1	D0	ROW20
15h	X	X	X	D4	D3	D2	D1	D0	ROW21
16h	X	X	X	D4	D3	D2	D1	D0	ROW22
17h	X	X	X	D4	D3	D2	D1	D0	ROW23
18h	X	X	X	D4	D3	D2	D1	D0	ROW24
19h	X	X	X	D4	D3	D2	D1	D0	ROW25
1Ah	X	X	X	D4	D3	D2	D1	D0	ROW26
1Bh	X	X	X	D4	D3	D2	D1	D0	ROW27
Bits	D7	D6	D5	D4	D3	D2	D1	D0	Data

Note: 1. The Universal SEG RAM is a static 28×8-bit RAM which stores the mapping data of the universal row address.

2.The USEG RAM addresses will continuously increment automatically. The address will be wrapped around to address 0x00h when it exceeds the maximum address value of 0x1Bh.

Matrix Masking RAM Data

The Matrix masking RAM is a static 28×8-bits RAM which stores the mask data. A logic "1" in the RAM bit-map indicates a "mask on" state of the corresponding LED ROW. Similarly a logic 0 indicates a "mask off" state.

There is a one-to-one correspondence between the Matrix display masking memory addresses and the ROW outputs and between the individual bits of a RAM word and the column outputs.

The following shows the mapping from the Matrix display masking RAM to the LED pattern.

Output	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	Address A[4:0]
ROW0	D7	D6	D5	D4	D3	D2	D1	D0	00h
ROW1	D7	D6	D5	D4	D3	D2	D1	D0	01h
ROW2	D7	D6	D5	D4	D3	D2	D1	D0	02h
ROW3	D7	D6	D5	D4	D3	D2	D1	D0	03h
ROW4	D7	D6	D5	D4	D3	D2	D1	D0	04h
ROW5	D7	D6	D5	D4	D3	D2	D1	D0	05h
ROW6	D7	D6	D5	D4	D3	D2	D1	D0	06h
ROW7	D7	D6	D5	D4	D3	D2	D1	D0	07h
ROW8	D7	D6	D5	D4	D3	D2	D1	D0	08h
ROW9	D7	D6	D5	D4	D3	D2	D1	D0	09h
ROW10	D7	D6	D5	D4	D3	D2	D1	D0	0Ah
ROW11	D7	D6	D5	D4	D3	D2	D1	D0	0Bh
ROW12	D7	D6	D5	D4	D3	D2	D1	D0	0Ch
ROW13	D7	D6	D5	D4	D3	D2	D1	D0	0Dh
ROW14	D7	D6	D5	D4	D3	D2	D1	D0	0Eh
ROW15	D7	D6	D5	D4	D3	D2	D1	D0	0Fh
ROW16	D7	D6	D5	D4	D3	D2	D1	D0	10h
ROW17	D7	D6	D5	D4	D3	D2	D1	D0	11h
ROW18	D7	D6	D5	D4	D3	D2	D1	D0	12h
ROW19	D7	D6	D5	D4	D3	D2	D1	D0	13h
ROW20	D7	D6	D5	D4	D3	D2	D1	D0	14h
ROW21	D7	D6	D5	D4	D3	D2	D1	D0	15h
ROW22	D7	D6	D5	D4	D3	D2	D1	D0	16h
ROW23	D7	D6	D5	D4	D3	D2	D1	D0	17h
ROW24	D7	D6	D5	D4	D3	D2	D1	D0	18h
ROW25	D7	D6	D5	D4	D3	D2	D1	D0	19h
ROW26	D7	D6	D5	D4	D3	D2	D1	D0	1Ah
ROW27	D7	D6	D5	D4	D3	D2	D1	D0	1Bh
Bits	D7	D6	D5	D4	D3	D2	D1	D0	Data

Note: 1. The Matrix display masking RAM is a static 28×8-bit RAM which stores the row output masking state.

2.The USEG RAM addresses will continuously increment automatically. The address will be wrapped around to address 0x00h when it exceeds the maximum address value of 0x1Bh.

3. In the Binary Mode the Matrix display masking function is invalid.

Command Description – Command Table

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Description
RAM R/W Command											
Write Display Data	W	1	0	0	0	0	0	0	0	80h	Write Display RAM Data
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM Address
	W	D7	D6	D5	D4	D3	D2	D1	D0	—	Display Data Range: 00h~1bh for Binary Mode Range: 00h~fbh for Gray Mode
Read Display Data	W	1	0	0	0	0	0	0	1	81h	Read Display RAM
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM Address
	R	0	0	0	0	0	0	0	0	—	Dummy Byte
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	Display data Range: 00h~1bh for Binary Mode Range: 00h~fbh for Gray Mode
Write Fade Data	W	1	0	0	0	0	0	1	0	82h	Write fade RAM Data
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM Address
	W	X	X	FSS	X	SD1	SD0	SC1	SC0	—	Set Parameters for Fade Mode FSS: Flash or Fade Mode select SD [3:2]: Delay Time Set SC [1:0]: Flash cycle time or Slope cycle time set
Read Fade Data	W	1	0	0	0	0	0	1	1	83h	Read Parameters of Fade RAM Data
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM Address
	R	0	0	0	0	0	0	0	0	—	Dummy Byte
	R	0	0	FSS	0	SD1	SD0	SC1	SC0	—	Parameters of Fade Data Range: 00h~fbh
Write UCOM Data	W	1	0	0	0	0	1	0	0	84h	Write UCOM RAM Data
	W	X	X	X	X	X	A2	A1	A0	00h	RAM Address
	W	D7	D6	D5	D4	D3	D2	D1	D0	—	UCOM Data Range: 00h~07h
Read UCOM Data	W	1	0	0	0	0	1	0	1	85h	Read UCOM Data
	W	X	X	X	X	X	A2	A1	A0	00h	RAM Address
	R	0	0	0	0	0	0	0	0	—	Dummy Byte
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	UCOM Data Range: 00h~07h
Write USEG Data	W	1	0	0	0	0	1	1	0	86h	Write USEG RAM Data
	W	X	X	X	A4	A3	A2	A1	A0	00h	RAM Address
	W	X	X	X	US4	US3	US2	US1	US1	—	USEG Data Range: 00h~1bh
Read USEG Data	W	1	0	0	0	0	1	1	1	87h	Read USEG Control Data
	W	X	X	X	A4	A3	A2	A1	A0	00h	RAM Address
	R	0	0	0	0	0	0	0	0	—	Dummy Byte
	R	X	X	X	US4	US3	US2	US1	US1	—	USEG Data Range: 00h~1bh
Write Matrix Masking Data	W	1	0	0	0	1	0	0	0	88h	Write Matrix Masking Data
	W	0	0	0	A4	A3	A2	A1	A0	00h	RAM Address
	W	D7	D6	D5	D4	D3	D2	D1	D0	—	Matrix Masking Data
Read Matrix Masking Data	W	1	0	0	0	1	0	0	1	89h	Read Matrix Masking Data
	W	0	0	0	A4	A3	A2	A1	A0	00h	RAM Address
	R	0	0	0	0	0	0	0	0	—	Dummy Byte
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	Matrix Masking Data Range: 00h~1bh
Function Command											
Read Flag	W	0	1	1	1	0	0	0	0	70h	Read Flag
	R	0	0	0	0	0	0	0	0	00h	Dummy Byte
	R	X	X	X	X	X	X	COM0 flag	TSD flag	00h	Flag Data parameters

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Description
Read Status	W	0	1	1	1	0	0	0	1	71h	Read internal command information
	R	0	0	0	0	0	0	0	0	00h	Dummy Byte
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	Internal command information
Scrolling Control	W	0	0	1	0	0	0	0	0	20h	SCEN: Scrolling SW on/off RL/UD: Set scrolling direction HEN: Horizontal Scrolling on/off VEN: Vertical Scrolling on/off
	W	SCEN	X	VEN	HEN	X	X	UD	RL	00h	
Scrolling Speed	W	0	0	1	0	0	0	0	1	21h	Scrolling speed control HSP0~3: Horizontal Speed VSP0~3: Vertical Speed
	W	VSP3	VSP2	VSP1	VSP0	HSP3	HSP2	HSP1	HSP0	00h	
Binary/Gray Select	W	0	0	1	1	0	0	0	1	31h	Binary Mode or Gray Mode select
	W	X	X	X	X	X	X	X	BGS	00h	
Number of COM Outputs	W	0	0	1	1	0	0	1	0	32h	Number of COM scan outputs and COM output type
	W	CNS	X	X	X	X	CN2	CN1	CN0	07h	
Global Blinking	W	0	0	1	1	0	0	1	1	33h	Blinking Time or Fade Time select
	W	BSS	X	X	X	X	X	BS1	BS0	80h	
Cascade Mode	W	0	0	1	1	0	1	0	0	34h	Master Mode or Slave Mode select
	W	X	X	X	X	X	MS2	MS1	MS0	00h	
Set System Control	W	0	0	1	1	0	1	0	1	35h	System oscillator on/off and display on/off control
	W	X	X	X	X	X	X	FON	DON	00h	
Constant current ratio	W	0	0	1	1	0	1	1	0	36h	Constant current ratio select – 8 steps
	W	X	X	X	X	0	CC2	CC1	CC0	00h	
Global Brightness	W	0	0	1	1	0	1	1	1	37h	Luminance control PWM adjustment – 64 steps
	W	X	BC6	BC5	BC4	BC3	BC2	BC1	BC0	40h	
Mode Control	W	0	0	1	1	1	0	0	0	38h	FDEN: FADE function on/off BKEN: Blink function on/off UCEN: UCOM function on/off MKEN: Display mask on/off USEN: USEG function on/off TSDSL: Select auto control or user control display on/off function when the over temperature protection is enabled TSDEN: Thermal protect circuit on/off
	W	TSD EN	TSD SL	X	USEN	MKEN	UCEN	BKEN	FDEN	00h	
COM Pin Control	W	0	1	0	0	0	0	0	1	41h	COM pin SW on/off
	W	C7	C6	C5	C4	C3	C2	C1	C0	00h	
ROW Pin Control	W	0	1	0	0	0	0	1	0	42h	ROW pin SW on/off
	W	R27	R26	R25	R24	R23	R22	R21	R20	00h	ROW27~ROW20 SW on/off
	W	R19	R18	R17	R16	R15	R14	R13	R12	00h	ROW12~ROW19 SW on/off
	W	R11	R10	R9	R8	R7	R6	R5	R4	00h	ROW4~ROW11 SW on/off
	W	X	X	X	X	R3	R2	R1	R0	00h	ROW3~ROW0 SW on/off
Direct Pin Control	W	0	1	0	0	0	0	1	1	43h	Set Direct Output Mode
	W	PW24	PW25	PW26	PW27	DR24	DR25	DR26	DR27	11h	DR [24:27]: ROW24~ROW27 can be set as direct pin or row pin. PW[24:27]: Direct PWM data output SW on/off, when ROW24~ROW27 pins are set as direct pins.
PWM Data for Direct ROW27	W	0	1	0	0	0	1	0	0	44h	PWM Data for Direct ROW27
	W	X	D6	D5	D4	D3	D2	D1	D0	00h	Write PWM Data
PWM data for Direct ROW26	W	0	1	0	0	0	1	0	1	45h	PWM data for Direct ROW26
	W	X	D6	D5	D4	D3	D2	D1	D0	00h	Write PWM Data
PWM Data for Direct ROW25	W	0	1	0	0	0	1	1	0	46h	PWM data for Direct ROW25
	W	X	D6	D5	D4	D3	D2	D1	D0	00h	Write PWM Data
PWM Data for Direct ROW24	W	0	1	0	0	0	1	1	1	47h	PWM data for Direct ROW24
	W	X	D6	D5	D4	D3	D2	D1	D0	00h	Write PWM Data

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Description
Soft Reset	W	1	1	0	0	1	1	0	0	CCh	Soft Reset Function

Note: 1. X: Don't care

2. Def.: Power on reset default

3. It is not recommended to change between Master and Slave mode after a system enable

4. It is not recommended to change direct output set mode after a system enable

5. If programmed command data is not defined the function will not be affected

Software Reset

This command is set to initialise all functions.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Soft Reset	W	1	1	0	0	1	1	0	0	CCh

The internal circuit status after initialisation is as follows.

- All registers are set to their default value but the contents of the DDRAM are not affected
- System Oscillator will be off
- All COM outputs will be high impedance
- All ROW outputs will be high impedance
- The LED display will be in an off state

Binary/Gray Select

The command can be used to set the Binary Mode or the Gray Scale Mode.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Binary/Gray Select	W	0	0	1	1	0	0	0	1	31h
	W	X	X	X	X	X	X	X	BGS	00h

Note: 1. In the Binary Mode the Matrix display masking function is not supported

2. It is not recommended to change between the Binary and Gray Mode after an LED on enable

BGS	Select	Remark
0	Gray	Default
1	Binary	—

Number of COM Outputs

This command can set the scan timing number from COM0 to COM7 and COM output level status. This command parameter is validated during the Timing 1 period of each frame when the command is set.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Number of COM output	W	0	0	1	1	0	0	1	0	32h
	W	CNS	X	X	X	X	CN2	CN1	CN0	07h

Note: 1. It is not recommended to change the scan number set after a system enable

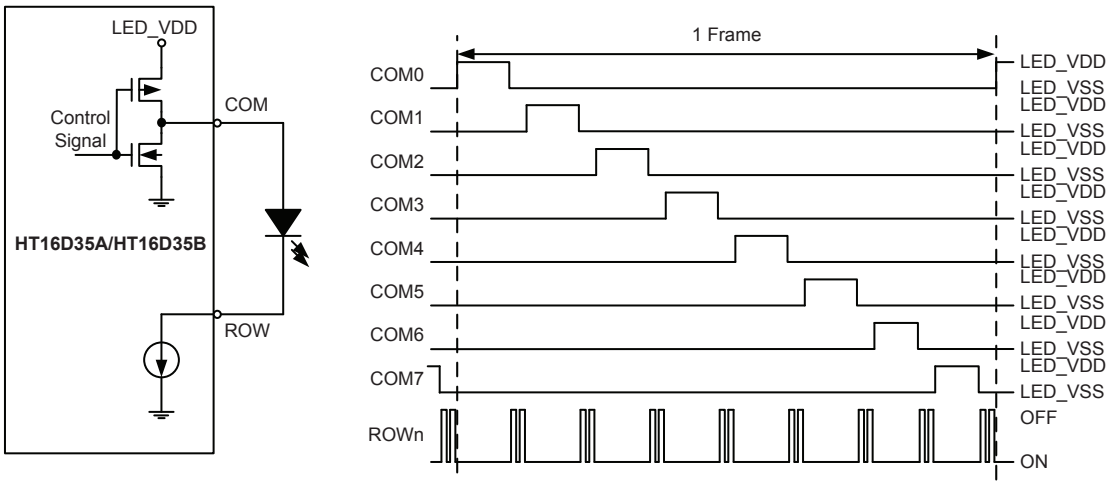
2. For further information see the "LED Driver Output Waveform" section

CNS	COM Scan type	Remarks
0	High scan	Default
1	Low scan	—

CN2	CN1	CN0	COM output number	Remarks
0	0	0	COM0	—
0	0	1	COM0~COM1	—
0	1	0	COM0~COM2	—
0	1	1	COM0~COM3	—
1	0	0	COM0~COM4	—
1	0	1	COM0~COM5	—
1	1	0	COM0~COM6	—
1	1	1	COM0~COM7	Default

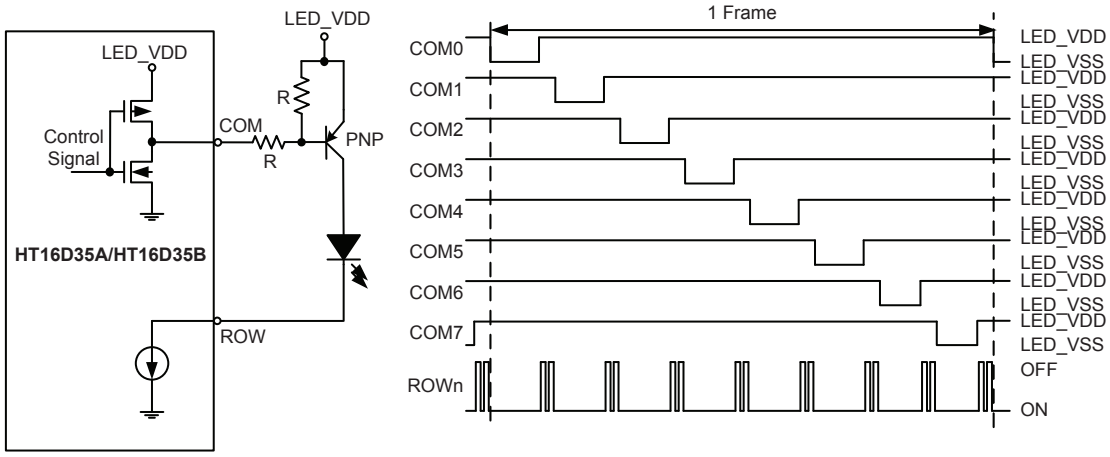
Example1: The setup condition is as follows.

Command	Setting Value	Note
Number of COM outputs (32h)	07h	COM0~COM7, High Scan



Example2: The setup condition is as follows.

Command	Setting Value	Note
Number of COM outputs (32h)	87h	COM0~COM7, Low Scan



Global Blinking

The device contains a versatile blinking function. The whole display can be made to blink or fade times selected by the global blinking/fade time command, this command parameter is validated by each Timing 1 of frame when the command is set.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Global blinking function	W	0	0	1	1	0	0	1	1	33h
	W	BSS	X	X	X	X	X	BS1	BS0	80h

Note: 1. Setting time is based on OSC frequency (f_{SYS}=4.92MHz, 1frame=(scan number)×4160×t_{SYS}).

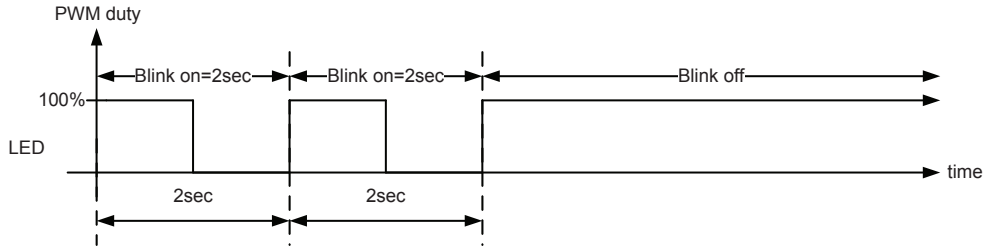
2. The blinking times are integer multiples of the system frequency. The ratios between the system oscillator and the blinking times depend upon the mode, in which the device is operating.

BSS	Select	Remark
0	Blink mode	—
1	Fade mode	Default

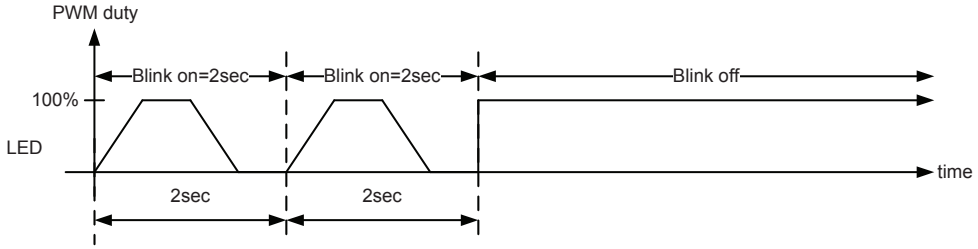
BS1	BS0	Blinking Time	Set Scan Number (duty) v.s. Blinking Time								Remarks
			1/1	1/2	1/3	1/4	1/5	1/6	1/7	1/8	
0	0	OFF	—	—	—	—	—	—	—	—	Default
0	1	≈1sec	1024 Frames	512 Frames	512 Frames	256 Frames	256 Frames	256 Frames	128 Frames	128 Frames	—
1	0	≈2sec	2048 Frames	1024 Frames	1024 Frames	512 Frames	512 Frames	512 Frames	256 Frames	256 Frames	—
1	0	≈4sec	4096 Frames	2048 Frames	2048 Frames	1024 Frames	1024 Frames	1024 Frames	512 Frames	512 Frames	—

Example:

1. Blink output type – blinking time=2sec



2. Fade output type – blinking time=2sec



Cascade Mode

This command will select master/slave mode and input clock source.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Cascade mode	W	0	0	1	1	0	1	0	0	34h
	W	X	X	X	X	X	MS2	MS1	MS0	00h

MS2	MS1	MS0	Clock Source	OSC pin Status	SYNC pin Status	Remark
0	0	0	IRC	Output Hi-Z	Output high	1. Default 2. Only single chip application
0	0	1		Active	Active	—
0	1	0	ERC	Input	Output high	Only single chip application
0	1	1		Input	Active	—
1	X	X		Input	Input	—

Note: It is not recommended to change between MASTER and SLAVE Mode after a system oscillator enable.

System Control

This command controls the system oscillator on/off and display on/off.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
System Control	W	0	0	1	1	0	1	0	1	35h
	W	X	X	X	X	X	X	FON	DON	00h

FON	DON	System oscillator	LED Display	Remark
0	X	OFF	OFF	1. Default 2. Standby mode 3. Temperature protection disable
1	0	ON	OFF	1. When a display off command is executed and the COM output scan high level command is setup: → The outputs of all COMs are at a low level 2. When the display off command is executed and the COM output scan low level command is setup: → The outputs of all COMs are at a high level
1	1	ON	ON	Normal display mode – COM scans active

Constant Current Ratio

This command is used to select the constant current ratio according to the LED panel characteristics.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Constant Current Ratio	W	0	0	1	1	0	1	1	0	36h
	W	X	X	X	X	0	CC2	CC1	CC0	00h

CC2	CC1	CC0	Constant Current Ratio	Remarks
0	0	0	I_{ROW_MAX}	Default
0	0	1	$15/16 \times I_{ROW\_MAX}$	—
0	1	0	$14/16 \times I_{ROW\_MAX}$	—
0	1	1	$13/16 \times I_{ROW\_MAX}$	—
1	0	0	$12/16 \times I_{ROW\_MAX}$	—
1	0	1	$11/16 \times I_{ROW\_MAX}$	—
1	1	0	$10/16 \times I_{ROW\_MAX}$	—
1	1	1	$9/16 \times I_{ROW\_MAX}$	—

Example: If I_{ROW_MAX}=32mA (R_EXT=470Ω) the I_{ROW} constant current setup values are shown as follows:

CC2	CC1	CC0	I_{ROW} Constant Current
0	0	0	32mA
0	0	1	30mA
0	1	0	28mA
0	1	1	26mA
1	0	0	24mA
1	0	1	22mA
1	1	0	20mA
1	1	1	18mA

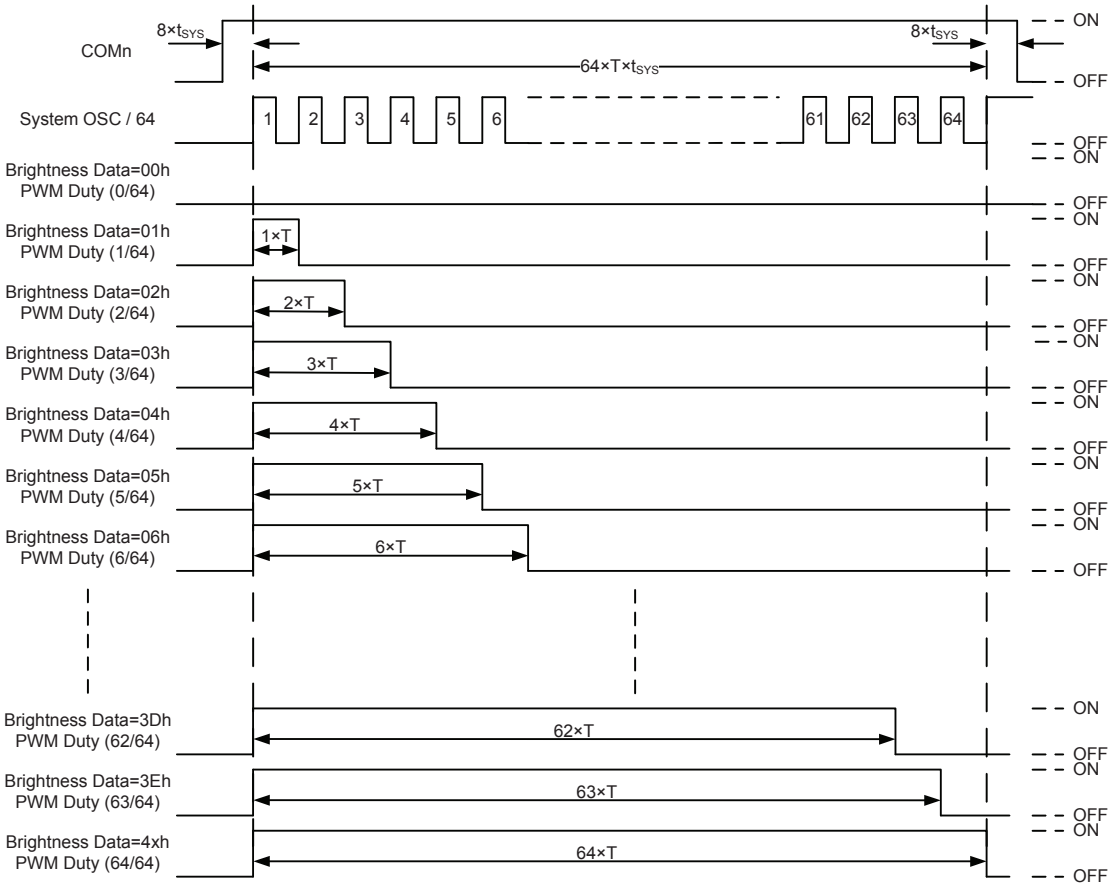
Global Brightness

This command controls the 64-step PWM luminance control. It has a common setting for all dots. This command parameter is validated during the Timing 1 period of each frame when the command is set.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Global Brightness	W	0	0	1	1	0	1	1	1	37h
	W	X	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00h

BC6	BC5	BC4	BC3	BC2	BC1	BC0	PWM duty	Remark
0	0	0	0	0	0	0	0/64	Default
0	0	0	0	0	0	1	1/64	—
0	0	0	0	0	1	0	2/64	—
				⋮			⋮	⋮
0	0	1	0	0	0	0	16/64	—
0	0	1	0	0	0	1	17/64	—
0	0	1	0	0	1	0	18/64	—
				⋮			⋮	⋮
0	1	0	0	0	0	0	32/64	—
0	1	0	0	0	0	1	33/64	—
0	1	0	0	0	1	0	34/64	—
				⋮			⋮	⋮
0	1	1	1	1	0	1	6164	—
0	1	1	1	1	1	0	62/64	—
0	1	1	1	1	1	1	63/64	—
1	X	X	X	X	X	X	64/64	—

The relationship between the PWM data width and brightness digital dimming duty times is shown in the accompanying diagram.



Note: 1. $T=64\times t_{SYS}$

2. $t_{SYS}=1/f_{SYS}$

Mode Control

This command is to control the fade function stop/start, group blinking/fade function stop/start, UCOM/USEG function on/off and thermal shutdown circuit on/off. This command parameter is validated during the Timing 1 period of each frame when the command is set.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Mode control	W	0	0	1	1	1	0	0	0	38h
	W	TSDEN	TSDSL	X	USEN	MKEN	UCEN	BKEN	FDEN	00h

Note: 1. If the TSDSL bit is "1", the Temperature protection function will force the device to enter the Auto Control Mode:

- When the chip junction temperatures exceeds 150°C, the entire IC display will be off and all the direct Brightness PWM SW will be turned off.
- When the chip junction temperatures drops below 125°C, the device will resume operation with a normal display.

2. If the TSDSL bit is "0", the Temperature protection function allows the device to remain in the User Control Mode:

- The TSD flag determines if the IC display is off and if the direct Brightness PWM SW (43h) are turned off or operate normally with a normal display.
- When the chip junction temperatures exceeds 150°C the TSD flag bit is set to "1".
- When the chip junction temperatures drops below 125°C the TSD flag bit is cleared to "0".

TSDEN	TSDSL	Temperature Protection SW	Control Mode	Remarks
0	X	OFF	—	Default
1	0	ON	User	Read the TSD flag for the display on/off control and turn off all direct Brightness PWM SW
1	1	ON	Auto	Auto control mode

USEN	USEG Function SW	Remarks
0	OFF	Default
1	ON	In the Scrolling Mode this function is invalid

MKEN	Matrix Display Masking Function SW	Remarks
0	OFF	Default
1	ON	In the Binary Mode this function is invalid

UCEN	UCOM Function SW	Remarks
0	OFF	Default
1	ON	In the Scrolling Mode this function is invalid

BKEN	Group Blinking Function SW	Remarks
0	OFF	Default
1	ON	—

FDEN	FADE FUNCTION SW	Remarks
0	OFF	Default
1	ON	In the Binary Mode this function is invalid

Scrolling Control

This command is used to control the scrolling on/off enable and scrolling type.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Scrolling Control	W	0	0	1	0	0	0	0	0	20h
	W	SCEN	X	VEN	HEN	X	X	UD	RL	00h

Note: 1. Single row horizontal scrolling.

2. Single row vertical scrolling.

3. When the scrolling mode is enabled, SCEN bit="1", the UCOM and USEG functions are invalid.

4. It is not recommended to execute the fade command and cascade mode.

SCEN	Scrolling Function SW	Remark
0	OFF	Default
1	ON	—

VEN	HEN	Vertical Scrolling SW	Horizontal Scrolling SW	Remark
0	0	OFF	OFF	Default
0	1	OFF	ON	—
1	0	ON	OFF	—
1	1	ON	ON	—

UD	RL	Scrolling Direction				Remark
		Up	Down	Right	Left	
0	0	O	—	O	—	Default
0	1	O	—	—	O	—
1	0	—	O	O	—	—
1	1	—	O	—	O	—

Scrolling Speed

This command is used to setup the scrolling speed.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Scrolling Speed	W	0	0	1	0	0	0	0	1	21h
	W	VSP3	VSP2	VSP1	VSP0	HSP3	HSP2	HSP1	HSP0	00h

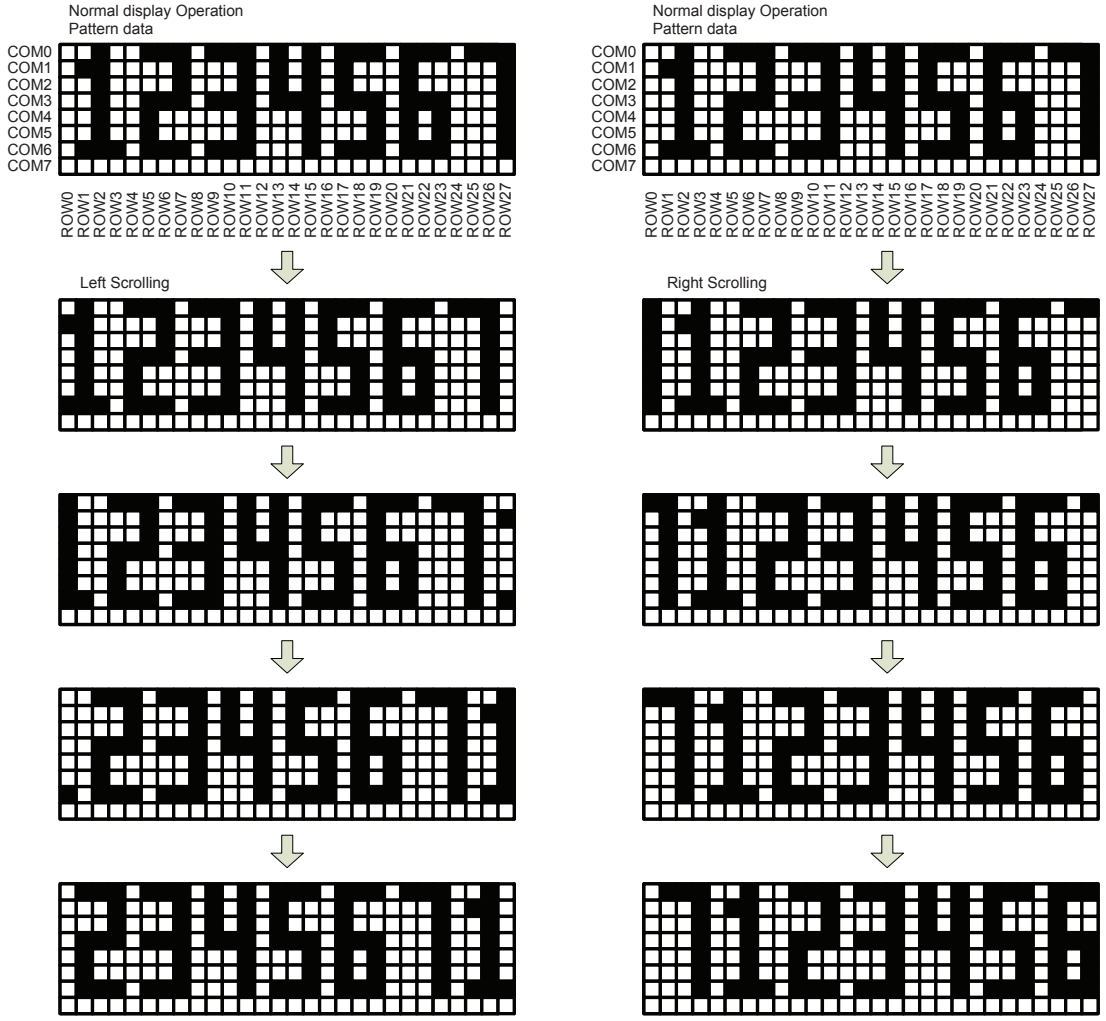
VSP3	VSP2	VSP1	VSP0	Vertical Scroll Speed	Remark
0	0	0	0	16 Frames	Default
0	0	0	1	32 Frames	—
0	0	1	0	48 Frames	—
0	0	1	1	64 Frames	—
0	1	0	0	80 Frames	—
0	1	0	1	96 Frames	—
0	1	1	0	112 Frames	—
0	1	1	1	128 Frames	—
1	0	0	0	144 Frames	—
1	0	0	1	160 Frames	—
1	0	1	0	176 Frames	—
1	0	1	1	192 Frames	—
1	1	0	0	208 Frames	—
1	1	0	1	224 Frames	—
1	1	1	0	240 Frames	—
1	1	1	1	256 Frames	—

Note: The time is based on the OSC frequency. (1frame=(scan number) × 4160 × t_{SYS})

HSP3	HSP2	HSP1	HSP0	Horizontal Scroll Speed	Remark
0	0	0	0	16 Frames	Default
0	0	0	1	32 Frames	—
0	0	1	0	48 Frames	—
0	0	1	1	64 Frames	—
0	1	0	0	80 Frames	—
0	1	0	1	96 Frames	—
0	1	1	0	112 Frames	—
0	1	1	1	128 Frames	—
1	0	0	0	144 Frames	—
1	0	0	1	160 Frames	—
1	0	1	0	176 Frames	—
1	0	1	1	192 Frames	—
1	1	0	0	208 Frames	—
1	1	0	1	224 Frames	—
1	1	1	0	240 Frames	—
1	1	1	1	256 Frames	—

Note: The time is based on the OSC frequency. (1frame=scan number × 4160 × t_{SYS})

Example 1: Left Scrolling and Right Scrolling



Example 2: Up Scrolling and Down Scrolling

COM Pin Control

This command is used to setup the COM pin output on/off status. This command parameter is validated during the Timing 1 period of each frame when the command is set.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
COM pin control	W	0	1	0	0	0	0	0	1	41h
	W	C7	C6	C5	C4	C3	C2	C1	C0	00h

Note: 1. C0~C7="0": COM pin outputs are off.

2. C0~C7="1": COM pin outputs are on.

3. The COM scan function is not affected.

ROW Pin Control

This command consists of four consecutive bytes to set up the ROW pin output on/off status. This command parameter is validated during the Timing 1 period of each frame when the command is set.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
ROW pin control	W	0	1	0	0	0	0	1	0	42h
	W	R27	R26	R25	R24	R23	R22	R21	R20	00h
	W	R19	R18	R17	R16	R15	R14	R13	R12	00h
	W	R11	R10	R9	R8	R7	R6	R5	R4	00h
	W	X	X	X	X	R3	R2	R1	R0	00h

Note: 1. R0~R27="0": ROW pin outputs are off.

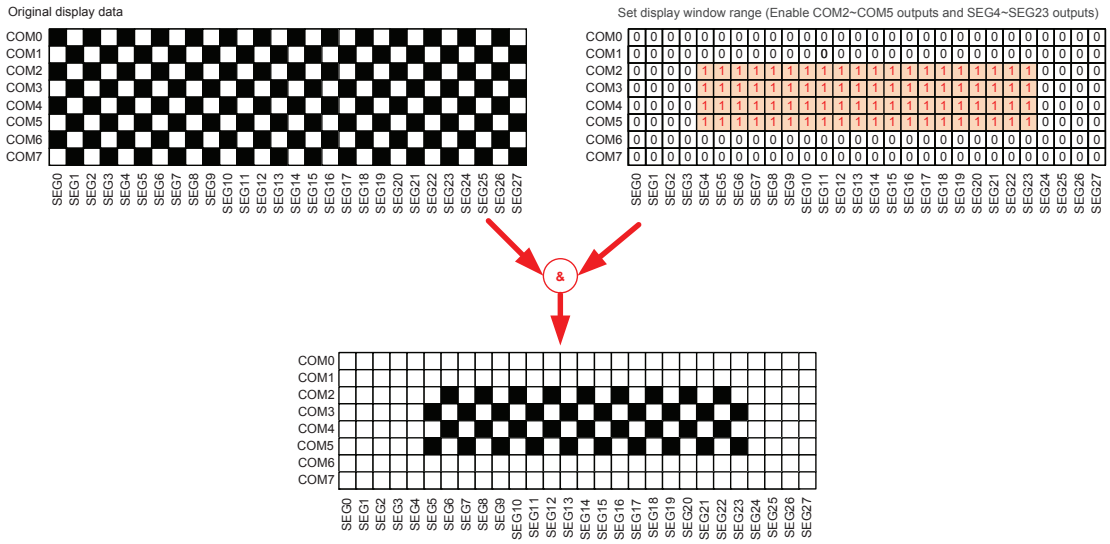
2. R0~R27="1": ROW pin outputs are on.

3. The display RAM contents are not changed.

Example: The setup conditions are shown as follows.

Command	Setup Value	Notes
COM pin control (41h)	00111100b	Display window range (X-axis) set: COM2~COM5
ROW pin control (42h)	00001111b	Display window range (Y-axis) set: ROW4~ROW23
	11111111b	
	11111111b	
	00000000b	

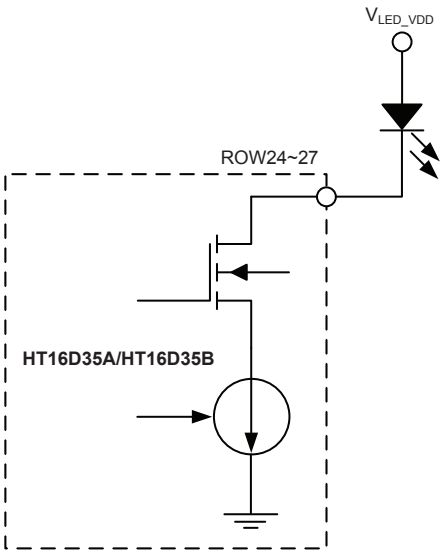
Output	ROW												..... →								
	0	1	2	3	4	5	6	7	8	9	9	10		20	21	22	23	24	25	26	27
COM0																					
COM1																					
COM2					Display window																
COM3																					
COM4																					
COM5																					
COM6																					
COM7																					



Direct Pin Control

This command is used to setup the output ROW24~ROW27 pin status. It is can be used to setup a direct pin or a ROW pin. It is a SW on / off function when these pins are set to be direct pins.

The ROW24~ROW27 port has an NMOS output structure. Data is written to the ROW port with the direct output set command, starting from the most significant bit. In user applications, the internal NMOS device is connected to an external LED as follows:



The command format is as follows:

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Direct pin control	W	0	1	0	0	0	0	1	1	43h
	W	PW24	PW25	PW26	PW27	DR24	DR25	DR26	DR27	11h
Direct ROW27 PWM data	W	0	1	0	0	0	1	0	0	44h
	W	X	D6	D5	D4	D3	D2	D1	D0	00h
Direct ROW26 PWM data	W	0	1	0	0	0	1	0	1	45h
	W	X	D6	D5	D4	D3	D2	D1	D0	00h
Direct ROW25 PWM data	W	0	1	0	0	0	1	1	0	46h
	W	X	D6	D5	D4	D3	D2	D1	D0	00h
Direct ROW24 PWM data	W	0	1	0	0	0	1	1	1	47h
	W	X	D6	D5	D4	D3	D2	D1	D0	00h

DR24	DR25	DR26	DR27	ROW Pin Output Type Select				Remarks
				ROW24 Pin	ROW25 Pin	ROW26 Pin	ROW27 Pin	
0	0	0	0	ROW pin	ROW pin	ROW pin	ROW pin	Default
0	0	0	1	ROW pin	ROW pin	ROW pin	Direct pin	—
0	0	1	X	ROW pin	ROW pin	Direct pin	Direct pin	—
0	1	X	X	ROW pin	Direct pin	Direct pin	Direct pin	—
1	X	X	X	Direct pin	Direct pin	Direct pin	Direct pin	—

PW 24	PW 25	PW 26	PW 27	Direct Function SW				Remarks
				ROW24 Pin	ROW25 Pin	ROW26 Pin	ROW27 Pin	
0	0	0	0	OFF	OFF	OFF	OFF	Default
0	0	0	1	OFF	OFF	OFF	ON	—
0	0	1	X	OFF	OFF	ON	ON	—
0	1	X	X	OFF	ON	ON	ON	—
1	X	X	X	ON	ON	ON	ON	—

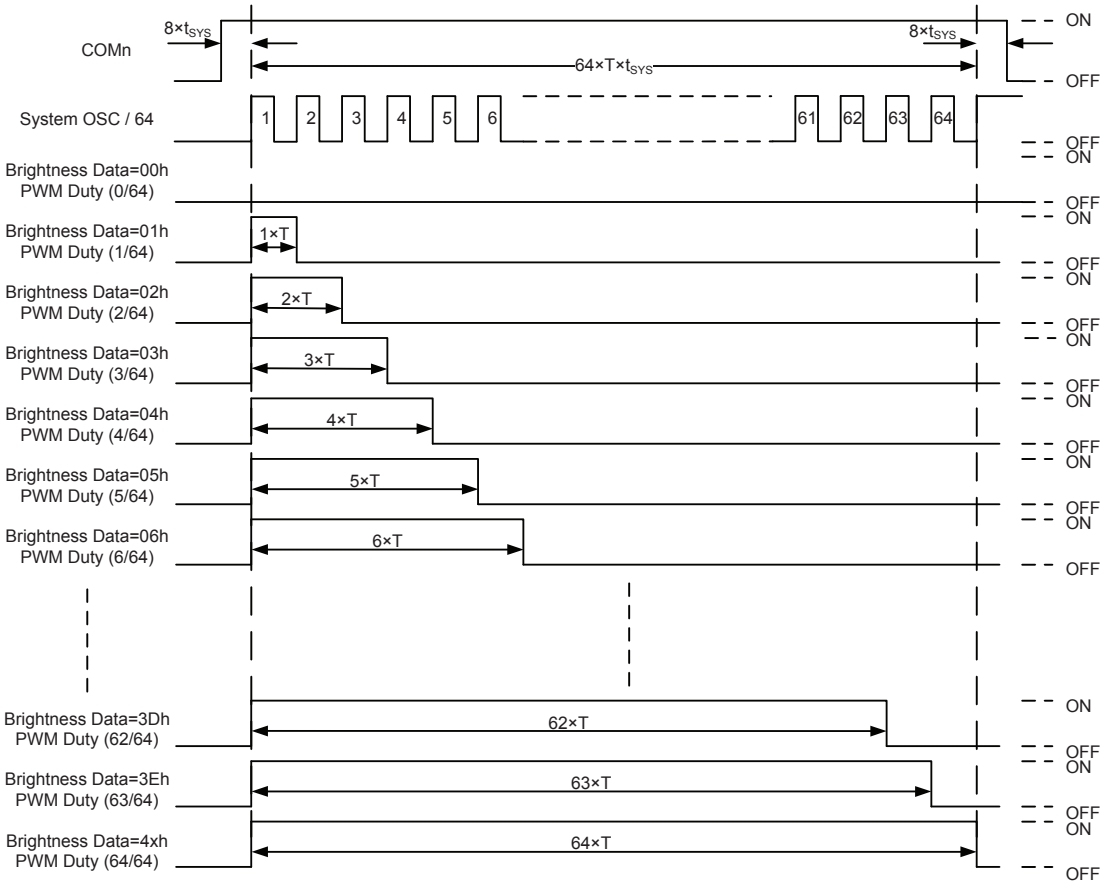
Note: The condition here is when the ROW24~ROW27 pins are set to be direct pins.

PWM data set for each direct row pin

The relationship between the brightness digital dimming duty times and the PWM data of the direct pins is as follows.

D6	D5	D4	D3	D2	D1	D0	Brightness PWM duty	Remarks
0	0	0	0	0	0	0	0/64	Default
0	0	0	0	0	0	1	1/64	
0	0	0	0	0	1	0	2/64	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	0	1	0	0	0	0	16/64	
0	0	1	0	0	0	1	17/64	
0	0	1	0	0	1	0	18/64	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	0	0	0	0	0	32/64	
0	1	0	0	0	0	1	33/64	
0	1	0	0	0	1	0	34/64	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	0	1	6164	
0	1	1	1	1	1	0	62/64	
0	1	1	1	1	1	1	63/64	
1	X	X	X	X	X	X	64/64	

The relationship between the PWM data width and the brightness digital dimming duty times is shown in the accompanying diagram.



Note: 1. $T=64\times t_{SYS}$

2. $t_{SYS}=1/f_{SYS}$

3. When the LED ON bit is set to "1", in the direct output mode setting a ROW number change is prohibited

4. 6-bit PWM data input for each detect ROW

5. Not controlled by a COM scan

6. Not controlled by a scrolling function – Horizontal Scrolling or Vertical Scrolling

7. Not controlled by a Matrix display masking control command

8. Not controlled by a COM/ROW output pin control command

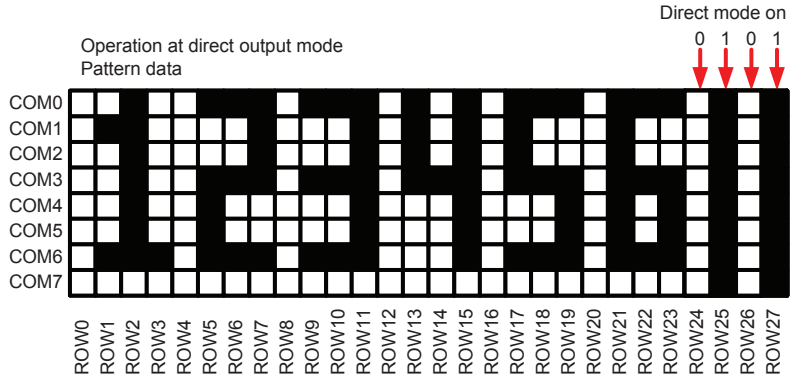
9. Not controlled by a UCOM control command

10. Not controlled by a fade function control command

Example 1: Only the direct output is set

The setup conditions are as follows.

Command	Setup Value	Note
Direct pin control (43H)	FFH	ROW24~ROW27 are set to be direct outputs
PWM data for direct ROW27 (44H)	40h	ROW27 PWM DATA=40H
PWM data for direct ROW26 (45H)	00h	ROW26 PWM DATA=00H
PWM data for direct ROW25 (46H)	40h	ROW25 PWM DATA=40H
PWM data for direct ROW24 (47H)	00h	ROW24 PWM DATA=00H



Example 2: Direct output and scrolling are set together.

- Left Scrolling and Right Scrolling

- Up Scrolling and Down Scrolling

Read Flag

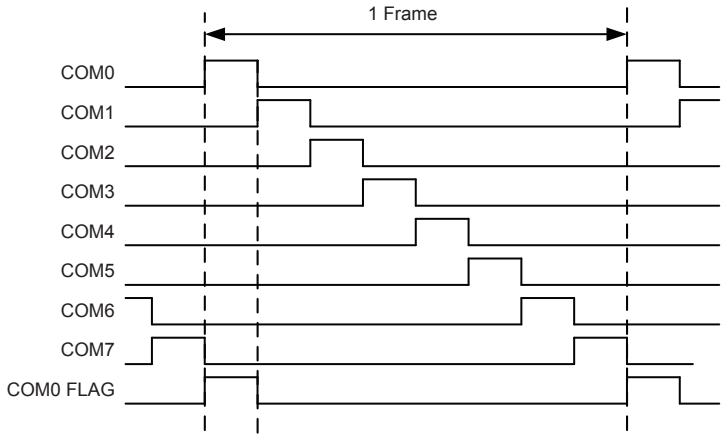
The read register status flag format is shown as follows.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Flag	W	0	1	1	1	0	0	0	1	70h
	R	0	0	0	0	0	0	0	0	00h
	R	X	X	X	X	X	X	COM0 flag	TSD flag	00h

COM0 Flag	COM Scanning Location	Remarks
0	Other COM	—
1	COM0	—

TSD Flag	Chip Junction Temperature	Remarks
0	<125°C	Default When the chip junction temperatures drops below 125°C. The TSD flag bit is cleared to “0”.
1	>150°C	When the chip junction temperatures exceeds 150°C. The TSD flag bit is set to “1”.

The relationship between the COM scanning location and the COM0 flag is shown is as follows.



Read Status

Indicates the device internal status. The read register status format is as follows.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Status	W	0	1	1	1	0	0	0	1	71h
	R	0	0	0	0	0	0	0	0	00h
	R	Read Data								—

Byte	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description	Def.
1st	0	1	1	1	0	0	0	1	Read Status Command	—
2nd	0	0	0	0	0	0	0	0	Read Dummy Data	00h
3rd	X	X	X	X	X	X	X	BGS	Binary/Gray Mode	00h
4th	CNS	X	X	X	X	CN2	CN1	CN0	Scan Output Type	07h
5th	BFS	X	X	X	X	X	BF1	BF0	Blanking Time	80h
6th	X	X	X	X	X	MS2	MS1	MS0	Master or Slave Mode	00h
7th	X	X	X	X	X	X	FON	DON	Controls the system oscillator and display on/off status	00h
8th	X	X	X	X	0	CC2	CC1	CC0	Constant Current Ratio	00h
9th	X	BC6	BC5	BC4	BC3	BC2	BC1	BC0	Luminance – 64 steps	40h
10th	TSDEN	TSDSL	X	USEN	MKEN	UCEN	BKEN	FDEN	Function Mode on/off control	00h
11st	SCEN	X	VCEN	HEN	X	X	UP	RL	Read scrolling status Set Scroll Direction Horizontal Scroll on/off Vertical Scroll on/off	00h
12nd	VSP3	VSP2	VSP1	VSP0	HSP3	HSP2	HSP1	HSP0	Set Scrolling Speed.	00h
13rd	C7	C6	C5	C4	C3	C2	C1	C0	COM0~7 Output on/off Status	00h
14th	R27	R26	R25	R24	R23	R22	R21	R20	ROW27~20 Output on/off Status	00h
15th	R19	R18	R17	R16	R15	R14	R13	R12	ROW19~13 Output on/off Status	00h
16th	R11	R10	R9	R8	R7	R6	R5	R4	ROW12~4 Output on/off Status	00h
17th	X	X	X	X	R3	R2	R1	R0	ROW3~0 Output on/off Status	00h
18th	PW24	PW25	PW26	PW27	DR24	DR25	DR26	DR27	ROW24~ROW27 direct port set and direct Brightness PWM SW on/off control	00h
19th	X	D6	D5	D4	D3	D2	D1	D0	ROW27 PWM Data for Direct output	00h
20th	X	D6	D5	D4	D3	D2	D1	D0	ROW26 PWM Data for Direct Output	00h
21st	X	D6	D5	D4	D3	D2	D1	D0	ROW25 PWM Data for Direct Output	00h
22nd	X	D6	D5	D4	D3	D2	D1	D0	ROW24 PWM Data for Direct Output	00h

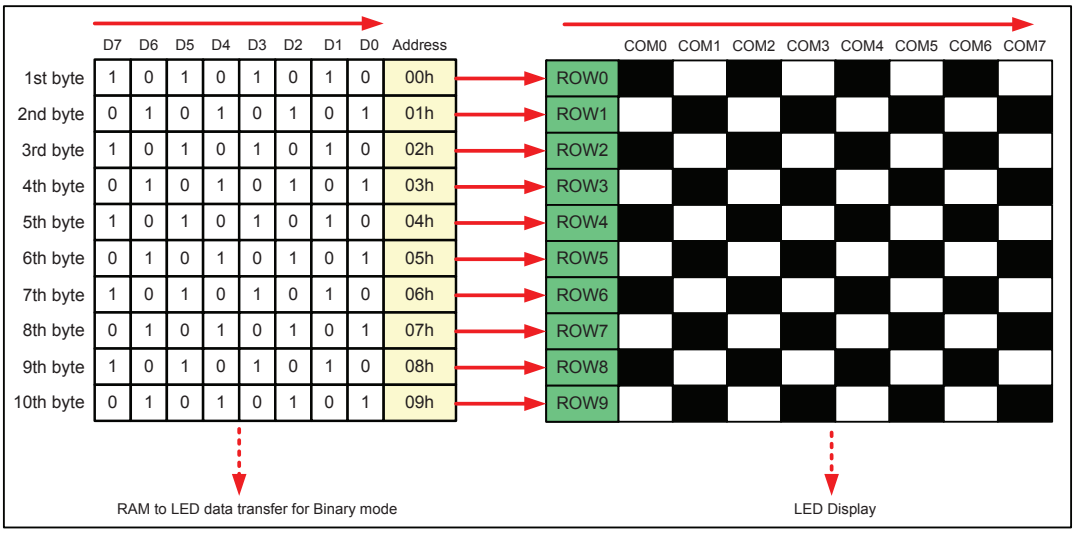
Write Display Data

This command programs the display status of the LED panel. Binary 64-step or Gray Scale Mode is selectable using command control. There is a one-to-one correspondence between the display memory addresses and the ROW outputs, and between the individual bits of a RAM word and the column outputs. The following shows the mapping from the RAM to the LED pattern.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Write Display RAM	W	1	0	0	0	0	0	0	0	80h
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h
	W	D7	D6	D5	D4	D3	D2	D1	D0	—

1. Binary Mode

The setup condition is shown as follows: Write RAM data: SNOW

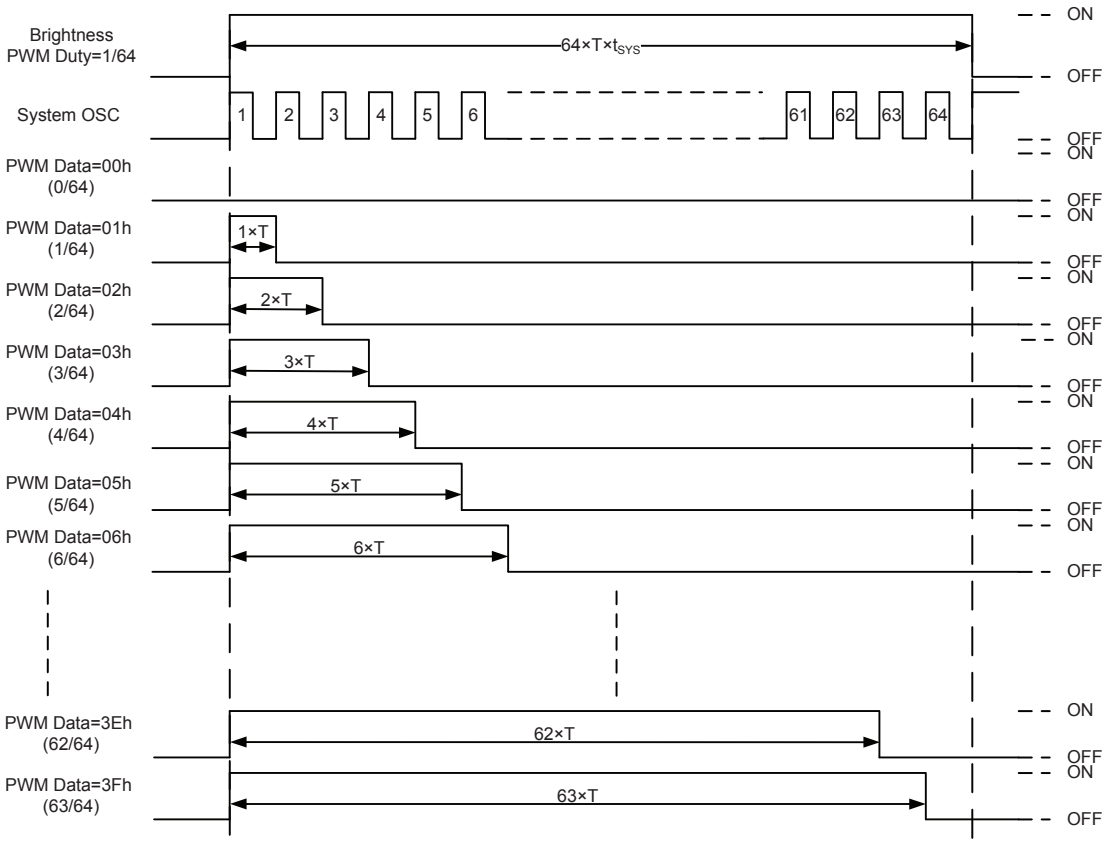


2. Gray Mode

The device provides 6-bit PWM data to control the length of the section. Therefore a max. of 64 gray scales are generated by the 6-bit binary PWM data. The max. of 64 sections can be programmed to suit a satisfactory gray scale in every level. The relationship between PWM data and Gray scale is as follows.

Value	8 bit PWM Data Input								PWM Duty (on width)	Gray Scale	PWM Width
	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0			
0	X	X	0	0	0	0	0	0	0/64		$0\times t_{SYS}$
↓				↓						↓	
10	X	X	0	0	1	0	1	0	10/64		$10\times t_{SYS}$
↓				↓						↓	
20	X	X	0	1	0	1	0	0	20/64		$20\times t_{SYS}$
↓				↓						↓	
30	X	X	0	1	1	1	1	0	30/64		$30\times t_{SYS}$
↓				↓						↓	
40	X	X	1	0	1	0	0	0	40/64		$40\times t_{SYS}$
↓				↓						↓	
50	X	X	1	1	0	0	1	0	50/64		$50\times t_{SYS}$
↓				↓						↓	
63	X	X	1	1	1	1	1	1	63/64		$63\times t_{SYS}$

The relationship between the PWM data and digital PWM duty times is shown in the accompanying diagram.



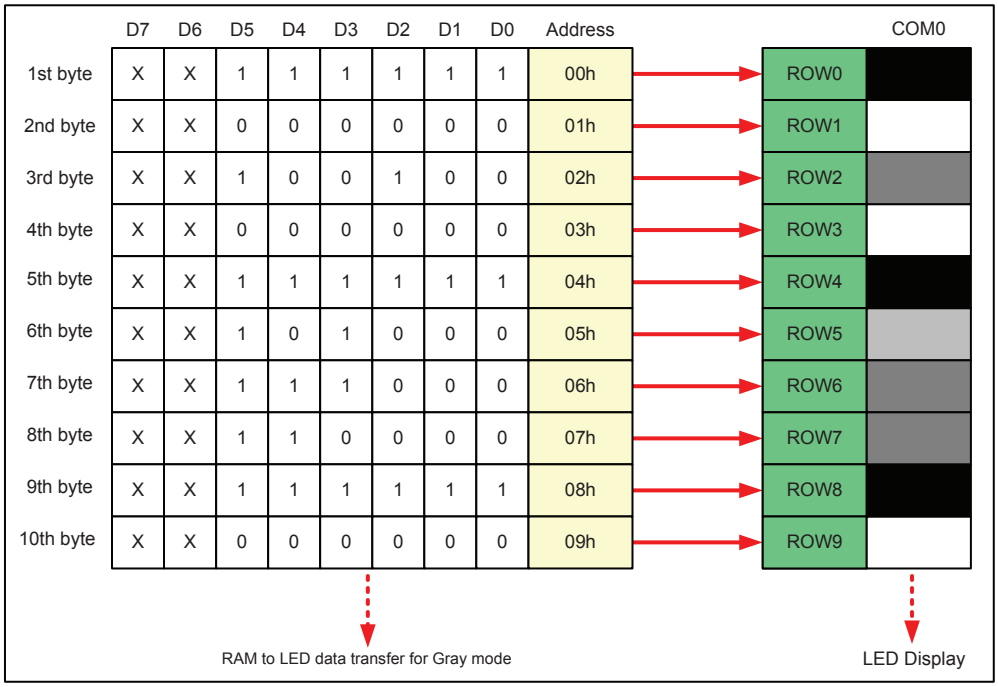
Note: 1. $T=1\times t_{SYS}$

2. $t_{SYS}=1/f_{SYS}$

Example:

The setup condition is shown as follows.

Write RAM data: FFh → 00h → 30h → 00h → FFh → 28h → 30h → 30h → FFh → 00h



Write Fade Data

The device contains a versatile fade function, otherwise known as slope function. The whole display can be made to fade and also blink selected for each dot using the FADE control command. This command parameter is validated using the Timing 1 period of each frame when the command is set. This command is used to control the delay and cycle time for both the fade or blink operations.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Write Fade Data	W	1	0	0	0	0	0	1	0	82h
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h
	W	X	X	FSS	X	SD1	SD0	SC1	SC0	—

Note: The function is suitable for the Gray Mode only.

FSS	Select	Remarks
0	Blink	—
1	Slope	—

The delay time is setup as follows.

SD1	SD0	Delay time	Remarks
0	0	No delay time	Default
0	1	1/4 × slope cycle time	—
1	0	2/4 × slope cycle time	—
1	1	3/4 × slope cycle time	—

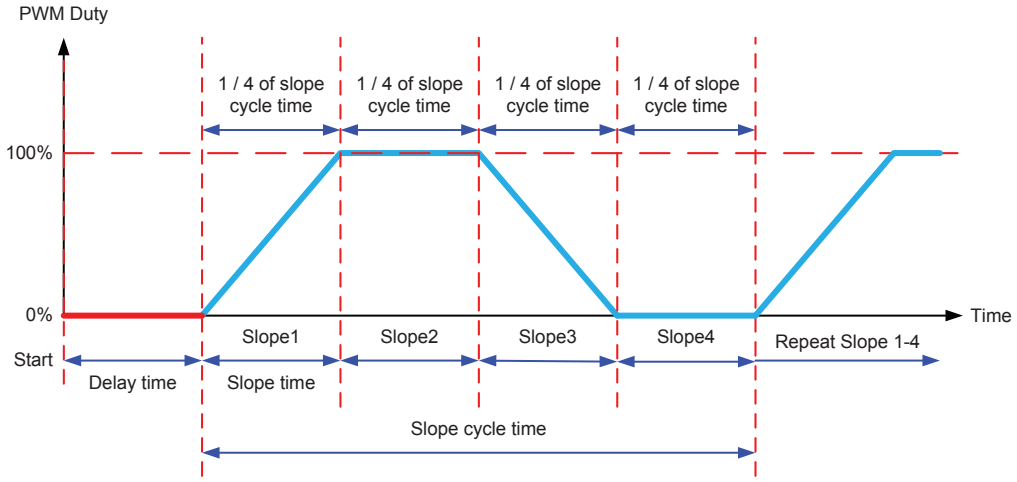
The fade cycle time set is setup as follows.

SC1	SC0	Slope Cycle Time	Set Scan Number (duty)								Remarks
			1/1	1/2	1/3	1/4	1/5	1/6	1/7	1/8	
0	0	off	—	—	—	—	—	—	—	—	Default
0	1	≈1sec	1024 frame	512 frame	512 frame	256 frame	256 frame	256 frame	128 frame	128 frame	—
1	0	≈2sec	2048 frame	1024 frame	1024 frame	512 frame	512 frame	512 frame	256 frame	256 frame	—
1	1	≈4sec	4096 frame	2048 frame	2048 frame	1024 frame	1024 frame	1024 frame	512 frame	512 frame	—

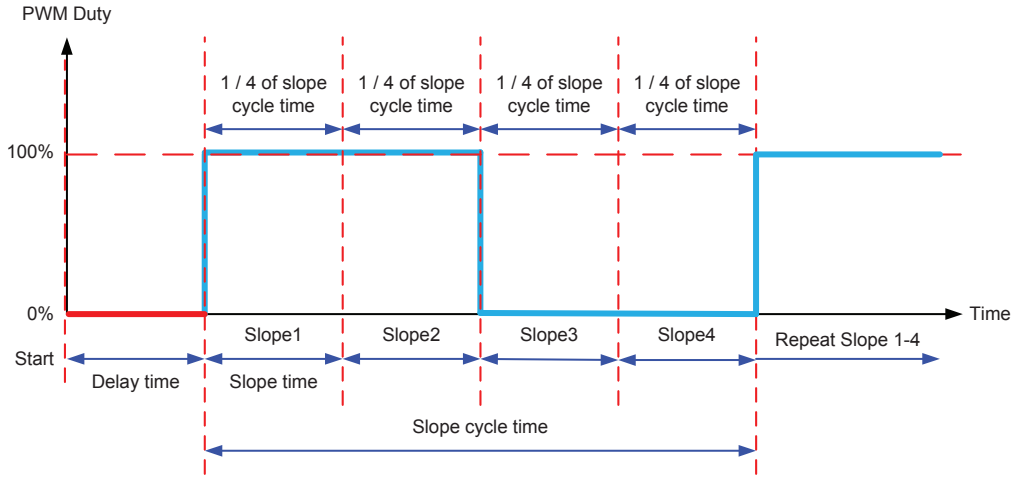
Note: 1. The setup time is based on the OSC frequency (f_{SYS}=4.92MHz, 1frame=(scan number)×4160×t_{SYS}).

2. In the Cascade Mode, it is not recommended to change the delay time function and fade cycle time settings.

The Fade (slope) Mode function waveforms is shown as follows.



The Blink Mode function waveform is shown as follows.



When SLPEN=1 and SCLEN=0, the FADE function operation will be initiated.

After delay time slope1~4 the operation repeats.

Period	Mode	Description
Slope1	Slope	1 step is 1/64 of the global brightness PWM duty – the duty is incremented in 1.587% steps
	Blink	Max. global brightness PWM duty set – 100%
Slope2	Slope	Max. global brightness PWM duty set – 100%
	Blink	Max. global brightness PWM duty set – 100%
Slope3	Slope	1 step is 1/64 of the global brightness PWM duty – the duty is decrement in 1.587% steps
	Blink	Duty is fixed at 0%
Slope4	Slope	Duty is fixed at 0%
	Blink	Duty is fixed at 0%

Example: firefly lighting

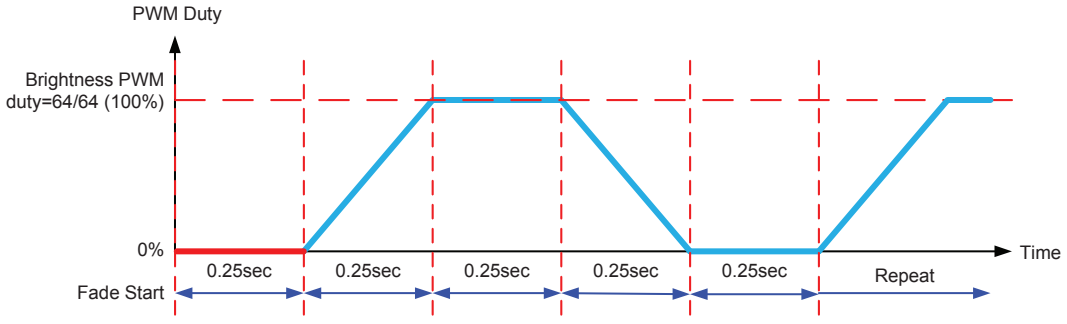
The following command set is an example for LED matrix firefly lighting.

It can control the turn on/off time in detail using the fade setting registers.

The setup condition is shown as follows.

Command	Setup Value	Note
COM pin control (41h)	FFh	Enable COM0~COM7 outputs
ROW pin control (42h)	FFh → FFh → FFh → FFh	Enable ROW0~ROW27 outputs
Binary/Gray select (31h)	00h	Gray Mode
Number of COM output (32h)	07h	COM0~COM7, Scan High type
Global Brightness (37h)	40h	Brightness PWM duty=64/64
Write Display RAM (80h)	00h	Start display RAM Address point=00h
Write PWM data	3Fh (repeat 224 times) for each dot	Write same data to display RAM
System control (34h)	03h	Oscillator on and display on
Write Fade data	00h	Start fade RAM Address point=00h
Write Slope data	25h (repeat 224 times) for each dot	Write same data to set slope time. Delay time=0.25sec, slope cycle time=1sec
Mode control (38h)	01h	Start FADE function – firefly lighting
Mode control (38h)	00h	Stop FADE function – firefly lighting
System control (34h)	00h	Oscillator off and display off – extinguish

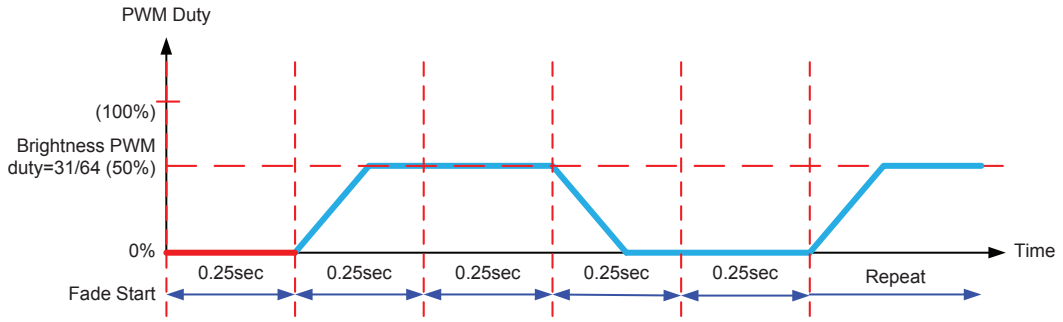
The output waveform of each ROW is shown as follows.



If only the setup condition is changed then see as follows.

Command	Setting Value	Note
Write Display RAM (80h)	00h	Start display RAM Address point=00h
Write display data	1Fh (repeat 216 times)	Write same data to display RAM

The output waveform of each ROW is shown as follows.



Write UCOM Data

The device contains a versatile UCOM control function. This command is used to setup universal data on the COM outputs. The command format is shown as follows.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Write UCOM Data	W	1	0	0	0	0	0	1	0	84h
	W	X	X	X	X	X	A2	A1	A0	00h
	W	Write Universal COM Data								00h

Note: It is not recommended to execute the UCOM command and a scrolling command at the same time.

A2	A1	A0	Duty Time	Remark
0	0	0	T0	—
0	0	1	T1	—
0	1	0	T2	—
0	1	1	T3	—
1	0	0	T4	—
1	0	1	T5	—
1	1	0	T6	—
1	1	1	T7	—

Note: T0~T7 remap to the COM0~COM7 scan sequence before enabling the UCOM functions.

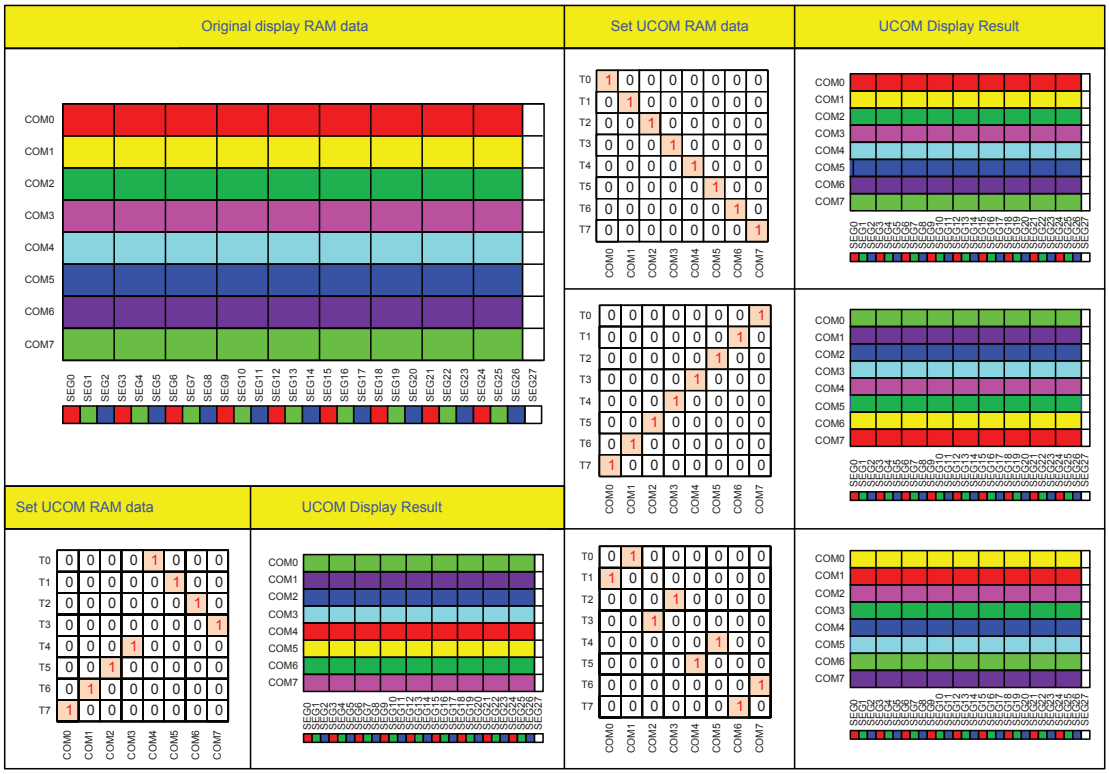
The relationship between the duty time (T0~T7) and the COM output SW on/off control after enabling UCOM function is shown as follows.

Name	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7
T0	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T1	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T2	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T3	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T4	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T5	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T6	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T7	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF
Bits	D7	D6	D5	D4	D3	D2	D1	D0

Example:

1. When the UCOM function is enabled – UCOM display

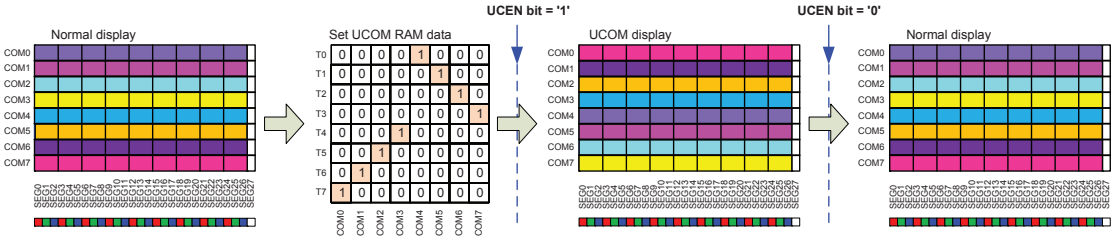
The setup conditions for the UCOM RAM data control and the UCOM enable function is shown as follows.



2. When the UCOM function is disabled – Normal display

The relationship between the duty time (T0~T7) and the COM output SW on/off control is shown as follows.

Duty Time	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7
T0	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
T1	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
T2	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
T3	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
T4	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
T5	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
T6	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
T7	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Bits	D7	D6	D5	D4	D3	D2	D1	D0



Write USEG Data

The device contains a versatile USEG control function. This command is used to set the USEG address and results in directs ROW outputs. The command format is as follows.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Write USEG Data	W	1	0	0	0	0	1	1	0	86h
	W	X	X	X	A4	A3	A2	A1	A0	00h
	W	X	X	X	US4	US3	US2	US1	US1	00h

Note: At the same time it is not recommended to executed USEG command and scrolling command.

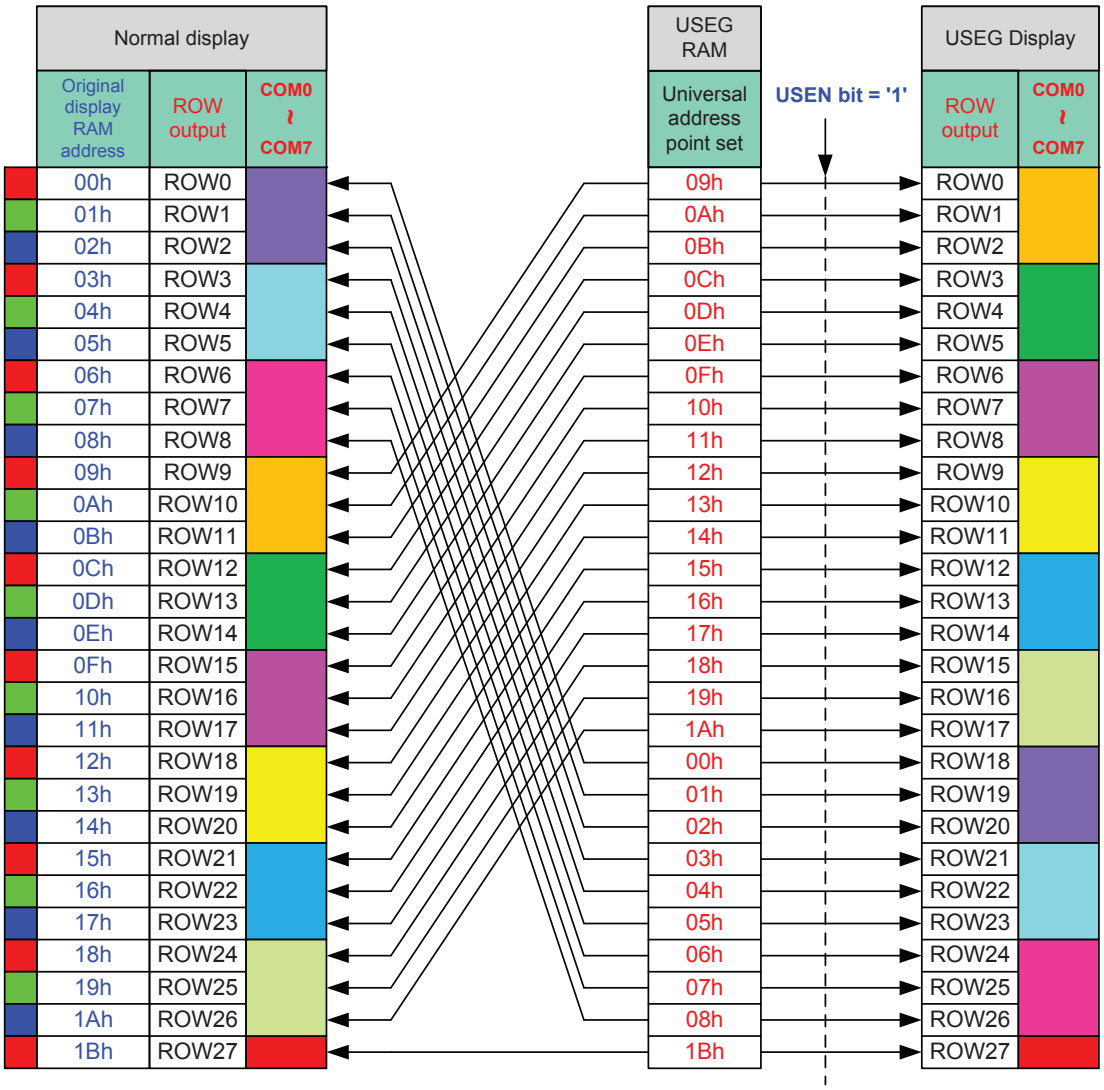
Example:

1. When USEG function is enabled – USEG display

The setup condition for the USEG RAM data control and the Enable USEG function is shown as follows.

The current ROW display is remapped to the new ROW output using the USEG control command.

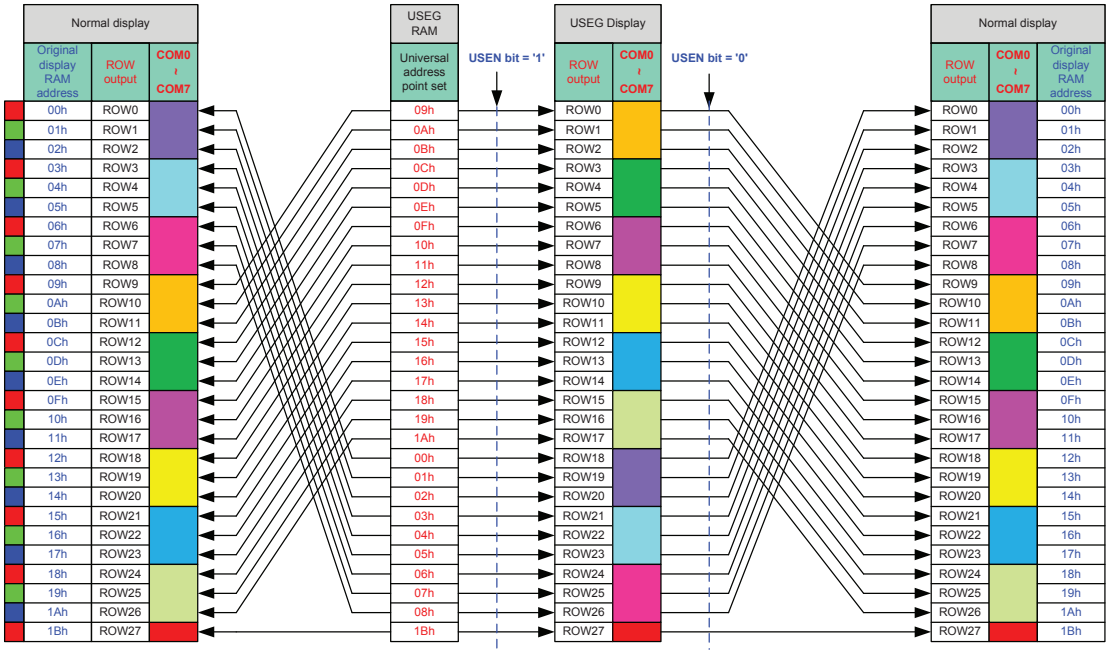
The following diagram shows the relationship between the driving ROW outputs and USEG.



2. When USEG function is disabled – Normal display

The setup condition for the USEG RAM data control and for disabling the USEG function is shown as follows.

The relationship between the driving ROW and the USEG RAM is as follows.



Write Matrix Masking Data

The device contains a versatile Matrix display masking control function. The whole display can be made to display a masking range for each dot by the Matrix display masking command. This command parameter is validated during the Timing 1 period of each frame when the command is set.

This command is used to setup the Matrix display masking address and control the on/off state of the COM and ROW pins. The command format is as follows.

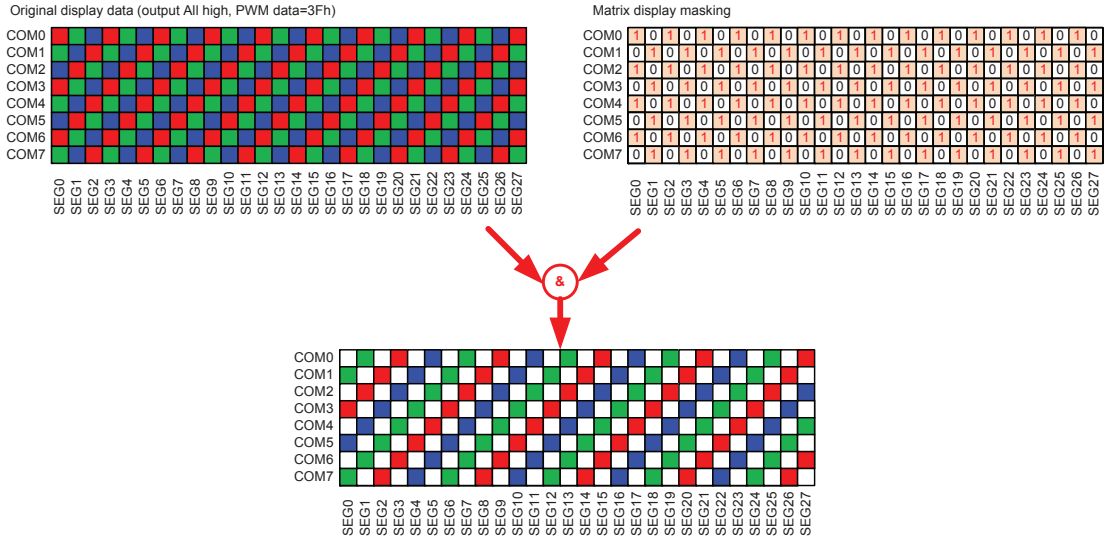
Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Write Matrix Masking Data	W	1	0	0	0	1	0	0	0	88h
	W	0	0	0	A4	A3	A2	A1	A0	00h
	W	Write Matrix Masking Data								00h

Note: The function is suitable for the Gray Mode only.

Example 1:

The setup conditions are as follows.

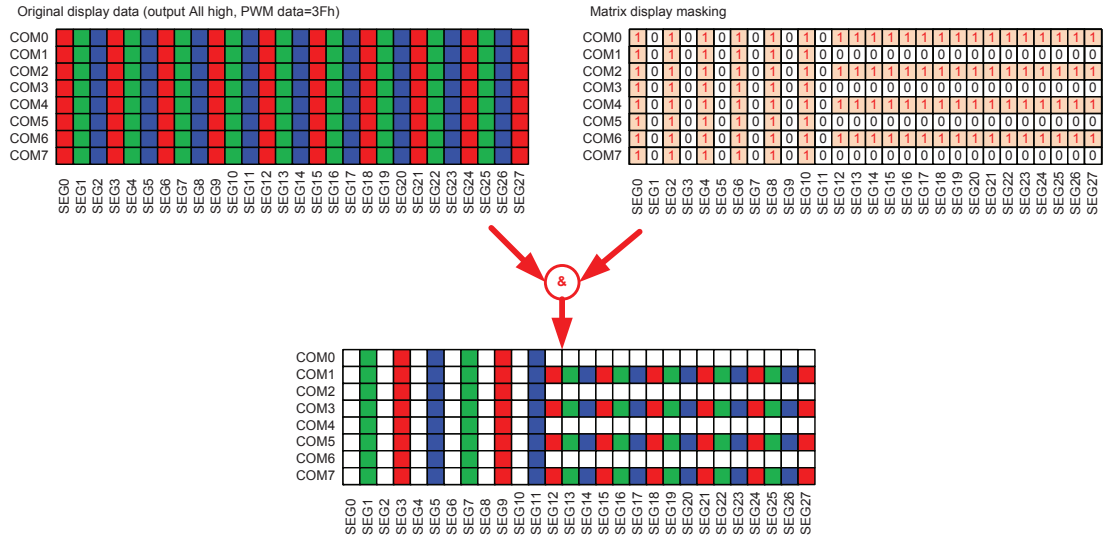
Command	Setting Value	Note
Write Matrix Masking Data (88h)	00h	Start Address point=00h
Write Masking Data	—	AAh→55h→AAh→55h→AAh→55h→AAh→55h→AAh→55h→ AAh→55h→AAh→55h→AAh→55h→AAh→55h→AAh→55h→ AAh→55h→AAh→55h→AAh→55h→AAh→55h



Example 2:

The setup conditions are as follows.

Command	Setting Value	Note
Write Matrix Masking Data (88h)	00h	Start Address point=00h
Write Masking Data	—	FFh→00h→FFh→00h→FFh→00h→FFh→00h→FFh→00h→ FFh→00h→AAh→AAh→AAh→AAh→AAh→AAh→AAh→AAh→ AAh→AAh→AAh→AAh→AAh→AAh→AAh→AAh



SPI 3-wire Serial Interface

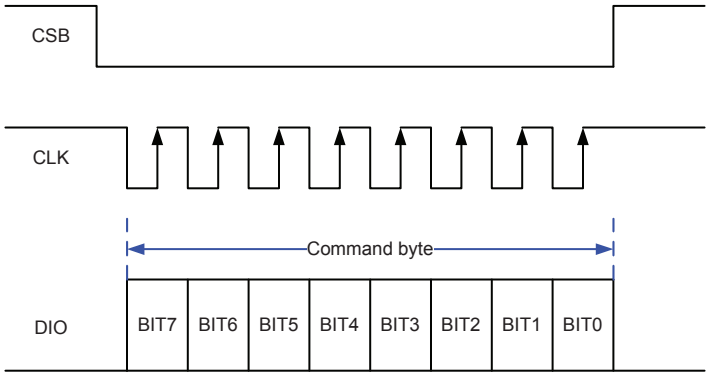
The HT16D35A device includes a SPI 3-wire serial interface.

- The CSB pin is used to identify the transmitted data. The transmission is controlled by the active low signal CSB. After the CSB falls to a low level, the data can start to be transferred.
- The data is transferred from the MSB of each byte – MSB First – the data are shifted into a register at the rising edge of CLK.
- The input data is automatically loaded into a register for every 8-bits of input data. The sequence starts from the falling edge of the CSB signal.
- For the read mode, when CSB is low the DIO pin will change into an output mode after sending a read command code and read the start address setup value. If the MCU sets the CSB signal to a high level after receiving the output data, the DIO pin will be changed into an input mode and the read mode cycle will terminate.
- For the read mode the data will be output on the DIO pin at the falling edge of CLK.

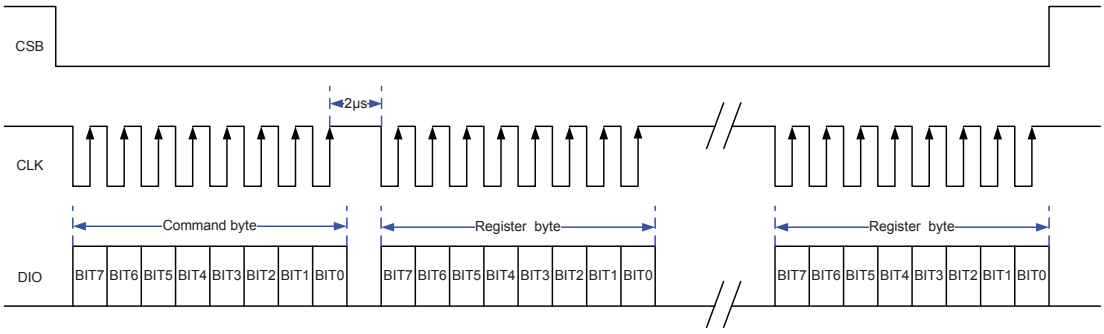
Write Operation

- **Command Byte Transfer**

1. Single Command Byte

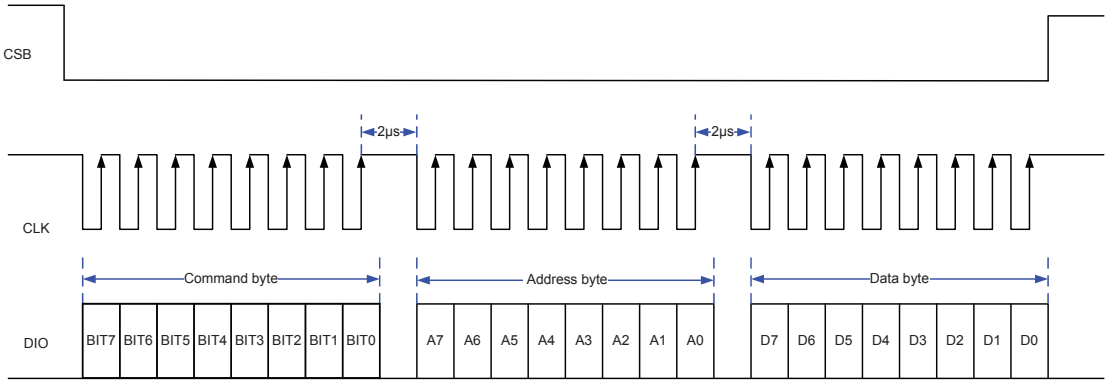


2. Compound Command Byte



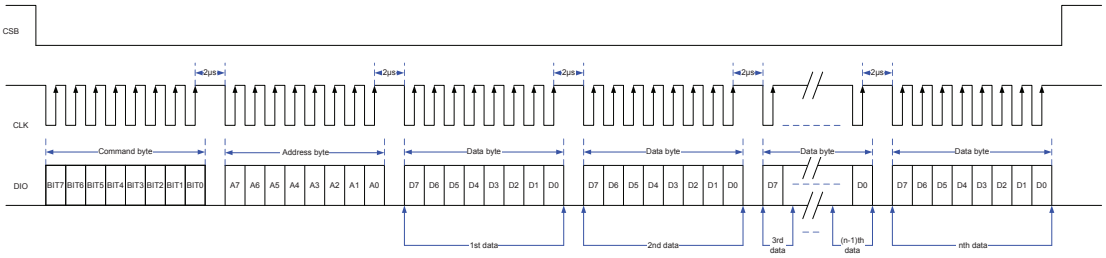
- **Data Byte Transfer**

1. Single Write RAM Data Operation



Note: If the input memory location has a value greater than the limit value the input memory location value will be invalid.

2. Page Write RAM Data Operation



Note: If the memory location exceeds the limit value, the memory pointer will return to 00H. The memory location limit values are shown as follows.

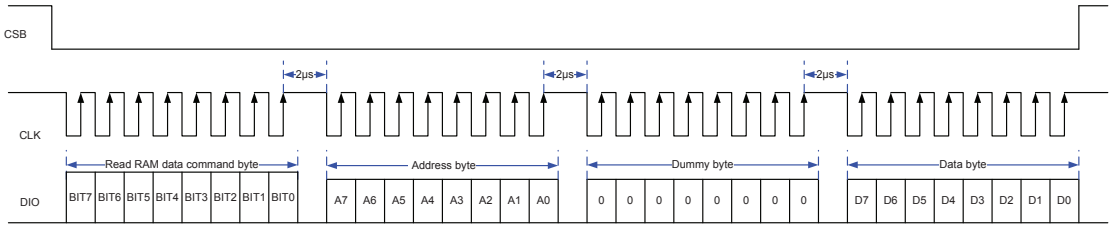
Mode	Duty	Memory Location Limit Value				
		Display Data	Fade Data	UCOM Data	USEG Data	Matrix Display Masking
Binary	1/1~1/8	1Bh	No support function	07h	1Bh	No support function
Gray	1/1	1Bh	1Bh	07h	1Bh	1Bh
	1/2	3Bh	3Bh	07h	1Bh	1Bh
	1/3	5Bh	5Bh	07h	1Bh	1Bh
	1/4	7Bh	7Bh	07h	1Bh	1Bh
	1/5	9Bh	9Bh	07h	1Bh	1Bh
	1/6	BBh	BBh	07h	1Bh	1Bh
	1/7	DBh	DBh	07h	1Bh	1Bh
	1/8	FBh	FBh	07h	1Bh	1Bh

Read Operation

1. The data must be read in byte units.

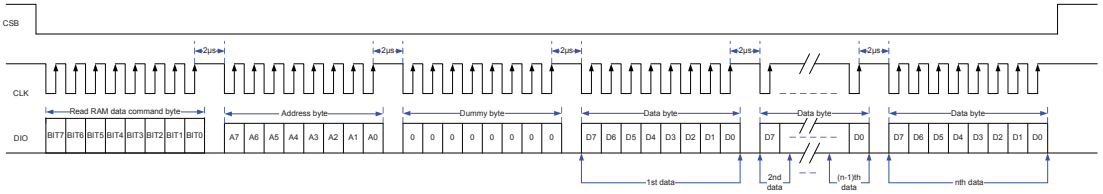
2. It is recommended that the host controller should read in the data from the DIO line between the rising edge of the CLK line and the falling edge of the next CLK line.

- **Single Read RAM Data Operation**



Note: If the input memory location value is greater than the limit value, the input memory location value will be invalid.

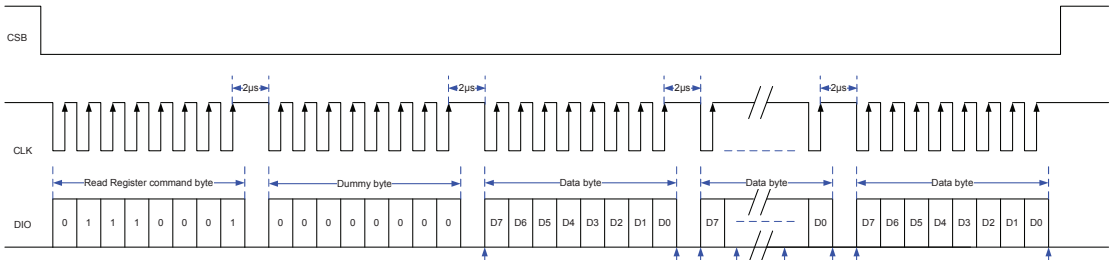
- **Page Read RAM Data Operation**



Note: If the memory location exceeds the limit value, the memory pointer will return to 00H. The memory location limit values are shown below.

Mode	Duty	Memory Location Limit Value				
		Display Data	Fade Data	UCOM Data	USEG Data	Matrix Display Masking
Binary	1/1~1/8	1Bh	No support function	07h	1Bh	No support function
Gray	1/1	1Bh	1Bh	07h	1Bh	1Bh
	1/2	3Bh	3Bh	07h	1Bh	1Bh
	1/3	5Bh	5Bh	07h	1Bh	1Bh
	1/4	7Bh	7Bh	07h	1Bh	1Bh
	1/5	9Bh	9Bh	07h	1Bh	1Bh
	1/6	BBh	BBh	07h	1Bh	1Bh
	1/7	DBh	DBh	07h	1Bh	1Bh
	1/8	FBh	FBh	07h	1Bh	1Bh

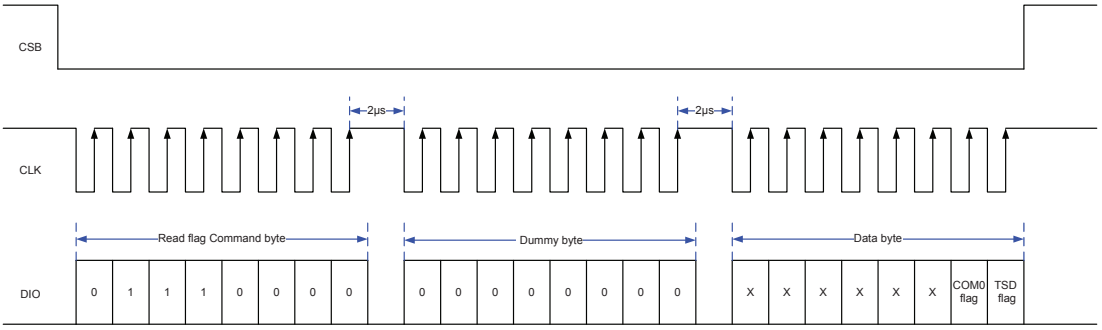
1. Read register status format is as follows



Note: 1. The display data must be read in byte units.

2. If the register location exceeds the limit value, the register pointer will return to the first one. The register location has a limit value of 20.

2. Read flag status format is as follows



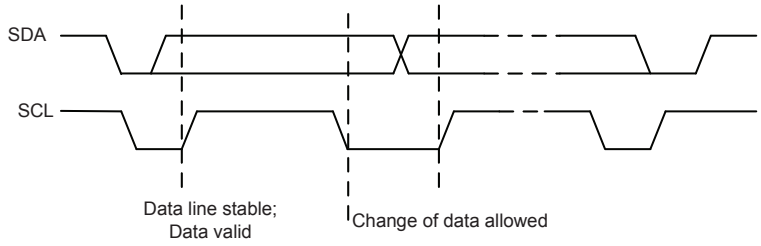
I²C Serial Interface

The HT16D35B device includes an I²C serial interface.

The I²C bus is a bidirectional, two-line communication link between different ICs or modules. The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to a positive supply via a pull-up resistor, typically a value of 10kΩ for a frequency of 100kHz. When the bus is free both lines are high. The output stages of any devices connected to the bus must have open-drain or open-collector types in order to implement a wired or function. Data transfer is initiated only when the bus is not busy.

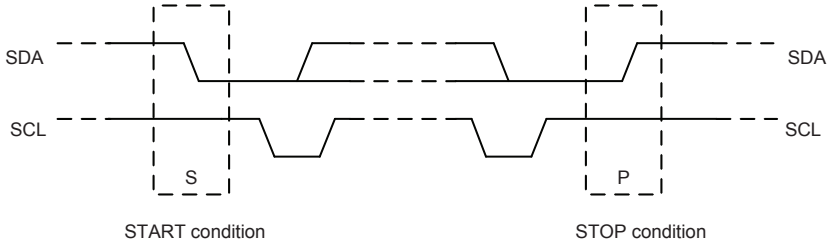
Data Validity

The data on the SDA line must be stable during the clock high period. The high or low state of the data line can only change state when the clock signal on the SCL line is low as shown in the accompanying diagram.



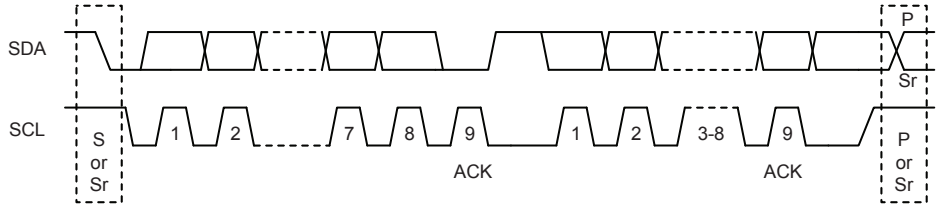
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus remains busy if a repeated START (Sr) is generated instead of a STOP condition. The START(S) and repeated START (Sr) conditions are functionally identical.



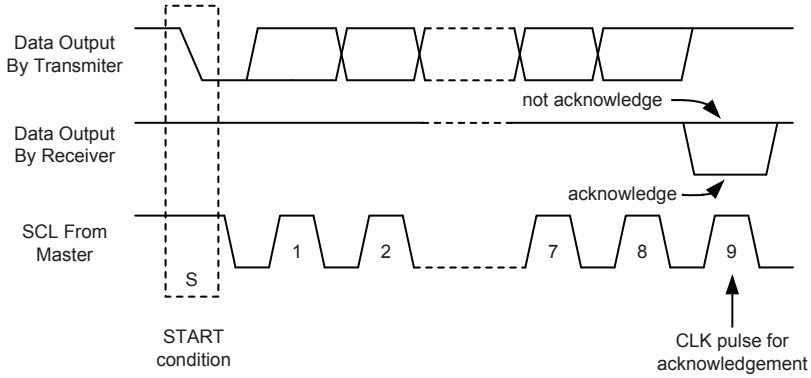
Byte Format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



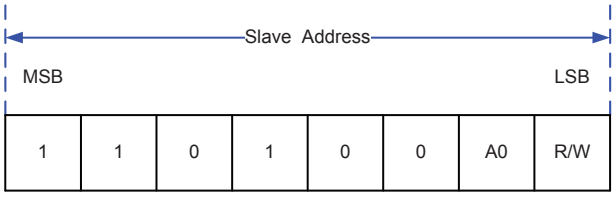
Acknowledge

- Each byte of eight bit length is followed by one acknowledge bit. This acknowledge bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an acknowledge, ACK, after the reception of each byte.
- The device that provides an acknowledge must pull down the SDA line during the acknowledge clock pulse so that it remains at a stable low level during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse so as to not acknowledge. The master will generate a STOP or a repeated START condition.



Slave Addressing

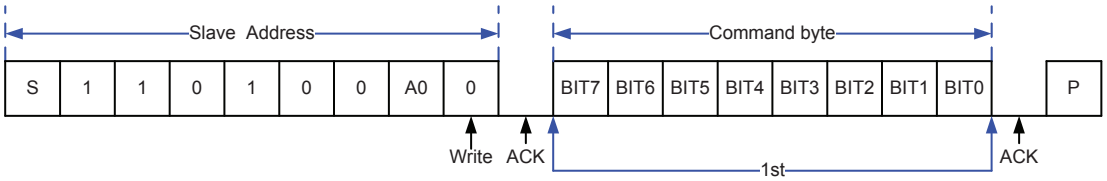
- The device requires an 8-bit slave address word following a start condition to enable the device for a write operation. The device address word consist of a mandatory one, zero sequence for the first four most significant bits. Refer to the diagram showing the slave Address. This is common to all LED devices.
- The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines whether a read or write operation is to be performed. When the R/W bit is “1”, then a read operation is selected. A “0” selects a write operation.
- The address bits are “1, 1, 0, 1, 0, 0, A0”. When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA line.



Write Operation

- **Single Command Byte**

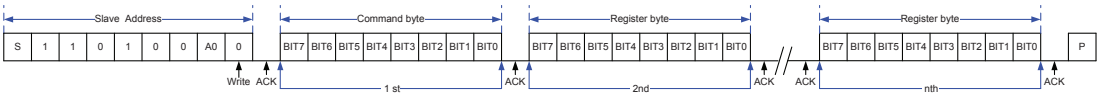
  A byte write operation requires a START condition, a slave address with a R/W bit, a command (1st) and a STOP condition for a single command byte.



Single Command Byte

- **Compound Command Byte**

  A byte write operation requires a START condition, a slave address with a R/W bit, a command (1st), one or more register byte commands (2nd~nth) and a STOP condition for a compound command byte.

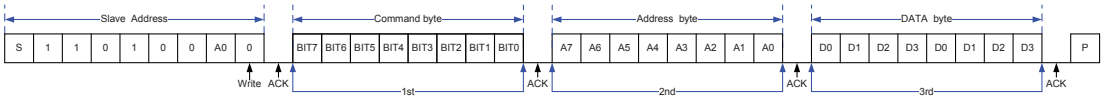


Compound Command Byte

- **Single Write RAM Data Byte Operation**

  If the input memory location value is greater than the limit value, the input memory location value will be invalid.

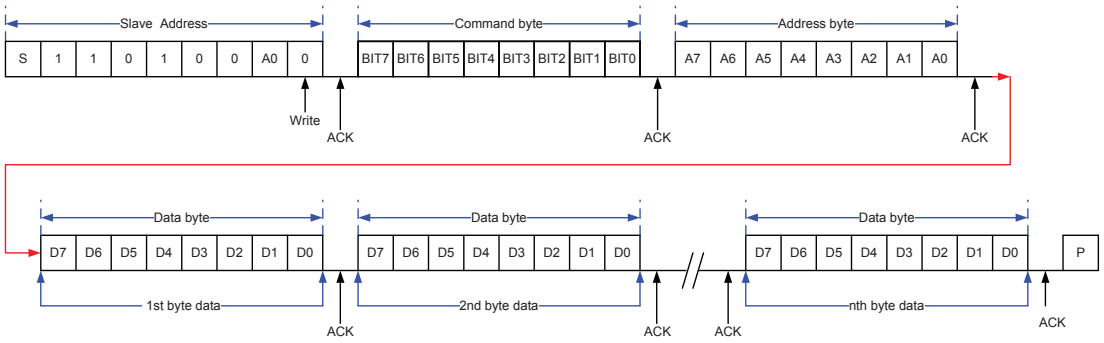
  Following a START condition, the slave address and R/W bit is placed on the bus. Then follows the display data address setup command code (1st). The address pointer (An) is then written to the address pointer (2nd) and then valid data and a STOP condition for a compound write single data byte.



Note: If the input memory location value is greater than the limit value, the input memory location value will be invalid.

- **Page Write RAM Data Operation**

  Following a START condition the slave address along with the R/W bit is placed on the bus along with the display data address setup command code (1st) and the address pointer, An, (2nd). The data to be written to the memory is next, after which the internal address pointer is incremented to the next address location on the reception of an acknowledge clock.



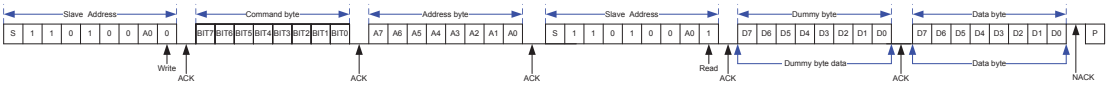
If memory location exceeds limit value, the memory pointer will return to 00H. The limit value of Memory location is shown as below:

Mode	Duty	Memory Location Limit Value				
		Display Data	Fade Data	UCOM Data	USEG Data	Matrix Display Masking
Binary	1/1~1/8	1Bh	No support function	07h	1Bh	No support function
Gray	1/1	1Bh	1Bh	07h	1Bh	1Bh
	1/2	3Bh	3Bh	07h	1Bh	1Bh
	1/3	5Bh	5Bh	07h	1Bh	1Bh
	1/4	7Bh	7Bh	07h	1Bh	1Bh
	1/5	9Bh	9Bh	07h	1Bh	1Bh
	1/6	BBh	BBh	07h	1Bh	1Bh
	1/7	DBh	DBh	07h	1Bh	1Bh
	1/8	FBh	FBh	07h	1Bh	1Bh

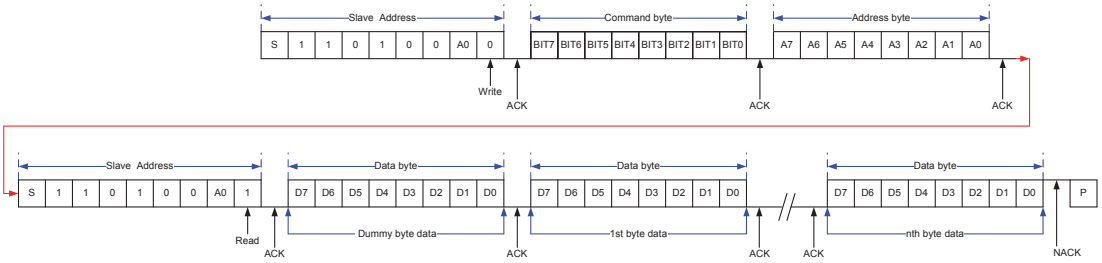
Read Operation

In this mode, the master reads the device data after setting the slave address. Following the R/W bit, which is zero, and the acknowledge bit, then follows the address setting command code (1st). After this is the address pointer (An) which is written to the address pointer (2nd). Following this is the START condition and slave address, followed by a R/W bit which is high. The addressed data is then transmitted. The address pointer is only incremented on reception of an acknowledge clock. The device will place the data at address An+1 onto the bus. The master reads and acknowledges the new byte and the address pointer is incremented to "An+2". If only a read command is sent to the I^2C interface, then dummy data is transmitted. This cycle for reading consecutive addresses will continue until the master sends a NACK and STOP condition.

- **Single Read RAM Data Operation**



- **Page Read RAM Data Operation**



Note: 1. The cycle to read consecutive addresses will continue until the master sends a NACK and STOP condition.

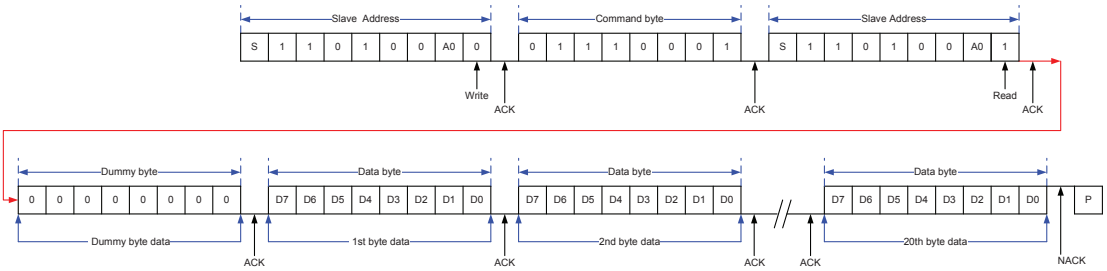
2. If a memory location exceeds the limit value, the memory pointer will return to 00H. The memory location limit values are shown as follows.

Mode	Duty	Memory Location Limit Value				
		Display Data	Fade Data	UCOM Data	USEG Data	Matrix Display Masking
Binary	1/1~1/8	1Bh	No support function	07h	1Bh	No support function
Gray	1/1	1Bh	1Bh	07h	1Bh	1Bh
	1/2	3Bh	3Bh	07h	1Bh	1Bh
	1/3	5Bh	5Bh	07h	1Bh	1Bh
	1/4	7Bh	7Bh	07h	1Bh	1Bh
	1/5	9Bh	9Bh	07h	1Bh	1Bh
	1/6	BBh	BBh	07h	1Bh	1Bh
	1/7	DBh	DBh	07h	1Bh	1Bh
	1/8	FBh	FBh	07h	1Bh	1Bh

Read Register Status

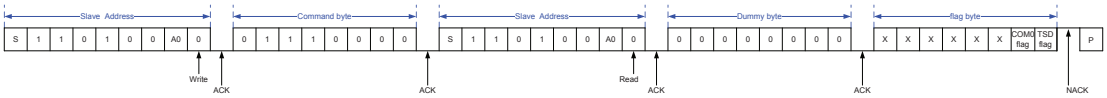
In this mode, the master reads the device data after setting the slave address. Following the R/W bit, which is zero, and the acknowledge bit, then follows the read status setup command code. Next is the START condition and slave address, followed by a R/W bit which is high. The addressed data is then transmitted.

1. Read register status format is as follows



Note: If the register location exceeds the limit value, the register pointer will return to the 1st value. The register location limit value is 20th address. The cycle for reading consecutive addresses will continue until the master sends a NACK and STOP condition.

2. Read flag status format is as follows



Power Supply Sequence

- If the power is individually supplied on the LED_VDD and VDD pins, it is strongly recommended to follow the Holtek power supply sequence requirement.
- If the power supply sequence requirement is not followed, it may result in malfunctions.

Holtek Power Supply Sequence Requirement.

1. Power-on sequence:

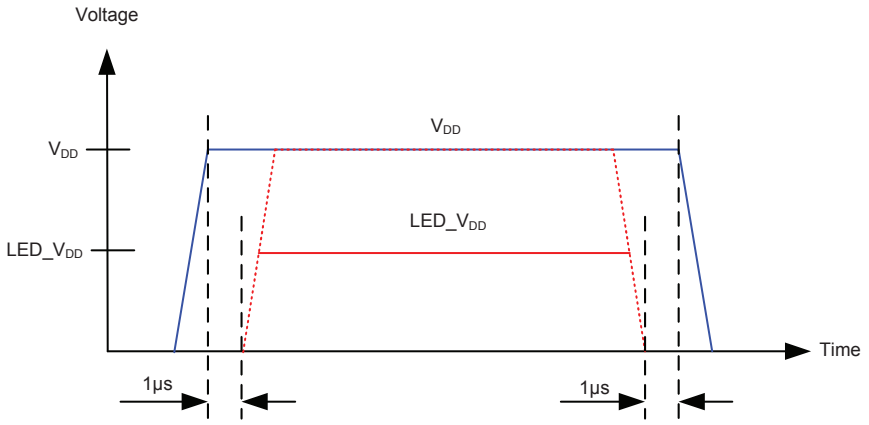
   Turn on the logic power supply V_{DD} first and then turn on the LED driver power supply LED_V_{DD}.

2. Power-off sequence:

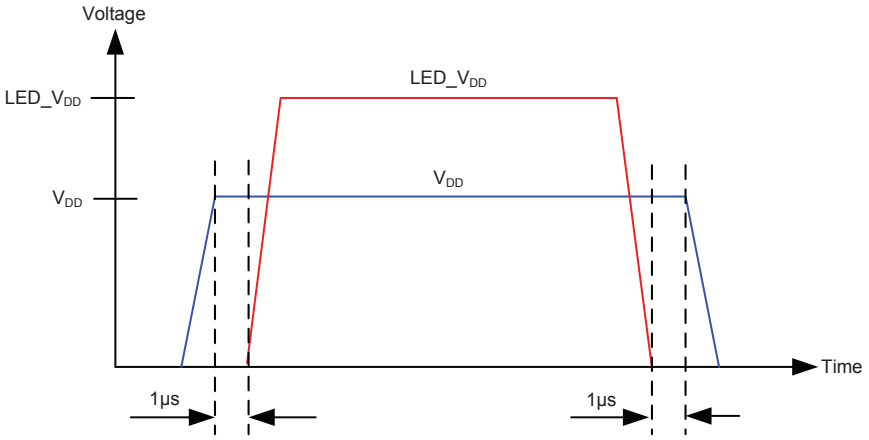
   Turn off the LED driver power supply LED_V_{DD} first and then turn off the logic power supply V_{DD}.

3. The Holtek Power Supply Sequence Requirement must be followed no matter whether the LED_V_{DD} voltage is higher than the V_{DD} voltage or not.

- When the LED_V_{DD} voltage is smaller than or is equal to the V_{DD} voltage application



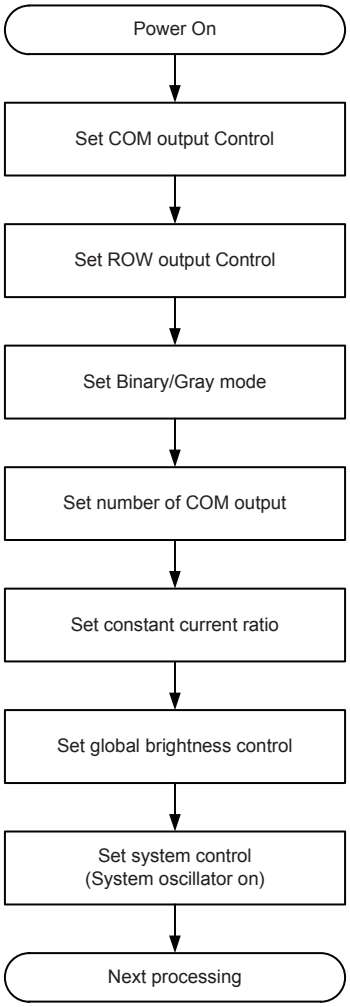
- When the LED_V_{DD} voltage is greater than the V_{DD} voltage application



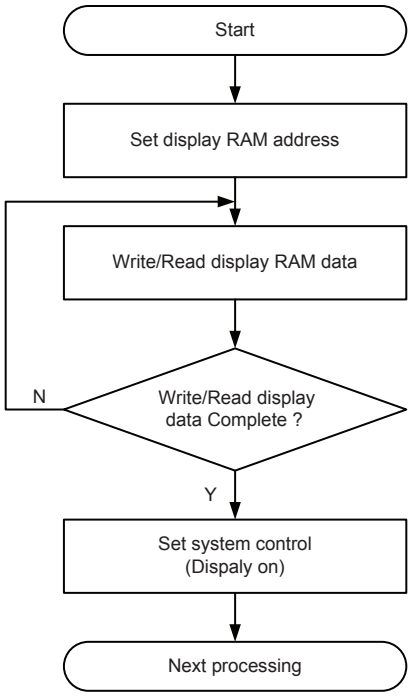
Operation Flow Chart

Access procedures are illustrated below by means of flowcharts.

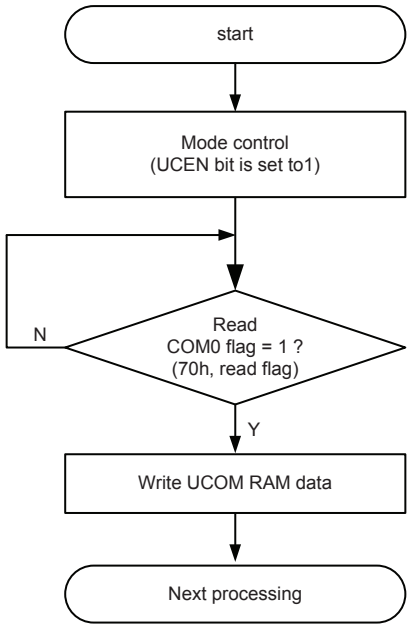
- **Initialisation**



- **Display Data Read/Write – Address Setting**

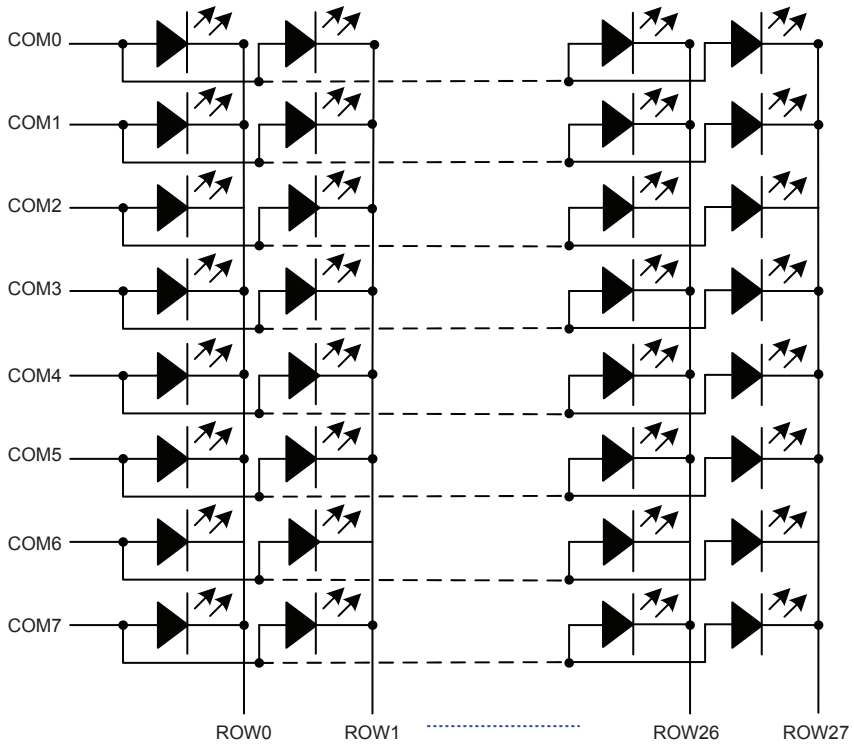


- **UCOM RAM Data Write**



Application Circuits

LED Matrix Circuit

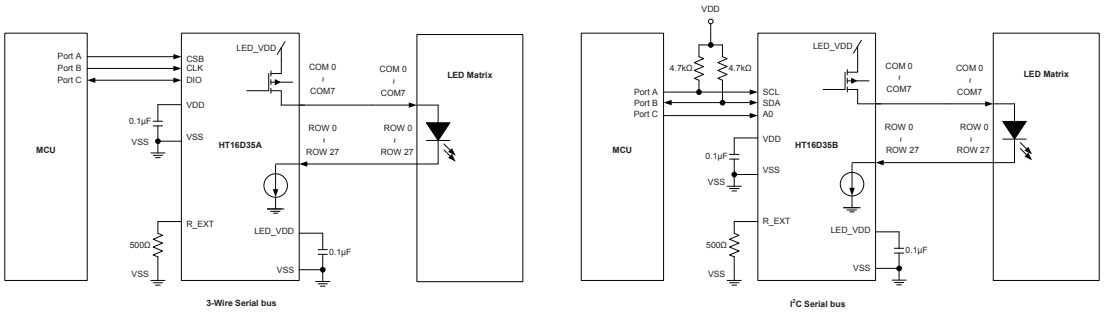


LED Display – 28 ROW × 8 COM

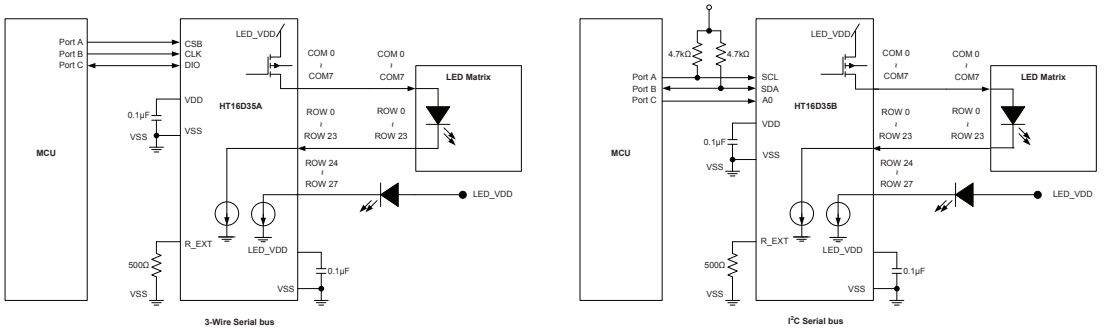
Single LED IC Application

- **28 ROW × 8 COM Example: P-MOS Open Drain Output**

1. Disable direct port function

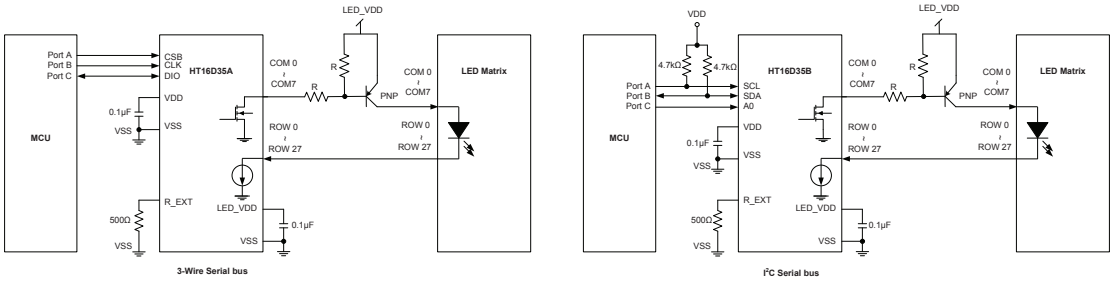


2. Enable direct port function



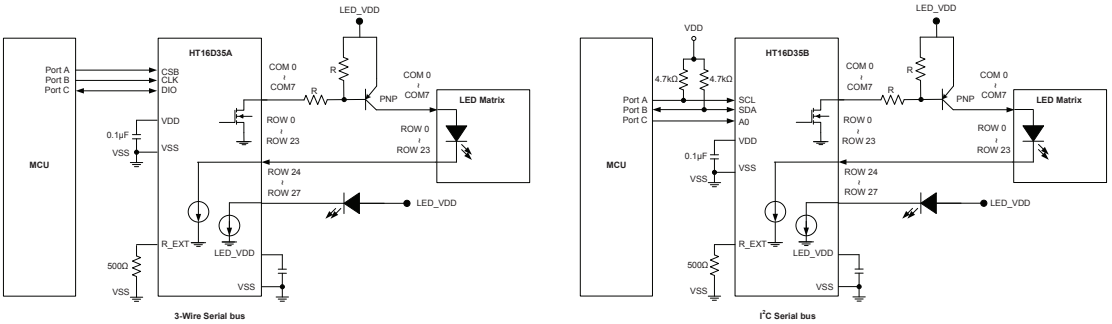
- **28 ROW × 8 COM Example: N-MOS Open Drain Output and COM with Transistor Buffer**

1. Disable direct port function



Note: The R resistor values depend upon the LED power consumption.

2. Enable direct port function

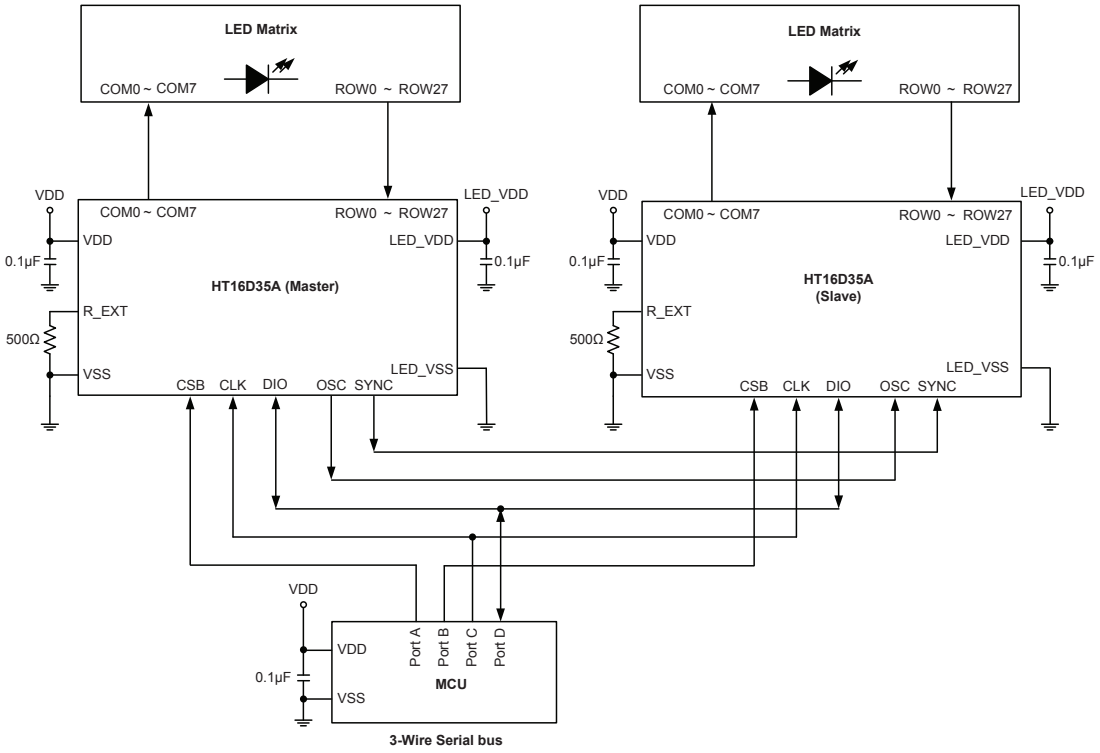


Note: The R resistor values depend upon the LED power consumption.

Cascade Function

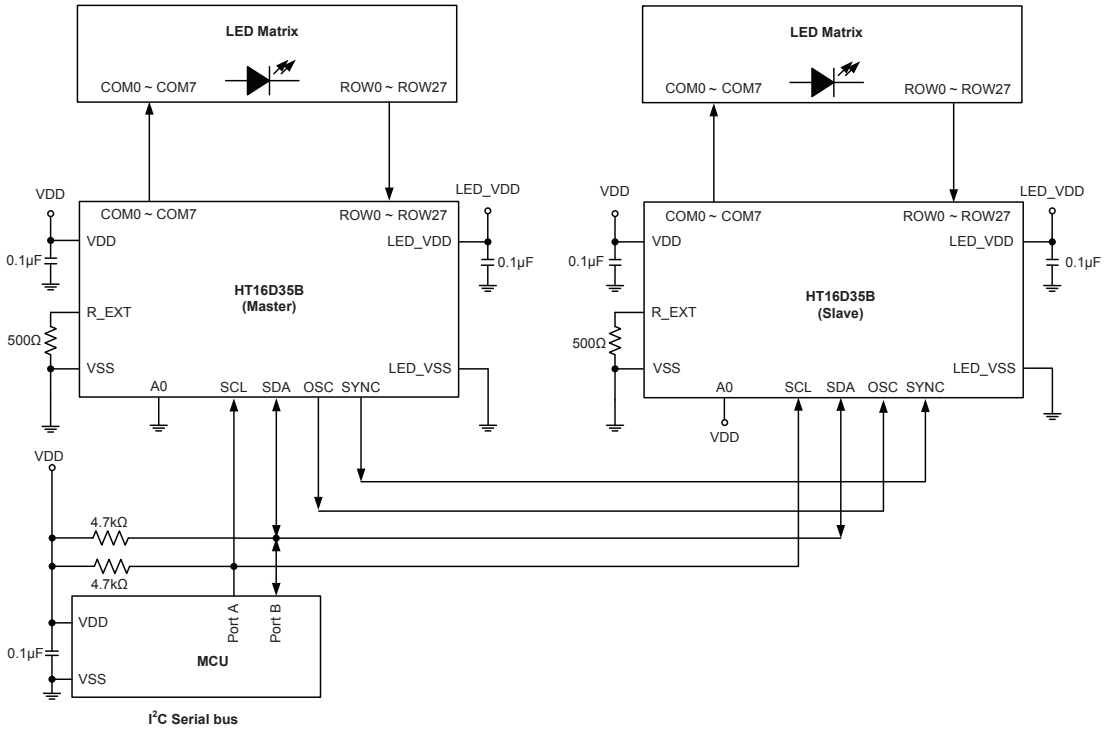
LED Application – P-MOS Open Drain Output

Example 1: SPI 3-wire serial bus



Note: Cascading can also be implemented using software. Users must set the master in the master mode and the slave in the slave mode using commands. The CSB pin must be connected to the MCU individually for independent read and write.

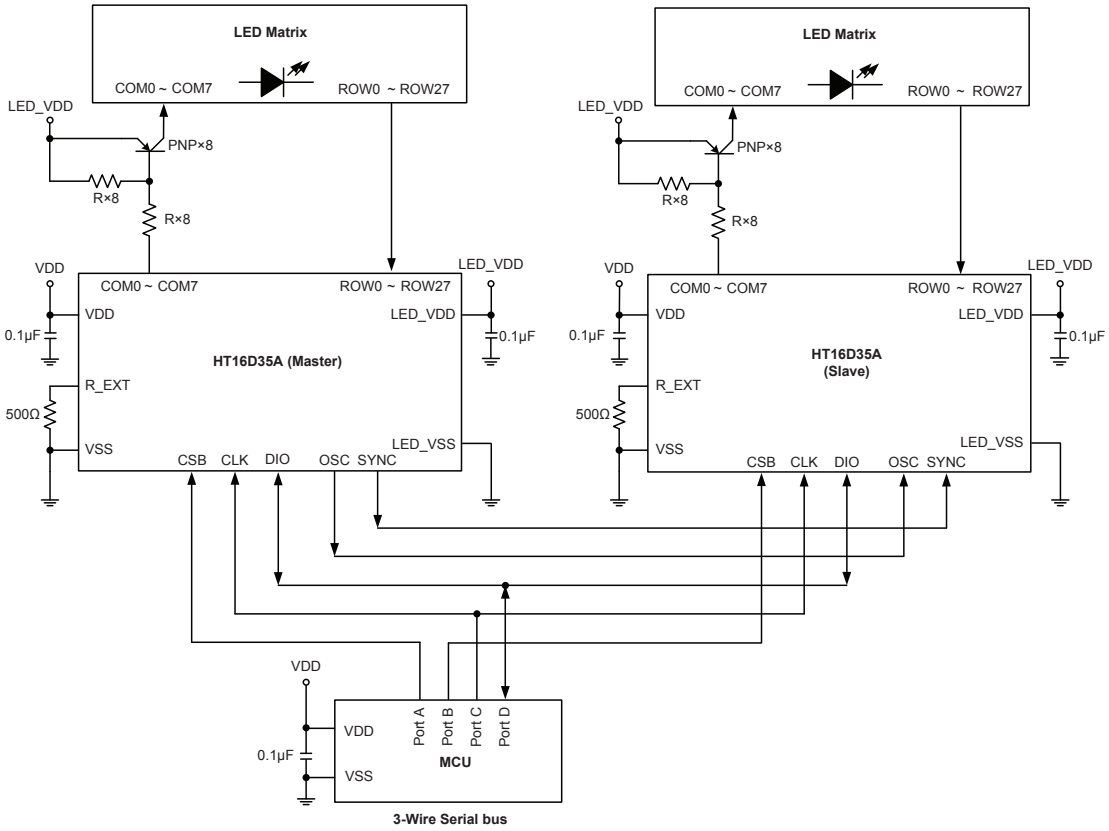
Example 2: I²C serial bus



Note: Cascading can also be implemented using software. Users must set the master in the master mode and the slave in the slave mode using commands. The CSB pin must be connected to the MCU individually for independent read and write.

LED Application – N-MOS Open Drain Output

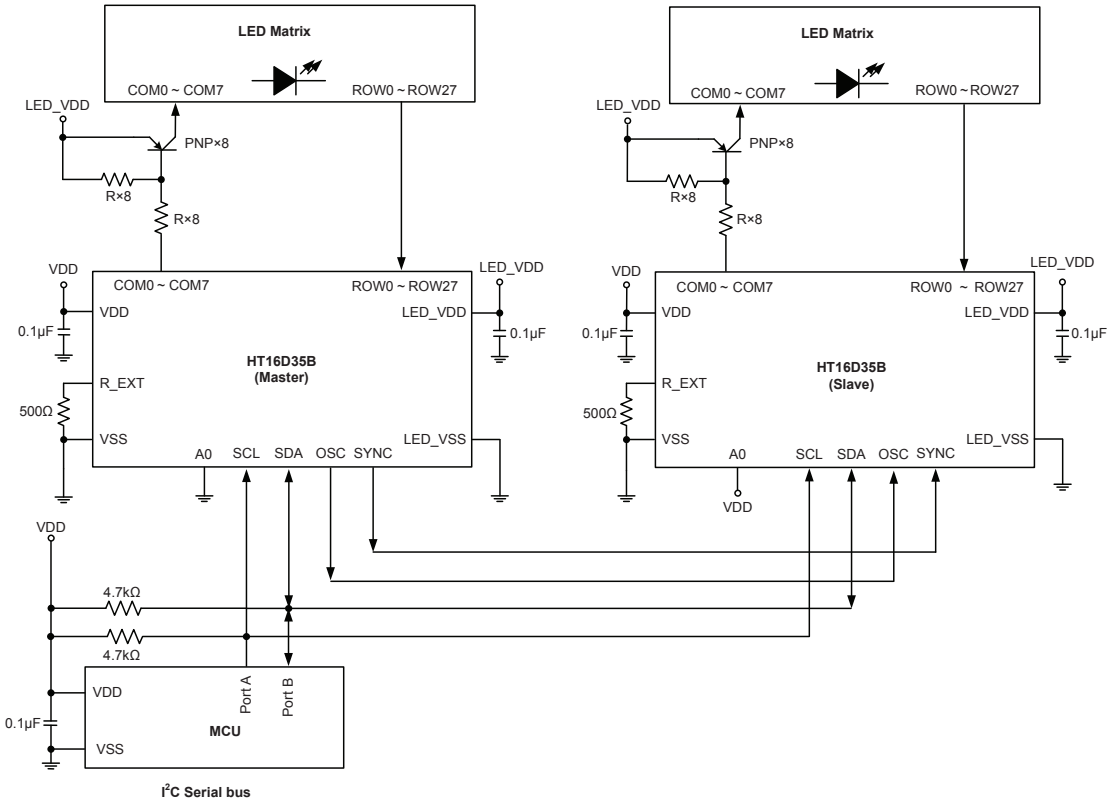
Example 1: COM with transistor buffer for SPI 3-wire serial bus



Note: 1. Cascading can also be implemented using software. Users must set the master in the master mode and the slave in the slave mode using commands. The CSB pin must be connected to the MCU individually for independent read and write.

2. The R resistor values depend upon the LED power consumption.

Example 2: COM with transistor buffer for I²C serial bus

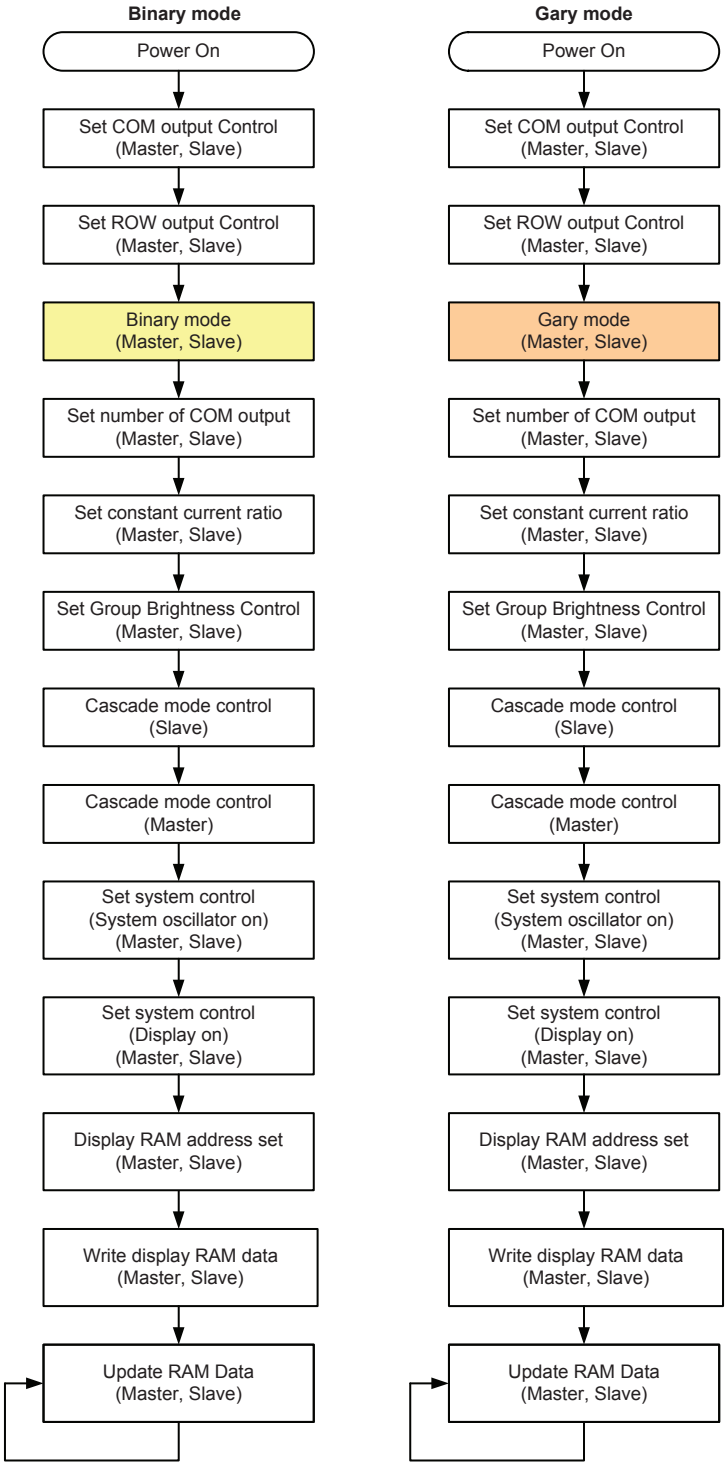


Note: 1. Cascading can also be implemented using software. Users must set the master in the master mode and the slave in the slave mode using commands. The CSB pin must be connected to the MCU individually for independent read and write.

2. The R resistor values depend upon the LED power consumption.

Cascade Control Flow

Access procedures are illustrated below using flowcharts.



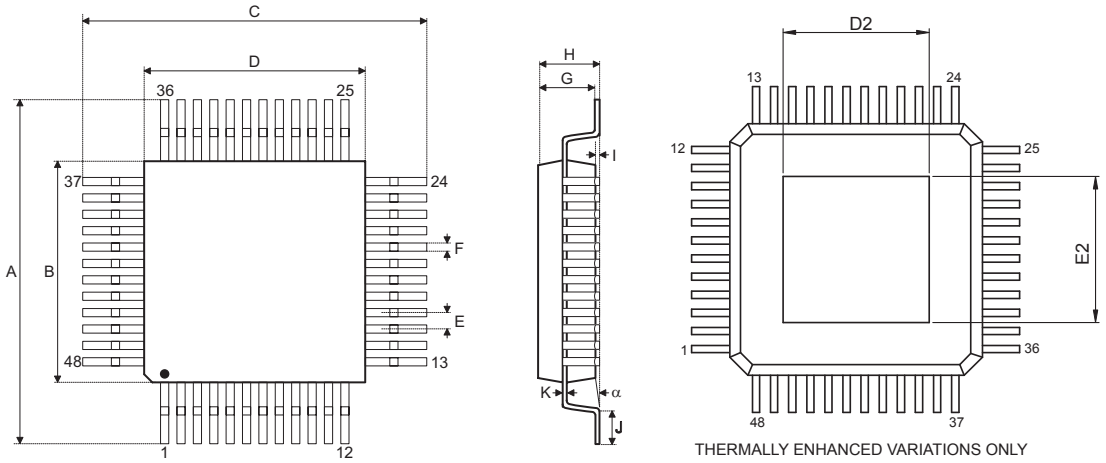
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

48-pin LQFP (7mm×7mm) Outline Dimensions (Exposed Pad)



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
D2	0.170	—	0.205
E	—	0.020 BSC	—
E2	0.079	—	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
D2	4.31	—	5.21
E	—	0.50 BSC	—
E2	2.00	—	—
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°