High Efficiency 700mA Current-Mode Synchronous Buck DC/DC Converter, 1MHz

DESCRIPTION

The TS30111 is a DC/DC synchronous switching regulator with fully integrated power switches, internal compensation, and full fault protection. The switching frequency of 1MHz enables the use of small filter components resulting in minimal board space and reduced BOM costs.

The TS30111 utilizes current mode feedback in normal regulation PWM mode. When the regulator is placed in standby (EN is low), the device draws less than 10uA quiescent current.

The TS30111 integrates a wide range of protection circuitry including input supply under-voltage lockout, output voltage soft start, current limit, and thermal shutdown.

The TS30111 includes supervisory reporting through the PG (Power Good) open drain output to interface other components in the system.

APPLICATIONS

- On-card switching regulators
- Set-top box, DVD, LCD, LED supply
- Industrial power supplies

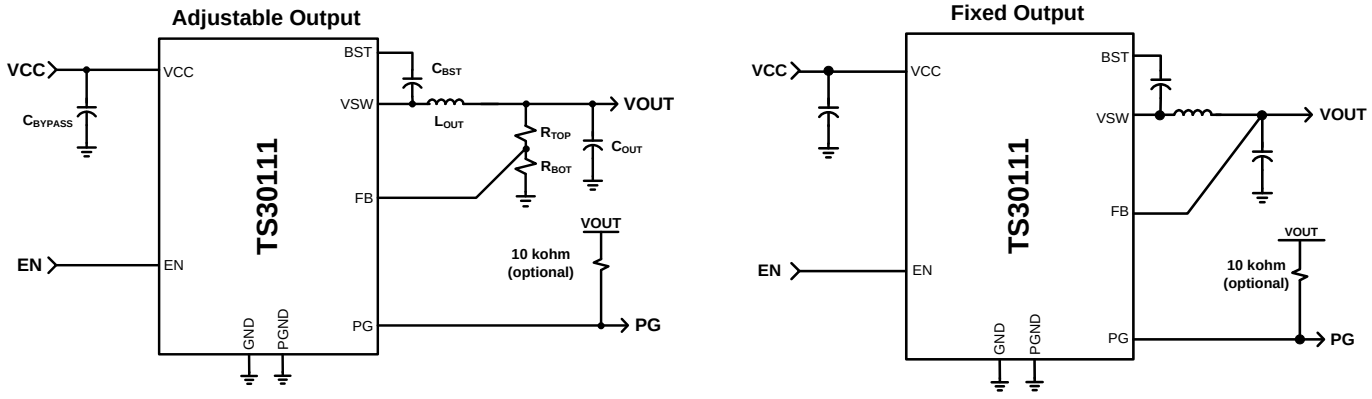
FEATURES

- Fixed output voltage choices: 1.5V, 1.8V, 2.5V, 3.3V, and 5V Adjustable version output voltage range: 0.8V to 5V
- Wide input voltage range 4.5V to 16V (18V Abs Max)
- 1MHz +/- 10% fixed switching frequency
- Continuous output current: 700mA
- High efficiency – up to 90%
- Current mode PWM control with PFM mode for improved light load efficiency
- Voltage supervisor for V_{OUT} reported at the PG pin
- Input supply under voltage lockout
- Soft start for controlled startup with no overshoot
- Full protection for over-current, over-temperature, and V_{OUT} over-voltage
- Less than 10uA in standby mode
- Low external component count

SUMMARY SPECIFICATION

- Junction operating temperature -40 °C to 125 °C
- Packaged in a 16pin QFN (3x3)

TYPICAL APPLICATIONS



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PINOUT

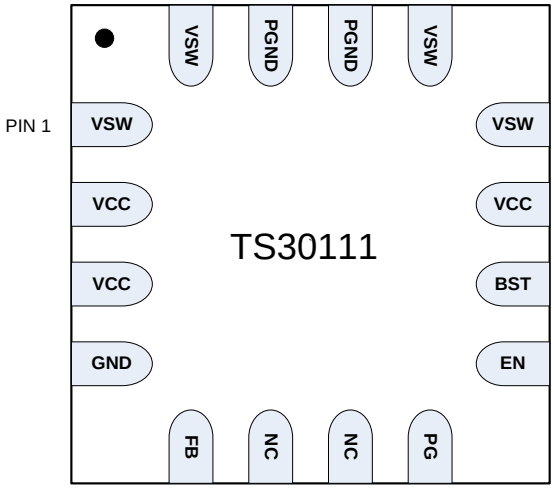


Figure 1: 16 Lead 3x3 QFN, Top View

PIN DESCRIPTION FOR 16 LEAD 3X3 QFN

Pin Symbol	Pin #	Function	Description
VSW	1	Switching Voltage Node	Connected to 3.3uH (typical) inductor
VCC	2	Input Voltage	Input voltage
VCC	3	Input Voltage	Input voltage
GND	4	GND	Primary ground for the majority of the device except the low-side power FET
FB	5	Feedback Input	Regulator FB Voltage. Connects to V_{OUT} for fixed mode and the output resistor divider for adjustable mode
NC	6	No Connect	Not Connected
NC	7	No Connect	Not Connected
PG	8	Power Good Output	Open-drain output
EN	9	Enable Input	Above 2.2V the device is enabled. GND the pin to put device in standby mode. Includes internal pull-up
BST	10	Bootstrap Capacitor	Bootstrap capacitor for the high-side FET gate driver. 22nF ceramic capacitor from BST pin to VSW pin
VCC	11	Input Voltage	Input Voltage
VSW	12	Switching Voltage Node	Connected to 3.3uH (typical) inductor
VSW	13	Switching Voltage Node	Connected to 3.3uH (typical) inductor
PGND	14	Power GND	GND supply for internal low-side FET/integrated diode
PGND	15	Power GND	GND supply for internal low-side FET/integrated diode
VSW	16	Switching Voltage Node	Connected to 3.3uH (typical) inductor

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FUNCTIONAL BLOCK DIAGRAM

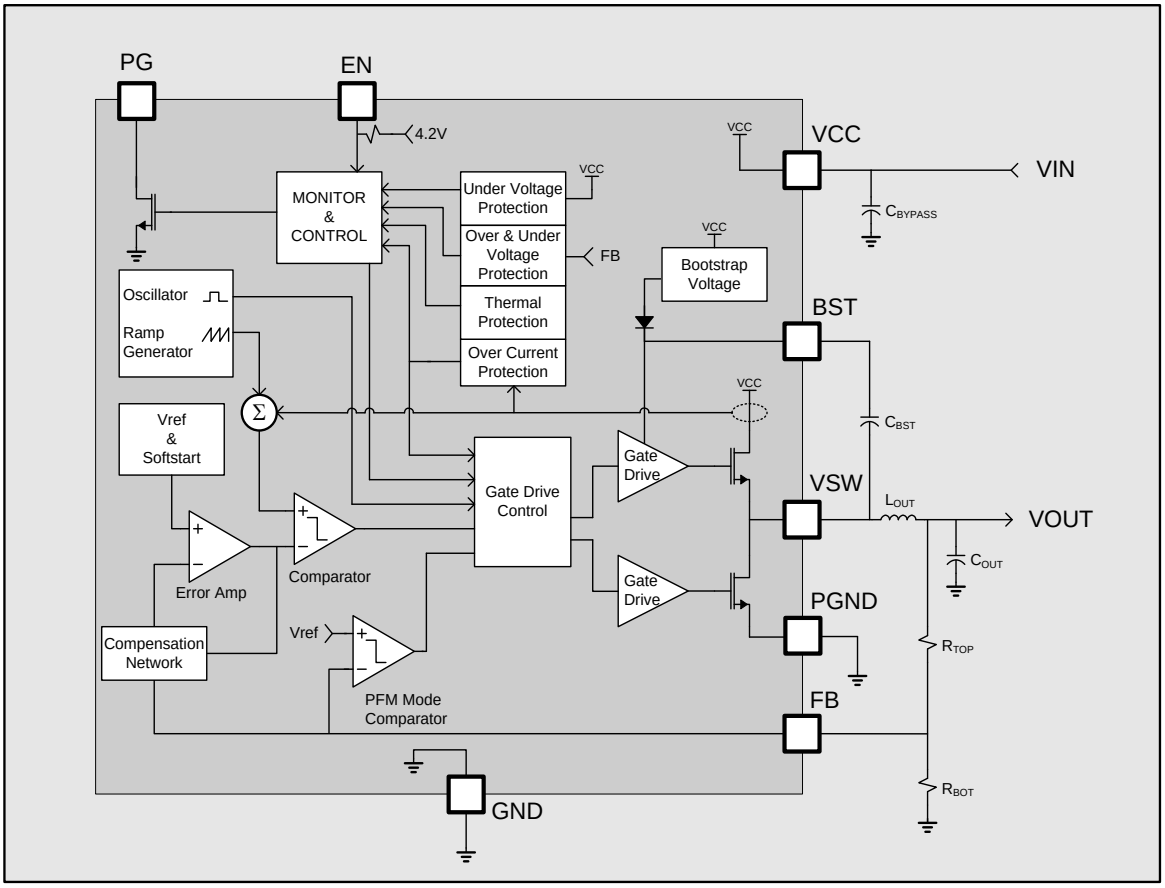


Figure 2: TS30111 Block Diagram

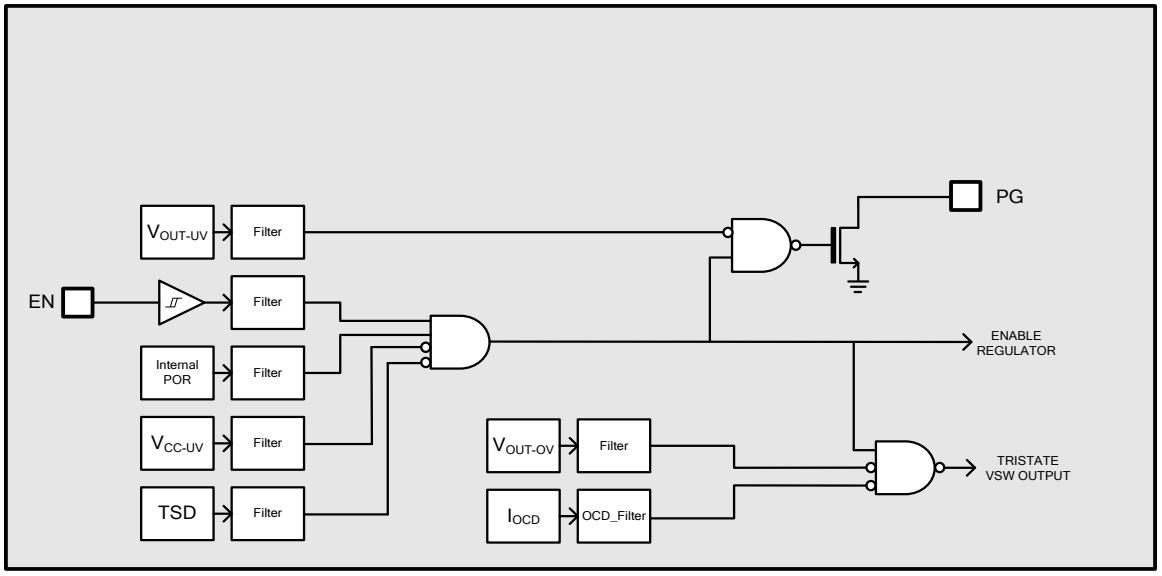


Figure 3: Monitor & Control Logic Functionality

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ABSOLUTE MAXIMUM RATINGS

Over operating free–air temperature range unless otherwise noted(1, 2)

Parameter	Value	Unit
VCC	-0.3 to 18	V
BST	-0.3 to (VCC+6)	V
VSW	-1 to 18	V
EN, PG,FB	-0.3 to 6	V
Electrostatic Discharge – Human Body Model	+/-2k	V
Electrostatic Discharge – Charge Device Model	+/-500	V
Lead Temperature (soldering, 10 seconds)	260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance Junction to Air (Note 1)	38	°C/W
T_{STG}	Storage Temperature Range	-65 to 150	°C
$T_{J\ MAX}$	Maximum Junction Temperature	150	°C
T_J	Operating Junction Temperature Range	-40 to 125	°C

Note 1: Assumes 16LD 3x3 QFN with hi-K JEDEC board and 13.5 inch² of 1 oz Cu

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Input Operating Voltage	4.5	12	16	V
C_{BST}	Bootstrap Capacitor	17.6	22	26.4	nF
L_{OUT}	Output Filter Inductor Typical Value (Note 1)		3.3		uH
C_{OUT}	Output Filter Capacitor Typical Value (Note 2)		22		uF
$C_{OUT-ESR}$	Output Filter Capacitor ESR	2		100	mΩ
C_{BYPASS}	Input Supply Bypass Capacitor Typical Value (Note 3)	8	10		uF

Note 1: For best performance, an inductor with a saturation current rating higher than the maximum V_{OUT} load requirement plus the inductor current ripple.
Note 2: For best performance, a low ESR ceramic capacitor should be used.
Note 3: For best performance, a low ESR ceramic capacitor should be used. If C_{BYPASS} is not a low ESR ceramic capacitor, a 0.1uF ceramic capacitor should be added in parallel to C_{BYPASS}.

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ELECTRICAL CHARACTERISTICS

Electrical Characteristics, T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC Supply Voltage						
VCC	Input Supply Voltage		4.5		16	V
$I_{CC-NORM}$	Quiescent current Normal Mode	VCC = 12V, I_{LOAD} = 0A		5.2		mA
$I_{CC-NOSWITCH}$	Quiescent current Normal Mode – Non-switching	VCC=12V, I_{LOAD}=0A, Non-switching		2.3		mA
$I_{CC-STBY}$	Quiescent current Standby Mode	VCC = 12V, EN = 0V		5	10	uA
VCC Under Voltage Lockout						
VCC_{-UV}	Input Supply Under Voltage Threshold	VCC Increasing		4.3		V
VCC_{-UV_HYST}	Input Supply Under Voltage Threshold Hysteresis			650		mV
OSC						
F_{OSC}	Oscillator Frequency			1		MHz
PG Open Drain Output						
T_{PG}	PG Release Timer			10		ms
I_{OH-PG}	High-Level Output Leakage	V_{PG} = 5V		0.5		uA
V_{OL-PG}	Low-Level Output Voltage	I_{PG} = -0.3mA			0.01	V
EN Input Voltage Thresholds						
V_{IH-EN}	High Level Input Voltage		2.2			V
V_{IL-EN}	Low Level Input Voltage				0.8	V
$V_{HYST-EN}$	Input Hysteresis			480		mV
I_{IN-EN}	Input Leakage	V_{EN}=5V		3.5		uA
		V_{EN}=0V		-1.5		uA
Thermal Shutdown						
TSD	Thermal Shutdown Junction Temperature	Note: not tested in production	150	170		°C
TSD_{HYST}	TSD Hysteresis	Note: not tested in production		10		°C

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REGULATOR CHARACTERISTICS

Electrical Characteristics, T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Switch Mode Regulator: L=3.3uH and C=22uF						
$V_{OUT-PWM}$	Output Voltage Error in PWM Mode	I_{LOAD} =700 mA		±2%		V
$V_{OUT-PFM}$	Output Voltage Tolerance in PFM Mode	I_{LOAD} = 0A		V_{OUT} + 1%		V
R_{DSON}	High Side Switch On Resistance	I_{VSW} = -700mA (Note 1)		240		mΩ
	Low Side Switch On Resistance	I_{VSW} = 700mA (Note 1)		160		mΩ
I_{OUT}	Output Current	TS30111			700	mA
I_{OCD}	Over Current Detect	HS switch current TS30111		1.2		A
FB_{TH}	Feedback Reference (Adjustable Mode)	(Note 3)		0.8		V
FB_{TH-TOL}	Feedback Reference Absolute Tolerance	(Note 3)		1.5		%
T_{SS}	Soft start Ramp Time			4		ms
FB_{TH-PFM}	PFM Mode FB Comparator Threshold			V_{OUT} + 1%		V
V_{OUT-UV}	V_{OUT} Under Voltage Threshold			93% V_{OUT}		
V_{OUT-UV_HYST}	V_{OUT} Under Voltage Hysteresis			1.5% V_{OUT}		
V_{OUT-OV}	V_{OUT} Over Voltage Threshold			103% V_{OUT}		
V_{OUT-OV_HYST}	V_{OUT} Over Voltage Hysteresis			1% V_{OUT}		
$DUTY_{MAX}$	Max Duty Cycle	(Note 2)	95%	97%	99%	

Note 1: R_{DSON} is characterized at 600mA and tested at lower current in production.
Note 2: Regulator VSW pin is forced off for 240ns every 8 cycles to ensure the BST cap is replenished.
Note 3: For the adjustable version, the ratio of VCC/Vout cannot exceed 16.
Note 4: Based on Over Current Detect testing

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FUNCTIONAL DESCRIPTION

The TS30111 current-mode synchronous step-down power supply product is ideal for use in the commercial, industrial, and automotive market segments. It includes flexibility to be used for a wide range of output voltages and is optimized for high efficiency power conversion with low R_{DSON} integrated synchronous switches. A 1MHz internal switching frequency facilitates low cost LC filter combinations. Additionally, the fixed output versions enable a minimum external component count to provide a complete regulation solution with only 4 external components: an input bypass capacitor, an inductor, an output capacitor, and the bootstrap capacitor. The regulator automatically transitions between PFM and PWM mode to maximize efficiency for the load demand.

The TS30111 was designed to provide these system benefits:

- Reduced board real estate
- Lower system cost
  - Lower cost inductor
  - Low external parts count
- Ease of design
  - Bill of Materials and suggested board layout provided
  - Power Good output
  - Integrated compensation network
  - Wide input voltage range
- Robust solution
  - Over current, over voltage and over temperature protection

DETAILED PIN DESCRIPTION

Unregulated input, VCC
This terminal is the unregulated input voltage source for the IC. It is recommended that a 10uF bypass capacitor be placed close to the device for best performance. Since this is the main supply for the IC, good layout practices need to be followed for this connection.

Bootstrap control, BST
This terminal will provide the bootstrap voltage required for the upper internal NMOS switch of the buck regulator. An external ceramic capacitor placed between the BST input terminal and the VSW pin will provide the necessary voltage for the upper switch. In normal operation the capacitor is re-charged on every low side synchronous switching action. In the case of where the switch mode approaches 100% duty cycle for the high side FET, the device will automatically reduce the duty cycle switch to a minimum off time on every 8^{th} cycle to allow this capacitor to re-charge.

Sense feedback, FB
This is the input terminal for the output voltage feedback.

For the fixed mode versions, this should be hooked directly to V_{OUT}. The connection on the PCB should be kept as short as possible, and should be made as close as possible to the capacitor. The trace should not be shared with any other connection. (Figure 23)

For adjustable mode versions, this should be connected to the external resistor divider. To choose the resistors, use the following equation:

$$V_{OUT} = 0.8\ (1 + R_{TOP}/R_{BOT})$$

The input to the FB pin is high impedance, and input current should be less than 100nA. As a result, good layout practices are required for the feedback resistors and feedback traces. When using the adjustable version, the feedback trace should be kept as short as possible and minimum width to reduce stray capacitance and to reduce the injection of noise.

For the adjustable version, the ratio of VCC/Vout cannot exceed 16.

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Switching output, VSW
This is the switching node of the regulator. It should be connected directly to the 3.3uH inductor with a wide, short trace and to one end of the Bootstrap capacitor. It is switching between VCC and PGND at the switching frequency.

Ground, GND
This ground is used for the majority of the device including the analog reference, control loop, and other circuits.

Power Ground, PGND
This is a separate ground connection used for the low side synchronous switch to isolate switching noise from the rest of the device. (Figure 23)

Enable, high-voltage, EN
This is the input terminal to activate the regulator. The input threshold is TTL/CMOS compatible. It also has an internal pull-up to ensure a stable state if the pin is disconnected.

Power Good Output, PG
This is an open drain, active low output. The switched mode output voltage is monitored and the PG line will remain low until the output voltage reaches the V_{OUT-UV} threshold. Once the internal comparator detects the output voltage is above the desired threshold, an internal delay timer is activated and the PG line is de-asserted to high once this delay timer expires. In the event the output voltage decreases below V_{OUT-UV}, the PG line will be asserted low and remain low until the output rises above V_{OUT-UV} and the delay timer times out. See Figure 2 for the circuit schematic for the PG signal.

INTERNAL PROTECTION DETAILS

Internal Current Limit
The current through the high side FET is sensed on a cycle by cycle basis and if current limit is reached, it will abbreviate the cycle. In addition, the device senses the FB pin to identify hard short conditions and will direct the VSW output to skip 4 cycles if current limit occurs when FB is low. This allows current built up in the inductor during the minimum on time to decay sufficiently. Current limit is always active when the regulator is enabled. Soft start ensures current limit does not prevent regulator startup.

Under extended over current conditions (such as a short), the device will automatically disable. Once the over current condition is removed, the device returns to normal operation automatically. (Alternately the factory can configure the device's NVM to shutdown the regulator if an extended over current event is detected and require a toggle of the Enable pin to return the device to normal operation.)

Thermal Shutdown
If the temperature of the die exceeds 170°C (typical), the VSW outputs will tri-state to protect the device from damage. The PG and all other protection circuitry will stay active to inform the system of the failure mode. Once the device cools to 160°C (typical), the device will start up again, following the normal soft start sequence. If the device reaches 170°C, the shutdown/restart sequence will repeat.

Reference Soft Start
The reference in this device is ramped at a rate of 4ms to prevent the output from overshoot during startup. This ramp restarts whenever there is a rising edge sensed on the Enable pin. This occurs in both the fixed and adjustable versions. During the soft start ramp, current limit is still active, and will still protect the device in case of a short on the output.

Output Overvoltage
If the output of the regulator exceeds 103% of the regulation voltage, the VSW outputs will tri-state to protect the device from damage. This check occurs at the start of each switching cycle. If it occurs during the middle of a cycle, the switching for that cycle will complete, and the VSW outputs will tri-state at the beginning of the next cycle.

VCC Under-Voltage Lockout
The device is held in the off state until VCC reaches 4.3V (typical). There is a 300mV hysteresis on this input, which requires the input to fall below 4V (typical) before the device will disable.

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TYPICAL PERFORMANCE CHARACTERISTICS

VCC = 12V, C_{OUT} = 2 x 22uF (unless otherwise noted)

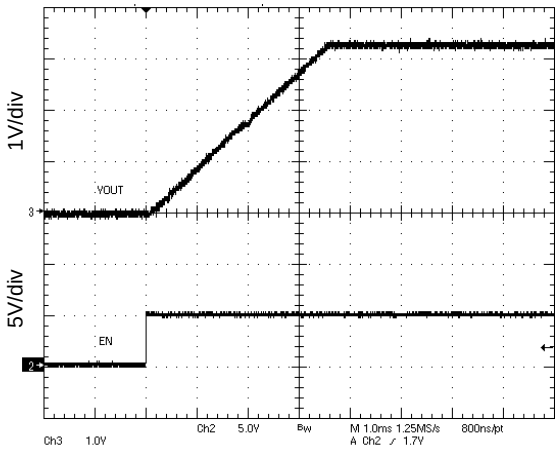


Figure 4. Startup Response

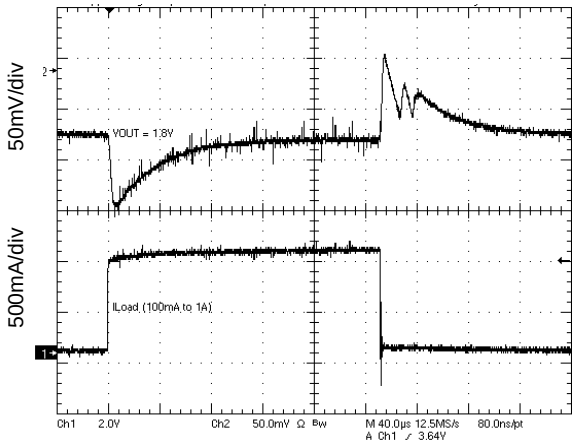


Figure 5. 100mA to 1A Load Step (Vcc=12V, V_{OUT}=1.8V)

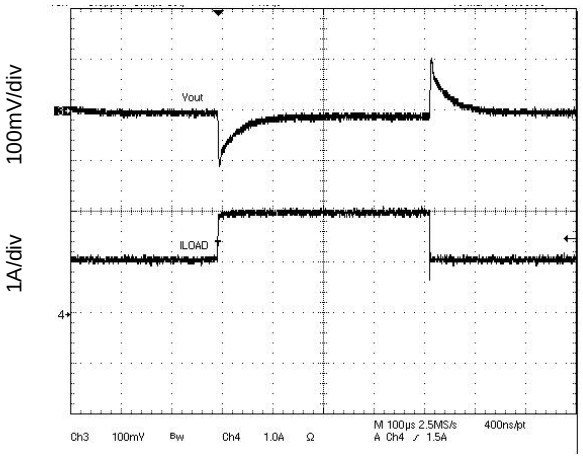


Figure 6. 100mA to 1A Load Step (V_{CC}=12V, V_{OUT}=3.3V)

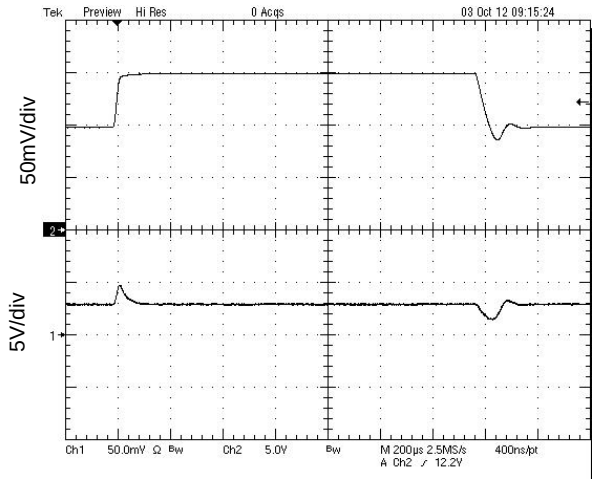


Figure 7. Line Transient Response (VCC=12V, V_{OUT}=3.3V)

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TYPICAL PERFORMANCE CHARACTERISTICS

VCC = 12V, C_{OUT} = 2 x 22uF (unless otherwise noted)

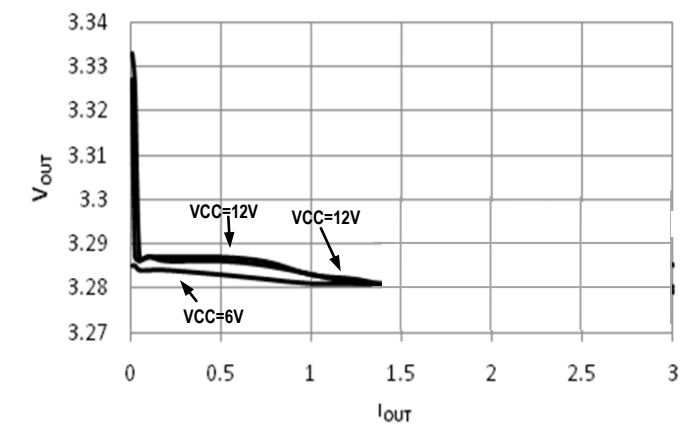


Figure 8. Load Regulation

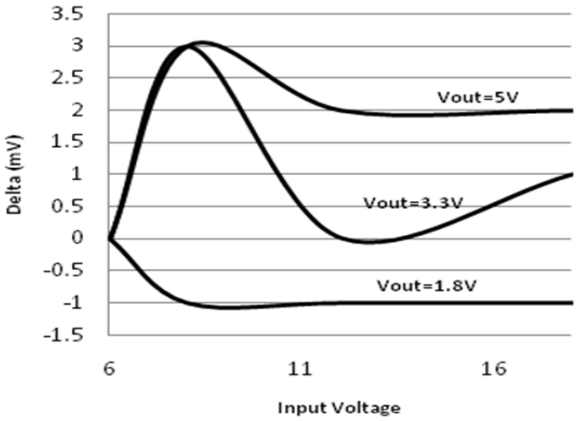


Figure 9. Line Regulation (I_{OUT}=1A)

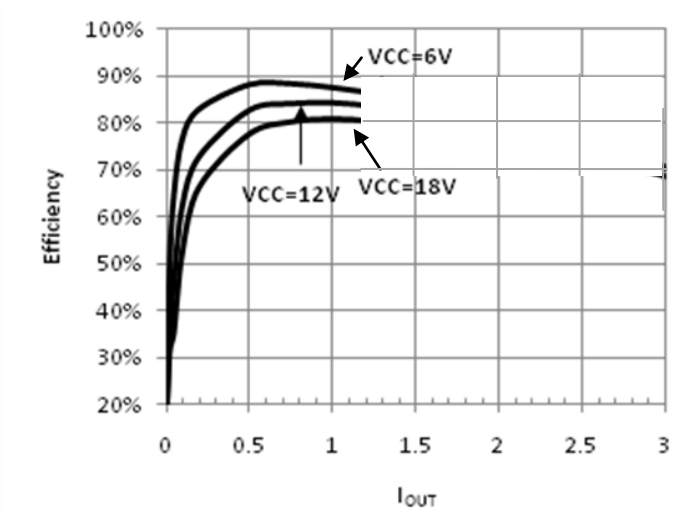


Figure 10. Efficiency vs. Output Current (V_{OUT} = 1.8V)

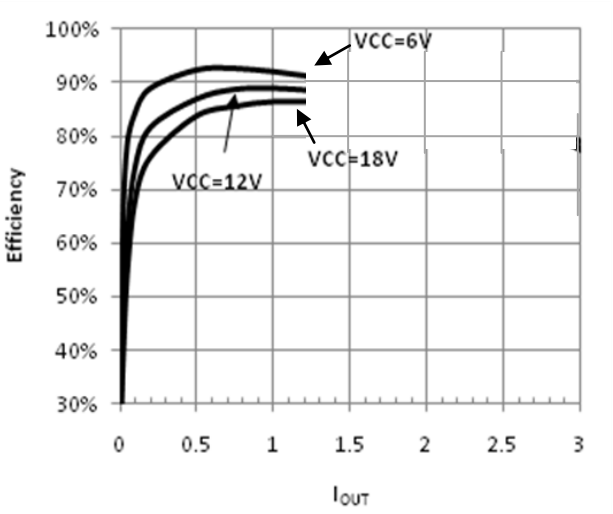


Figure 11. Efficiency vs. Output Current (V_{OUT} = 3.3V)

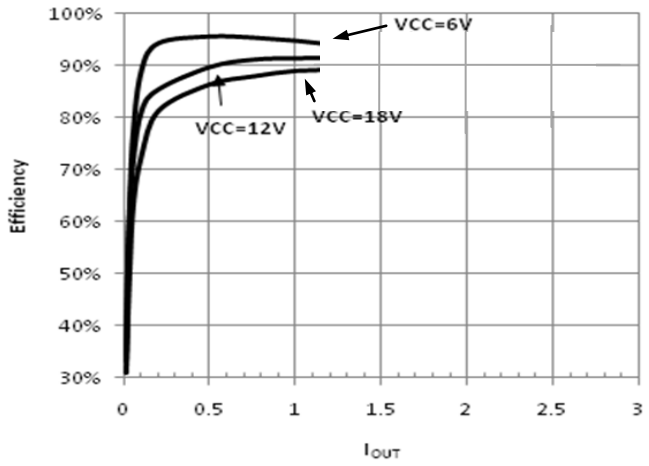


*Figure **12**. Efficiency vs. Output Current (V_{OUT} = 5V)*

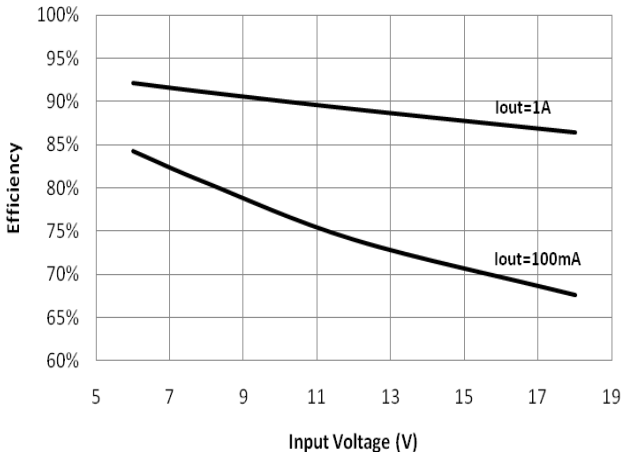


*Figure **13**. Efficiency vs. Input Voltage (V_{OUT} = 3.3V)*

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TYPICAL PERFORMANCE CHARACTERISTICS

VCC = 12V, C_{OUT} = 2 x 22uF (unless otherwise noted)

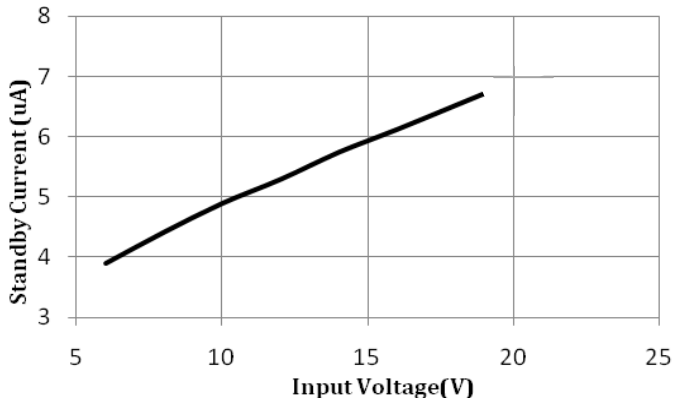


Figure 14. Standby Current vs. Input Voltage

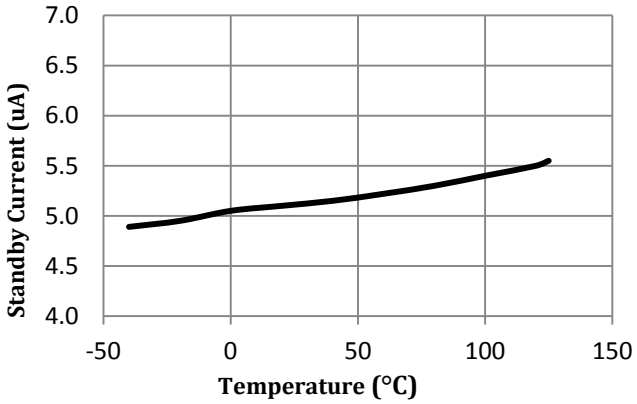


Figure 15. Standby Current vs. Temperature

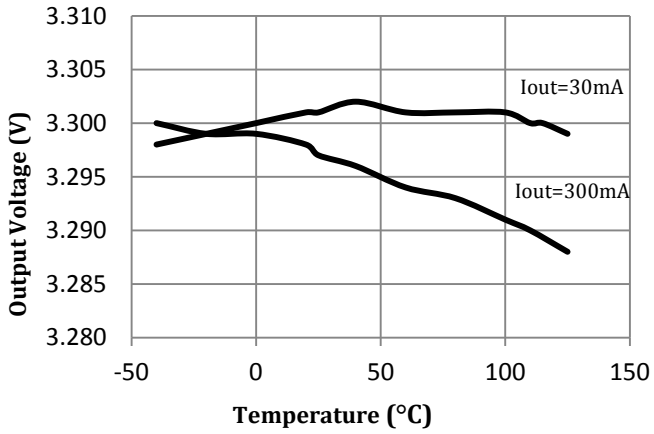


Figure 16. Output Voltage vs. Temperature

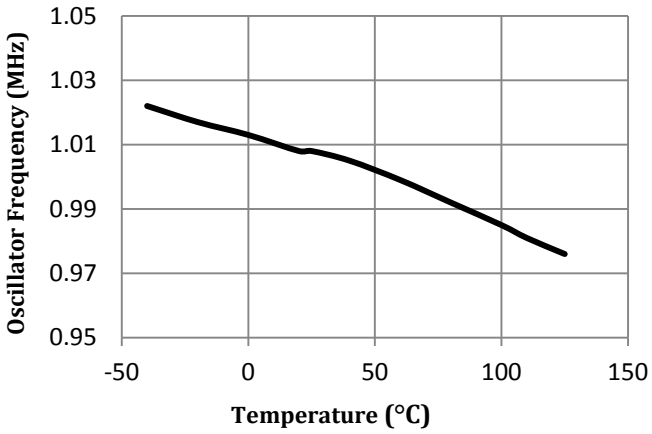


Figure 17. Oscillator Frequency vs. Temperature (Iout=300mA)

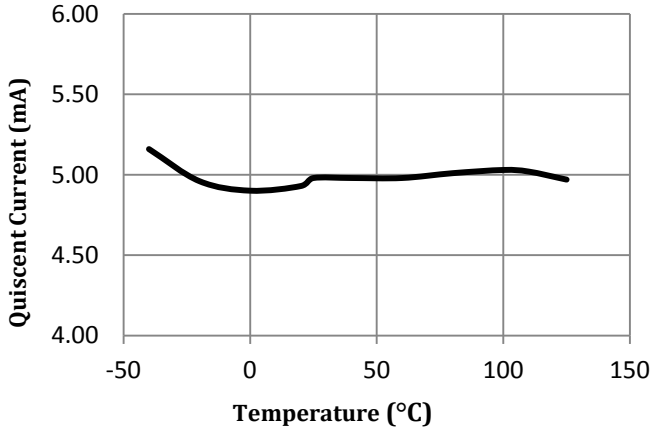


Figure 18. Quiescent Current vs. Temperature (No load)

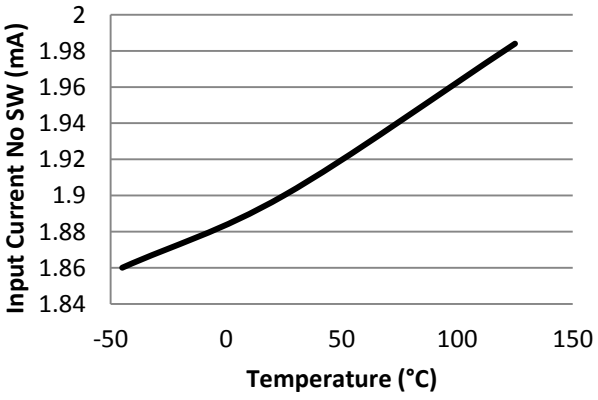


Figure 19. Input Current vs. Temperature (No load, No switching)

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TYPICAL APPLICATION SCHEMATIC

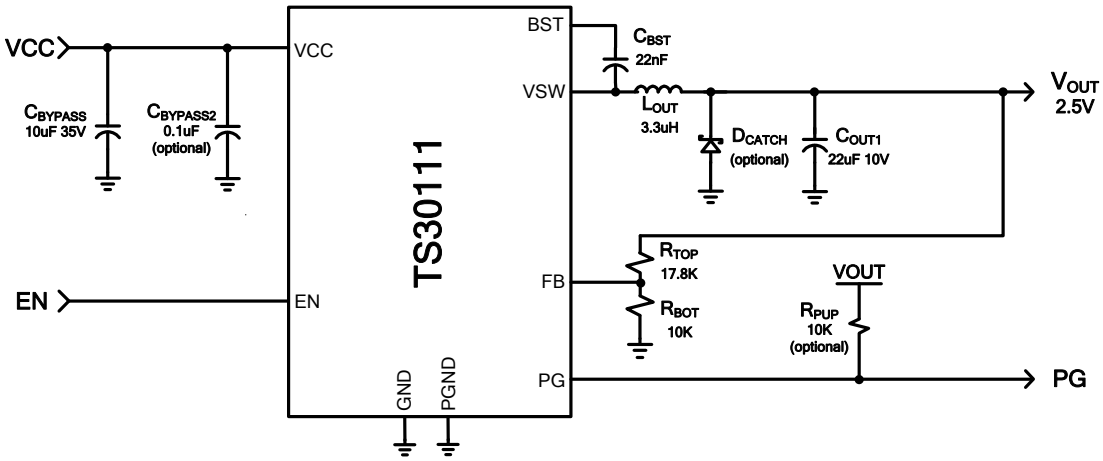


Figure 20: TS30111 Application Schematic

A minimal schematic suitable for most applications is shown on page 1. Figure 22 includes optional components that may be considered to address specific issues as listed in the External Component Selection section.

PCB LAYOUT

For proper operation and minimum EMI, care must be taken during PCB layout. An improper layout can lead to issues such as poor stability and regulation, noise sensitivity and increased EMI radiation. (figure 23) The main guidelines are the following:

- provide low inductive and resistive paths for loops with high di/dt,
- provide low capacitive paths with respect to all the other nodes for traces with high di/dt,
- sensitive nodes not assigned to power transmission should be referenced to the analog signal ground (GND) and be always separated from the power ground (PGND).

The negative ends of C_{BYPASS}, C_{OUT} and the Schottky diode D_{CATCH} (optional) should be placed close to each other and connected using a wide trace. Vias must be used to connect the PGND node to the ground plane. The PGND node must be placed as close as possible to the TS30111 PGND pins to avoid additional voltage drop in traces.

The bypass capacitor C_{BYPASS} (optionally paralleled to a 0.1µF capacitor) must be placed close to the VCC pins of TS30111.

The inductor must be placed close to the VSW pins and connected directly to C_{OUT} in order to minimize the area between the VSW pin, the inductor, the C_{OUT} capacitor and the PGND pins. The trace area and length of the switching nodes VSW and BST should be minimized.

For the adjustable output voltage version of the TS30111, feedback resistors R_{BOT} and R_{TOP} are required for Vout settings greater than 0.8V and should be placed close to the TS30111 in order to keep the traces of the sensitive node FB as short as possible and away from switching signals. R_{BOT} should be connected to the analog ground pin (GND) directly and should never be connected to the ground plane. The analog ground trace (GND) should be connected in only one point to the power ground (PGND). A good connection point is under the TS30111 package to the exposed thermal pad and vias which are connected to PGND. R_{TOP} will be connected to the V_{OUT} node using a trace that ends close to the actual load.

For fixed output voltage versions of the TS30111, R_{BOT} and R_{TOP} are not required and the FB pin should be connected directly to the Vout.

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The exposed thermal pad must be soldered to the PCB for mechanical reliability and to achieve good power dissipation. Vias must be placed under the pad to transfer the heat to the ground plane.

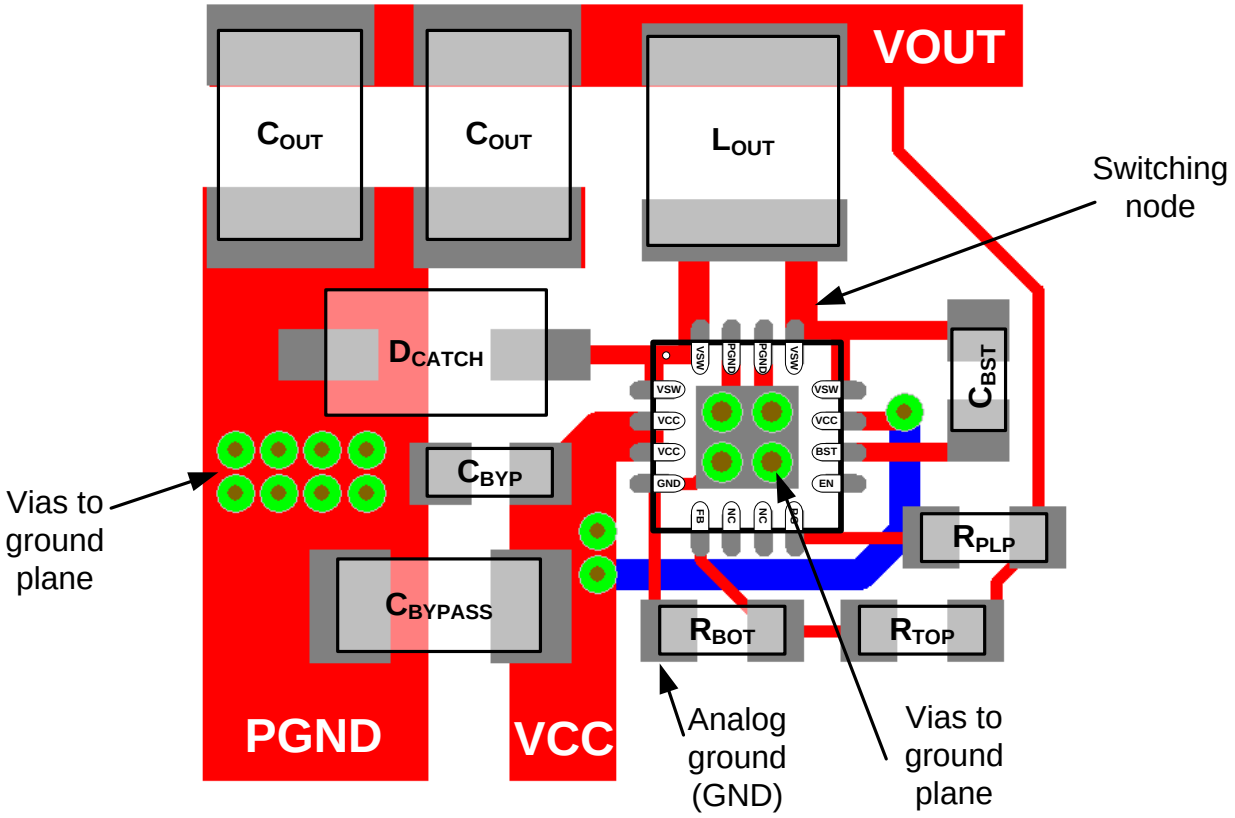


Figure 21: TS30111 PCB Layout, Top View

EXTERNAL COMPONENT BILL OF MATERIALS

Designator	Function	Description	Suggested Manufacturer	Manufacturer Code	Qty
C_{BYPASS}	Input Supply Bypass Capacitor	10uF 10% 35V	TDK	CGA5L3X5R1V106K160AB	1
C_{OUT}	Output Filter Capacitor	22uF 10% 10V	TDK	C2012X5R1A226K125AB	1
L_{OUT}	Output Filter Inductor	3.3uH 900mA	TDK Wurth	MLP2012S3R3MT 744045003	1
C_{BST}	Boost Capacitor	22nF 10V	TDK	C1005X7R1C223K	1
R_{TOP}	Voltage Feedback Resistor (optional)	17.8K (Note 1)			1
R_{BOT}	Voltage Feedback Resistor (optional)	10K (Note 1)			1
R_{PLP}	PG Pin Pull-up Resistor (optional)	10K			1
D_{CATCH}	Catch Diode (optional)	30V 2A SOD-123FL	On Semiconductor	MBR230LSFT1G	1

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Note 1: The voltage divider resistor values are calculated for an output voltage of 2.5V. For fixed output versions, the FB pin is connected directly to V_{OUT}.

EXTERNAL COMPONENT SELECTION

The 1MHz internal switching frequency of the TS30111 facilitates low cost LC filter combinations. Additionally, the fixed output versions enable a minimum external component count to provide a complete regulation solution with only 4 external components: an input bypass capacitor, an inductor, an output capacitor, and the bootstrap capacitor. The internal compensation is optimized for a 22uF output capacitor and a 3.3uH inductor.

For best performance, a low ESR ceramic capacitor should be used for C_{BYPASS}. If C_{BYPASS} is not a low ESR ceramic capacitor, a 0.1uF ceramic capacitor should be added in parallel to C_{BYPASS}.

The minimum allowable value for the output capacitor is 22uF. To keep the output ripple low, a low ESR (less than 35mOhm) ceramic is recommended. Multiple capacitors can be paralleled to reduce the ESR.

The inductor range is 3.3uH +/-20%. For optimal over-current protection, the inductor should be able to handle up to the regulator current limit without saturation. Otherwise, an inductor with a saturation current rating higher than the maximum I_{OUT} load requirement plus the inductor current ripple should be used.

For high current modes, the optional Schottky diode will improve the overall efficiency and reduce the heat. It is up to the user to determine the cost/benefit of adding this additional component in the user's application. The diode is typically not needed.

For the adjustable output version of the TS30111, the output voltage can be adjusted by sizing R_{TOP} and R_{BOT} feedback resistors. The equation for the output voltage is $V_{OUT} = 0.8\ (1 + R_{TOP}/R_{BOT})$.

For the adjustable version, the ratio of VCC/Vout cannot exceed 16.

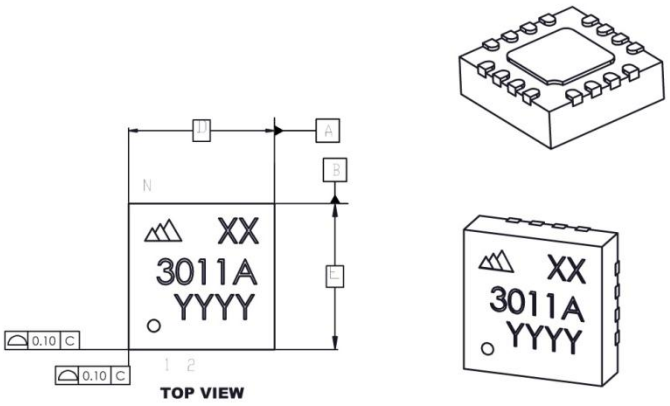
R_{PUP} is only required when the Power Good signal (PG) is utilized.

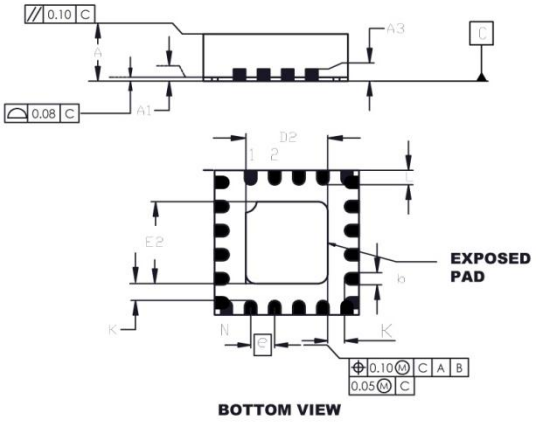
THERMAL INFORMATION

TS30111 is designed for a maximum operating junction temperature T_j of 125°C. The maximum output power is limited by the power losses that can be dissipated over the thermal resistance given by the package and the PCB structures. The PCB must provide heat sinking to keep the TS30111 cool. The exposed metal on the bottom of the QFN package must be soldered to a ground plane. This ground should be tied to other copper layers below with thermal vias. Adding more copper to the top and the bottom layers and tying this copper to the internal planes with vias can reduce thermal resistance further. For a hi-K JEDEC board and 13.5 square inch of 1 oz Cu, the thermal resistance from junction to ambient can be reduced to θ_{JA} = 38°C/W. The power dissipation of other power components (catch diode, inductor) cause additional copper heating and can further increase what the TS30111 sees as ambient temperature.

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PACKAGE MECHANICAL DRAWINGS (all dimensions in mm)





Units		MILLIMETERS		
Dimensions Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	1.55	1.70	1.80
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.55	1.70	1.80
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.30	0.40
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

Dimensions and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

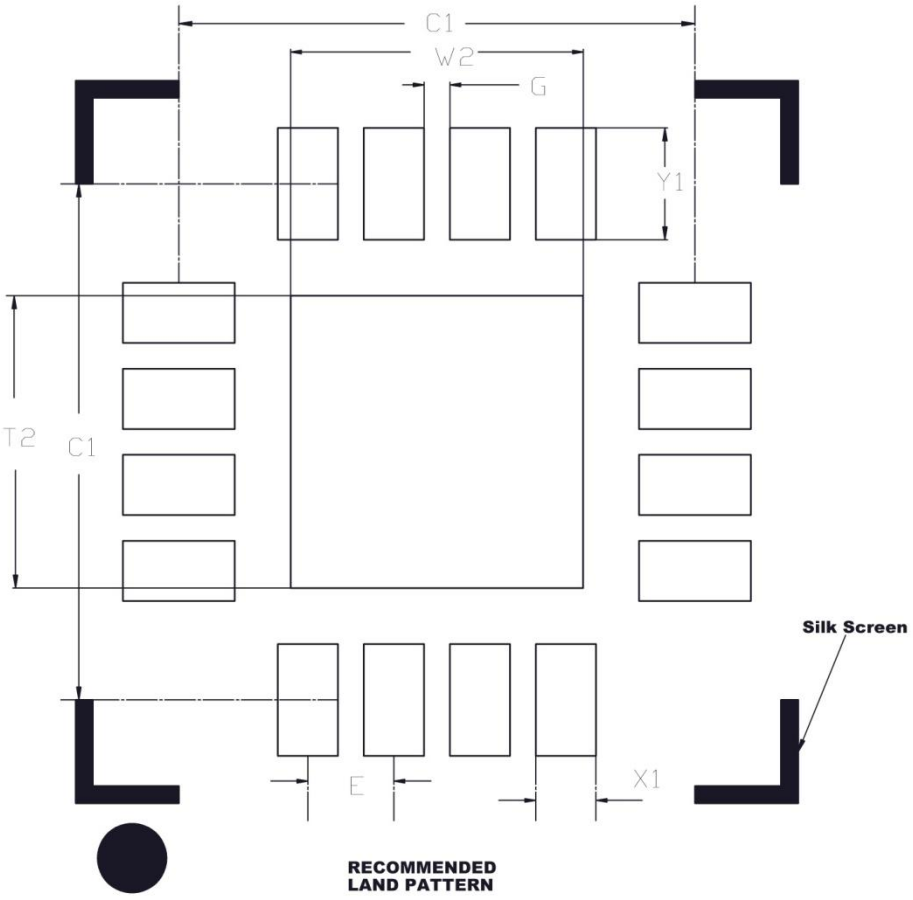
REF: Refernce Dimension, usually without tolerance, for information only.

YYYY = Internal trace code.

XX = Internal Year and assembly code.

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RECOMMEDED PCB LAND PATTERN



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2	-	-	1.70
Optional Center Pad Length	T2	-	-	1.70
Contact Pad Spacing	C1	-	3.00	-
Contact Pad Spacing	C2	-	3.00	-
Contact Pad Width (X16)	X1	-	-	0.35
Contact Pad Length (X16)	Y1	-	-	0.65
Distance Between Pads	G	0.15	-	-

Notes:

Dimensions and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Refernce Dimension, usually without tolerance, for information only.

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PACAKGING INFORMATION

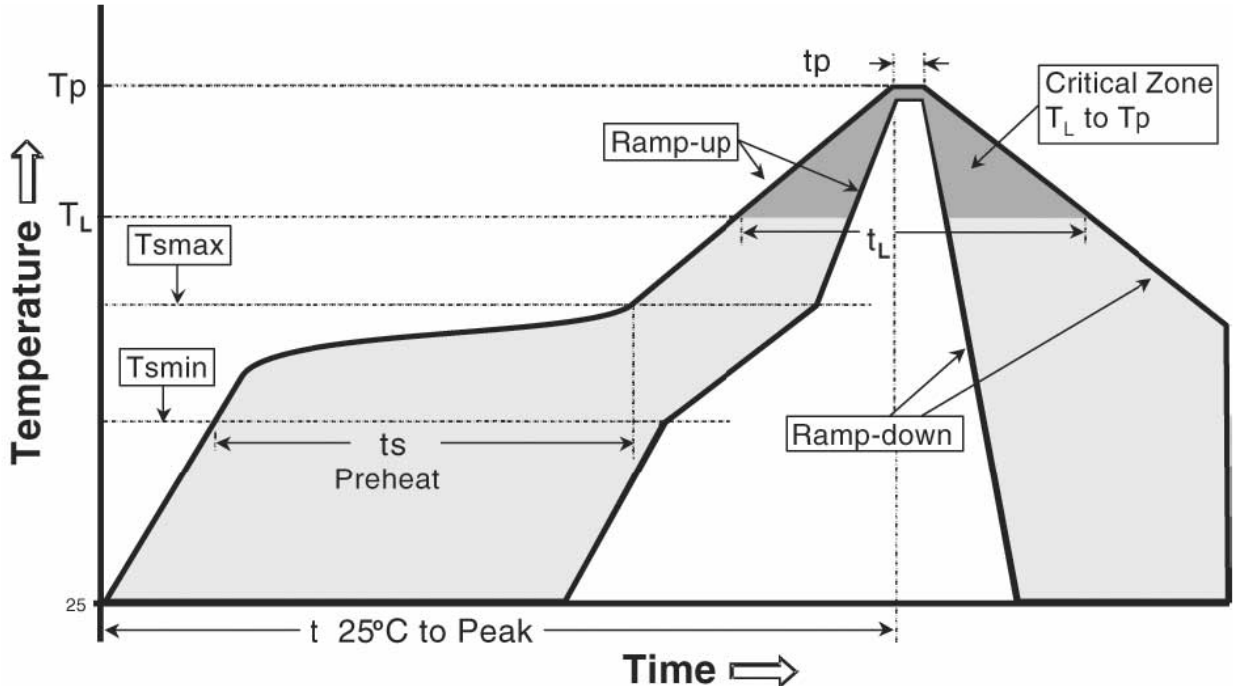
Pb-Free (RoHS): The TS30111 devices are fully compliant for all materials covered by European Union Directive 2002/95/EC, and meet all IPC-1752 Level 3 materials declaration requirements.

MSL, Peak Temp: The TS30111 family has a Moisture Sensitivity Level (MSL) 1 rating per JEDEC J-STD-020D. These devices also have a Peak Profile Solder Temperature (Tp) of 260°C.

IR REFLOW PROFILE

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (Tsmax to Tp)	3° C/second max.	3° C/second max.
Preheat - Temperature Min (Ts_{min}) - Temperature Max (Ts_{max}) - Time (Ts_{min} to Ts_{max}) (ts)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	 183 °C 60-150 seconds	 217 °C 60-150 seconds
Peak Temperature (Tp)	See Table 4.1	See Table 4.2
Time within 5°C of actual Peak Temperature (tp)[2]	10-30 seconds	20-40 seconds
Ramp-down Rate	6 °C/second max.	6 °C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.
Note 2: Time within 5 °C of actual peak temperature (tp) specified for the reflow profiles is a "supplier" minimum and "user" maximum.



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Table 4-1 SnPb Eutectic Process - Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥ 350
<2.5 mm	240 +0/-5 °C	225 +0/-5°C
≥ 2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 4-2 Pb-free Process - Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 > 2000
< 1.6 mm	260 °C *	260 °C *	260 °C *
1.6 mm - 2.5 mm	260 °C *	250 °C *	245 °C *
> 2.5 mm	250 °C *	245 °C *	245 °C *
* Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature at the rated MSL level			

Note 1: Package volume excludes external terminals (balls, bumps, lands, leads) and/or non-integral heat sinks.

Note 2: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Note 3: Components intended for use in a ''lead-free'' assembly process shall be evaluated using the ''lead free'' peak temperature and profiles defined in Tables 4-1, 4.2 and 5-2 whether or not lead free.

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ROHS AND REACH COMPLIANCE

Triune Systems is fully committed to environmental quality. All Triune Systems materials and suppliers are fully compliant with RoHS (European Union Directive 2011/65/EU), REACH SVHC Chemical Restrictions (EC 1907/2006), IPC-1752 Level 3 materials declarations, and their subsequent amendments. Triune Systems maintains certified laboratory reports for all product materials, from all suppliers, which show full compliance to restrictions on the following:

- Cadmium (Cd)
- Chlorofluorocarbons (CFCs)
- Chlorinate Hydrocarbons (CHCs)
- Halons
- Hexavalent Chromium (CrVI)
- Hydrobromofluorocarbons (HBFCs)
- Hydrochlorofluorocarbons (HCFCs)
- Lead (Pb)
- Mercury (Hg)
- Perfluorocarbons (PFCs)
- Polybrominated biphenyls (PBB)
- Polybrominated Diphenyl Ethers (PBDEs)

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ORDERING INFORMATION

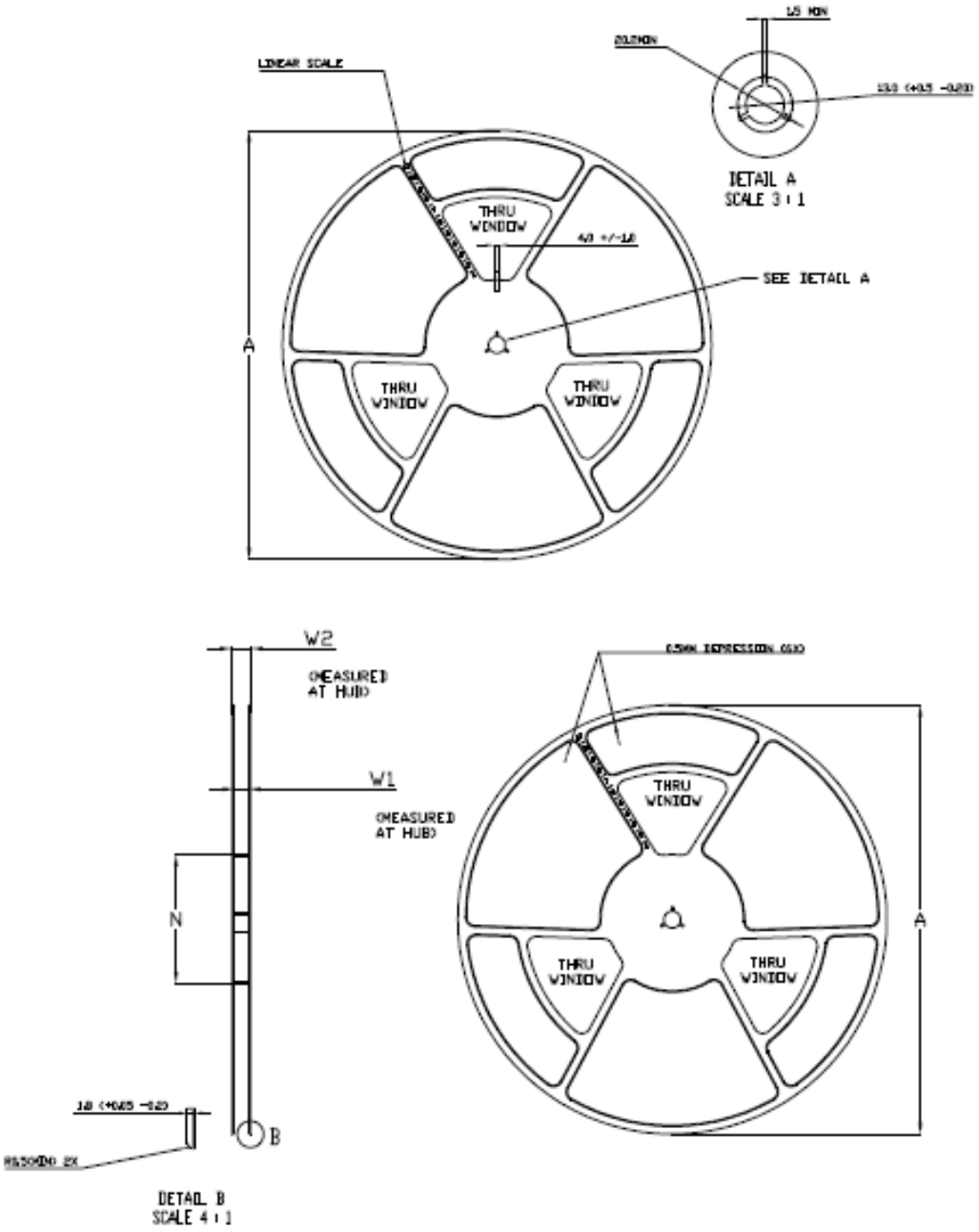
Part Number:

TS30111-MvvvQFNR-13 (13 inch reel)

vvv	Output Voltage
015	1.5 V
018	1.8 V
025	2.5 V
033	3.3 V
050	5.0 V
000	Adjustable

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REEL DIMENSIONS (13 INCH)

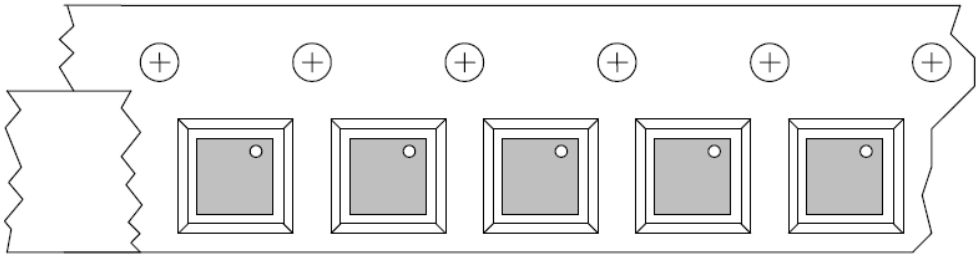


PRODUCT SPECIFICATIONS				
TAPE WIDTH	A (MAX)	N (MIN)	W1	W2
8MM	330	100	8.4	14.4
12MM	330	100	12.4	18.4
16MM	330	100	16.4	22.4

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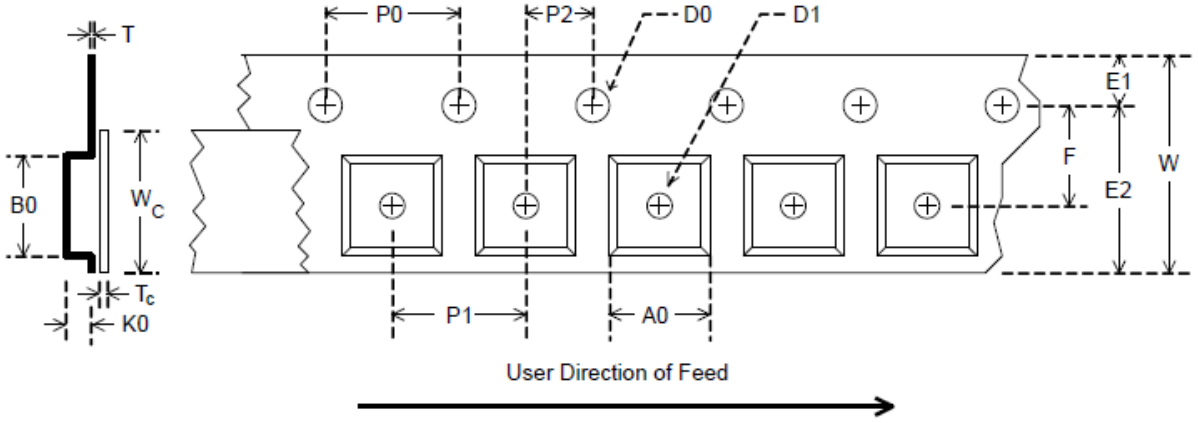
CARRIER TAPE SPECIFICATION

All DFN and QFN packages will be oriented so that the index package locations will be on the upper right corner of the sprocket side of the carrier tape.



User Direction of Feed

All carrier tape used for packing Triune System Components will be specifically formulated to provide protection from physical and electro-static discharge (ESD) damage during shipping and storage. Embossed carrier tape must be EIA Standard-481-1 compliant and meet the mechanical characteristics shown in Table 3.



Dimensions are in millimeters														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
2x2mm DFN	2.3	2.3	8.0 +/- 0.2	1.50 +/- 0.10	1.10 +/- 0.10	1.75 +/- 0.10	6.25 min	3.5 +/- 0.05	4	4	1.5	0.25 +/- 0.05	8	0.21-0.35
3x3mm QFN	3.3	3.3	12	1.50 +/- 0.10	1.10 +/- 0.10			3.5 +/- 0.05	8	8	1.1		4.5	0.21-0.35
4x4mm QFN	4.35	4.35	12	1.50 +/- 0.10	1.10 +/- 0.10			3.5 +/- 0.05	8	8	1.1		5.4	0.21-0.35
5x5mm QFN	5.25	5.25	12	1.50 +/- 0.10	1.10 +/- 0.10			3.5 +/- 0.05	8	8	1.1		9.2	0.21-0.35
6x6mm QFN	6.3 +/- 0.10	6.3 +/- 0.10	16 +/- 0.30	1.50 +/- 0.10	1.50 +/0 0.10	1.75 +/- 0.10	14.25	7.5 +/- 0.10	12	2	1.1	0.30 +/- 0.05	13.3	0.21-0.35

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