3.3V DIFFERENTIAL LVPECL-to-LVTTL TRANSLATOR

FEATURES

- **3.3V power supply**
- **2.0ns typical propagation delay**
- **Low power**
- **Differential LVPECL inputs**
- **24mA TTL outputs**
- **Flow-through pinouts**
- **Available in 8-pin SOIC package**

DESCRIPTION

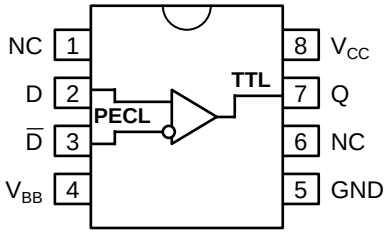
The SY10/100ELT21L are single differential LVPECL-to-LVTTL translators using a single +3.3V power supply. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3V and ground are required. The small outline 8-lead SOIC package and low skew single gate design make the ELT21L ideal for applications that require the translation of a clock or data signal where minimal space, low power, and low cost are critical.

V_{BB} allows a differential, single-ended, or AC-coupled interface to the device. If used, the V_{BB} output should be bypassed to V_{CC} with 0.01µF capacitor.

Under open input conditions, the /D will be biased at a $V_{CC}/2$ voltage level and the D input will be pulled to ground. This condition will force the Q output low to provide added stability.

The ELT21L is available in both ECL standards: the 10ELT is compatible with positive ECL 10H logic levels, while the 100ELT is compatible with positive ECL 100K logic levels.

PIN CONFIGURATION/BLOCK DIAGRAM



PIN NAMES

Pin	Function
Q	TTL Output
D, /D	Differential LVPECL Inputs
V_{CC}	+3.3V Supply
V_{BB}	Reference Output
GND	Ground

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Paramter	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +3.8	V
V_I	PECL Input Voltage	0V to V_{CC}+0.5	V
V_O	Voltage Applied to Output at HIGH State	–0.5 to V_{CC}	V
I_O	Current Applied to Output at LOW State	Twice the Rated I_{OL}	mA
T_{store}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	–40 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

D	/D	Q
L	H	L
H	L	H
Open	Open	L

TTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±5%

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
I_{OS}	Output Short Circuit Current	–80	–275	–80	–275	–80	—	–275	–80	–275	mA	V_{OUT} = 0V
I_{CC}	Power Supply Current	—	20	—	20	—	14	20	—	20	mA	
V_{OH}	Output HIGH Voltage	2.0	—	2.0	—	2.0	—	—	2.0	—	V	I_{OH} = –3.0mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	—	0.5	—	0.5	V	I_{OL} = 24mA

PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±5%

Symbol	Parameter		T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current		—	150	—	150	—	—	150	—	150	µA	
I_{IL}	Input LOW Current	D	0.5	—	0.5	—	0.5	—	—	0.5	—	µA	
		/D	–300	—	–300	—	–300	—	—	–300	—		
V_{IH}	Input HIGH Voltage(2)	10ELT	2070	2410	2130	2460	2170	—	2490	2240	2580	mV	
		100ELT	2135	2420	2135	2420	2135	—	2420	2135	2420		
V_{IL}	Input LOW Voltage(2)	10ELT	1350	1800	1350	1820	1350	—	1820	1350	1855	mV	
		100ELT	1490	1825	1490	1825	1490	—	1825	1490	1825		
V_{BB}	Reference Output(2)	10ELT	1870	2000	1920	2030	1950	2000	2050	1990	2110	mV	
		100ELT	1920	2040	1920	2040	1920	1980	2040	1920	2040		

NOTES:

1. These values are for V_{cc} = 3.3V. Level Specifications will vary 1:1 V_{cc}.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±5%

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay	1.5	2.5	1.5	2.5	1.5	2.0	2.5	1.5	2.5	ns	C_L = 20pF
t_{skpp}	Part-to-Part Skew(1,2)	—	0.5	—	0.5	—	—	0.5	—	0.5	ns	C_L = 20pF
f_{MAX}	Maximum Input Frequency(2,3,4)	275	—	275	—	275	—	—	275	—	MHz	C_L = 20pF
V_{CMR}	Common Mode Range	1.2	V_{CC}	1.2	V_{CC}	1.2	—	V_{CC}	1.2	V_{CC}	V	
V_{PP}	Minimum Peak-to-Peak Input(5)	100	—	100	—	100	—	—	100	—	mV	
t_r t_f	Output Rise/Fall Time (1.0V to 2.0V)	0.5	1.0	0.5	1.0	0.5	—	1.0	0.5	1.0	ns	C_L = 20pF

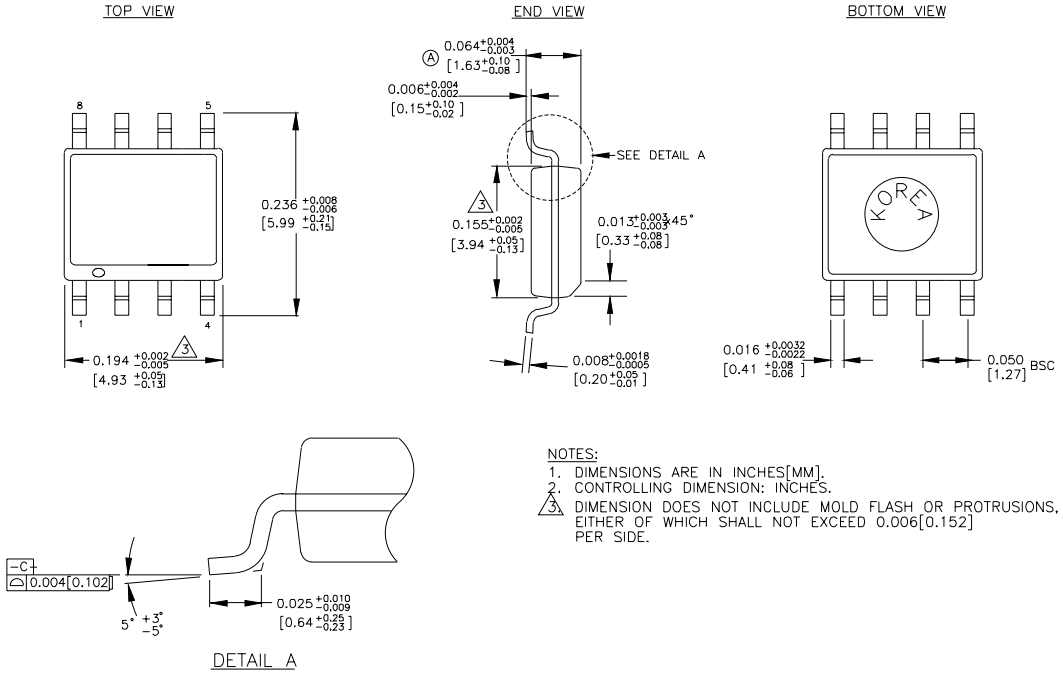
NOTES:

1. Part-to-Part Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
2. These parameters are guaranteed but not tested.
3. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
4. The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.
5. 100mV input guarantees full logic at output.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	Vcc Range (V)
SY10ELT21LZC	Z8-1	Commercial	+3.3V ±5%
SY10ELT21LZCTR	Z8-1	Commercial	+3.3V ±5%
SY100ELT21LZC	Z8-1	Commercial	+3.3V ±5%
SY100ELT21LZCTR	Z8-1	Commercial	+3.3V ±5%

8 LEAD SOIC .150" WIDE (Z8-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

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